cussion will be restricted to the concept of electron current flow, which travels from a negative to a positive terminal.)

DESIGN AND FABRICATION

The ultimate aim of all transistor fabrication techniques is the construction of two parallel p-n junctions with controlled spacing between the junctions and controlled impurity levels on both sides of each junction. A variety of structures has been developed in the course of transistor evolution.

The earliest transistors made were of the point-contact type. In this type of structure, two pointed wires were placed next to each other on an n-type block of semiconductor material. The p-n junctions were formed by electrical pulsing of the wires. This type has been superseded by junction transistors, which are fabricated by various alloy, diffusion, and crystal-growth techniques.

In grown-junction transistors, the impurity content of the semiconductor material is changed during the growth of the original crystal ingot to provide the p-n-p or n-p-n regions. The grown crystal is then sliced into a large number of small-area devices, and contacts are made to each region of the devices. Fig. 18(a) shows a cross-section of a grown-junction transistor.

In alloy-junction transistors, two small "dots" of a p-type or n-type impurity element are placed on opposite sides of a thin wafer of n-type or p-type semiconductor material, respectively, as shown in Fig. 18(b). After proper heating, the impurity "dots" alloy with the semiconductor material to form the regions for the emitter and collector junctions. The base connection in this structure is made to the original semiconductor wafer.

The drift-field transistor is a modified alloy-junction device in which the impurity concentration in the base wafer is diffused or graded, as

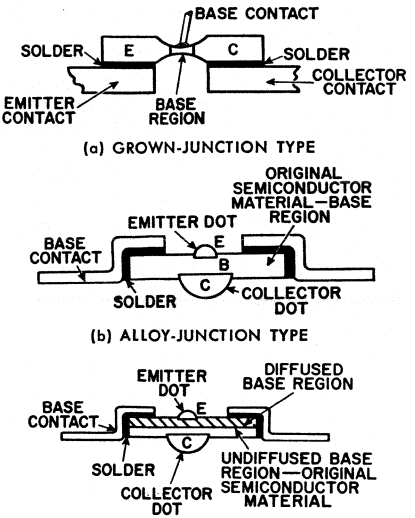


Fig. 18—Cross-sections of junction transistors.

shown in Fig. 18(c). Two advantages are derived from this structure: (a) the resultant built-in voltage or "drift field" speeds current flow, and (b) the ability to use a heavy impurity concentration in the vicinity of the emitter and a light concentration in the vicinity of the collector makes it possible to minimize capacitive charging times. Both these advantages lead to a substantial extension of the frequency performance over the alloy-junction device.

The **diffused-junction** transistor represents a major advance in transistor technology because increased control over junction spacings and impurity levels makes possible significant improvements in transistor performance capabilities. A cross-section of a **single-diffused** "hometaxial" structure is shown in Fig. 19(a). Hometaxial transistors are fabricated by simultaneous diffusion of impurity from each side of a homogeneously doped base wafer. A **mesa** or flat-topped peak is etched on one side of the wafer in an intricate design to define the transistor emitter

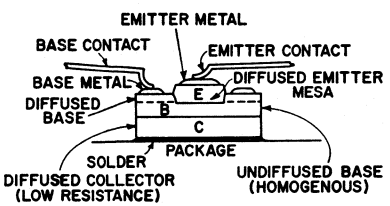
and expose the base region for connection of metal contacts. Large amounts of heat can be dissipated from a hometaxial structure through the highly conductive solder joint between the semiconductor material and the device package. This structure provides a very low collector resistance.

Double-diffused transistors have an additional degree of freedom for selection of the impurity levels and junction spacings of the base, emitter, and collector. This structure provides high voltage capability through a lightly doped collector region without compromise of the junction spacings which determine device frequency response and other important characteristics. Fig. 19(b) shows a typical double-diffused transistor; the emitter and base junctions are diffused into the same side of the original semiconductor wafer, which serves as the collector. A mesa is usually etched through the base region to reduce the collector area at the base-to-collector junction and to provide a stable semiconductor surface.

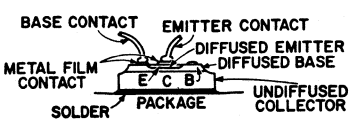
Double-diffused **planar** transistors provide the added advantage of protection or passivation of the emitter-to-base and collector-to-base junction surfaces. Fig. 19(c) shows a typical double-diffused planar transistor. The base and emitter regions terminate at the top surface of the semiconductor wafer under the protection of an insulating layer. Photolithographic and masking techniques are used to provide for diffusion of both base and emitter impurities in selective areas of the semiconductor wafer.

In **triple-diffused** transistors, a heavily doped region diffused from the bottom of the semiconductor wafer effectively reduces the thickness of the lightly doped collector region to a value dictated only by electric-field considerations. Thus, the thickness of the lightly doped or high-resistivity portion of the collector is minimized to obtain a low collector resistance. A section of a triple-diffused planar structure is shown in Fig. 19(d).

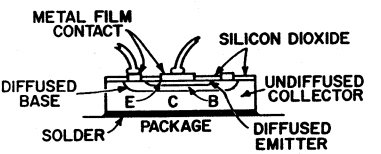
Epitaxial transistors differ from diffused structures in the manner in which the various regions are fabricated. Epitaxial structures are grown on top of a semiconductor wafer in a high-temperature reaction chamber. The growth proceeds atom by atom, and is a perfect extension of the crystal lattice of the wafer on which it is grown. In the epitaxial-base transistor shown in Fig. 20(a) a lightly doped base region is deposited by epitaxial techniques on a heavily doped collector wafer of opposite-type dopant. Photolithographic and masking techniques and



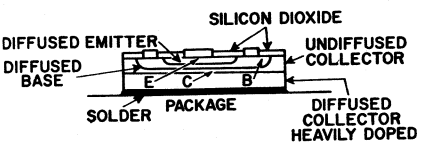
(a) SINGLE-DIFFUSED "HOMETAXIAL" TYPE



(b) DOUBLE-DIFFUSED TYPE



(c) DOUBLE-DIFFUSED PLANAR TYPE



(d) TRIPLE-DIFFUSED PLANAR TYPE

Fig. 19—Cross-sections of diffused transistors.

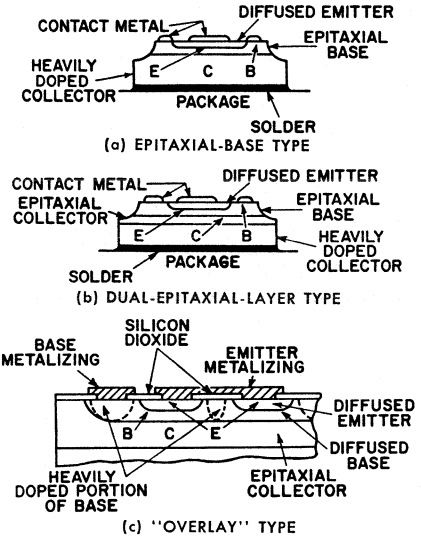


Fig. 20—Cross-sections of epitaxial transistors.

a single impurity diffusion are used to define the emitter region. This structure offers the advantages of low collector resistance and easy control of impurity spacings and emitter geometry. A variation of this structure uses two epitaxial layers. A thin lightly doped epitaxial layer used for the collector is deposited over the original heavily doped semiconductor wafer prior to the epitaxial deposition of the base region. The collector epitaxial layer is of opposite-type dopant to the epitaxial base layer. This structure, shown in Fig. 20(b), has the added advantage of higher voltage ratings provided by the epitaxial collector layer.

The **overlay** transistor is a double-diffused epitaxial device which employs a unique emitter structure. A large number of separate emitters are tied together by diffused and metalized regions to increase the emitter edge-to-area ratio and reduce the charging-time constants of the transistor without compromise of current- and power-handling capability. Fig. 20(c) shows a section through a typical overlay emitter region.

After fabrication, individual transistor chips are mechanically separated and mounted on individual headers. Connector wires are then bonded to the metalized regions, and each unit is encased in plastic or a hermetically sealed enclosure. In power transistors, the wafer is usually soldered or alloyed to a solid metal header to provide for high thermal conductivity and low-resistance collector contacts, and low-resistance contacts are soldered or metal-bonded from the emitter or base metalizing contacts to the appropriate package leads. This packaging concept results in a simple structure that can be readily attached to a variety of circuit heat sinks and can safely withstand power dissipations of hundreds of watts and currents of tens of amperes.

BASIC CIRCUITS

Bipolar transistors are ideal current amplifiers. When a small signal current is applied to the input terminals of a bipolar transistor, an amplified reproduction of this signal appears at the output terminals. Although there are six possible ways of connecting the input signal, only three useful circuit configurations exist for current or power amplification: common-base, common-emitter, and common-collector. In the **common-base** (or grounded-base) connection shown in Fig. 21, the signal is introduced into the emitter-base circuit and extracted from the collector-base circuit. (Thus the base element of the transistor is common to both the input and output circuits). Because the input or emitter-base circuit has a low impedance (resistance plus reactance) in the order of 0.5 to 50 ohms, and the output or collector-base circuit has a high impedance in the order of 1000 ohms to one megohm, the voltage or power gain in this type of configuration may be in the order of 1500.