

Low Power 315/433.92 MHz OOK Receiver

Features

- Operation Frequency: 315 / 433.92 MHz
- OOK Demodulation
- Data Rate: 1.0 - 5.0 kbps
- Sensitivity: -109 dBm (3.0 kbps, 0.1% BER)
- Receiver Bandwidth: 330 kHz
- Large Signal Handling: 10 dBm
- Periodically operating (2s/3ms), no external MCU control required
- No Register Configuration Required
- Supply voltage: 1.8 -3.6 V
- Low Power Consumption:
 - 3.3 mA @ 315 MHz
 - 3.8 mA @ 433.92 MHz

Descriptions

The CMT2210LC is a low power, high performance OOK stand-alone RF receiver for 315/433.92 MHz wireless applications. It is part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The CMT2210LC is a true plug-and-run device, no register configuration and manually-tune is required. The device operates at either 315 MHz or 433.92 MHz through selecting a 19.7008 MHz or 27.1383 MHz crystal, the data rate is optimized to 1 - 5 kbps which fits well with the low-end data encoder or a MCU based transmitter. It consumes 3.3 mA current at 315 MHz and 3.8 mA at 433.92 MHz while achieving -109 dBm receiving sensitivity. The SOP8 package is available for easier and lower-cost manufacturing. The CMT2210LC receiver together with the CMT21xx transmitter enables an ultra-low cost RF link. For NextGenRF™ receivers with more flexibility, the user can use the CMT2210AW.

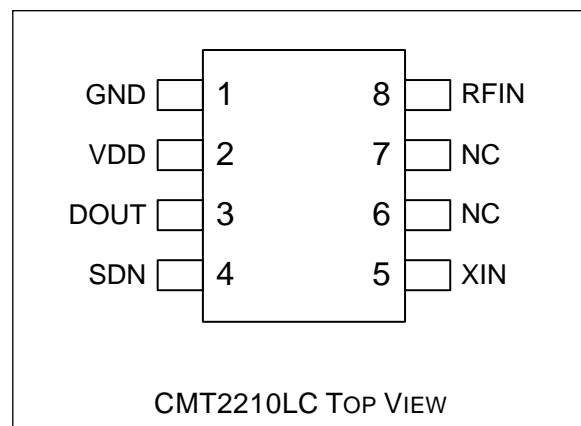
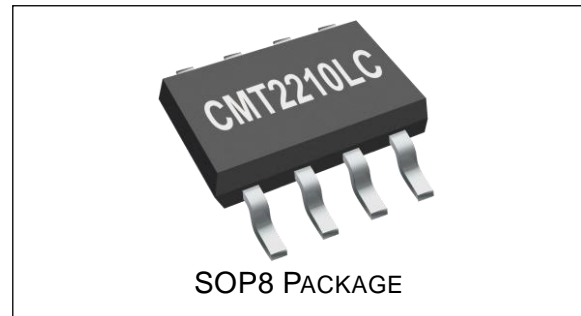
Application

- Low-Cost Consumer Electronics Applications
- Home and Building Automation
- Infrared Receiver Replacements
- Industrial Monitoring and Controls
- Remote Automated Meter Reading
- Remote Lighting Control System
- Wireless Alarm and Security Systems
- Remote Keyless Entry (RKE)

Ordering Information

Part Number	Frequency	Package	MOQ
CMT2210LC-ESR	315/433.92MHz	SOP8/T&R	2,500 pcs
CMT2210LC-ESB	315/433.92 MHz	SOP8/Tube	1,000 pcs

More Ordering Info: See [Page 15](#)



Typical Application

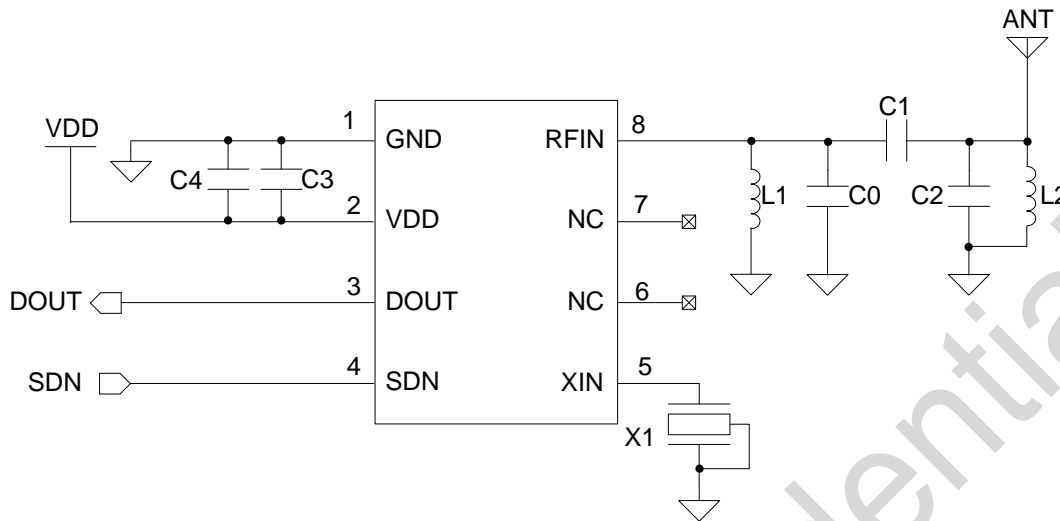


Figure 1. CMT2210LC Typical Application Schematic of Enhanced Anti-interference

Table 1. BOM of Enhanced Anti-interference Typical Application

Designator	Descriptions	Value (Match to $\lambda/4$ ANT)		Unit	Manufacturer
		315 MHz	433.92 MHz		
U1	CMT2210LC, low power 315/433.92 MHz OOK receiver	-		-	CMOSTEK
X1	± 20 ppm, SMD32*25 mm, crystal	19.7008	27.1383	MHz	EPSON
L1	$\pm 5\%$, 0603 multi-layer chip inductor	39	33	nH	Murata LQG18
C0	± 0.25 pF, 0402 NP0, 50 V	3.6	NA	pF	Murata GRM15
C1	± 0.25 pF, 0402 NP0, 50 V	3.6	2.7	pF	Murata GRM15
L2	$\pm 5\%$, 0603 multi-layer chip inductor, optional	22	22	nH	Murata LQG18
C2	± 0.25 pF, 0402 NP0, 50 V, optional	12	6.2	pF	Murata GRM15
C3	$\pm 20\%$, 0402 X7R, 25 V	0.1		uF	Murata GRM15
C4	$\pm 20\%$, 0603 NP0, 50 V	1		nF	Murata GRM15

Abbreviations

Abbreviations used in this data sheet are described below

AGC	Automatic Gain Control	PC	Personal Computer
AN	Application Notes	PCB	Printed Circuit Board
BER	Bit Error Rate	PLL	Phase Lock Loop
BOM	Bill of Materials	PN9	Pseudorandom Noise 9
BSC	Basic Spacing between Centers	POR	Power On Reset
BW	Bandwidth	PUP	Power Up
DC	Direct Current	QFN	Quad Flat No-lead
EEPROM	Electrically Erasable Programmable Read-Only Memory	RF	Radio Frequency
ESD	Electro-Static Discharge	RFPDK	RF Products Development Kit
ESR	Equivalent Series Resistance	RoHS	Restriction of Hazardous Substances
IF	Intermediate Frequency	RSSI	Received Signal Strength Indicator
LNA	Low Noise Amplifier	Rx	Receiving, Receiver
LO	Local Oscillator	SAR	Successive Approximation Register
LPOSC	Low Power Oscillator	SOP	Small Outline Package
Max	Maximum	SPI	Serial Port Interface
MCU	Microcontroller Unit	TH	Threshold
Min	Minimum	Tx	Transmission, Transmitter
MOQ	Minimum Order Quantity	Typ	Typical
NP0	Negative-Positive-Zero	VCO	Voltage Controlled Oscillator
NC	Not Connected	XOSC	Crystal Oscillator
OOK	On-Off Keying	XTAL/Xtal	Crystal

Table of Contents

1. Electrical Characteristics	5
1.1 Recommended Operation Conditions	5
1.2 Absolute Maximum Ratings.....	5
1.3 Receiver Specifications	6
1.4 Crystal Oscillator	6
2. Pin Descriptions	7
3. Typical Performance Characteristics	8
4. Typical Application Schematic	9
5. Functional Descriptions	10
5.1 Overview	10
5.2 Modulation, Frequency and Data Rate.....	10
5.3 Internal Blocks Description.....	11
5.3.1 RF Front-end and AGC.....	11
5.3.2 IF Filter	11
5.3.3 RSSI	11
5.3.4 SAR ADC	11
5.3.5 Crystal Oscillator.....	11
5.3.6 Frequency Synthesizer	12
5.4 Periodical Operating.....	13
6. Ordering Information	15
7. Package Outline	16
8. Top Marking	17
9. Other Documentations	18
10. Document Change List	19
11. Contact Information	20

1. Electrical Characteristics

$V_{DD} = 3.3\text{ V}$, $T_{OP} = 25\text{ }^{\circ}\text{C}$, $F_{RF} = 433.92\text{ MHz}$, sensitivities are measured in receiving a PN9 sequence and matching to $50\ \Omega$ impedance, with the BER of 0.1%. All measurements are performed using the board CMT2210LC-EM V1.0, unless otherwise noted.

1.1 Recommended Operation Conditions

Table 2. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}	Within $-10\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	1.8		3.6	V
		Within $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	2.4		3.6	V
Operation Temperature	T_{OP}		-40		85	$^{\circ}\text{C}$
Supply Voltage Slew Rate			1			mV/us

1.2 Absolute Maximum Ratings

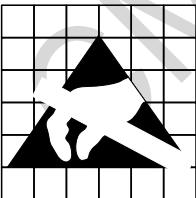
Table 3. Absolute Maximum Ratings^[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	$V_{DD} + 0.3$	V
Junction Temperature	T_J		-40	125	$^{\circ}\text{C}$
Storage Temperature	T_{STG}		-50	150	$^{\circ}\text{C}$
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	$^{\circ}\text{C}$
ESD Rating ^[2]		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ $85\text{ }^{\circ}\text{C}$	-100	100	mA

Notes:

[1]. Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2]. The CMT2210LC is high-performance RF integrated circuits. Handling and assembly of this device should only be done at ESD-protected workstations.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Receiver Specifications

Table 4. Receiver Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range	F_{RF}	Use a 19.7008 MHz crystal		315		MHz
		Use a 27.1383 MHz crystal		433.92		MHz
Data Rate	DR		1		5	kbps
Sensitivity	S_{315}	$F_{RF} = 315$ MHz, DR = 3 kbps, BER = 0.1%		-109		dBm
	$S_{433.92}$	$F_{RF} = 433.92$ MHz, DR = 3 kbps, BER = 0.1%		-109		dBm
Saturation Input Signal Level	P_{LVL}			10		dBm
Working Current	I_{DD315}	$F_{RF} = 315$ MHz		3.3		mA
	$I_{DD433.92}$	$F_{RF} = 433.92$ MHz		3.8		mA
Sleep Current	$I_{SHUTDOWN}$			60		nA
Frequency Synthesizer Settle Time	T_{LOCK}	Counting from the crystal oscillator settled		150		us
Blocking Immunity	BI	DR = 1 kbps, ± 1 MHz offset, CW interference		32		dB
		DR = 1 kbps, ± 2 MHz offset, CW interference		42		dB
		DR = 1 kbps, ± 10 MHz offset, CW interference		61		dB
Input 3 rd Order Intercept Point	IIP3	Two tone test at 1 MHz and 2 MHz offset frequency. Maximum system gain settings		-23		dBm
Receiver Bandwidth	BW_{315}	$F_{RF} = 315$ MHz		240		kHz
	$BW_{433.92}$	$F_{RF} = 433.92$ MHz		330		kHz
Receiver Start-up Time ^[1]	$T_{START-UP}$	From power up to receive		3		ms
Note:						
[1]. This parameter is to a large degree crystal dependent.						

1.4 Crystal Oscillator

Table 5. Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency ^[1]	$F_{XTAL315}$	$F_{RF} = 315$ MHz		19.7008		MHz
	$F_{XTAL433.92}$	$F_{RF} = 433.92$ MHz		27.1383		MHz
Crystal Tolerance ^[2]				± 20		ppm
Load Capacitance	C_{LOAD}			15		pF
Crystal ESR	R_m				60	Ω
XTAL Startup Time ^[3]	t_{XTAL}			400		us
Notes:						
[1]. The CMT2210LC can directly work with external reference clock input to XIN pin (a coupling capacitor is required) with peak-to-peak amplitude of 0.3 to 0.7 V.						
[2]. This is the total tolerance including: (1) initial tolerance; (2) crystal loading; (3) aging; and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.						
[3]. This parameter is to a large degree crystal dependent.						

2. Pin Descriptions

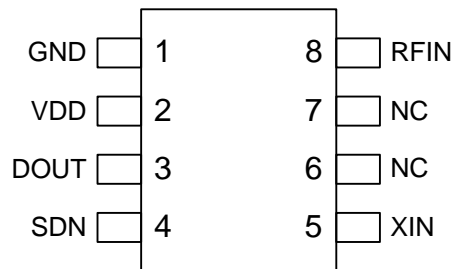


Figure 2. CMT2210LC Pin Assignments

Table 6. CMT2210LC Pin Descriptions

Pin Number	Name	I/O	Description
1	GND	I	Ground
2	VDD	I	Power supply input
3	DOUT	O	Received data output
4	SDN	I	Chip on / off control, pull low to enable the receiver, pull high to disable the receiver
5	XIN	I	Crystal oscillator input or external reference clock input
6, 7	NC	--	Not connected
8	RFIN	I	RF signal input to the LNA

3. Typical Performance Characteristics

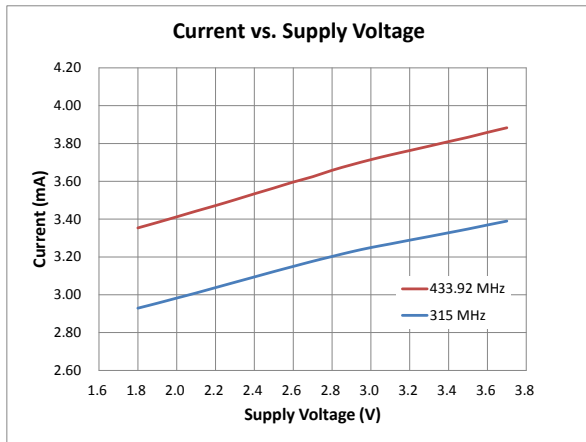


Figure 3. Current vs. Voltage, $F_{RF} = 315/433.92$ MHz, DR = 1 kbps

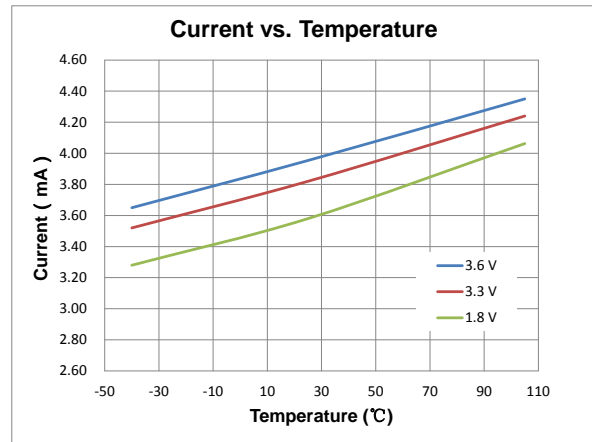


Figure 4. Current vs. Temperature, $F_{RF} = 433.92$ MHz, DR = 1 kbps

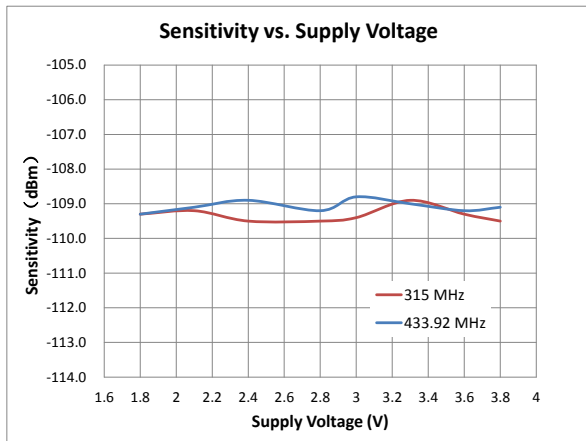


Figure 5. Sensitivity vs. Supply Voltage, $F_{RF} = 315/433.92$ MHz, DR = 3 kbps, BER = 0.1%

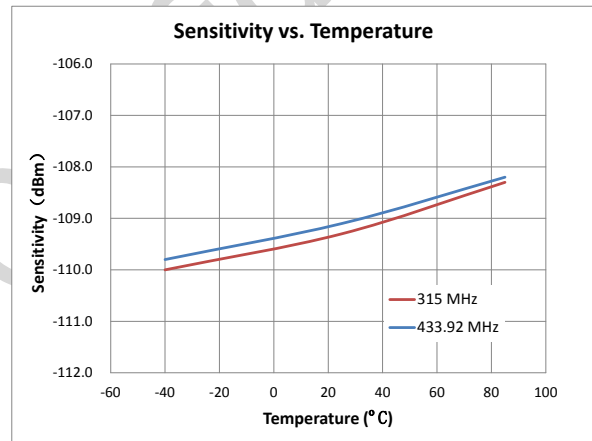


Figure 6. Sensitivity vs. Temperature, $F_{RF} = 315/433.92$ MHz, $V_{DD} = 3.3$ V, DR = 1 kbps, BER = 0.1%

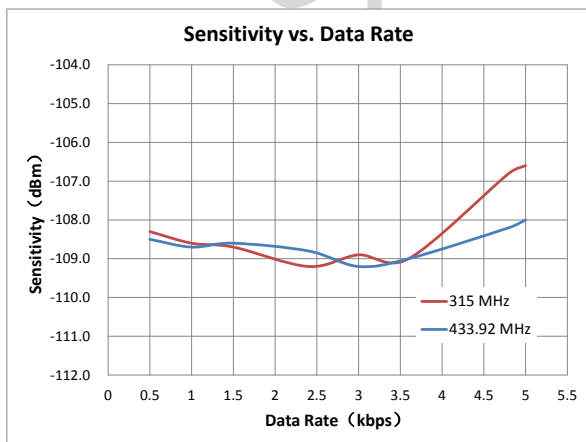


Figure 7. Sensitivity vs. DR, $F_{RF} = 315/433.92$ MHz, $V_{DD} = 3.3$ V, BER = 0.1%

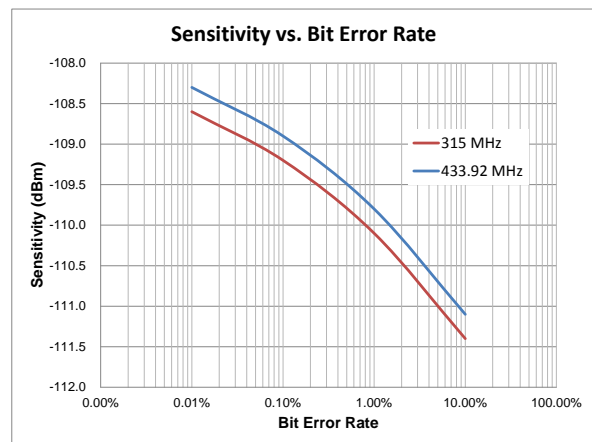


Figure 8. Sensitivity vs. BER, $F_{RF} = 315/433.92$ MHz, $V_{DD} = 3.3$ V, DR = 3 kbps

4. Typical Application Schematic

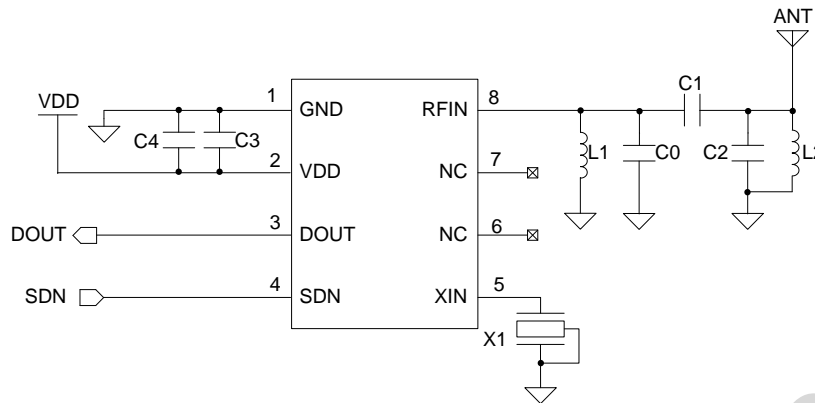


Figure 9. Typical Application Schematic of Enhanced Anti-interference

Notes:

1. The general layout guidelines are listed below.
 - Use as much continuous ground plane metallization as possible.
 - Avoid using long and/or thin transmission lines to connect the components.
 - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
 - Place C3 and C4 as close to the CMT2210LC as possible for better filtering.
 - Place the crystal as close to the CMT2210LC as possible, the metal case of crystal needs grounding.
2. Based on the chip default settings in factory, the chip is configured as receiving 2s and then resetting for 3ms. Users do not need to pull the SDN pin high or low or periodically power on and off to reset the chip regularly. Users can just pull the SDN pin low all the time.
3. For more design details, please refer to “AN110 CMT221x-5x Schematic and PCB Layout Design Guideline.

Table 7. BOM of Enhanced Anti-interference Typical Application

Designator	Descriptions	Value (Match to λ/4 ANT)		Unit	Manufacturer
		315 MHz	433.92 MHz		
U1	CMT2210LC, low power 315/433.92 MHz OOK receiver	-		-	CMOSTEK
X1	±20 ppm, SMD32*25 mm, crystal	19.7008	27.1383	MHz	EPSON
L1	±5%, 0603 multi-layer chip inductor	39	33	nH	Murata LQG18
C0	±0.25 pF, 0402 NP0, 50 V	3.6	NA	pF	Murata GRM15
C1	±0.25 pF, 0402 NP0, 50 V	3.6	2.7	pF	Murata GRM15
L2	±5%, 0603 multi-layer chip inductor, optional	22	22	nH	Murata LQG18
C2	±0.25 pF, 0402 NP0, 50 V, optional	12	6.2	pF	Murata GRM15
C3	±20%, 0402 X7R, 25 V	0.1		uF	Murata GRM15
C4	±20%, 0603 NP0, 50 V	1		nF	Murata GRM15

Table 8. Modulation, Frequency and Data Rate

Parameter	Value	Unit
Demodulation	OOK	-
Frequency	315 / 433.92	MHz
Data Rate	1.0 – 5.0	kbps

5.3 Internal Blocks Description

5.3.1 RF Front-end and AGC

The CMT2210LC features a low-IF receiver. The RF front-end of the receiver consists of a Low Noise Amplifier (LNA), I/Q mixer and a wide-band power detector. Only a low-cost inductor and a capacitor are required for matching the LNA to any 50 Ω antennas. The input RF signal induced on the antenna is amplified and down-converted to the IF frequency for further processing.

By means of the wide-band power detector and the attenuation networks built around the LNA, the Automatic Gain Control (AGC) loop regulates the RF front-end's gain to get the best system linearity, selectivity and sensitivity performance, even though the receiver suffers from strong out-of-band interference.

With a low cost inductor and a capacitor, the input of the LNA can be matched to a 50 Ω antenna or other common used antennas.

5.3.2 IF Filter

The signals coming from the RF front-end are filtered by the fully integrated 3rd-order band-pass image rejection IF filter. The IF center frequency is dynamically adjusted to enable the IF filter to locate to the right frequency band, thus the receiver sensitivity and out-of-band interference attenuation performance are kept optimal despite the manufacturing process tolerances. The IF bandwidth is fixed at 330 kHz when the device works at 433.92 MHz.

5.3.3 RSSI

The subsequent multistage I/Q Log amplifiers enhance the output signal from IF filter before it is fed for demodulation. Receive Signal Strength Indicator (RSSI) generators are included in both Log amplifiers which produce DC voltages that are directly proportional to the input signal level in both of I and Q path. The resulting RSSI is a sum of both these two paths. Extending from the nominal sensitivity level, the RSSI achieves dynamic range over 66 dB.

5.3.4 SAR ADC

The on-chip 8-bit SAR ADC digitalizes the RSSI for OOK demodulation.

5.3.5 Crystal Oscillator

The CMT2210LC uses a 1-pin crystal oscillator circuit with the required crystal load capacitance fully integrated. The recommended specification for the crystal is 27.1383/19.7008 MHz with ± 20 ppm, ESR (R_m) < 60 Ω , with 15 pF load capacitance.

If a 27.1383/19.7008 MHz RCLK (reference clock) is available in the system, the user can directly use it to drive the CMT2210LC by feeding the clock into the chip via the XIN pin. This further saves the system cost due to the removal of the crystal. A coupling capacitor is required if the RCLK is used. The recommended peak-to-peak amplitude of the RCLK is 0.3 to 0.7 V on the XIN pin.

5.3.6 Frequency Synthesizer

A fully integrated frequency synthesizer is used to generate the LO frequency for the down conversion I/Q mixer. Using the 19.7008 MHz or 27.1383 MHz reference clock provided by the crystal oscillator or the external clock source, the frequency synthesizer can generate the frequencies of 315 and 433.92 MHz for the receiver.

CMOSTEK Confidential

5.4 Periodical Operating

Based on the chip default settings in factory, CMT2210LC is in the duty cycle (Duty-Cycle) receiving mode by default, in which the receiving state (RX) lasts for about 2 s, and then the reset process (RESET) lasts about 3 ms. In the duty cycle receiving mode, the SDN pin is always pulled low, and the chip will automatically repeat the loop of SLEEP->XTAL->TUNE->RX-> SLEEP after the power-on (PUP) process until the chip is powered off. This allows the chip to be recalibrated and tuned regularly in a complicated and changeable environment to maintain the best performance. In the RX state, the chip will continue receiving RF input signals and outputting demodulated data through the DOUT pin. For the operating timing and current consumption of the chip in duty cycle receiving mode, please refer to the figure below for details.

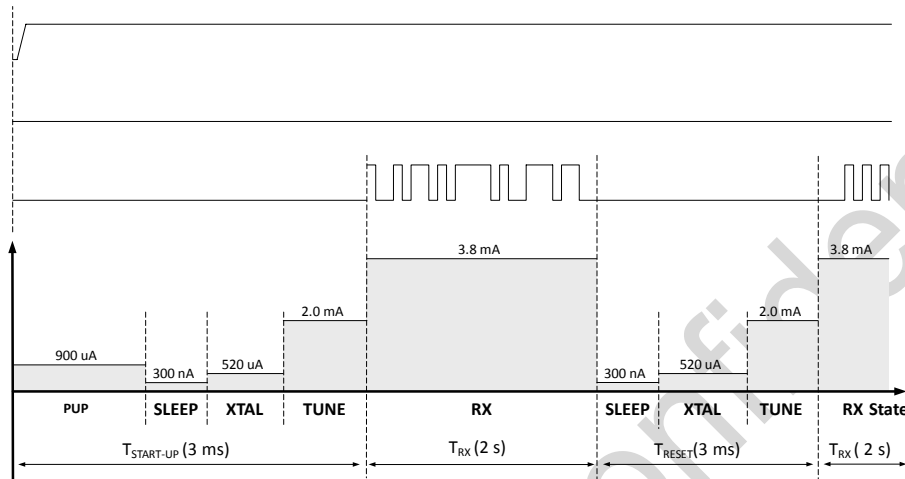


Figure 10-1. Chip Operating Timing and Current Consumption in Duty Cycle Mode
(SDN pin is always pulled low)

The advantages of the duty cycle receiving mode are as follows:

- By periodically re-tuning the frequency, it can keep the chip performance in an optimized state.
- By resetting most modules through periodic reset, it can increase the system stability.

Through pulling up and down the SDN pin periodically, it can control the chip to operate periodically. This co-working with the duty cycle mode will make the operating timing more complicated as shown in the figure below.

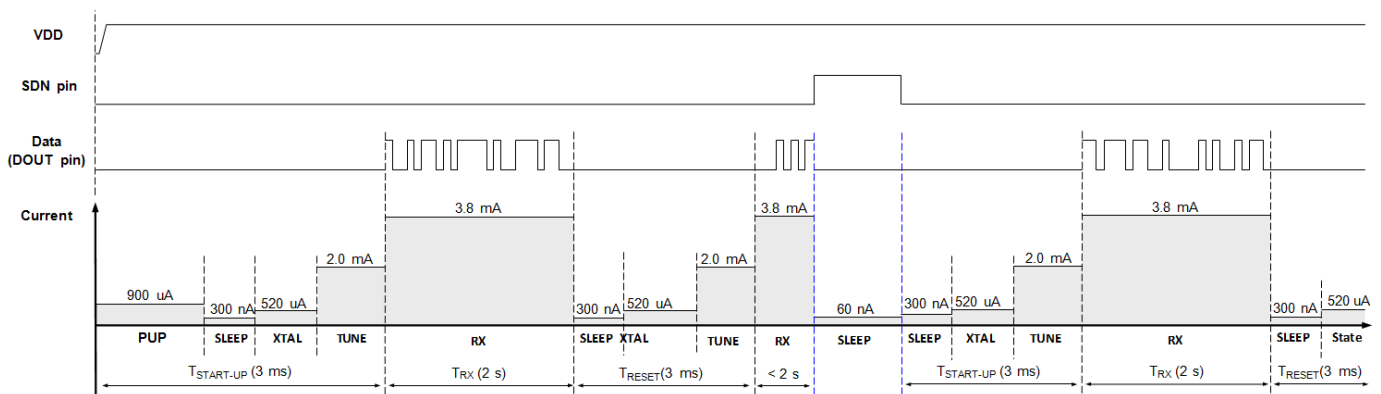


Figure 10-2. Chip Operating Timing and Current Consumption in Duty Cycle Receiving Mode
(controlled by SDN pin)

It can be seen that when the SDN pin is kept low, the chip will work periodically according to default configuration. That is, after a power-on lasting for 2 s, there is a reset process lasting for 3 ms. When the SDN pin is pulled high, the configured periodic operating mode by default is broken. During the period when the SDN pin is pulled high, the chip enters and then remains in the SLEEP state, and the DOUT pin outputs invalid data. When the SDN pin is pulled low again, the chip restarts and continues to operate in the duty cycle receiving mode.

CMOSTEK Confidential

6. Ordering Information

Table 9. CMT2210LC Ordering Information

Part Number	Descriptions	Package Type	Package Option	Operating Condition	MOQ/Multiple
CMT2210LC-ESR ^[1]	Low power 315/433.92 MHz OOK Receiver	SOP8	Tape & Reel	1.8 to 3.6 V, -40 to 85 °C	2,500
CMT2210LC-ESB ^[1]	Low power 315/433.92 MHz OOK Receiver	SOP8	Tube	1.8 to 3.6 V, -40 to 85 °C	1,000

Note:

[1]. “E” stands for extended industrial product grade, which supports the temperature range from -40 to +85 °C.
“S” stands for the package type of SOP8.
“R” stands for the tape and reel package option, the minimum order quantity (MOQ) for this option is 2,500 pieces. “B” stands for the tube package option, the minimum order quantity (MOQ) for this option is 1,000 pieces.

If the CMT2210LC-ESR cannot meet the application requirements, the user can order other CMT2210x products with SPI interface for self-customizing with the RFPDK.

Visit www.cmostek.com/products/wireless to know more about the product and product line.

Contact sales@cmostek.com or your local sales representatives for more information.

7. Package Outline

The SOP8 illustrates the package details for the CMT2210LC. The table below lists the values for the dimensions shown in the illustration.

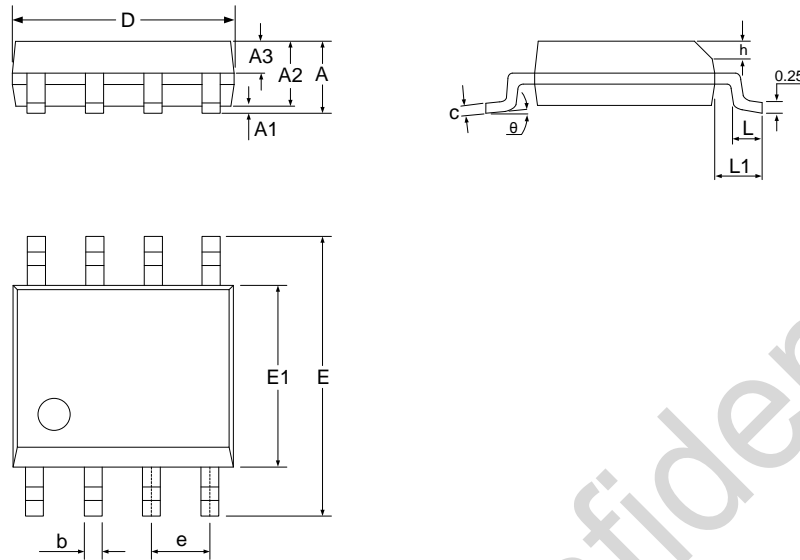


Figure 11. SOP8 Package

Table 10. SOP8 Package Dimensions

Symbol	Size (millimeters)		
	Min	Typ	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
c	0.21	-	0.26
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05 BSC		
θ	0	-	8°

8. Top Marking



Figure 12. CMT2210LC Top Marking

Table 11. CMT2210LC Top Marking Explanation

Mark Method	Laser
Pin 1 Mark	Circle's diameter = 1 mm
Font Height	0.6 mm, right-justified
Font Width	0.4 mm
Line 1 Marking	CMT2210LC, represents part number CMT2210LC
Line 2 Marking	YYWW is the Date code assigned by the assembly house. YY represents the last two digits of the mold year and WW represents the workweek. ①②③④⑤⑥ is the internal tracking number

9. Other Documentations

Table 12. Other Documentations for CMT2210LC

Brief	Name	Descriptions
AN107	CMT221x Schematic and PCB Layout Design Guideline	Details of CMT2210/13/17/19A and CMT2210L/Lx PCB schematic and layout design rules, RF matching network and other application layout design related issues. English edition.
AN110	CMT221x-5x Schematic and PCB Layout Design Guideline	Details of CMT221x and CMT225x PCB schematic and layout design rules, RF matching network and other application layout design related issues. Chinese edition.

10. Document Change List

Table 13. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.6	All	Initial released version	2015-12-23
0.7	All	Added the Support of 315 MHz	2016-02-25
0.8	All	Update the supply voltage, temperature range	2016-12-27
0.9	5.4 and all	Add description of periodically operating (English version updated in 2021)	2017-08-17

11. Contact Information

CMOSTEK Microelectronics Co., Ltd. Shenzhen Branch

Address: 30th floor of 8th Building, C Zone, Vanke Cloud City, Xili Sub-district, Nanshan, Shenzhen, GD, P.R. China

Tel: +86-755-83231427

Post Code: 518055

Sales: sales@cmostek.com

Supports: support@cmostek.com

Website: www.cmostek.com

Copyright. CMOSTEK Microelectronics Co., Ltd. All rights are reserved.

The information furnished by CMOSTEK is believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies and specifications within this document are subject to change without notice. The material contained herein is the exclusive property of CMOSTEK and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of CMOSTEK. CMOSTEK products are not authorized for use as critical components in life support devices or systems without express written approval of CMOSTEK. The CMOSTEK logo is a registered trademark of CMOSTEK Microelectronics Co., Ltd. All other names are the property of their respective owners.