

XMC1100 V9

FIFO

	Protokoll	Tx	Rx	Clk	CS	Bitrate 1/s	MSB/LSB	Stop Bits	Parity	Bytes Tx	Bytes Rx	
USIC0	DH0	ASC	P0.14			50000	MSB	1	0	1	<input type="checkbox"/> DH0_TxInterruptCall	<input type="checkbox"/> DH0_RxInterruptCall
	DH1	ASC	P0.15			50000	MSB	1	0	1	<input type="checkbox"/> DH1_TxInterruptCall	<input type="checkbox"/> DH1_RxInterruptCall

	G0	G1
VADC	Tx	P2.0
	Tx	P2.1

	Slice 0	Slice 1	Slice 2	Slice 3	
CDU	Output	DB_C	Comb	Comb	Comb
	Input	DB_C	Comb	Comb	Comb

Port	Direction	Pin
P2.4		
P2.5		XMC1100
P2.6		
P2.7		
P2.8		
P2.9		
P2.10		
P2.11		
Vss		
VDD		
P1.5		
P1.4		
P1.3		
P1.2		
P1.1		
P1.0		
P0.0		
P0.1		
P0.2		
P2.3		
P2.2		
P2.1		
P2.0		
P0.15		
P0.14		
P0.13		
P0.12		
P0.11		
P0.10		
P0.9		
P0.8		
Vssb		
Vsup		
P0.7		
P0.6		
P0.5		
P0.4		
P0.3		

DE

XMC1100 V9

FIFO

USIC0

Protocol: Tx: ASC, Rx: P1.0, CS: []

Bitrate 1/s: 50000, MSB/LSB: MSB, Stop Bits: 1, Parity: 0, Bytes Tx: 1, Bytes Rx: 1

DH0: [], DH1: []

Interrupts: []

VADC

GO: Tx, GI: Tx

CDU

Slice 0: [], Slice 1: [], Slice 2: [], Slice 3: []

Output: [], Input: []

Push-Pull: []

P2.4, P2.5, P2.6, P2.7, P2.8, P2.9, P2.10, P2.11, **Vss**, **VDD**, P1.5, P1.4, P1.3, P1.2, P1.1, P1.0 T4(DH0), P0.0, P0.1, P0.2

XMC1100

P2.3, P2.2, P2.1, P2.0, P0.15, P0.14, P0.13, P0.12, P0.11, P0.10, P0.9, P0.8, **Vss**, **VDD**, P0.7, P0.6, P0.5, P0.4, P0.3

DE

XMC1100 V9

FIFO

USIC0

CH0: SSC, Tx: P1.0, Rx: P1.1, CK: P0.7, CS: P0.0, Bitrate 1/s: 50200, MSB/LSB: MSB, Stop Bits: 0, Parity: 0, Bytes Tx: 4, CH0_TxInterruptCall: , Bytes Rx: 1, CH0_RxInterruptCall:

CH1: SSC, Tx: P1.2, Rx: P1.3, Bitrate 1/s: 50200, MSB/LSB: MSB, Stop Bits: 1, Parity: 0, Bytes Tx: 1, CH1_TxInterruptCall: , Bytes Rx: 1, CH1_RxInterruptCall:

VADC

G0: Tx, G1: Tx

CDJ

Slice 0: Output: CB_C, Input: CB_C
 Slice 1: Comb, Comb
 Slice 2: Comb, Comb
 Slice 3: Comb, Comb

P2.4	XMC1100	P2.3
P2.5		P2.2
P2.6		P2.1
P2.7		P2.0
P2.8		P0.15
P2.9		P0.14
P2.10		P0.13
P2.11		P0.12
Vss		P0.11
VDD		P0.10
P1.5		P0.9
P1.4	P0.8	
cont. sampl. P1.3 Rx(CH1)	Vddp	P0.7 SCK(CH0) Push-Pull
Push-Pull P1.2 Tx(CH1)	Vssp	P0.6
cont. sampl. P1.1 Rx(CH0)		P0.5
Push-Pull P1.0 Tx(CH0)		P0.4
Push-Pull P0.0 CS(CH0)		P0.3
P0.1		
P0.2		

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// Channel0
//***** Globale Funktionen *****
void IRQ_Hub_9 (void) {CH0_TxInterruptCall(); //Aufruf bei IRQ 9;
void CH0_TxInterruptCall();
Register (&USIC0_CH0->TCSR,0xFFFF3FF,0x00); //TDEN=1
};
//***** Globale Funktionen Ende *****
//Interrupt
Register (&USIC0_CH0->INPR,0xFFFFF0F,0x00); //TBINP=0; In: 9 -> SP0
NVIC_SetPriority(IRQn_Type)9,3); //Interrupt Priority= 3
NVIC_EnableIRQ(IRQn_Type)9); //Enable Interrupt

//USIC Parameter
ssc_Init(0, 50200, 0, 0, 0); // Channel, Bitrate, MSB, StopBits, Parity
Register (&PORT1->IDCR0, 0xFFFFF00, 0x88); // Tx: P1.0
Register (&USIC0_CH0->IDCR, 0xFFFFF00, 3); // DSEL=0x0D
Register (&PORT1->IDCR4, 0xFFFF00FF, 0x1800); // Rx: P1.1
Register (&PORT0->IDCR4, 0xFFFFF0, 0x80000000); // CK: P0.7
Register (&PORT0->IDCR0, 0xFFFFF00, 0x80); // CS: P0.0

//FIFO
Register (&USIC0_CH0->TBCTR,0xFFFFFC0,0x00); //DPTR=0
Register (&USIC0_CH0->TBCTR,0xFFFFC0FF,0x200); //LIMIT=2
Register (&USIC0_CH0->TBCTR,0xF8FFFFFF,0x2000000); //SIZE=2
Register (&USIC0_CH0->TBCTR,0xFFFFFFFF,0x10000000); //LDF=1
Register (&USIC0_CH0->TBCTR,0xBFFFFFFF,0x40000000); //STBIEN=1
Register (&USIC0_CH0->TCSR,0xFFFF7FF,0x00); //TDEN=0
Register (&USIC0_CH0->TCSR,0xFFFFFEFF,0x100); //TDSSM=1

// Channel 1
//USIC Parameter
ASC_Init(1, 50200, 0, 1, 0); // Channel, Bitrate, MSB, StopBits, Parity
Register (&PORT1->IDCR0, 0xF00FFFF, 0x800000); // Tx: P1.2
Register (&USIC0_CH1->IDCR, 0xFFFFF00, 0); // DSEL=0x1A

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