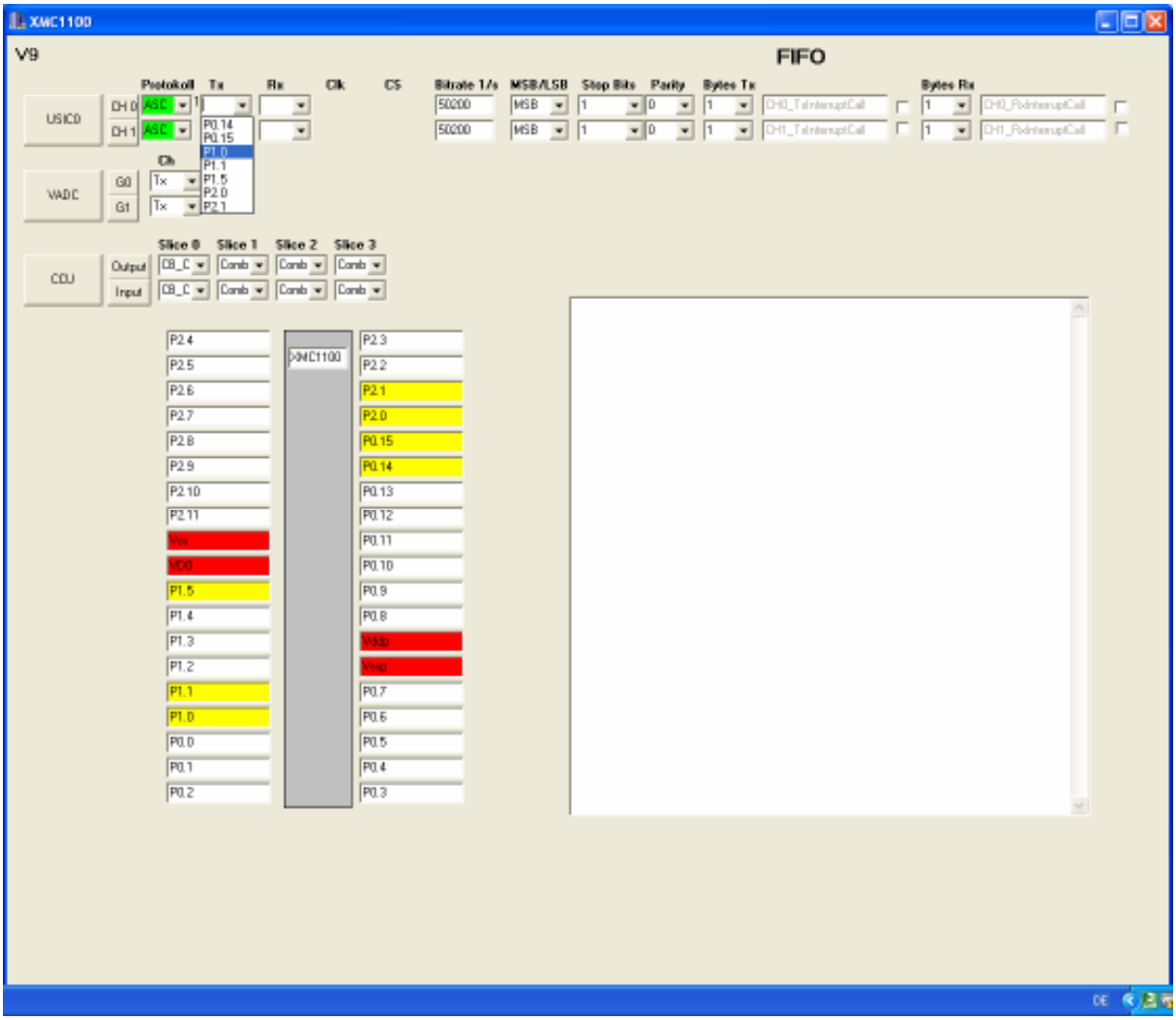
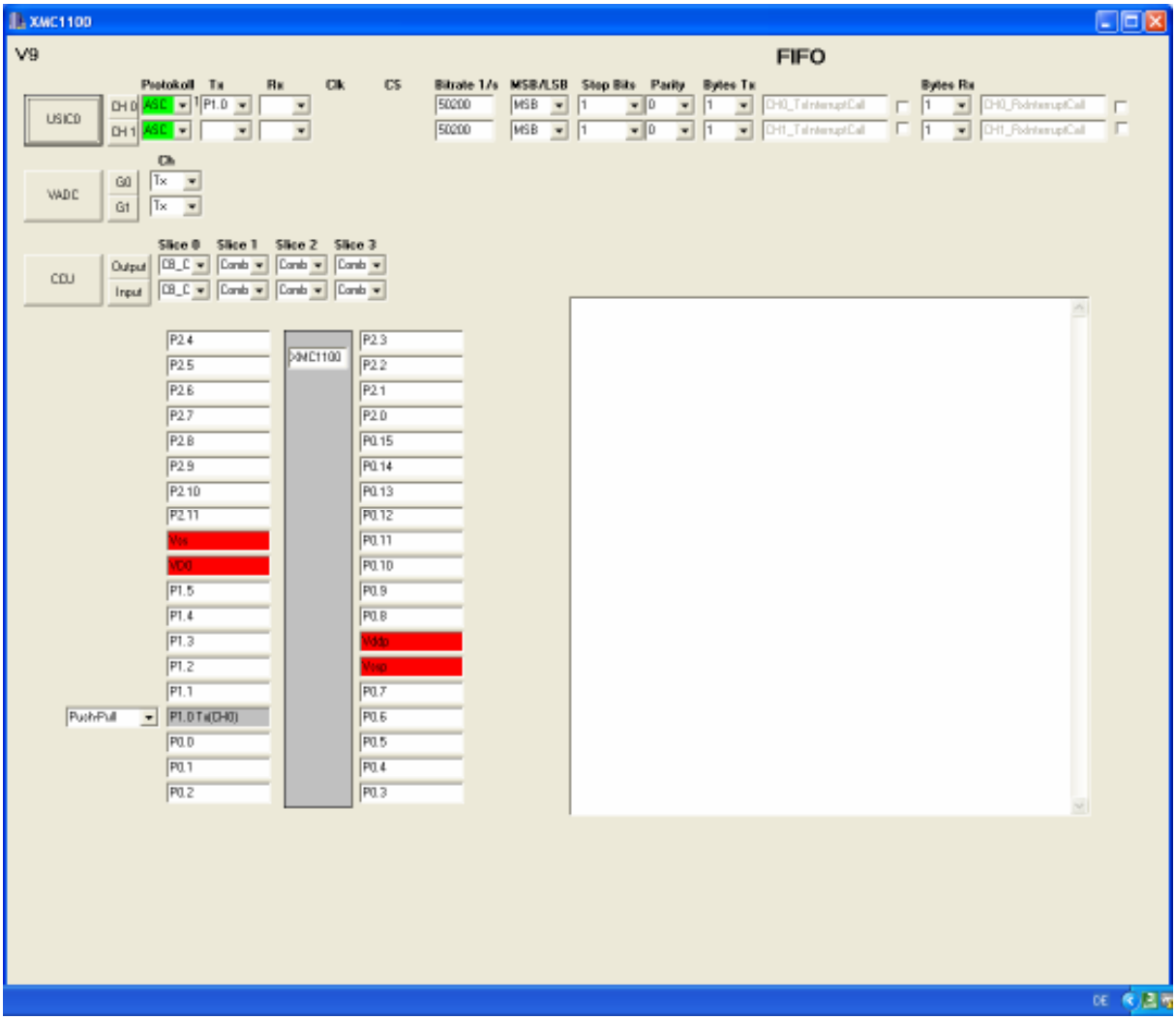
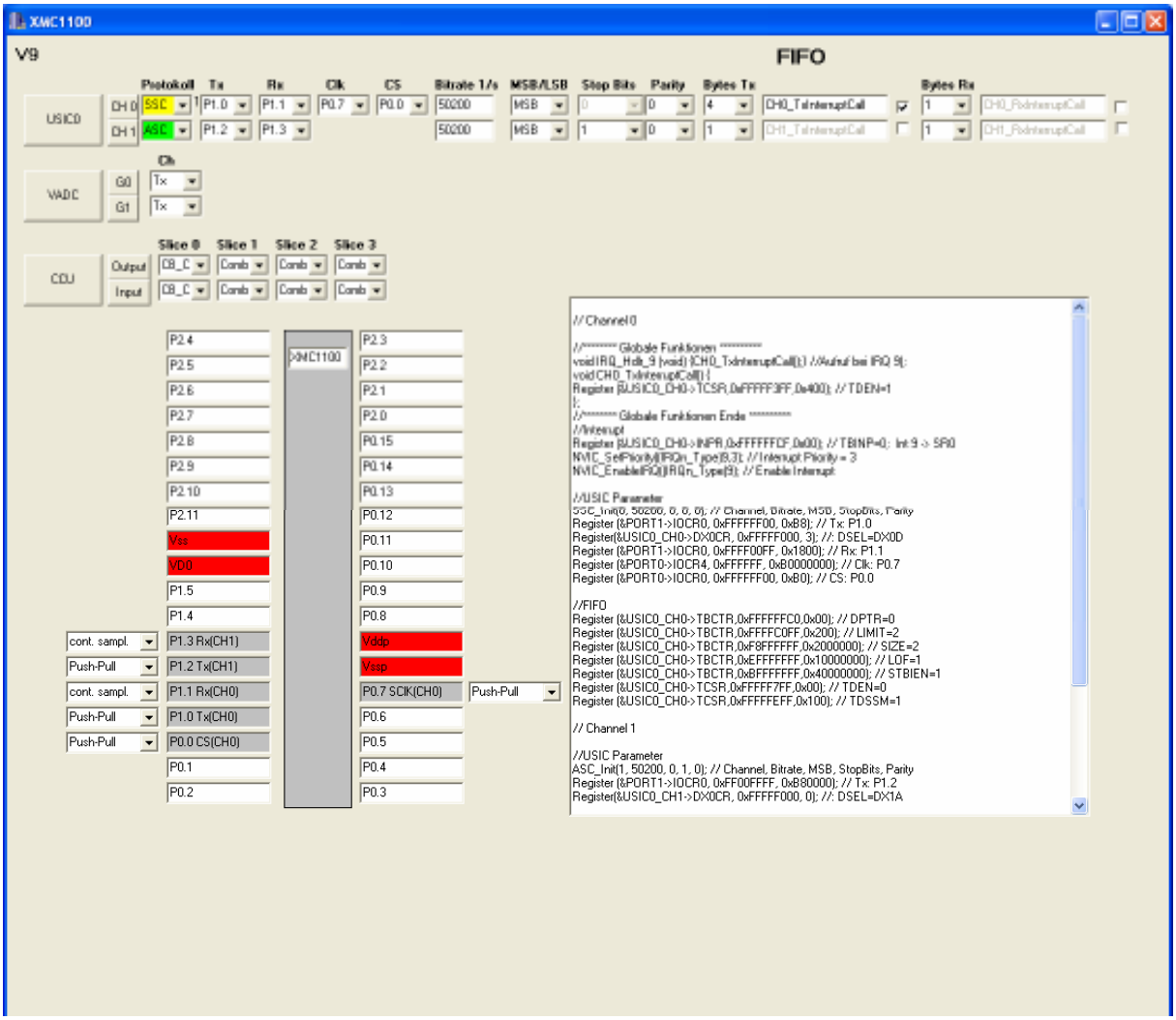

XMC1100
V9
FIFO
USICD
CH 0
CH 1
Protokoll
Tx
Rx
Clk
CS
Bitrate 1/s
MSB/LSB
Stop Bits
Parity
Bytes Tx
Bytes Rx
ASC
50000
MSB
VADC
G0
G1
CDU
Output
Input
Slice 0
Slice 1
Slice 2
Slice 3
P0.14
P0.15
P1.0
P1.1
P1.5
P2.0
P2.1
P2.4
P2.5
P2.6
P2.7
P2.8
P2.9
P2.10
P2.11
Vss
VDD
P1.5
P1.4
P1.3
P1.2
P1.1
P1.0
P0.0
P0.1
P0.2
XMC1100
P2.3
P2.2
P2.1
P2.0
P0.15
P0.14
P0.13
P0.12
P0.11
P0.10
P0.9
P0.8
Vddp
Vssp
P0.7
P0.6
P0.5
P0.4
P0.3


XMC1100
V9
FIFO
Protokoll
Tx
Rx
Clk
CS
Bitrate 1/s
MSB/LSB
Stop Bits
Parity
Bytes Tx
Bytes Rx
USIC0
CH 0
CH 1
ASC
P1.0
50000
MSB
VADC
G0
G1
Clk
Tx
CCU
Output
Input
Slice 0
Slice 1
Slice 2
Slice 3
Comb
XMC1100
P2.4
P2.5
P2.6
P2.7
P2.8
P2.9
P2.10
P2.11
Vss
VDD
P1.5
P1.4
P1.3
P1.2
P1.1
P1.0 Tx(CH0)
P0.0
P0.1
P0.2
P2.3
P2.2
P2.1
P2.0
P0.15
P0.14
P0.13
P0.12
P0.11
P0.10
P0.9
P0.8
Vddp
Vssp
P0.7
P0.6
P0.5
P0.4
P0.3
PushPull


XMC1100
V9
FIFO
Protokoll
Tx
Rx
Clk
CS
Bitrate 1/s
MSB/LSB
Stop Bits
Parity
Bytes Tx
Bytes Rx
USIC0
CH 0
CH 1
SSC
ASC
P1.0
P1.1
P0.7
P0.0
50000
MSB
CH0_TxInterruptCall
CH0_RxInterruptCall
CH1_TxInterruptCall
CH1_RxInterruptCall
VADC
G0
G1
Ch
Tx
CCU
Output
Input
Slice 0
Slice 1
Slice 2
Slice 3
Comb
XMC1100
P2.4
P2.5
P2.6
P2.7
P2.8
P2.9
P2.10
P2.11
Vss
VDD
P1.5
P1.4
P1.3 Rx(CH1)
P1.2 Tx(CH1)
P1.1 Rx(CH0)
P1.0 Tx(CH0)
P0.0 CS(CH0)
P0.1
P0.2
P2.3
P2.2
P2.1
P2.0
P0.15
P0.14
P0.13
P0.12
P0.11
P0.10
P0.9
P0.8
Vddp
Vssp
P0.7 SCIK(CH0)
P0.6
P0.5
P0.4
P0.3
cont. sampl.
Push-Pull
// Channel 0
//********** Globale Funktionen **********
void IRQ_Hdlr_9 (void) {CH0_TxInterruptCall();} //Aufruf bei IRQ 9;
void CH0_TxInterruptCall() {
Register (&USIC0_CH0->TCSR, 0xFFFFF3FF,0x400); // TDEN=1
};
//********** Globale Funktionen Ende **********
//Interrupt
Register (&USIC0_CH0->INPR,0xFFFFFFCF,0x00); // TBINP=0; Int 9 -> SR0
NVIC_SetPriority(IRQn_Type(9,3); //Interrupt Priority = 3
NVIC_EnableIRQ(IRQn_Type(9); // Enable Interrupt
//USIC Parameter
SSC_Init(0, 50000, 0, 0, 0); // Channel, Bitrate, MSB, StopBits, Parity
Register (&PORT1->IOCR0, 0xFFFFFF00, 0xB8); // Tx: P1.0
Register(&USIC0_CH0->DX0CR, 0xFFFFF000, 3); //: DSEL=DX0D
Register (&PORT1->IOCR0, 0xFFFF00FF, 0x1800); // Rx: P1.1
Register (&PORT0->IOCR4, 0xFFFFFF, 0xB0000000); // Clk: P0.7
Register (&PORT0->IOCR0, 0xFFFFFF00, 0xB0); // CS: P0.0
//FIFO
Register (&USIC0_CH0->TBCTR,0xFFFFFFC0,0x00); // DPTR=0
Register (&USIC0_CH0->TBCTR,0xFFFFC0FF,0x200); // LIMIT=2
Register (&USIC0_CH0->TBCTR,0xF8FFFFFF,0x2000000); // SIZE=2
Register (&USIC0_CH0->TBCTR,0xEFFFFFFF,0x10000000); // LOF=1
Register (&USIC0_CH0->TBCTR,0xBFFFFFFF,0x40000000); // STBIEN=1
Register (&USIC0_CH0->TCSR,0xFFFFF7FF,0x00); // TDEN=0
Register (&USIC0_CH0->TCSR,0xFFFFFEFF,0x100); // TDSSM=1
// Channel 1
//USIC Parameter
ASC_Init(1, 50200, 0, 1, 0); // Channel, Bitrate, MSB, StopBits, Parity
Register (&PORT1->IOCR0, 0xFF00FFFF, 0xB80000); // Tx: P1.2
Register(&USIC0_CH1->DX0CR, 0xFFFFF000, 0); //: DSEL=DX1A