ESP32-C3 **Chip series**

Technical Specification

Carry RISC-V 32 **Extremely low power consumption of a single-core processor** SoC

stand by 2.4 GHz Wi-Fi **with** Bluetooth LE

include

ESP32-C3

ESP32-C3FH4

Pre-release version 0.3

Espressif Information Technology

product description

ESP32-C3 Series is a very low power consumption, high integration MCU System-on-chip (SoC) ,integrated 2.4 GHz Wi-Fi And Bluetooth Low Energy (Bluetooth® LE) Dual-mode wireless communication, with:

- complete Wi-Fi Subsystem, in line with IEEE 802.11b/g/n Agreement with Station , SoftAP with SoftAP + Station Mixed three modes
- Bluetooth low energy subsystem, support Bluetooth 5 with Bluetooth mesh
- Industry-leading low-power performance and RF performance
- RISC-V 32 Single-core processor, four-stage pipeline architecture, main Frequency up to 160 MHz
- Built-in 400 KB SRAM , 384 KB ROM Storage space and support multiple external SPI , Dual SPI , Quad SPI , QPI flash
- Perfect safety mechanism
  - Hardware encryption accelerator can support AES-128/256 , Hash , RSA , HMAC , Digital signature and security move
  - Integrated true random number generator
  - Support access to on-chip memory, off-chip memory and peripherals authority management
  - Support for off-chip memory encryption and decryption
- Rich communic n interface and GPIO Pin, can support multiple scenarios And com applications

Functional block diagram

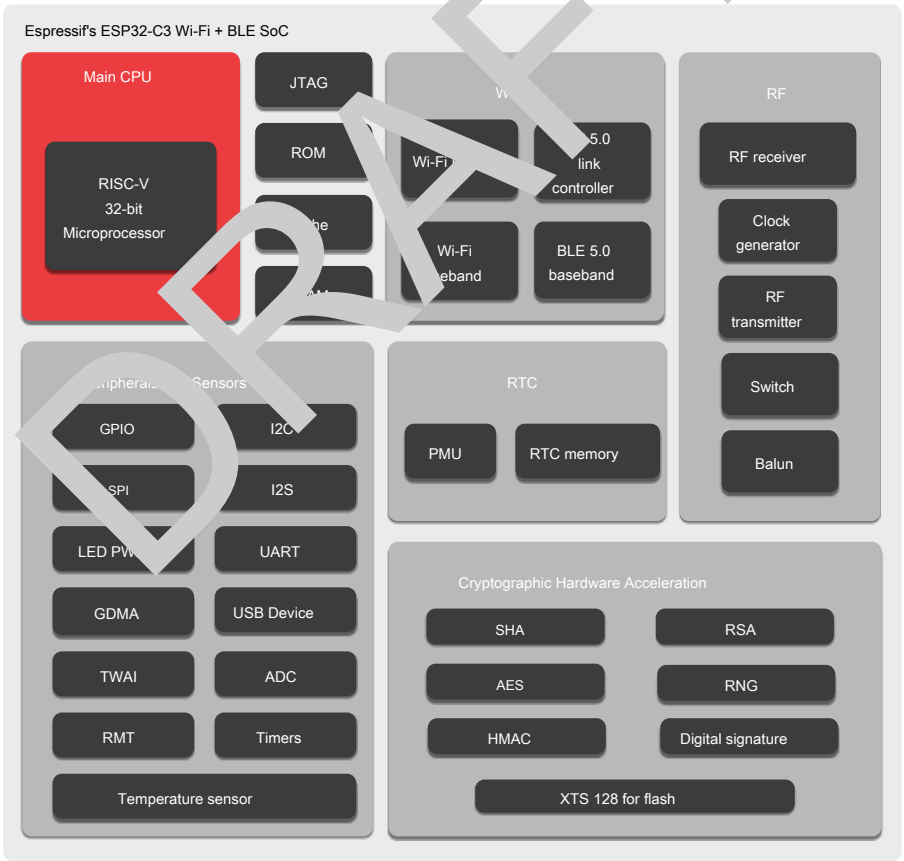

Figure 1: **Functional block diagram**

Product Features

Wi-Fi

- stand by IEEE 802.11 b/g/n protocol
- in 2.4 GHz Band support 20 MHz with 40 MHz bandwidth
- stand by 1T1R Mode, data rate up to 150 Mbps
- Wireless Multimedia (WMM)
- Frame aggregation (TX/RX A-MPDU, RX A-MSDU)
- Block reply immediately (Immediate Block ACK)
- Fragmentation and reorganization (Fragmentation and defragmentation)
- Beacon Automatic monitoring (hardware TSF)
- 4 × virtual Wi-Fi interface
- At the same time support infrastructure network (Infrastructure BSS) Station mode, SoftAP Pattern and Station + SoftAP Promiscuous mode

  Please note ESP32-C3 in Station When scanning in mode, SoftAP Channel will change at the same time
- Antenna diversity
- 802.11 mc FTM

Bluetooth

- Bluetooth Low Energy (Bluetooth LE) : Bluetooth 5 , Bluetooth mesh
- Rate support 125 Kbps , 500 Kbps , 1Mbps , 2Mbps
- Broadcast ext…on (Advertising Extensions)
- Mult… Multiple Advertisement Sets)
- Channel selec… Channel Selection Algorithm #2)

CPU **And storage**

- 32 Bit RISC-V Single-core processor, clocked up to 160 MHz
- 384 KB ROM
- 400 KB SRAM
- … KB RTC SRAM
- S… Dual SPI , Quad SPI , QPI Multiple external interfaces flash

Advanced peripheral interfaces and sensors

- 22 × GPIO mouth
- 2 × 12 Bit SAR A/D convert… …hannel…
- 1 × Temperature Sensor
- 3 × SPI
- 2 × UART
- 1 × I2C
- 1 × I2S
- Infrared transceiver, 2 Send channels and 2 Receive channels
- LED PWM Controller, up to 6 Channels
- USB 1.1 interface(USB to UART converter, USB to JTAG converter)
- Universal DMA Controller (abbreviated GDMA) , 3 Receiving channels and 3 Send channels
- 1 × TWAI TM Controller (compatible ISO11898-1)

Low power management

- Power management unit, five power consumption modes

Security Mechanism

- Safe boot
- Flash encryption
- 4096 Bit OTP , Users are available up to 1792 Bit
- Encryption hardware accelerator:

- AES-128/256 (FIPS PUB 197)

- Access management
  - Hash (FIPS PUB 180-4)
  - RSA
  - Random number generator (RNG)
  - HMAC
  - digital signature

Application (some examples)

With ultra-low power consumption ESP32-C3 Series designed for the Internet of Things (IoT) Designed for equipment, application areas include:

- Smart home
  - Smart lighting
  - Smart button
  - Smart socket
  - Indoor Positioning
- automated industry
  - Industrial robot
  - Mesh Networking
  - HMI
  - Industrial bus application
- medical insurance
  - Health monitoring
  - Baby monitor
- Consumer Electronics
  - Smart watch, smart bracelet
  - OTT TV box, set-top box equipment
  - Wi-Fi And bluetooth speakers
  - Toys with data upload function and proximity-sensing toys
- Smart agriculture
  - Smart greenhouse
  - Smart irrigation
  - Agricultural robot
- Retail ca g
  - POS m
  - Service rob
- A equipment
  - Network music player
  - Audio streaming device
  - Webcast
- Universal low power consumption IoT Sensor hub
- Universal low power consumption IoT Data logger

• USB equipment

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1. Product model comparison

1.1 ESP32-C3 Series chip naming

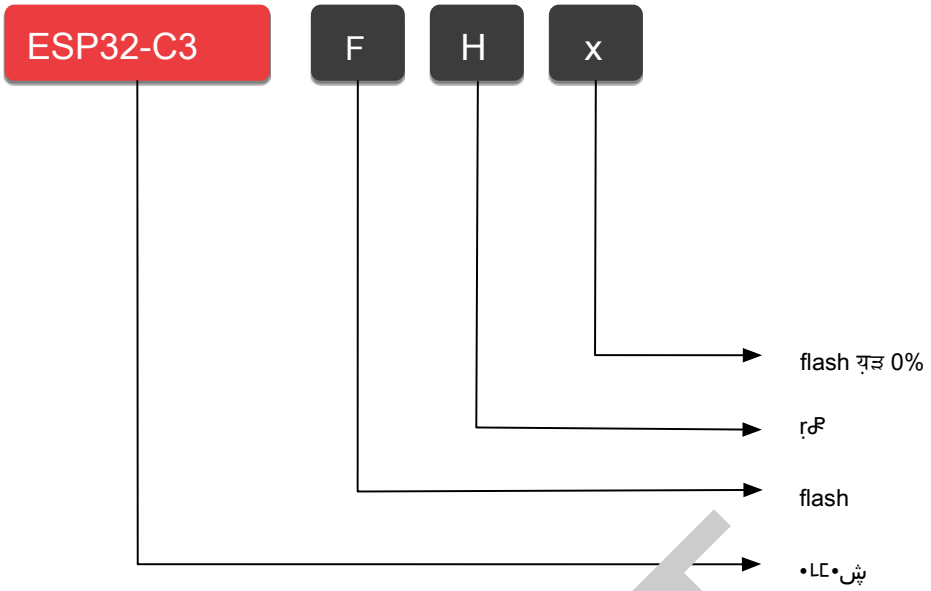


Figure 2: ESP32-C3 **Series chip na ng**

1.2 ESP32-C3 Series chip comparison

Order model	Embedded flash	erature (°C)	Junction temperature (°C)	Package (mm)
ESP32-C3	no	- 25 - 40 ~	125	QFN32 (5*5)
ESP32-C3FH4	4 MB	- 40 ~ 85 - 40 ~	105	QFN32 (5*5)

2. Pin definition

2.1 Pin layout

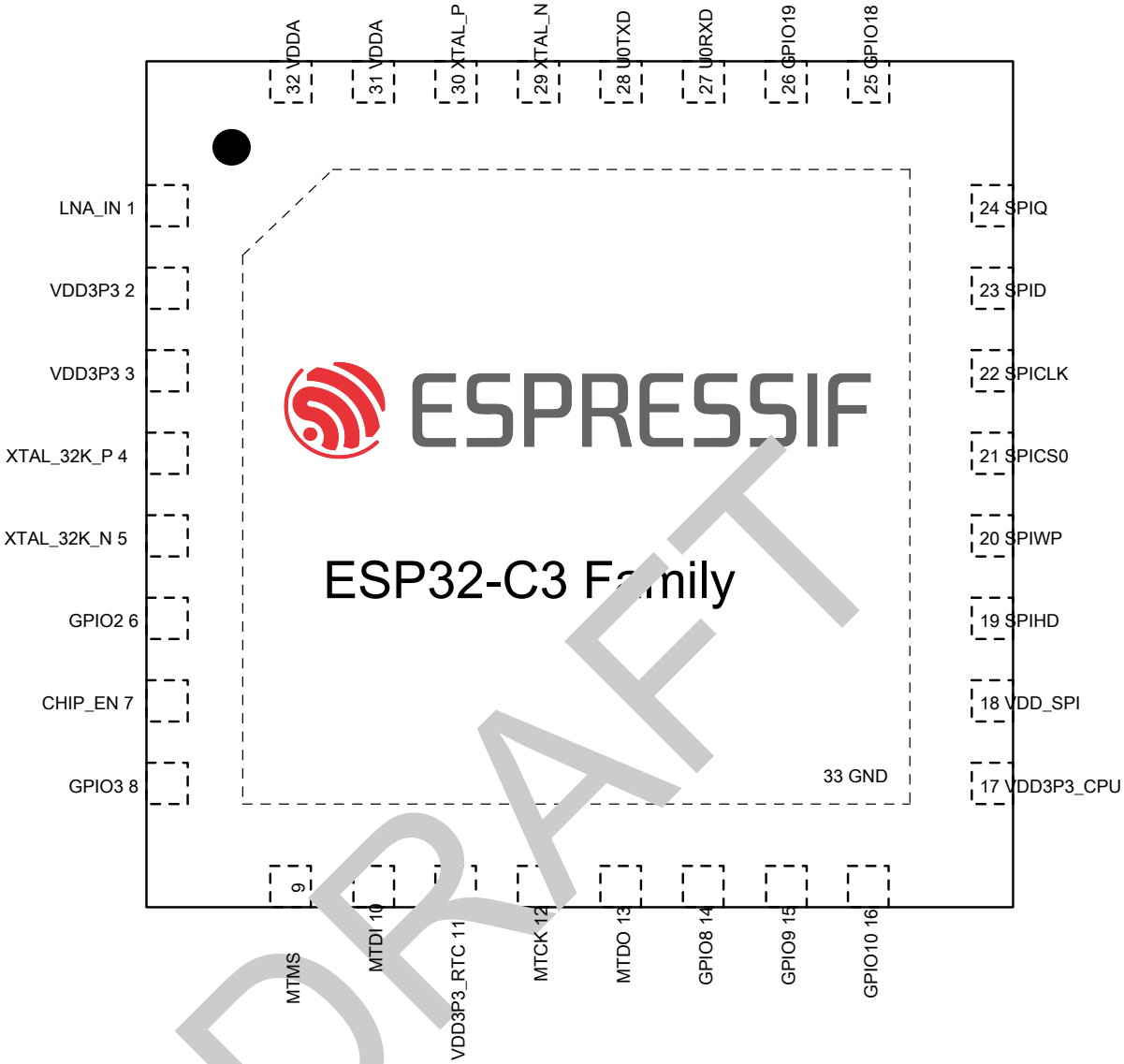


Figure 3: ESP32-C3 **Series chip pin layout (top view)**

2.2 Pin description

table 2: **Pin description**

name	No.	Types of	Power domain	Features
LNA_IN	1	I/O	—	RF input and output
VDD3P3	2	PA	—	Analog power
VDD3P3	3	PA	—	Analog power
XTAL_32K_P	4	I/O/T	VDD3P3_RTC GPIO0, ADC1_CH0, XTAL_32K_P VDD3P3_RTC GPIO1,	
XTAL_32K_N	5	I/O/T	ADC1_CH1, XTAL_32K_N	

name	No.	Types of	Power domain	Features
GPIO2	6	I/O/T	VDD3P3_RTC	GPIO2, ADC1_CH2, FSPIQ
CHIP_EN	7	I	VDD3P3_RTC	High level: chip enable; Low level: the chip is off; Be careful not to let CHIP_PU The pin is floating.
GPIO3	8	I/O/T	VDD3P3_RTC	GPIO3, ADC1_CH3
MTMS	9	I/O/T	VDD3P3_RTC	GPIO4, ADC1_CH4, FSPIHD, MTMS
MTDI	10	I/O/T	VDD3P3_RTC	GPIO5, ADC2_CH0, FSPIWP MTDI
VDD3P3_RTC	11	PD	—	RTC power input
MTCK	12	I/O/T	VDD3P3_CPU	GPIO6, FSPICLK, MTCK
MTDO	13	I/O/T	VDD3P3_CPU	GPIO7, FSPID, MTDO
GPIO8	14	I/O/T	VDD3P3_CPU	GPIO8
GPIO9	15	I/O/T	VDD3P3_CPU	GPIO9
GPIO10	16	I/O/T	VDD3P3_CPU	GPIO10, FSPICS0
VDD3P3_CPU	17	PD	—	CPU IO power input
VDD_SPI	18	I/O/T/PD	VDD3P3_CPU	GPIO11, flash Power Output
SPIHD	19	I/O/T	VDD3P3_CPU	GPIO12, SPIHD
SPIWP	20	I/O/T	VDD3P3_CPU	GPIO13, SPIWP
SPICS0	twenty one	I/O/T	VDD3P3_CPU	GPIO14, SPICS0
SPICLK	twenty two	I/O/T	VDD3P3_CPU	GPIO15, SPICLK
SPID	twenty three	I/O/T	VDD3P3_CPU	GPIO16, SPID
SPIQ	twenty four	I/O/T	VDD3P3_CPU	GPIO17, SPIQ
GPIO18	25	I/O/T	VDD3P3_CPU	GPIO18, USB_D-
GPIO19	26	I/O/T	VDD3P3_CPU	GPIO19, USB_D+
U0RXD	27	I/O/T	VDD3P3_CPU	GPIO20, U0RXD
U0TXD	28	I/O/T	VDD3P3_CPU	GPIO21, U0TXD
XTAL_N	29	—	—	External main crystal output
XTAL_P	30	—	—	External main crystal input
VDDA	31	PA	—	Analog power
VDDA	32	PA	—	Analog power
GND	33	G	—	Grounded

Description:

1. P : Power supply pin; I :enter; O : , T : Can be set to high impedance.
2. ESP32-C3FH4 Pin VDD_SPI , SPIHD , SPIWP , SPICS0 , SPICLK , SPIQ with SPID Already used to connect embedded flash , Not recommended for other functions.
3. ESP32-C3 Series chips and flash Please refer to the chapter for the connection of the data port of the chip 2 Function description.
4. The pin functions in this table only refer to some fixed settings. GPIO The input and output signals of the matrix are not limited by this table. related GPIO exchange For more information about the matrix, please refer to " ESP32-C3 Technical Reference Manual.

2.3 Power management

ESP32-C3 The digital pins can be divided into three different power domains:

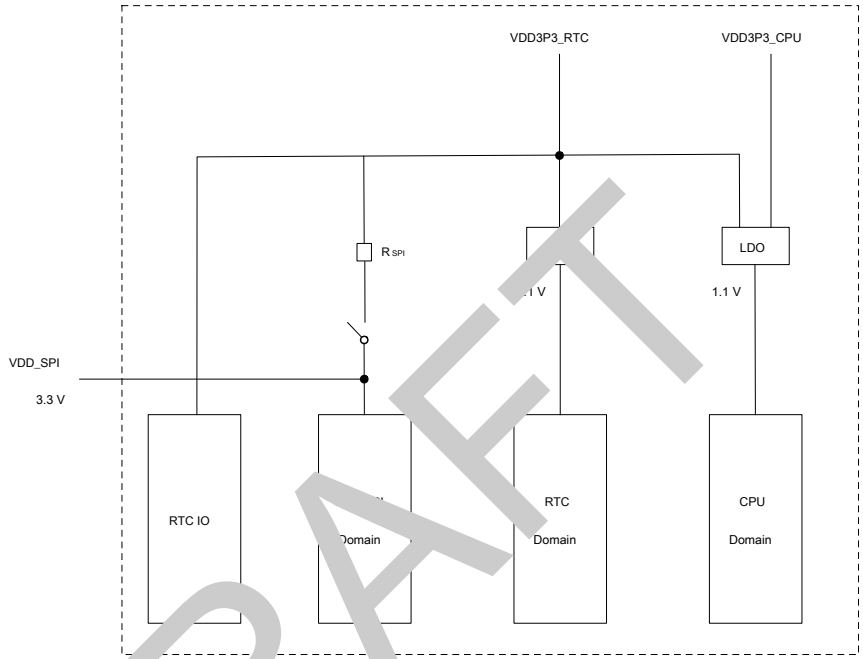
- VDD3P3_CPU
- VDD_SPI
- VDD3P3_RTC

VDD3P3_CPU Yes CPU Input power.

VDD_SPI Can be used as input power or output power.

VDD3P3_RTC At the same time RTC with CPU Input power.

ESP32-C3 The digital power management is shown in the figure 4 Shown:



igure 4: ES Digital power management

VDD_SPI When used as an output er source, VDD3P3_ Through tance R SPI Rear power supply (typical voltage 3.3 V). in Deep-sleep Mode, in order to make flash Leakage is minimized and can be turned off by software VDD_ ower supply.

3. Function description

This chapter describes ESP32-C3 Various functional modules.

3.1 CPU And storage

3.1.1 CPU

ESP32-C3 Series equipped with low power consumption RISC-V 32 A single-core processor with the following characteristics:

- Four-stage pipeline architecture, support 160 MHz Clock frequency
- RV32IMC ISA
- stand by 32 Bit multiplier, 32 Bit divider
- Support the most 32 Vector interrupts, total 7 Priority
- Support the most 8 Hardware breakpoints/watchpoints
- Support the most 16 A PMP area
- For debugging JTAG interface

3.1.2 On-chip storage

ESP32-C3 On-chip storage includes:

- 384 KB **of** ROM : Used for program startup and kernel function call
- 400 KB **Chip** SRAM : Used for data and instruction storage
- RTC **Memory** :for 8 KB of SRAM , Can be mastered CPU Visi… Deep-sleep Data … be saved in mode
- 4 Kbit **of** eFuse :among them 1792 Bits are reserved for user use, for exa…e to store … devices ID

3.1.3 external flash

ESP32-C3 Support multiple external SPI , Du… PI , Quad SP… with QPI flas…

CPU The command space and read-only data space can be… …o the outside flash ,external flash Can support 16 MB . ESP32-C3 Support based on XTS-AES Hardware encryption and decry… …protect u… …pers flash Programs and data in.

Through the cache, ESP… C3 At most, you c… have:

- 8 MB The command space is 6… The blocks are m… …ed to flash ,stand by 8 Bit, 16 Bit sum 32 Bit read.
- 8 MB Data space with 64 KB The blo… …apped to flash ,stand by 8 Bit, 16 Bit sum 32 Bit read.

> **Description:**
>
> After the chip is started, the software can customize off-chip flash To CPU Mapping of address space.

3.1.4 Memory map

ESP32-C3 The address mapping structure is shown in the figure 5 Shown.

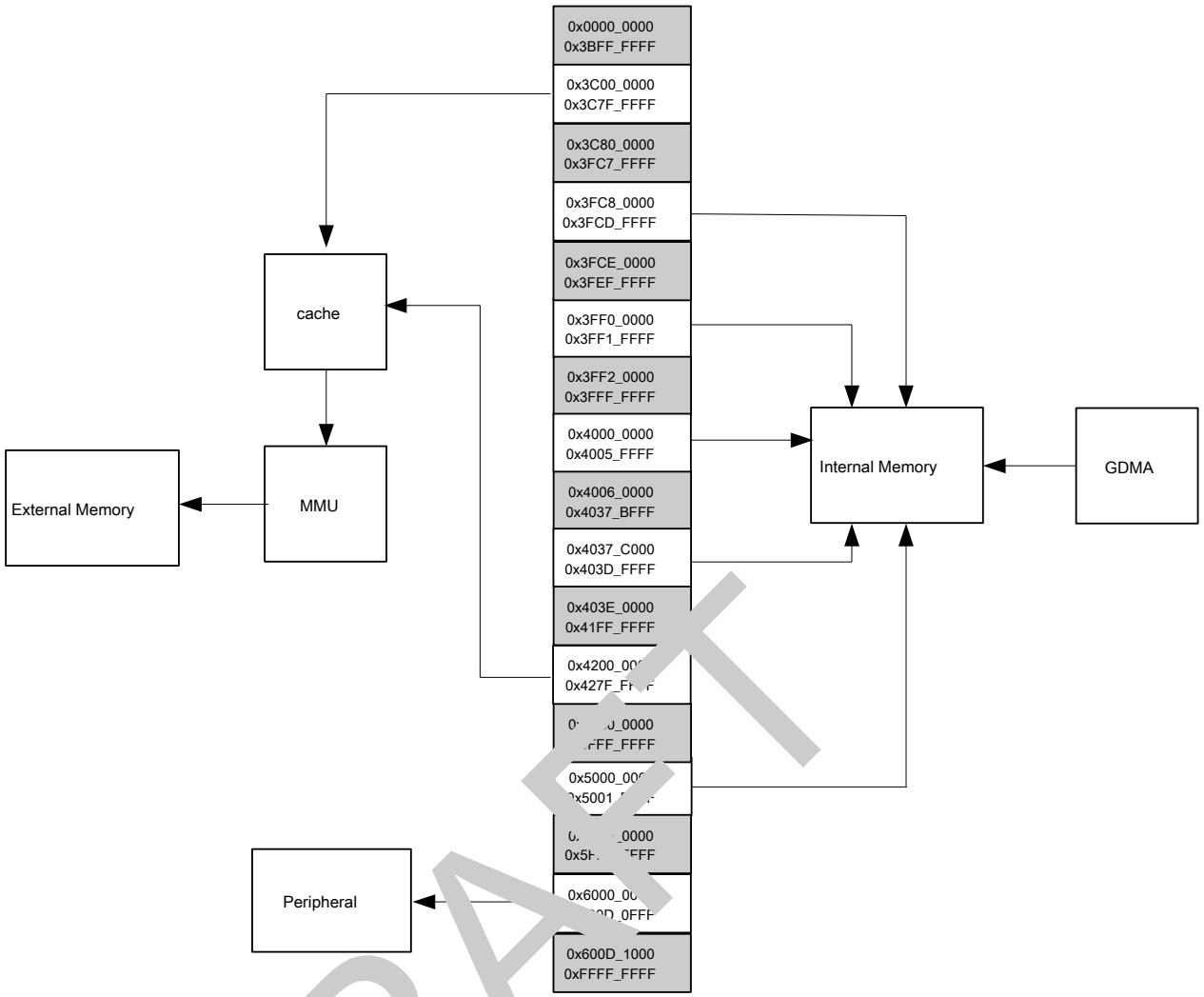


Figure 5: **Address mapping structure**

Description:

The address space marked with a gray backgro... the fi... is not available.

3.1.5 Cache

ESP32-C3 Use eight-way group to connect read-only cache The structure has the following characteristics:

- cache The size is 16 KB
- cache The block size is 32 byte
- stand by pre-load Features
- stand by lock Features
- Support keyword priority (critical word first) And restart early (early restart)

3.2 System clock

3.2.1 CPU clock

CPU There are three possible clock sources for the clock:

- External main crystal oscillator clock
- Built-in 20 MHz Oscillator clock
- PLL clock

The application can be installed in the external main crystal, PLL Clock and built-in 20 MHz Choose one of the clocks as the clock source. According to different applications, the selected clock source is driven directly or after frequency division CPU clock.

3.2.2 RTC clock

RTC Slow clock used RTC counter, RTC There are three possible clock sources for watchdogs and low-power controllers:

- External low speed (32 kHz) Crystal clock
- Built-in RC Oscillator (usually 150 kHz , Frequency can be adjusted)
- Built-in 78.125 kHz Clock (by built-in 20 MHz Oscillator clock 256 Frequency division generation)

RTC Fast clock application RTC Peripherals and sensor controllers, there are 2 Possible clock sources:

- External main crystal oscillator 2 Divided clock
- Built-in 20 MHz Oscillator clock

3.3 Analog peripherals

3.3.1 A/D converter (ADC)

ESP32-C3 Integrated two 12 Bit SAR ADC , Total support 6 Analog chan input.

3.3.2 Temperature Sensor

The temperature sensor generates a voltage that chang ith temperatur ternal ADC Conv the sensor voltage into a digital quantity.

The measuring range of the temperature sensor is – 20 °C To Temperature sensors are generally only suitable for monitoring changes in the internal temperature of the chip, and the temperature value will vary with the microcontroller c requency The loa es. Generally speaking, the internal temperature of the chip will be higher than the external temperature.

3.4 Digital peripherals

3.4.1 Universal input/output interface ( )

ESP32-C3 Share twenty two A GPIO Pins can be assigned different functions by configuring the corresponding registers. Except as digital signal pins, some GPIO The pins can also be configured as analog function pins, such as ADC Wait for the pins.

all GPIO Both can choose internal pull-up/pull-down or set to high impedance. When configured as an input, the input value can be obtained by reading the register. enter Pins can also be set to be generated by edge trigger or level trigger CPU Interrupted. digital IO The pins are bidirectional, non-inverting and tri-state, including input and output buffers with tri-state control. These pins can be reused for other functions, such as UART , SPI Wait. When the chip runs at low power consumption Time, GPIO Can be set to hold state.

IO MUX with GPIO The switching matrix is used to transmit signals from peripherals to GPIO pad . The two together make up the chip IO control. use GPIO Switching matrix, the input signal of the configurable peripheral module comes from any IO Pin, and the output signal of the peripheral module can also be connected to any IO Pin.

3.4.2 Serial Peripheral Interface (SPI)

ESP32-C3 There are three SPI (SPI0 , SPI1 with SPI2). SPI0 with SPI1 Can only be configured as SPI Memory mode, SPI2 Can be configured as SPI Memory mode can be configured as universal SPI mode.

- SPI **Memory (** SPI Memory) **mode**

  SPI Memory mode (SPI0 , SPI1 with SPI2) To connect SPI External memory of the interface. SPI The data transfer length in memory mode is in bytes, and supports up to four lines STR Read and write operations. The clock frequency is configurable, STR The highest clock frequency supported in the mode is 120 MHz .

- SPI2 **Universal** SPI (GP-SPI) **mode**

  SPI2 As universal SPI It can be configured as master mode or slave mode. Both master mode and slave mode support dual-line full-duplex and single-line, dual-line or four-line half-duplex communication. Universal SPI The host clock frequency is configurable; the data transmission length is in bytes;

  Clock polarity (CPOL) And phase (CPHA) Configurable; connectable GDMA aisle.

  - In the two-wire full-duplex communication mode, the highest clock frequency of the master and slave is 80 MHz . stand by SPI Four clock modes of transmission.
  - In the host single-wire, two-wire or four-wire half-duplex communication mode, the maximum clock frequency is 80 MHz ,stand by SPI Four clock modes of transmission.
  - In the slave single-wire, two-wire or four-wire half-duplex communication mode, the clock frequency is up to 6[illegible]z , Also supports SPI Four clock modes of transmission.

usually, ESP32-C3 with flash The data port connection relationship of the chip is:

SPI **In 4-wire mode** :

- SPID (SPID) = IO0
- SPIQ (SPIQ) = IO1
- SPIWP (SPIWP) = IO2
- SPIHD (SPIHD) = IO3

SPI **In two-wire mode** :

- SPID (SPID) = IO0
- SPIQ (SPIQ) = IO1

SPI **In single-line mode** :

- SPIQ (SPIQ) = DO
- SPID (SPID) = DI
- SPIHD (SPIHD) = HOLD#
- SPIWP (SPIWP) = WP#

3.4.3 Universal Asynchronous Receiver Transmitter (UART)

ESP32-C3 There are two UART Interface, ie UART0 with UART1 , Supports asynchronous communication (RS232 with RS485)with IrDA , The communication rate can reach 5 Mbps . UART stand by CTS with RTS Signal hardware flow control and software flow control (XON with XOFF) . Two UART Interface through the total use UHCI0 Interface with GDMA Connected, can be GDMA Visit or CPU direct interview.

3.4.4 I2C interface

ESP32-C3 Have a I2C Bus interface, according to the user's configuration, the bus interface can be used as I2C Master or slave mode. I2C Interface support:

- Standard mode (100 Kbit/s)

- Quick mode (400 Kbit/s)
- Up to speed 800 Kbit/s , But subject to SCL with SDA Pull-up strength

• 7 Bit addressing mode and 10 Bit addressing mode

- Dual addressing mode

• 7 Bit broadcast address

The user can configure the instruction register to control I2C Interface to achieve more flexible applications.

3.4.5 I2S interface

ESP32-C3 There is a standard I2S The interface can work in master or slave mode, in full-duplex or half-duplex mode, and can be configured as I2S

Serial 8/16/24/32 Bit mode of sending and receiving data, support frequency from 10 kHz To 40 MHz of BCK clock.

I2S Interface connection GDMA Controller. stand by TDM PCM , TDM MSB Align, TDM Standard and PDM TX interface.

3.4.6 Infrared remote control

Infrared remote control (RMT) Support dual-channel infrared emission and dual-channel infrared reception. The pulse waveform is controlled by the program, the remote control can support a variety of

Infrared protocol and single wire protocol. Four channels share one 192 × 32 Bit storage module to store the received and sent waveforms.

3.4.7 LED PWM Controller

LED PWM The controller can be used to generate six independent digital waveforms, with the following characteristi

- The period and duty cycle of the waveform can be configured, and the duty cycle accuracy is u .8 Bit
- Multiple clock source options, including APB Bus clock, external main crystal oscillator c
- Available at Light-sleep Work in mode
- Support hardware to increase or decrease the duty cycle step by step auto ifica can be used fo RGB Color gradient generator

3.4.8 Universal DMA Controller

ESP32-C3 Contains a six-channel universal DMA Controller reviated GD), including sending channels and three receiving channels, each channel is independent of each other. These six

channels are DMA Functions are shared by peripherals, dynamic pric ted betwe channels.

Universal DMA The controller is based on the linked list to realiz control of data transmission and reception, and supports the high speed between the peripheral and the memory and between the memory and the memory

data transmission. Each channel supp ccess to on- PAM .

ESP32-C3 Six peripherals e DMA Function, t e six peripherals are SPI2 , UHCI0 , I2S , AES , SHA with ADC .

3.4.9 USB equipment

ESP32-C3 Includes a support USB 1.1 Full speed US Equipment module. USB The device module contains two channels, one is compatible USB CDC ACM Virtual serial channel and a USB turn JTAG aisle.

Except control endpoint 0 outside, USB The equipment module also contains three IN Endpoints and two

OUT Endpoint. The maximum packet length it supports is 64 byte.

USB The host can send commands to USB Device, make the chip enter the download mode and control the chip USB The digital part outside the device is reset.

3.4.10 TWAI Controller

ESP32-C3 With a TWAI The controller has the following characteristics:

- compatible ISO 11898-1 protocol
- Support standard frame format (11 Bit ID) And extended frame format (29 Bit ID)
- Bit rate from 1 Kbit/s To 1 Mbit/s

- Multiple operation modes: working mode, monitoring mode and self-check mode (transmission without confirmation)
- 64 Byte receive FIFO
- Data receiving filter (support single filter and double filter mode)
- Error detection and processing: error counter, configurable error interrupt threshold, error code record, arbitration loss record

3.5 RF and Wi-Fi

ESP32-C3 The radio includes the following main modules:

- 2.4 GHz receiver
- 2.4 GHz launcher
- Offset (Bias) And linear regulator
- Balun And transceiver switch
- Clock generator

3.5.1 2.4 GHz receiver

2.4 GHz The receiver will 2.4 GHz The RF signal is demodulated into a quadrature baseband signal, and two high-precision, low-speed ADC Convert the latter to a digital signal. In order to adapt to different channel conditions, ESP32-C3 Integrated RF Filter, automatic gain control (AGC) , DC Offset compensation circuit and baseband filter.

3.5.2 2.4 GHz launcher

2.4 GHz The transmitter modulates the quadrature baseband signal to 2.4 GHz RF signal, using high-performance complementary metal oxide semiconductor (CMOS) The power amplifier drives the antenna. Digital calibration further improves the linearity of the power amplifier.

In order to offset the defects of the RF receiver, ESP32-C3 Calibration measures have also been adopted, such as:

- Carrier leakage elimination
- I/Q Phase matching
- Baseband nonlinear suppression
- RF nonlinear suppression
- Antenna matching

These built-in calibration measures shorten the test time of the product and no longer need test equipment.

3.5.3 Clock generator

Clock generator generates for receiver and transmitter 2.4 GHz For quadrature clock signals, all components are integrated on the chip, including inductors, varactor diodes, loop filters, linear regulators and frequency dividers.

The clock generator has a built-in calibration circuit and a self-test circuit. Using optimization algorithms with independent intellectual property rights, the phase and phase noise of the quadrature clock Optimized processing, so that the receiver and transmitter have the best performance.

3.5.4 Wi-Fi RF and baseband

ESP32-C3 Wi-Fi The radio frequency and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 stand by 20 MHz with 40 MHz bandwidth

- 802.11n MCS32
- 802.11n 0.4 μs Guard interval
- Data rate up to 150 Mbps
- receive STBC (Single spatial stream)
- Adjustable transmit power
- Antenna diversity

  ESP32-C3 Support antenna diversity and selection based on external RF switches. The external RF switch consists of one or more GPIO Pin control is used to select the most suitable antenna to reduce the influence of channel fading.

3.5.5 Wi-Fi MAC

ESP32-C3 Follow exactly 802.11 b/g/n Wi-Fi MAC Protocol stack, supporting distributed control function (DCF) Set of basic services under (BSS) STA with SoftAP operating. Supports optimization of effective working hours by minimizing host interaction to achieve power management.

ESP32-C3 Wi-Fi MAC The underlying protocol functions supported by itself are as follows:

- 4 × virtual Wi-Fi interface
- At the same time support infrastructure network (Infrastructure BSS) Station mode, SoftAP Pattern and Station + SoftAP Promiscuous mode
- RTS protection, CTS Protection, immediate block reply (Immediate Block ACK)
- Fragmentation and reorganization (Fragmentation and defragmentation)
- TX/RX A-MPDU , RX A-MSDU
- TXOP
- Wireless Multimedia (WMM)
- GCMP , CCMP , TKIP , WAPI , WEP with BIP
- automatic Beacon Monitoring (hardware TSF)
- 802.11mc FTM

3.5.6 **Networking characteristics**

Firmware support provided by Espressif lightweight IP network, ESP-WIFI-MESH Internet or other Wi-Fi Networking protocol and also supports TLS 1.0 , 1.1 , 1.2 .

3.6 **Bluetooth Low Energy**

ESP32-C3 Contains a Bluetooth Low Energy (Bluetooth Low Energy) The subsystem integrates a hardware link layer controller, radio frequency/modem module and a fully functional software protocol stack. Bluetooth Low Energy Subsystem Support Bluetooth 5 with Bluetooth mesh .

3.6.1 **Bluetooth low energy radio frequency and physical layer**

ESP32-C3 The Bluetooth low energy radio frequency and physical layer support the following features:

- 1 Mbps PHY
- 2 Mbps PHY , Used to increase transmission speed and data throughput
- Coded PHY (125 Kbps and 500 Kbps) , Used to improve receiving sensitivity and transmission distance
- No external PA , Can support up to + 20 dBm Transmit power

• NZIF The receiver has high sensitivity, 1 Mbps The receiving sensitivity at speed is- 97 dBm ,in 125 Kbps The receiving sensitivity at speed is- 102 dBm

- Hardware implementation Listen Before Talk (LBT)
- Antenna diversity (Antenna diversity) : Support antenna diversity and selection with external RF switch. The external RF switch consists of one or more GPIO Pin control, used to select the most suitable antenna to reduce the influence of channel attenuation

3.6.2 Bluetooth Low Energy Link Layer Controller

ESP32-C3 The Bluetooth low energy link controller supports the following features:

- Broadcast extension (Advertising Extensions) , Used to enhance broadcasting capabilities, can broadcast more intelligent data
- Multicast
- Support simultaneous broadcasting and scanning
- Multiple connections, support center equipment (Central) And peripheral equipment (Peripheral) Run simultaneously
- Adaptive frequency hopping and channel selection
- Channel selection algorithm # 2 (Channel Selection Algorithm #2)
- Connection parameter update
- High-speed unconnectable broadcast (High Duty Cycle Non-Connectable Advertising)

• LE Privacy 1.2

- Packet length extension (LE Data Packet Length Extension)
- Link layer extended scan filtering strategy (Link Layer Extended Scanner Filter p...as)
- Low-speed connectable directed broadcast (Low duty cycle directed a...g)
- Link layer encryption

• LE Ping

3.7 Low power management

ESP32-C3 Using advanced power manag...y, you ca...itch between different power consumption modes. ESP32-C3 The supported power modes are:

• Active mode: CPU And th...p radio frequency is in ...ing condit...n. The chip can receive, transmit and listen to signals.

• Modem-sleep mode: CPU Can ...lock frequency ca...configured. Wi-Fi and Bluetooth LE Baseband and radio frequency are turned off, but Wi-Fi or Bluetooth LE Can stay conn...d.

• Light-sleep mode: CPU Suspend operation. Any wakeup event (MAC , Host, RTC Timer or external interrupt) will wake up the chip. Wi-Fi or Bluetooth LE Can stay connected.

• Deep-sleep mode: CPU And most peripherals will be powered down, only RTC The memory is working. Wi-Fi Connection data is stored in RTC in.

• Hibernation Mode: Built-in 20 MHz The oscillator is disabled. only 1 On a low-speed clock RTC The clock timer is working. RTC Clock timer or RTC GPIO You can change the chip from Hibernation Wake up in mode.

3.8 Timer

3.8.1 Universal timer

ESP32-C3 Built-in two 54 Bit general-purpose timer with 16 Bit divider and 54 Up/down timer with automatic reload. The timer has the following functions:

- 16 Bit clock prescaler, the division factor is 1-65536
- 54 Bit time base counter can be configured to increment or decrement
- Read the real-time value of the time base counter
- Pause and resume time base counter
- Configurable alarm generation mechanism
- Level triggered interrupt

3.8.2 System timer

ESP32-C3 Built-in 52 Bit system timer, the system timer contains two 52 The clock counter and three alarm comparators have the following functions:

- The frequency of the clock counter is fixed at 16 MHz
- Three alarm comparators can generate three independent interrupts according to different alarm values
- Two alarm modes: single specific alarm value alarm and periodic alarm
- Support settings 52 Bit single specific alarm value and 26 Periodic alarm value of the bit
- Counter value reload
- Support when CPU Paused or in OCD In mode, the clock counter is also

3.8.3 Watchdog timer

ESP32-C3 There are three watchdog timers: one in each of the two timer groups (called main system watchdog timer, abbreviated as MWDT) , RTC One of the modules (called RTC Watchdog timer, abbreviated as RWDT)

At boot load flash During the firmware, RWDT And timer group MWDT It will be automatically enabled to detect errors during the boot process and resume operation.

The watchdog timer has the following characteristics:

- Four stages, each stage can be configured with a timeout period. Each stage can be individually configured, enabled and closed.
- If a timeout occurs at a certain stage, Will take interruption, CPU One of the three timeout actions of reset and core reset, RWDT Will take interruption, CPU One of the four timeout actions of reset, core reset and system reset.
- protection 32 Bit timeout counter
- prevent RWDT with MWDT The configuration of was changed by mistake.
- flash Start protection

  If within the scheduled time SPI flash If the boot process is not completed, the watchdog will restart the entire main system.

3.9 Encrypted hardware accelerator

ESP32-C3 Equipped with a hardware accelerator to support some common encryption algorithms, such as AES-128/AES-256 (FIPS PUB 197) , ECB/CBC/OFB/CFB/CTR (NIST SP 800-38A) , SHA1/SHA224/SHA256 (FIPS PUB 180-4) , RSA3072 with ECC Etc, also supports large numbers

Independent operations such as multiplication and large number modular multiplication, among which RSA The maximum length of modular multiplication operations with large numbers can reach 3072 Bits, the maximum length

1536 Bit.

3.10 Physical security features

- external flash by AES-XTS The algorithm is encrypted, and the key used by the encryption algorithm cannot be read and written by the software, so the user's application code and data will not be illegally obtained.
- The safe start function ensures that only signed (with RSA-PSS Signature) firmware, the credibility of this function is rooted in the hardware logic.
- HMAC The module can use a security key that is inaccessible to the software to generate an authentication or other purpose MAC signature.
- The digital signature module can be accessed using software RSA Key generation for authentication RSA signature.
- The world controller module provides two software operating environments, which can divide all hardware and software resources into two types and place them in the safe area and the general Through the area, it is ensured that ordinary area hardware cannot access the safe area, thereby building a safe boundary between these two areas.

3.11 Peripheral pin assignment

table 3: **Peripheral and sensor pin assignment**

interface	signal	Pin	Features
ADC	ADC1_CH0	GPIO0	Two [illegible] Bit SAR [illegible]C
	ADC1_CH1	GPIO1	
	ADC1_CH2	GPIO2	
	ADC1_CH3	GPIO3	
	ADC2_CH0	GPIO5	
JTAG	MTDI	MTDI	Softw[illegible]ebugging JTAG
	MTCK	MTCK	
	MTMS	MTMS	
	MTDO	M[illegible]DO	
UART	U0RXD_in	[illegible]trary GPIO Two [illegible]s UART Equipment, supports hardware flow control and GDMA	
	U0CTS_in		
	U0DSR_i		
	U0T[illegible]_out		
	U0R[illegible]ut		
	U0DTR_o		
	U1RXD_in		
	U1CTS_in		
	U1DSR_in		
	U1TXD_out		
	U1RTS_out		
	U1DTR_out		

interface	signal	Pin	Features
I2C	I2CEXT0_SCL_in	Arbitrary GPIO	One pin I2C Device, support master or slave mode
	I2CEXT0_SDA_in		
	I2CEXT1_SCL_in		
	I2CEXT1_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
	I2CEXT1_SCL_out		
	I2CEXT1_SDA_out		
LED PWM	ledc_ls_sig_out0~5	Arbitrary GPIO	Six independent channels on pins; clock selectable 80 MHz clock/ RTC Time bell/ XTAL clock. Duty cycle accuracy: 14 Bit.
I2S	I2SO_BCK_in	Arbitrary GPIO	The pin is used for the input and output of serial stereo data.
	I2S_MCLK_in		
	I2SO_WS_in		
	I2SI_SD_in		
	I2SI_BCK_in		
	I2SI_WS_in		
	I2SO_BCK_out		
	I2S_MCLK_out		
	I2SO_WS_out		
	I2SO_SD_out		
	I2SI_BCK_out		
	I2SI_WS_out		
	I2SO_SD1_out		
Infrared remote control	RMT_SIG_IN0~1	Arbitrary	The transceiv supports different waveform standards.
	RMT_SIG_OUT0~1		
SPI0/1	SPICLK_out_mux	ICLK	stand by SPI , Dual SPI , Quad SPI ,with QPI , Can be connected outside the chip flash .
	SPICS0_out	S CS0	
	SPICS1_out		
	SPID_in/_out	SPID	
	SPIQ_in/_out	SPIQ	
	SPIWP_in/_out	SPIWP	
	SPIHD_in/_out	SPIHD	
SPI2	FSPICLK_in/_out_mux	Arbitrary GPIO Pin	The following functions are supported: • SPI , Dual SPI , Quad SPI with QPI Master-slave mode; • Can be connected outside the chip flash , RAM and other SPI equipment • SPI Four clock modes of transmission; • Configurable SPI frequency; • 64 Byte buffer or GDMA Data cache.
	FSPICS0_in/_out		
	FSPICS1~5_out		
	FSPID_in/_out		
	FSPIQ_in/_out		
	FSPIWP_in/_out		
	FSPIHD_in/_out		