# USI Register

D.E. 2010

## USICTL0 - USI Control Register 0

| | | | 0 | 1 |
|---|---|---|---|---|
| Bit 7 | **USIPE7** | **USI SDI/SDA Port Enable** | function disabled | function enabled |
| Bit 6 | **USIPE6** | **USI SDO/SCL Port Enable** | function disabled | function enabled |
| Bit 5 | **USIPE5** | **USI SCLK Port Enable** | function disabled | function enabled |
| Bit 4 | **USILSB** | **LSB First Select** | MSB first | LSB first |
| Bit 3 | **USIMST** | **Master Select** | slave mode | master mode |
| Bit 2 | **USIGE** | **Output Latch Control** | latch enable depends on shift clk | latch enabled/transparent |
| Bit 1 | **USIOE** | **Data Output Enable** | output disabled | output enabled |
| Bit 0 | **USISWRST** | **USI Software Reset** | USI released for operation | USI logic held in reset state |

## USICTL1 - USI Control Register 1

| | | | 0 | 1 |
|---|---|---|---|---|
| Bit 7 | **USICKPH** | **Clock Phase Select** | data changed on 1st edge / captured on 2nd | data captured on 1st edge / changed on 2nd |
| Bit 6 | **USII2C** | **I2C Mode Enable** | I2C mode disabled | I2C mode enabled |
| Bit 5 | **USISTTIE** | **START Condition Int. Enable** | interrupt on START condition disabled | interrupt on START condition enabled |
| Bit 4 | **USIIE** | **USI Counter Interrupt Enable** | interrupt disabled | interrupt enabled |
| Bit 3 | **USIAL** | **Arbitration Lost** | no arbitration lost condition | arbitration lost |
| Bit 2 | **USISTP** | **STOP Condition Received** | no STOP condition received | STOP condition received |
| Bit 1 | **USISTTIFG** | **START Condition IFG** | no START condition received / no interrupt pending | output enabled |
| Bit 0 | **USIIFG** | **USI Counter Interrupt Flag** | no interrupt pending | interrupt pending |

## USICKCTL - USI Clock Control Register

| | | | 0 | 1 |
|---|---|---|---|---|
| Bit 7<br>Bit 6<br>Bit 5 | **USIDIVx** | **Clock Divider Select** | 000 divide by 1<br>001 divide by 2<br>010 divide by 4<br>011 divide by 8 | 100 divide by 16<br>101 divide by 32<br>110divide by 64<br>111 divide by 128 |
| Bit 4<br>Bit 3<br>Bit 2 | **USISSELx** | **Clock Source Select** | 000 SCLK (not used in SPI mode)<br>001 ACLK<br>010 SMCLK<br>011 SMCLK | 100 USISWCLK bit<br>101 TACCR0<br>110 TACCR1<br>111 TACCR2 |
| Bit 1 | **USICKPL** | **Clock Polarity Select** | inactive state is low | inactive state is high |
| Bit 0 | **USISWCLK** | **Software Clock** | input clock is low | input clock is high |

## USICNT - USI Bit Counter Register

| | | | 0 | 1 |
|---|---|---|---|---|
| Bit 7 | **USISCLREL** | **SCL Release - SCL low to idle** | SCL line is held low if USIIFG is set | SCL line is released |
| Bit 6 | **USI16B** | **16-Bit Shift Register Enable** | 8-Bit mode - low byte USISRL is used | 16-Bit mode - USISRL/USISRH are used |
| Bit 5 | **USIIFGCC** | **USI IFG Clear Control** | USIIFG auto cleared on USICNT > 0 update | USIIFG is not cleared automatically |
| Bit 4<br>Bit 3<br>Bit 2<br>Bit 1<br>Bit 0 | **USICNTx** | **USI Bit Count** | USICNT bits set the number of bits to be received or transmitted | |

## USISRL - USI Low Byte Shift Register

| | | | |
|---|---|---|---|
| Bit 7-0 | **USISRLx** | **USI Low Byte Shift Register** | contents of the USI low byte shift register |

## USISRH - USI High Byte Shift Register

| | | | |
|---|---|---|---|
| Bit 7-0 | **USISRHx** | **USI High Byte Shift Register** | contents of the USI high byte shift register |