SSD1353

Product Preview

160RGB x 132 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

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FIGURES

1 GENERAL DESCRIPTION

The SSD1353 is a CMOS OLED/PLED driver with 480 segments and 132 commons output, supporting up to 160RGB x 132 dot matrix display. This chip is designed for Common Cathode type OLED/PLED panel.

The SSD1353 had embedded Graphic Display Data RAM (GDDRAM). It supports with 8, 9, 16, 18 bits 8080 / 6800 parallel interface as well as Serial Peripheral Interface. It has 256-step contrast and 262K color control, giving vivid color display to OLED panels. This driver IC can be widely used in many applications such as MP3, PDA, PMP, mobile phone and Digital Camera.

2 FEATURES

- Resolution: 160 RGB x 132 dot matrix panel
- Portrait and Landscape mode data input
- 262k color depth supported by embedded 160x132x18 bit SRAM display buffer
- Power supply
  - V_{DD} = 2.4V – 2.6V (Core V_{DD} power supply)
  - V_{DDIO} = 1.6V – V_{CI} (MCU interface logic level)
  - V_{CI} = 2.4V - 3.5V (Low voltage power supply)
  - V_{CC} = 10.0V – 21.0V (Panel driving power supply)
- Segment maximum source current: 160uA
- Common maximum sink current: 60mA
- 256 step brightness current control for the each color component plus 16 step master current control
- Pin selectable MCU Interfaces:
  - 8/9/16/18 bits 6800-series parallel interface
  - 8/9/16/18 bits 8080-series parallel interface
  - Serial Peripheral Interface
- Color swapping function (RGB – BGR)
- Support various color depth
  - 262k color (6:6:6)
  - 65k color (5:6:5)
  - 256 color (3:3:2)
- Screen saving continuous scrolling function in both horizontal and vertical action
- Graphic Accelerating Command (GAC) set
- Programmable Gamma functions
- RAM write synchronization signal
- Programmable Frame Rate
- On Chip Oscillator
- Power saving mode
- Dim mode
- Non-Volatile Memory (OTP) for calibration
- Slim chip layout best suit for COF
- Operating temperature range -40°C to 85°C.

3 ORDERING INFORMATION

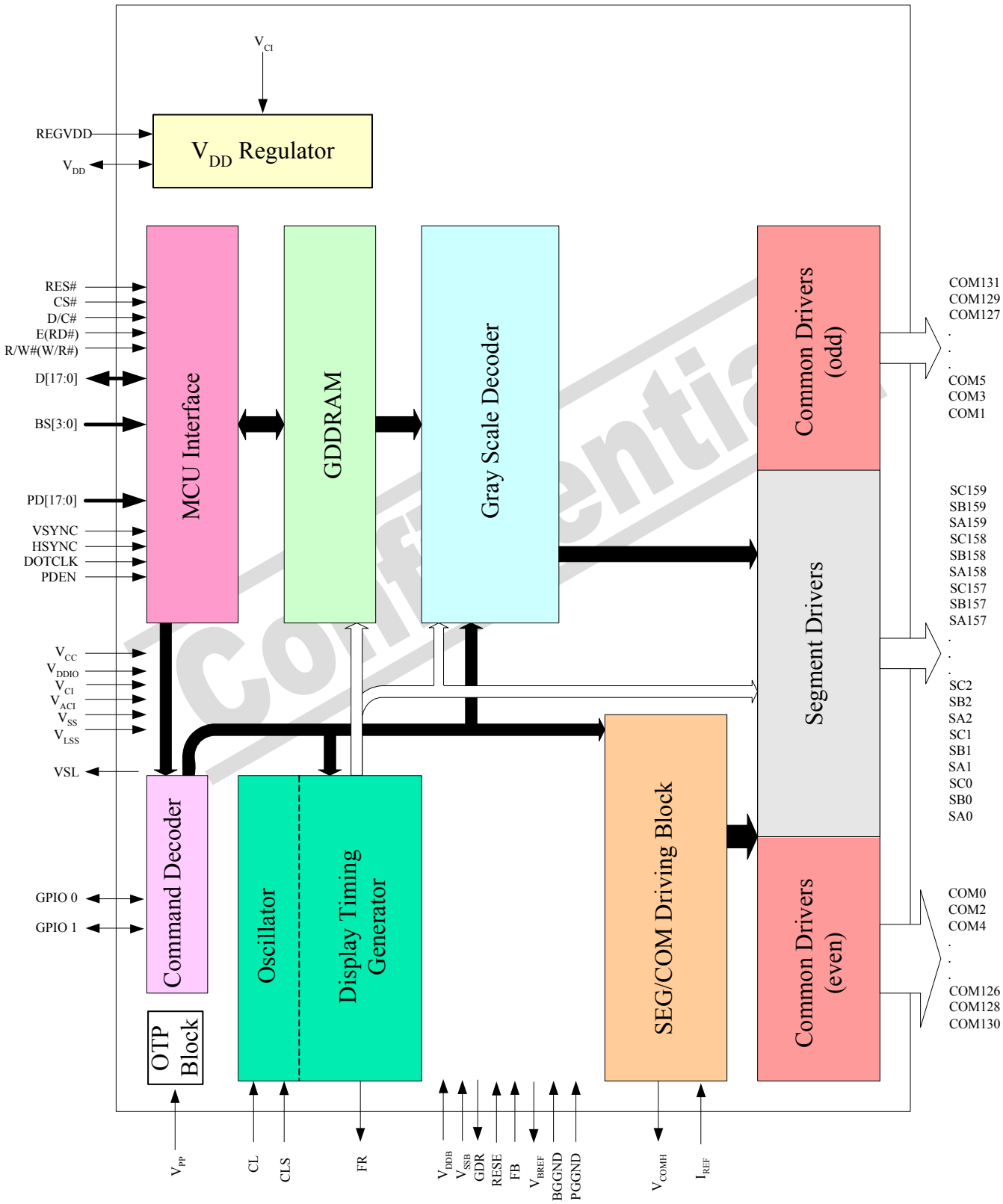
Table 3-1 :Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark

SSD1353U4R1	160RGB	128	COF	Page 9, 63	• 48mm film, 5 sprocket holes
					• Output lead pitch:
					  • SEG: 0.05mm x 0.999=0.04995mm
					  • COM: 0.07mm x 0.999=0.06993mm
					• 8-/9-/16-/18-bit 80 / 68 parallel & SPI interface

4 BLOCK DIAGRAM

Figure 4-1 : SSD1353 Block Diagram



5 PIN ASSIGNMRNT

5.1 SSD1353U4R1 pin assignment

Table 5-1 : SSD1353U4R1 Pin assignment

Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name
1	NC	81	COM61	161	SA148	241	SB121	321	SC94
2	VCC	82	COM59	162	SC147	242	SA121	322	SB94
3	VCOMH	83	COM57	163	SB147	243	SC120	323	SA94
4	VLSS	84	COM55	164	SA147	244	SB120	324	SC93
5	VSS	85	COM53	165	SC146	245	SA120	325	SB93
6	IREF	86	COM51	166	SB146	246	SC119	326	SA93
7	D17	87	COM49	167	SA146	247	SB119	327	SC92
8	D16	88	COM47	168	SC145	248	SA119	328	SB92
9	D15	89	COM45	169	SB145	249	SC118	329	SA92
10	D14	90	COM43	170	SA145	250	SB118	330	SC91
11	D13	91	COM41	171	SC144	251	SA118	331	SB91
12	D12	92	COM39	172	SB144	252	SC117	332	SA91
13	D11	93	COM37	173	SA144	253	SB117	333	SC90
14	D10	94	COM35	174	SC143	254	SA117	334	SB90
15	D9	95	COM33	175	SB143	255	SC116	335	SA90
16	D8	96	COM31	176	SA143	256	SB116	336	SC89
17	D7	97	COM29	177	SC142	257	SA116	337	SB89
18	D6	98	COM27	178	SB142	258	SC115	338	SA89
19	D5	99	COM25	179	SA142	259	SB115	339	SC88
20	D4	100	COM23	180	SC141	260	SA115	340	SB88
21	D3	101	COM21	181	SB141	261	SC114	341	SA88
22	D2	102	COM19	182	SA141	262	SB114	342	SC87
23	D1	103	COM17	183	SC140	263	SA114	343	SB87
24	D0	104	COM15	184	SB140	264	SC113	344	SA87
25	E	105	COM13	185	SA140	265	SB113	345	SC86
26	R/W#	106	COM11	186	SC139	266	SA113	346	SB86
27	D/C#	107	COM9	187	SB139	267	SC112	347	SA86
28	RESB	108	COM7	188	SA139	268	SB112	348	SC85
29	CSB	109	COM5	189	SC138	269	SA112	349	SB85
30	FR	110	COM3	190	SB138	270	SC111	350	SA85
31	BS3	111	COM1	191	SA138	271	SB111	351	SC84
32	BS2	112	NC	192	SC137	272	SA111	352	SB84
33	BS1	113	NC	193	SB137	273	SC110	353	SA84
34	BS0	114	NC	194	SA137	274	SB110	354	SC83
35	REGVDD	115	NC	195	SC136	275	SA110	355	SB83
36	VDDIO	116	NC	196	SB136	276	SC109	356	SA83
37	VDD	117	NC	197	SA136	277	SB109	357	SC82
38	VPP	118	NC	198	SC135	278	SA109	358	SB82
39	VCI	119	NC	199	SB135	279	SC108	359	SA82
40	VSL	120	NC	200	SA135	280	SB108	360	SC81
41	VBREF	121	NC	201	SC134	281	SA108	361	SB81
42	VSS	122	NC	202	SB134	282	SC107	362	SA81
43	VLSS	123	NC	203	SA134	283	SB107	363	SC80
44	VCOMH	124	NC	204	SC133	284	SA107	364	SB80
45	VCC	125	NC	205	SB133	285	SC106	365	SA80
46	NC	126	SC159	206	SA133	286	SB106	366	SC79
47	NC	127	SB159	207	SC132	287	SA106	367	SB79
48	COM127	128	SA159	208	SB132	288	SC105	368	SA79
49	COM125	129	SC158	209	SA132	289	SB105	369	SC78
50	COM123	130	SB158	210	SC131	290	SA105	370	SB78
51	COM121	131	SA158	211	SB131	291	SC104	371	SA78
52	COM119	132	SC157	212	SA131	292	SB104	372	SC77
53	COM117	133	SB157	213	SC130	293	SA104	373	SB77
54	COM115	134	SA157	214	SB130	294	SC103	374	SA77
55	COM113	135	SC156	215	SA130	295	SB103	375	SC76
56	COM111	136	SB156	216	SC129	296	SA103	376	SB76
57	COM109	137	SA156	217	SB129	297	SC102	377	SA76
58	COM107	138	SC155	218	SA129	298	SB102	378	SC75
59	COM105	139	SB155	219	SC128	299	SA102	379	SB75
60	COM103	140	SA155	220	SB128	300	SC101	380	SA75
61	COM101	141	SC154	221	SA128	301	SB101	381	SC74
62	COM99	142	SB154	222	SC127	302	SA101	382	SB74
63	COM97	143	SA154	223	SB127	303	SC100	383	SA74
64	COM95	144	SC153	224	SA127	304	SB100	384	SC73
65	COM93	145	SB153	225	SC126	305	SA100	385	SB73
66	COM91	146	SA153	226	SB126	306	SC99	386	SA73
67	COM89	147	SC152	227	SA126	307	SB99	387	SC72
68	COM87	148	SB152	228	SC125	308	SA99	388	SB72
69	COM85	149	SA152	229	SB125	309	SC98	389	SA72
70	COM83	150	SC151	230	SA125	310	SB98	390	SC71
71	COM81	151	SB151	231	SC124	311	SA98	391	SB71
72	COM79	152	SA151	232	SB124	312	SC97	392	SA71
73	COM77	153	SC150	233	SA124	313	SB97	393	SC70
74	COM75	154	SB150	234	SC123	314	SA97	394	SB70
75	COM73	155	SA150	235	SB123	315	SC96	395	SA70
76	COM71	156	SC149	236	SA123	316	SB96	396	SC69
77	COM69	157	SB149	237	SC122	317	SA96	397	SB69
78	COM67	158	SA149	238	SB122	318	SC95	398	SA69
79	COM65	159	SC148	239	SA122	319	SB95	399	SC68
80	COM63	160	SB148	240	SC121	320	SA95	400	SB68

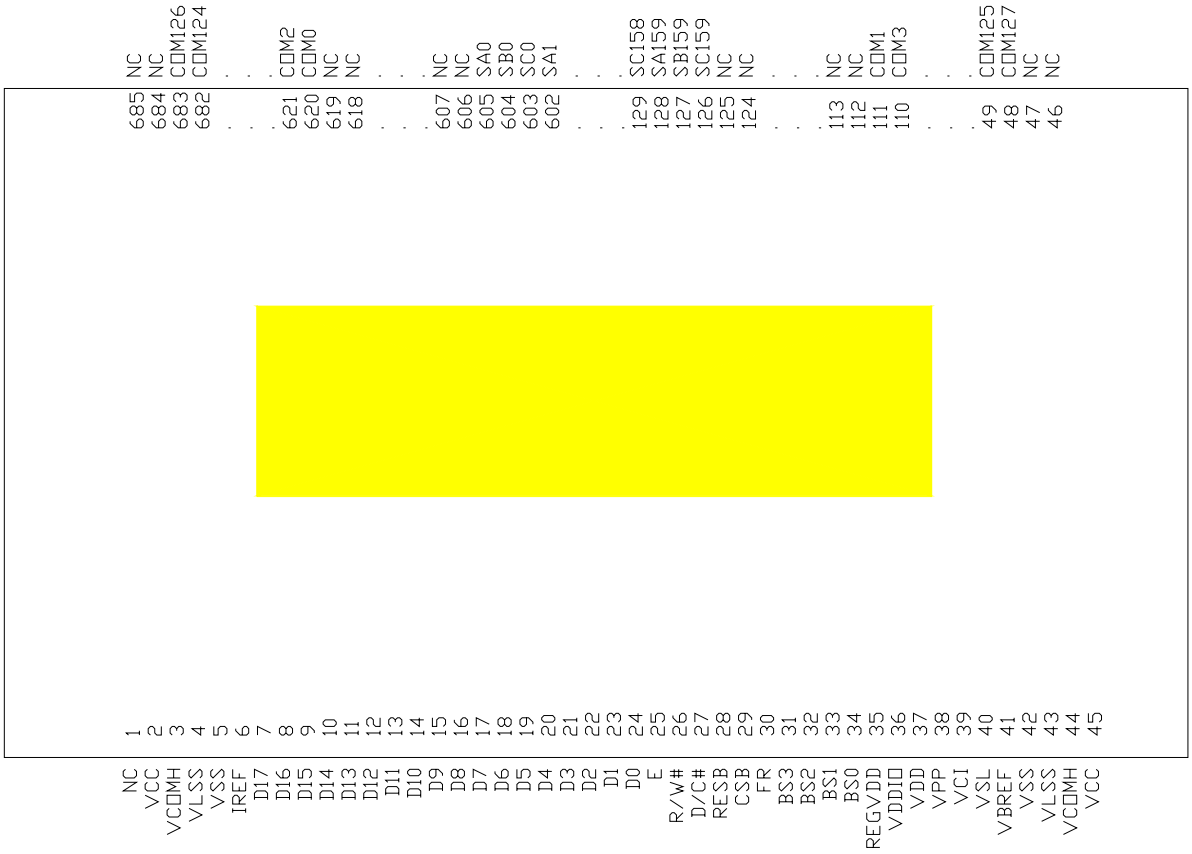
Pad No.	Pad Name
401	SA68
402	SC67
403	SB67
404	SA67
405	SC66
406	SB66
407	SA66
408	SC65
409	SB65
410	SA65
411	SC64
412	SB64
413	SA64
414	SC63
415	SB63
416	SA63
417	SC62
418	SB62
419	SA62
420	SC61
421	SB61
422	SA61
423	SC60
424	SB60
425	SA60
426	SC59
427	SB59
428	SA59
429	SC58
430	SB58
431	SA58
432	SC57
433	SB57
434	SA57
435	SC56
436	SB56
437	SA56
438	SC55
439	SB55
440	SA55
441	SC54
442	SB54
443	SA54
444	SC53
445	SB53
446	SA53
447	SC52
448	SB52
449	SA52
450	SC51
451	SB51
452	SA51
453	SC50
454	SB50
455	SA50
456	SC49
457	SB49
458	SA49
459	SC48
460	SB48
461	SA48
462	SC47
463	SB47
464	SA47
465	SC46
466	SB46
467	SA46
468	SC45
469	SB45
470	SA45
471	SC44
472	SB44
473	SA44
474	SC43
475	SB43
476	SA43
477	SC42
478	SB42
479	SA42
480	SC41

Pad No.	Pad Name
481	SB41
482	SA41
483	SC40
484	SB40
485	SA40
486	SC39
487	SB39
488	SA39
489	SC38
490	SB38
491	SA38
492	SC37
493	SB37
494	SA37
495	SC36
496	SB36
497	SA36
498	SC35
499	SB35
500	SA35
501	SC34
502	SB34
503	SA34
504	SC33
505	SB33
506	SA33
507	SC32
508	SB32
509	SA32
510	SC31
511	SB31
512	SA31
513	SC30
514	SB30
515	SA30
516	SC29
517	SB29
518	SA29
519	SC28
520	SB28
521	SA28
522	SC27
523	SB27
524	SA27
525	SC26
526	SB26
527	SA26
528	SC25
529	SB25
530	SA25
531	SC24
532	SB24
533	SA24
534	SC23
535	SB23
536	SA23
537	SC22
538	SB22
539	SA22
540	SC21
541	SB21
542	SA21
543	SC20
544	SB20
545	SA20
546	SC19
547	SB19
548	SA19
549	SC18
550	SB18
551	SA18
552	SC17
553	SB17
554	SA17
555	SC16
556	SB16
557	SA16
558	SC15
559	SB15
560	SA15

Pad No.	Pad Name
561	SC14
562	SB14
563	SA14
564	SC13
565	SB13
566	SA13
567	SC12
568	SB12
569	SA12
570	SC11
571	SB11
572	SA11
573	SC10
574	SB10
575	SA10
576	SC9
577	SB9
578	SA9
579	SC8
580	SB8
581	SA8
582	SC7
583	SB7
584	SA7
585	SC6
586	SB6
587	SA6
588	SC5
589	SB5
590	SA5
591	SC4
592	SB4
593	SA4
594	SC3
595	SB3
596	SA3
597	SC2
598	SB2
599	SA2
600	SC1
601	SB1
602	SA1
603	SC0
604	SB0
605	SA0
606	NC
607	NC
608	NC
609	NC
610	NC
611	NC
612	NC
613	NC
614	NC
615	NC
616	NC
617	NC
618	NC
619	NC
620	COM0
621	COM2
622	COM4
623	COM6
624	COM8
625	COM10
626	COM12
627	COM14
628	COM16
629	COM18
630	COM20
631	COM22
632	COM24
633	COM26
634	COM28
635	COM30
636	COM32
637	COM34
638	COM36
639	COM38
640	COM40

Pad No.	Pad Name
641	COM42
642	COM44
643	COM46
644	COM48
645	COM50
646	COM52
647	COM54
648	COM56
649	COM58
650	COM60
651	COM62
652	COM64
653	COM66
654	COM68
655	COM70
656	COM72
657	COM74
658	COM76
659	COM78
660	COM80
661	COM82
662	COM84
663	COM86
664	COM88
665	COM90
666	COM92
667	COM94
668	COM96
669	COM98
670	COM100
671	COM102
672	COM104
673	COM106
674	COM108
675	COM110
676	COM112
677	COM114
678	COM116
679	COM118
680	COM120
681	COM122
682	COM124
683	COM126
684	NC
685	NC

Figure 5-1 : SSD1353U4R1 Pin assignment



Note:
(1) COM sequence (Split) is under command setting: ADh, 60h

6 PIN DESCRIPTIONS

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
IO = Bi-directional (input/output)	Pull HIGH= connect to V_{DDIO}
P = Power pin	

Table 6-1: SSD1353 Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply pin for core logic operation Refer to Section 7.10 for details.
V_{DDIO}	P	Power supply for interface logic level. It should be match with the MCU interface voltage level. Refer to Section 7.10 for details.
V_{CI}	P	Low voltage power supply V_{CI} must always be equal or higher than V_{DD} and V_{DDIO}. Refer to Section 7.10 for details.
V_{ACI}	P	Analog Low voltage power supply Connect to V_{CI}.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V_{PP}	P	Power supply for programming OTP. In OTP programming, this pin is powered up to 7.5V. In operation mode (without programming OTP), this pin must be connected to V_{DD}.
V_{SS}	P	Ground pin
V_{LSS}	P	Analog system ground pin
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
REGVDD	I	Internal V_{DD} regulator selection pin. When this pin is pulled HIGH, internal V_{DD} regulator is enabled. When this pin is pulled LOW, external V_{DD} is used. Refer to Section 7.10 for details.
BGGND	P	This is a reserved pin. It should be connected to Ground.
PGGND	P	This is a reserved pin. It should be connected to Ground.
V_{DDB}	P	This is a reserved pin. It should be connected to V_{CI}.
V_{SSB}	P	This is a reserved pin. It should be connected to Ground
GDR	O	This is a reserved pin. It should be kept NC.
RESE	I	This is a reserved pin. It should be kept NC.
FB	I	This is a reserved pin. It should be kept NC.

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>V_{BREF}</td><td>O</td><td>This is an internal voltage reference pin. A capacitor should be connected to this pin and V_{SS}.</td></tr>
<tr><td>GPIO0</td><td>I/O</td><td>This is a reserved pin. It should be kept NC.</td></tr>
<tr><td>GPIO1</td><td>I/O</td><td>This is a reserved pin. It should be kept NC.</td></tr>
<tr><td>VSL</td><td>P</td><td>This is segment voltage reference pin.
When external VSL is not used, this pin should be left open.
When external VSL is used, connect with resistor and diode to ground. (details depend on application)</td></tr>
<tr><td>BS[3:0]</td><td>I</td><td>MCU bus interface selection pins. Select appropriate logic setting as described in the following table.
Table 6-2 : Bus Interface selection
<table><tr><th>BS[3:0]</th><th>Bus Interface Selection</th></tr><tr><td>0000</td><td>4 line SPI</td></tr><tr><td>0001</td><td>Invalid</td></tr><tr><td>0010</td><td>Invalid</td></tr><tr><td>0011</td><td>Invalid</td></tr><tr><td>0100</td><td>8-bit 6800 parallel</td></tr><tr><td>0101</td><td>16-bit 6800 parallel</td></tr><tr><td>0110</td><td>8-bit 8080 parallel</td></tr><tr><td>0111</td><td>16-bit 8080 parallel</td></tr><tr><td>1000</td><td>Invalid</td></tr><tr><td>1001</td><td>Invalid</td></tr><tr><td>1010</td><td>Invalid</td></tr><tr><td>1011</td><td>Invalid</td></tr><tr><td>1100</td><td>9-bit 6800 parallel</td></tr><tr><td>1101</td><td>18-bit 6800 parallel</td></tr><tr><td>1110</td><td>9-bit 8080 parallel</td></tr><tr><td>1111</td><td>18-bit 8080 parallel</td></tr></table>Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}</td></tr>
<tr><td>I_{REF}</td><td>I</td><td>This pin is the segment output current reference pin.
A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA. Please refer to section 7.6 for the formula of resistor value from I_{REF}.</td></tr>
<tr><td>CL</td><td>I</td><td>Internal clock I/O pin.
When internal clock is enable (i.e. pull HIGH in CLS pin), this pin is not used and should be connected to Ground.
When internal clock is disable (i.e. pull LOW is CLS pin), this pin is the external clock source input pin.</td></tr>
<tr><td>CLS</td><td>I</td><td>Internal clock selection pin.
When this pin is pulled HIGH, internal oscillator is enabled (normal operation).
When this pin is pulled LOW, an external clock signal should be connected to CL.</td></tr>
<tr><td>CS#</td><td>I</td><td>This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.</td></tr>
<tr><td>RES#</td><td>I</td><td>This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
</table>

Pin Name	Pin Type	Description
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the content at D[17:0] will be interpreted as data. When the pin is pulled LOW, the content at D[17:0] will be interpreted as command.
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) must be connected to V_{SS}.
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to V_{SS}.
D[17:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode) Refer to Section 7.1 for different bus interface connection.
PD[17:0]	I	These are reserved pins. They should be connected to Ground.
PDEN	I	This is a reserved pin. It should be connected to Ground.
VSYNC	I	This is a reserved pin. It should be connected to Ground.
HSYNC	I	This is a reserved pin. It should be connected to Ground.
DOTCLK	I	This is a reserved pin. It should be connected to Ground.
FR	O	Ram Write Synchronization output Details refer to section 7.5.2
SA[159:0] SB[159:0] SC[159:0]	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF. The 480 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.
COM[131:0]	I/O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 MCU Interface

SSD1353 MCU interface consist of 18 data pin and 5 control pins. The pin assignment at different interface mode is summarized in Table 7-1. Different MCU mode can be set by hardware selection on BS[3:0] pins (refer to Table 6-2 for BS[3:0] pins setting)

Table 7-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data / Command Interface																Control Signal				
	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8b / 8080	Tie Low										D[7:0]								RD#	WR#	CS#	D/C#	RES#
8b / 6800	Tie Low										D[7:0]								E	R/W#	CS#	D/C#	RES#
9b / 8080	Tie Low										D[8:0]								RD#	WR#	CS#	D/C#	RES#
9b / 6800	Tie Low										D[8:0]								E	R/W#	CS#	D/C#	RES#
16b / 8080	Tie Low		D[15:0]																RD#	WR#	CS#	D/C#	RES#
16b / 6800	Tie Low		D[15:0]																E	R/W#	CS#	D/C#	RES#
18b / 8080	D[17:0]																		RD#	WR#	CS#	D/C#	RES#
18b / 6800	D[17:0]																		E	R/W#	CS#	D/C#	RES#
SPI	Tie Low															NC	SDIN	SCLK	Tie Low		CS#	D/C#	RES#

7.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

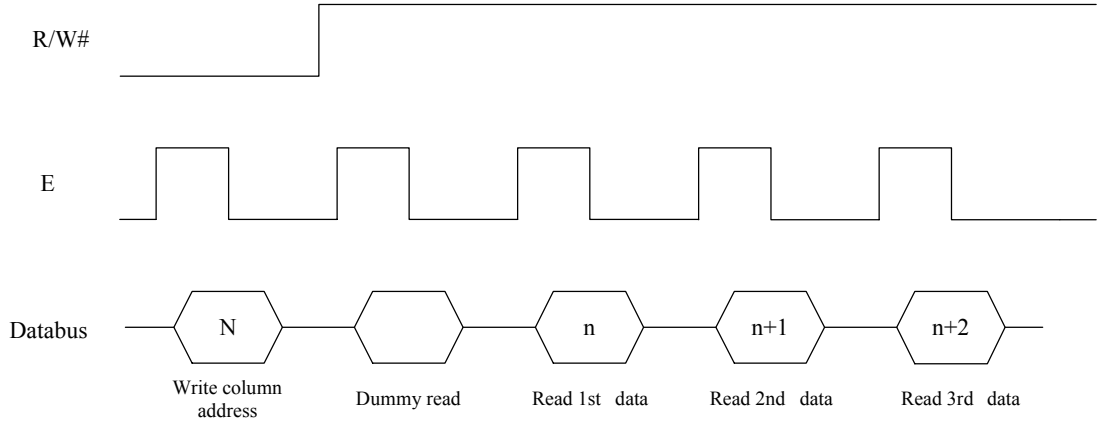
Table 7-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-1.

Figure 7-1 : Data read back procedure - insertion of dummy read



7.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 7-2 : Example of Write procedure in 8080 parallel interface mode

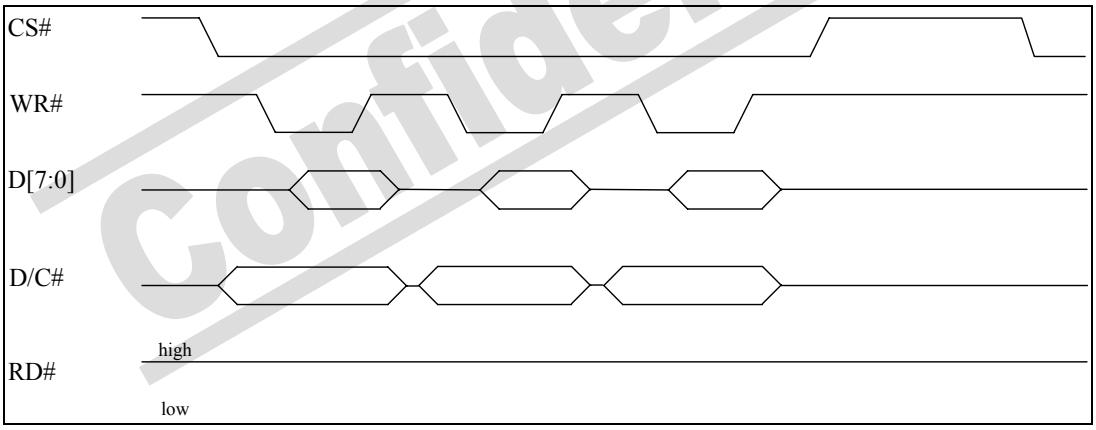


Figure 7-3 : Example of Read procedure in 8080 parallel interface mode

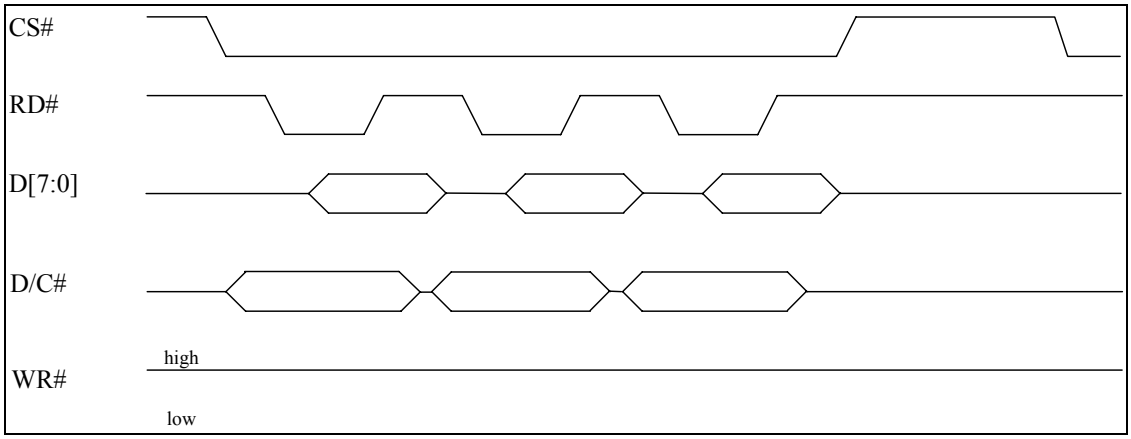


Table 7-3 : Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal
(4) Refer to Figure 12-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

Alternatively, RD# and WR# can be keep stable while CS# serves as the data/command latch signal.

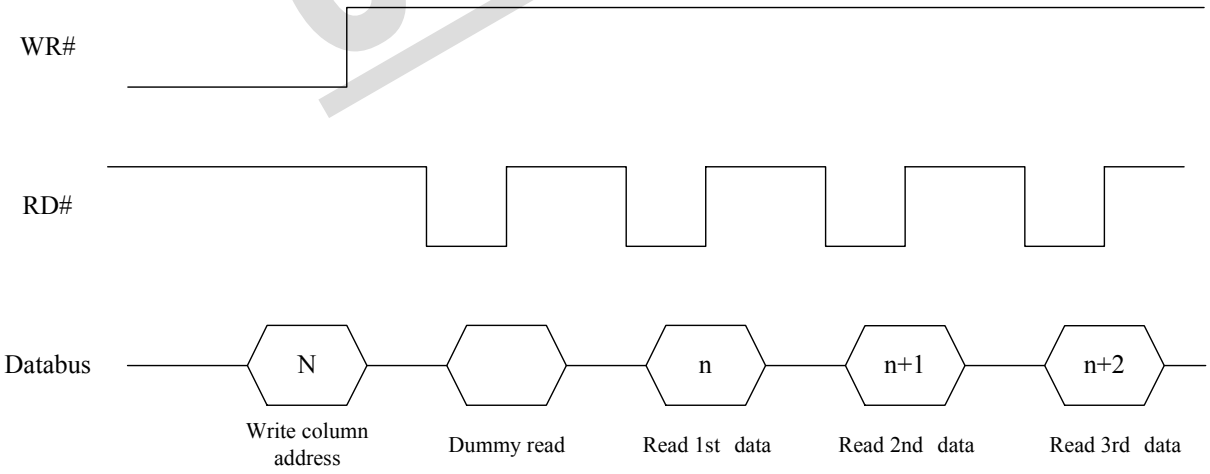
Table 7-4 : Control pins of 8080 interface (Form 2)

Function	RD#	WR#	CS#	D/C#
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal
(4) Refer to Figure 12-3 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-4.

Figure 7-4 : Display data read back procedure - insertion of dummy read



7.1.3 MCU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D17, E and R/W# can be connected to an external ground.

Table 7-5 : Control pins of Serial interface

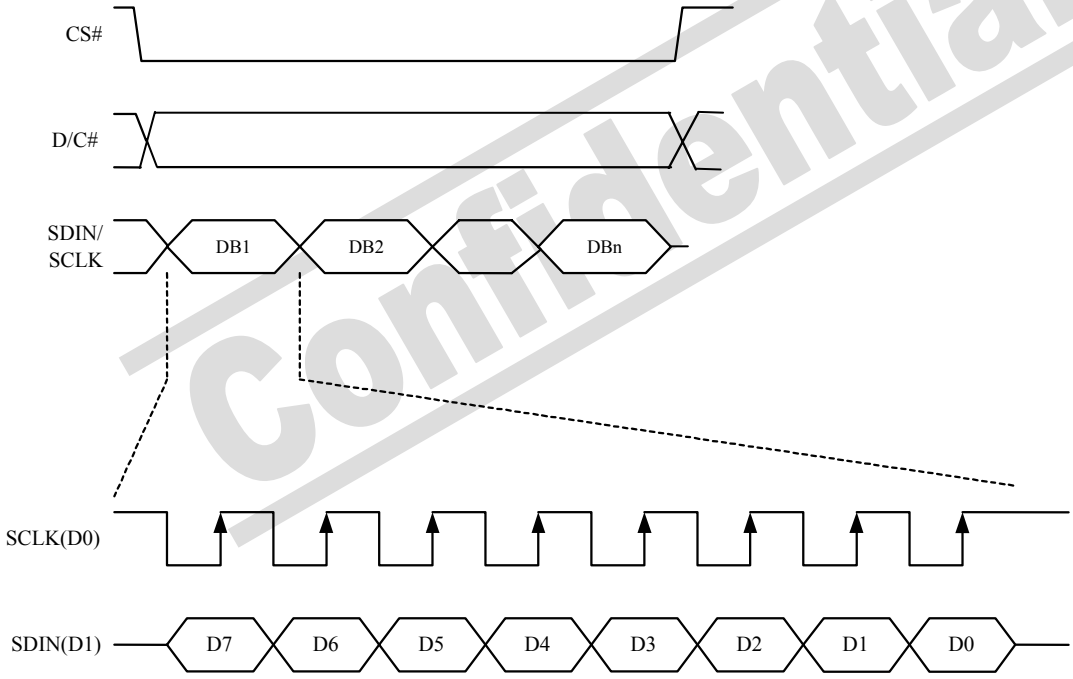
Function	E	R/W#	CS#	D/C#
Write command	Tie LOW	Tie LOW	L	L
Write data	Tie LOW	Tie LOW	L	H

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D16, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 7-5 : Write procedure in SPI mode



7.2 Reset Circuit

When RES# input is pulled LOW, the chip is initialized with the following status:

1. Display is OFF
2. 132 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Individual contrast control registers of color A, B, and C are set at 80h

7.3 GDDRAM

7.3.1 GDDRAM structure

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 160 x 132 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown in Table 7-6

Table 7-6 : 262k Color Depth Graphic Display Data RAM Structure

Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	?	?	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	?	?	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	?	?	C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2	?	?	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	?	?	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	?	?	C0	A0	B0	C0	Common output
Normal	Remapped														
0	131	6	6	6	6	6	6	6	?	?	6	6	6	6	COM0
1	130	6	6	6					?	?					COM1
2	129								?	?					COM2
3	128								?	?					COM3
4	127								?	?					COM4
5	126								?	?					COM5
6	125			no of bits in this cell					?	?					COM6
7	124								?	?					COM7
:	:	:	:	:	:	:	:	:	?	?	:	:	:	:	
:	:	:	:	:	:	:	:	:	?	?	:	:	:	:	
:	:	:	:	:	:	:	:	:	?	?	:	:	:	:	
127	4								?	?					
128	3								?	?					COM128
129	2								?	?					COM129
130	1								?	?					COM130
131	0								?	?					COM131
SEG output		SA0	SB0	SC0	SA1	SB1	SC1	SA2	?	?	SC158	SA159	SB159	SC159	

7.3.2 Data bus to RAM mapping under different input mode

Table 7-7 : Data bus usage under different bus width and color depth mode

			Data bus																
Bus width	**Color Depth**	**Input order**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
8 bits	**256**		X	X	X	X	X	X	X	X	X	X	C_2	C_1	C_0	B_2	B_1	B_0	A_1	A_0
16 bits	**65k**		X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
8 bits	**65k**	**1st**	X	X	X	X	X	X	X	X	X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3
		2nd	X	X	X	X	X	X	X	X	X	X	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
8 bits	**262k**	**1st**	X	X	X	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0
		2nd	X	X	X	X	X	X	X	X	X	X	X	X	B_5	B_4	B_3	B_2	B_1	B_0
		3rd	X	X	X	X	X	X	X	X	X	X	X	X	A_5	A_4	A_3	A_2	A_1	A_0
16 bits	**262k format 1**	**1st**	X	X	X	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0
		2nd	X	X	X	X	B_5	B_4	B_3	B_2	B_1	B_0	X	X	A_5	A_4	A_3	A_2	A_1	A_0
16 bits	**262k format 2**	**1st**	X	X	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$
		2nd	X	X	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X	$C2_5$	$C2_4$	$C2_3$	$C2_2$	$C2_1$	$C2_0$
		3rd	X	X	X	X	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	X	X	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$
9 bits	**262k**	**1st**	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3
		2nd	X	X	X	X	X	X	X	X	X	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0
18 bits	**262k**		C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0

7.3.3 RAM mapping and Different color depth mode

At 262k color depth mode, color A, B, C are directly mapped to the RAM content. At 256 and 65k color mode, the RAM content will be filled up to 262k format.

Table 7-8 : 256 and 65k color mode mapping

	SCn						**SBn**						**SAn**					
262k color	C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0
65k color	C_4	C_3	C_2	C_1	C_0	$*C_4$	B_5	B_4	B_3	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0	$*A_4$
256 color	C_2	C_1	C_0	$*C_2$	$*C_2$	$*C_2$	B_2	B_1	B_0	$*B_2$	$*B_2$	$*B_2$	A_1	A_0	$*A_1$	$*A_1$	$*A_1$	$*A_1$

Note

(1) n = 0 ~ 159d

(2) bits with * are copied from corresponding bits in order to fill up 262K format.

7.4 Command Decoder

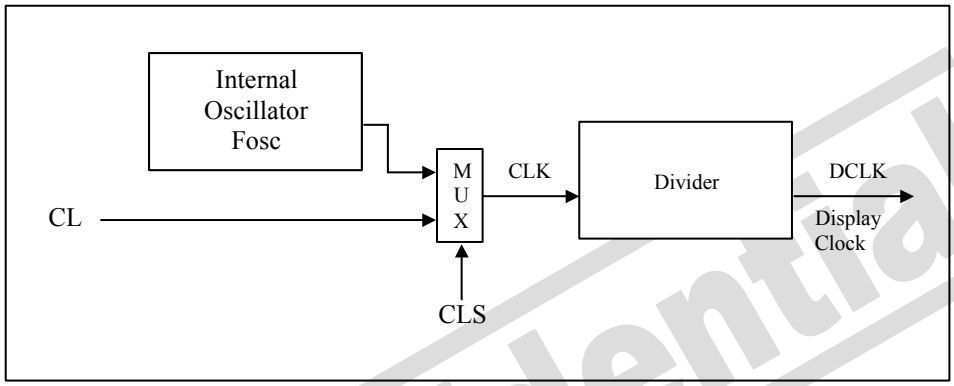
This module determines whether the input should be interpreted as data or command based upon the input of the D/C# pin.

If D/C# pin is HIGH, data is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the inputs at D0-D17 are interpreted as a Command and it will be decoded and be written to the corresponding command register.

7.5 Oscillator & Timing Generator

7.5.1 Oscillator

Figure 7-6 : Oscillator Circuit



This module is an On-Chip low power RC oscillator circuitry (Figure 7-6). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is HIGH, internal oscillator is selected. If CLS pin is LOW, external clock from CL pin will be used for CLK. The frequency of internal oscillator F_{OSC} can be programmed by command B3h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command B3h.

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula:

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

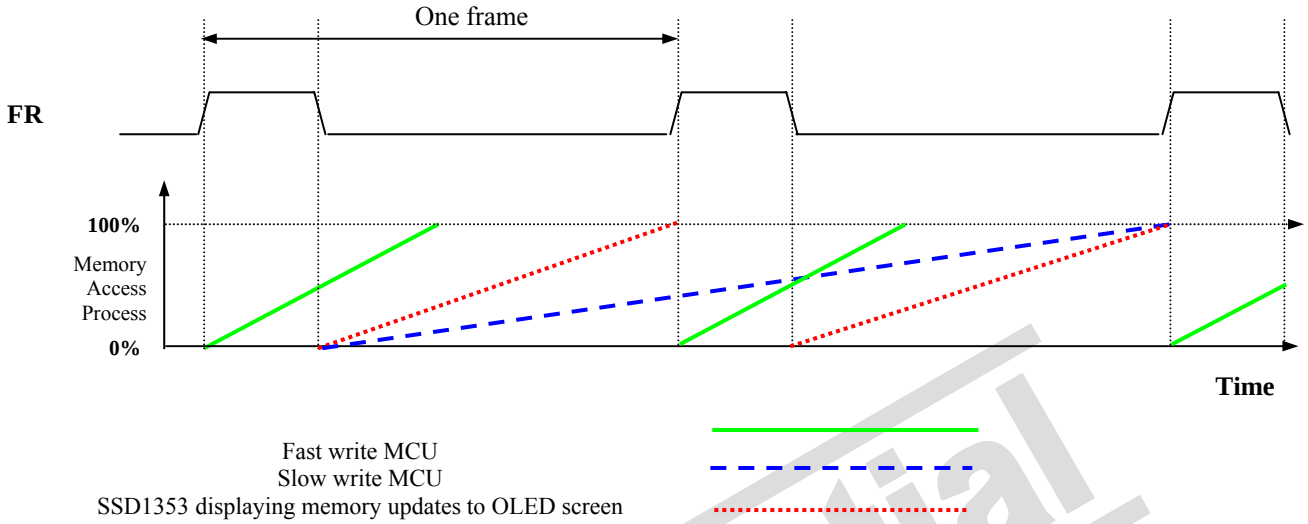
where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period +Phase 2 period + 98
  = 9 +7 +98 =114 (reset)
- Number of multiplex ratio is set by command A8h. The reset value is 131 (i.e. 132MUX).
- F_{osc} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in higher frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

7.5.2 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

7.6 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

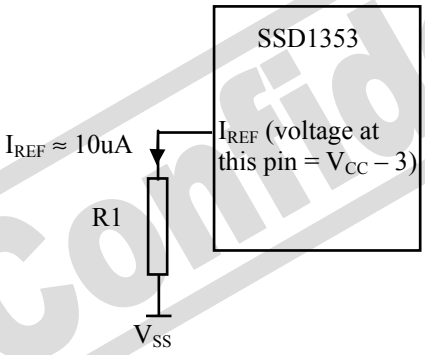
  I_{SEG} = Contrast / 256 * I_{REF} * scale factor

  in which
  the contrast (0~255) is set by Set Contrast command (81h,82h,83h); and
  the scale factor (1 ~ 16) is set by Master Current Control command (87h).

  For example, in order to achieve I_{SEG} = 160uA at maximum contrast 255, I_{REF} is set to around 10uA. This current value is obtained by connecting an appropriate resistor from IREF pin to V_{SS} as shown in Figure 7-7.

  Recommended I_{REF} = 10uA

Figure 7-7 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 3V, the value of resistor R1 can be found as below:

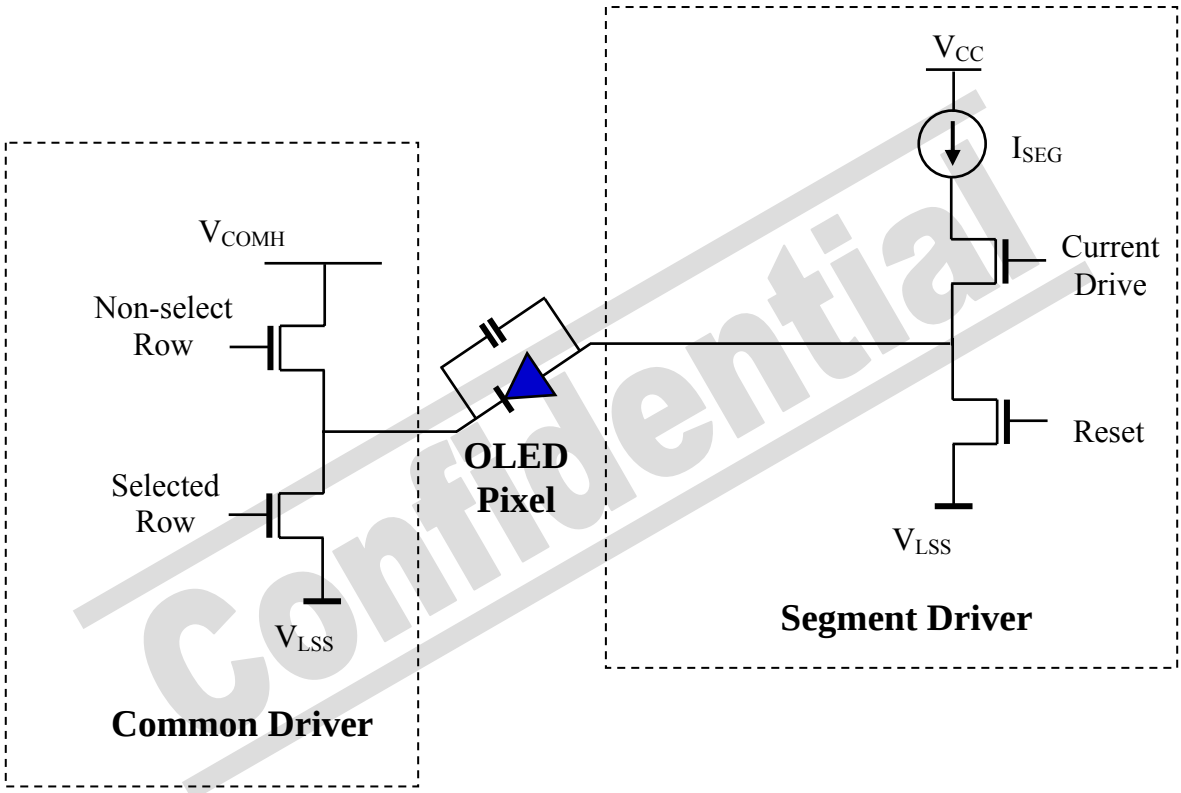
For I_{REF} =10uA, V_{CC} =18V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
= (18 – 3) / 10uA
= ≈ 1.5M Ω

7.7 SEG / COM Driver

Segment drivers consist of 480 (160 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted from 0 to 160uA with 256 steps by contrast setting command (81h, 82h, 83h). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

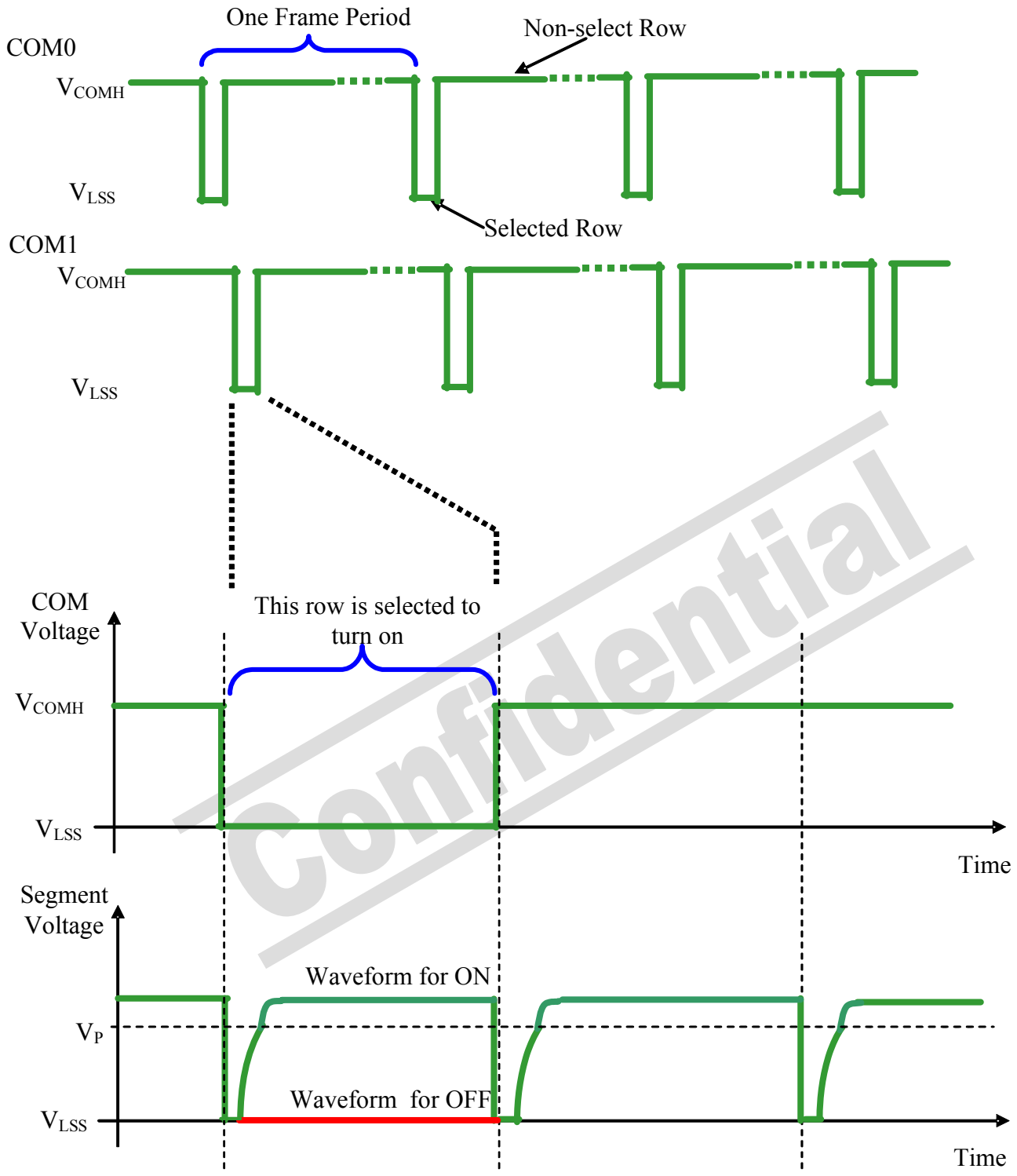
Figure 7-8 : Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 7-9.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 7-9 : Segment and Common Driver Signal Waveform



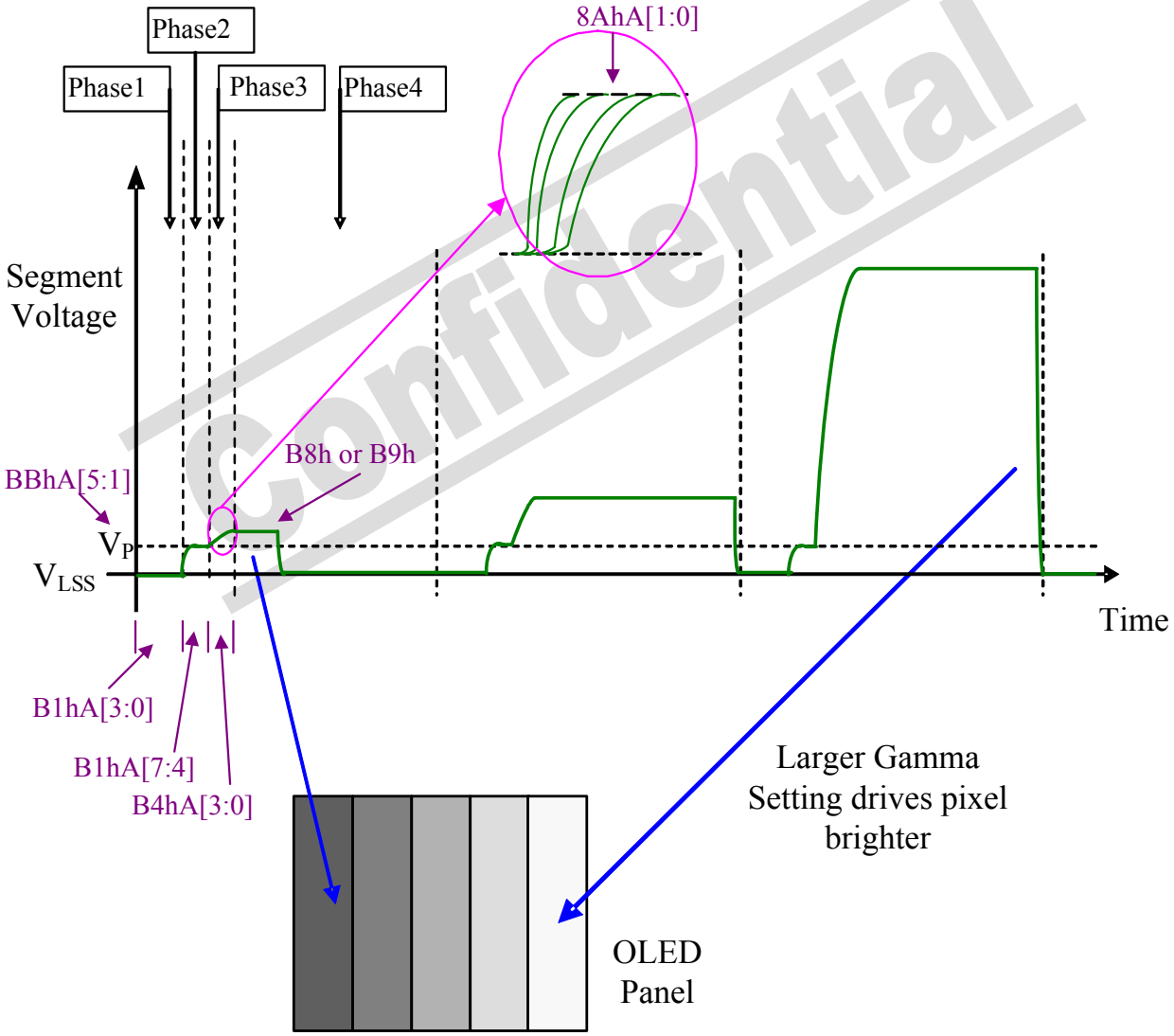
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS}. The amplitude of V_P can be programmed by the command BBh. The period of phase 2 can be programmed by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command B4h.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PAM+PWM (Pulse Area Modulation + Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command B8h/B9h. The bigger gamma setting in the current drive stage results in brighter pixels and vice versa (Details refer to Section 7.8). This is shown in the following figure.

Figure 7-10: Gray Scale Control in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

7.8 Gray Scale Decoder

The gray scale effect is generated by controlling the segment current in current drive phase. The segment current is controlled by the Gamma Settings (Setting 0~ Setting 128). The larger the setting, the brighter the pixel will be. The Gray Scale Table stores the corresponding Gamma Setting of the 64 gray scale levels (GS0~GS63) through the software commands B8h or B9h. A single Gray Scale Table supports all the three colors A, B and C.

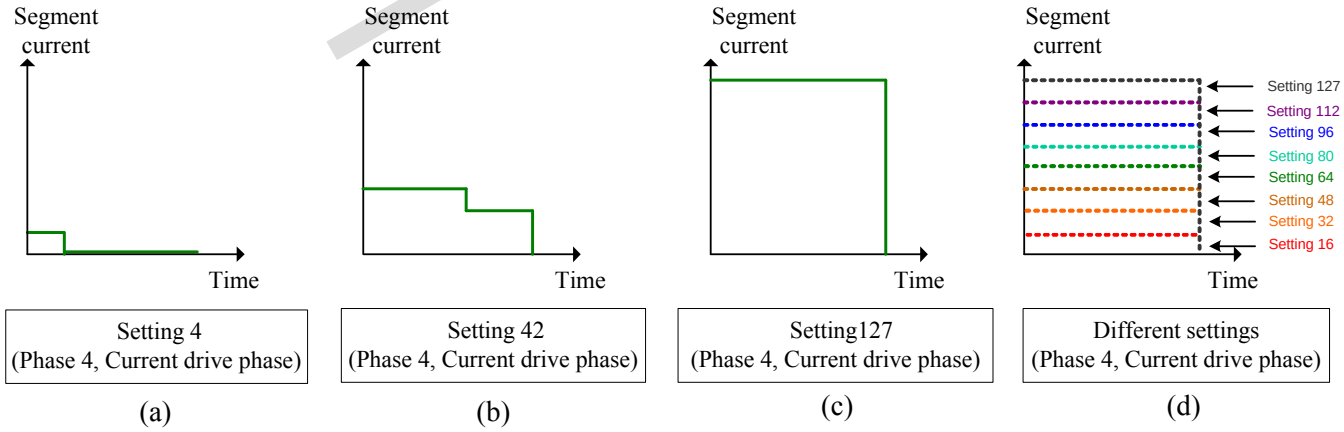
As shown in Figure 7-11, color A, B, C sub-pixel RAM data has 6 bits, represent the 64 gray scale level from GS0 to GS63.

Figure 7-11 : Relation between GDDRAM content and Gray Scale table entry for three colors in 262K color mode (under command B9h Enable Linear Gray Scale Table)

Color A,B ,C GDDRAM data (6 bits)	Gray Scale Table	Default Gamma Setting (Command B9h)
000000	GS0	Setting 0
000001	GS1	Setting 2
000010	GS2	Setting 4
000011	GS3	Setting 6
000100	GS4	Setting 8
:	:	:
011111	GS31	Setting 62
100000	GS32	Setting 65
100001	GS33	Setting 67
:	:	:
111100	GS60	Setting 121
111101	GS61	Setting 123
111110	GS62	Setting 125
111111	GS63	Setting 127

The Gray Scale Table can be programmed into different Gamma setting by command B8h. For example, if GS2 is programmed into Gamma setting 4, and the color A, B or C of GDDRAM is set as “000010b”, then the current drive phase will be similar to the illustration in Figure 7-12(a).

Figure 7-12 : Illustration of current drive phase (phase 4) under different Gamma Settings.



There are total 128 Gamma Settings (Setting 0 to Setting 127) available for the Gray Scale table. GS0 has no pre-charge and current drive stages so it is in Gamma Setting 0.

When setting the Gray Scale Table, the rules below must follow:

1) The gray scale is defined in incremental way, with reference to the length of previous table entry:
   0 < Setting of GS1 < Setting of GS2 < Setting of GS3..... Setting 62 < Setting 63.
2) Different GSs should be set within the maximum Gamma Setting as follow:

Table 7-9 : Maximum Gamma setting in different Gray Scale ranges

Gary Scale Range	Maximum Gamma Setting allowed
GS0	Setting 0
GS1 ~ G7	Setting 15
GS8 ~ GS15	Setting 31
GS16 ~ GS31	Setting 63
GS32 ~ GS63	Setting 127

It should be notice that, the brightness under the following pairs of Gamma Setting will be the same:

Table 7-10 : Gamma Settings with identical brightness in current drive phase

Setting 15 & Setting 16	Setting 63 & Setting 64	Setting 111 & Setting 112
Setting 31 & Setting 32	Setting 79 & Setting 80	
Setting 47 & Setting 48	Setting 95 & Setting 96	

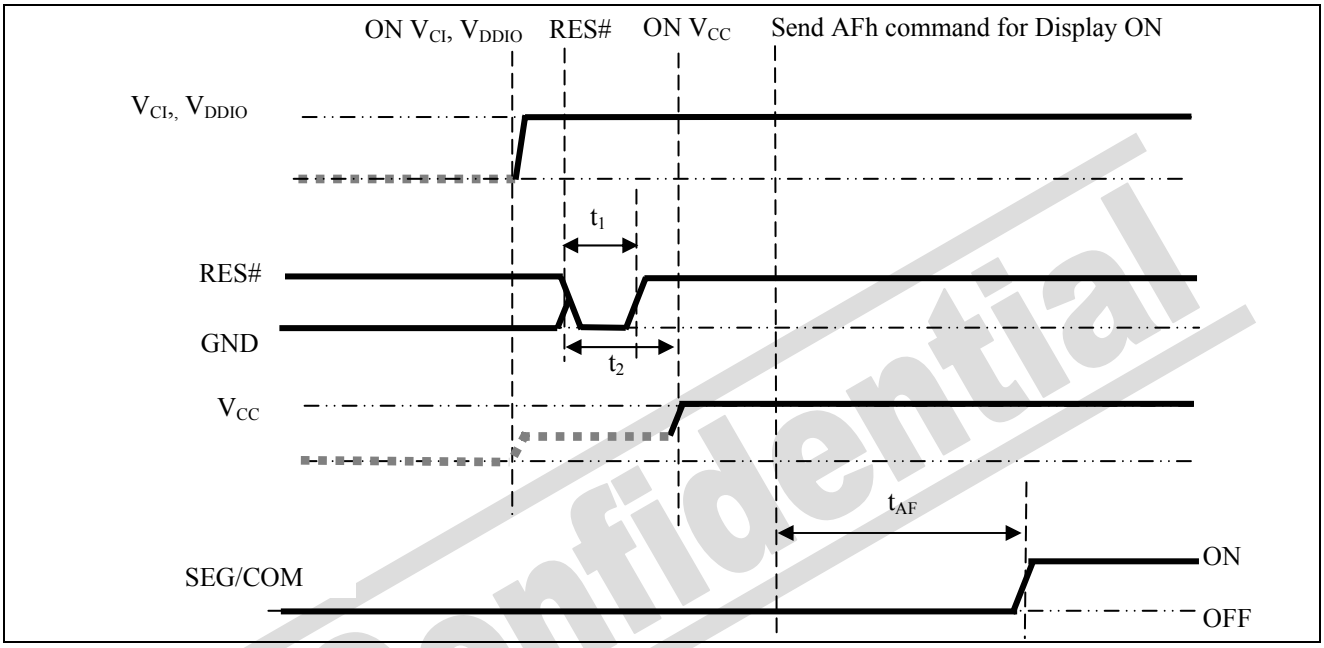
7.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1353 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

Power ON sequence:

1. Power ON $V_{CI,}$ $V_{DDIO.}$
2. After V_{CI}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 100us (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON $V_{CC.}$ (1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).

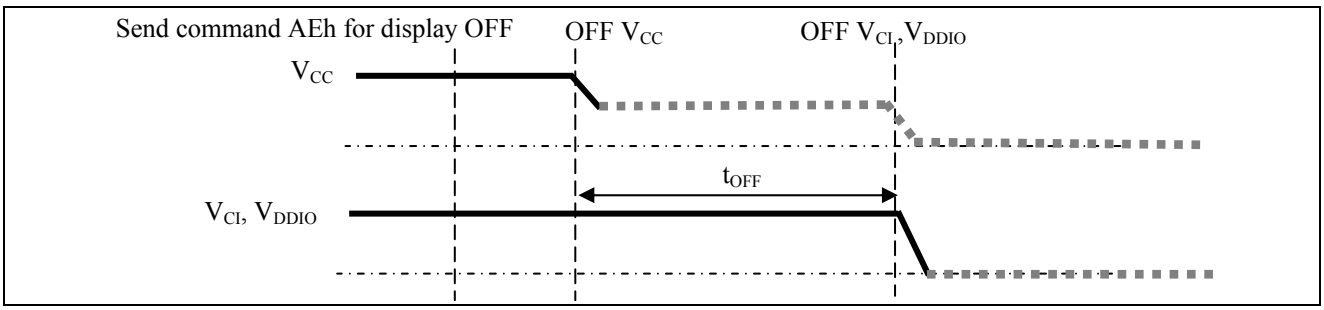
Figure 7-13: The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF $V_{CC.}$ (1), (2)
3. Wait for t_{OFF}. Power OFF $V_{CI,}$ $V_{DDIO.}$ (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)

Figure 7-14: The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever $V_{CI,}V_{DDIO}$ is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-13 and Figure 7-14.

(2) V_{CC} should be kept float when it is OFF.

7.10 V_{DD} Regulator

In SSD1353, the power supply pin for core logic operation: V_{DD}, can be supplied by external source or internally regulated through the V_{DD} regulator.

When the Internal V_{DD} regulator selections pin: REGVDD is pulled HIGH (i.e. connect to V_{DDIO}), the internal V_{DD} regulator is enabled. V_{CI} should be larger than 2.6V when using the internal V_{DD} regulator. The typical regulated V_{DD} is about 2.5V

When the Internal V_{DD} regulator selection pin: REGVDD is pulled LOW (i.e. connect to Ground), external V_{DD} should be used. (external V_{DD} range : 2.4V~2.6V)

It should be notice that, no matter V_{DD} is supplied by external source or internally regulated, V_{CI} must always be equal or higher than V_{DD} and V_{DDIO}.

The following figure shows the V_{DD} regulator pin connection scheme:

Figure 7-15 V_{CI} > 2.6V, V_{DD} regulator enable pin connection scheme

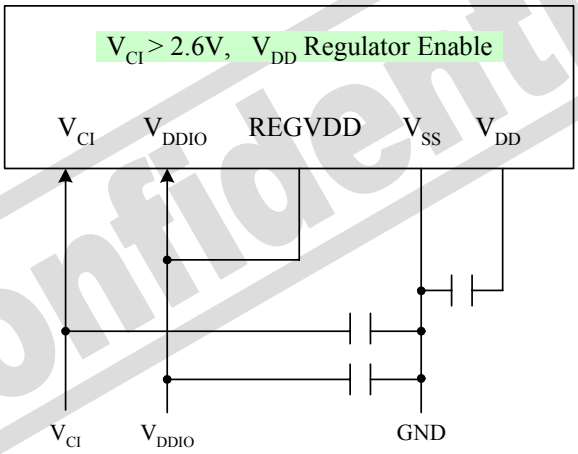
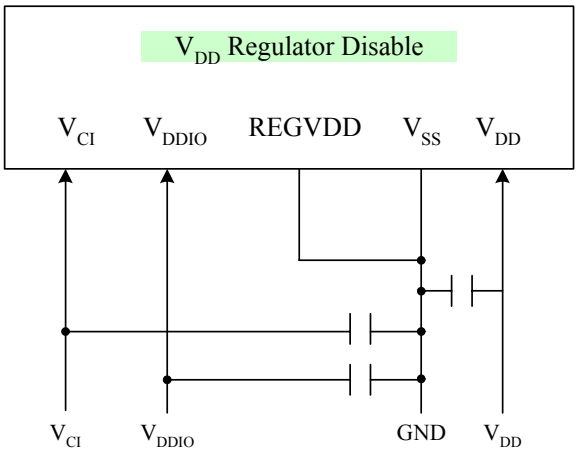


Figure 7-16 V_{DD} regulator disable pin connection scheme



8 COMMAND TABLE

Table 8-1 : Command table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1 1	15 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[7:0]: Set start column address from 00d-159d [reset= 0d (00h)] B[7:0]: Set end column address from 00d-159d [reset= 159d (9Fh)]
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[7:0] B[7:0]	0 A_7 B_7	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[7:0]: Set start row address from 00d-131d [reset= 0d (00h)] B[7:0]: Set end row address from 00d-131d [reset= 131d (83h)]
0 1	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast for Color "A"	Set contrast for all color "A" segment (Pins :SA0 – SA159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Contrast for Color "B"	Set contrast for all color "B" segment (Pins :SB0 – SB159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	83 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Contrast for Color "C"	Set contrast for all color "C" segment (Pins :SC0 – SC159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	87 A[3:0]	1 *	0 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Current Control	Set master current attenuation factor A[3:0] can be set from 00d to 15d corresponding to 1/16, 2/16… to 16/16 attenuation. [reset= 15d (0Fh)]

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	8A A[1:0]	1 0	0 0	0 0	0 0	1 0	0 0	1 A_1	0 A_0	Set Second Pre-charge speed	Set Second Pre-charge speed A[1:0]= 00b, Second Pre-charge speed =slowest A[1:0]= 01b, Second Pre-charge speed =slow A[1:0]= 10b, Second Pre-charge speed =normal [reset] A[1:0]= 11b, Second Pre-charge speed =Fast
0 1	A0 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Remap & Color Depth setting	Set driver remap and color depth A[0]=0, Horizontal address increment [reset] A[0]=1, Vertical address increment A[1]=0, RAM Column 0 to 159 maps to Pin SEG (SA,SB,SC) 0 to 159 [reset] A[1]=1, RAM Column 0 to 159 maps to Pin SEG (SA,SB,SC) 159 to 0 A[2]=0, normal order SA,SB,SC (e.g. RGB) [reset] A[2]=1, reverse order SC,SB,SA (e.g. BGR) A[3]=0, Disable left-right swapping on COM [reset] A[3]=1, Set left-right swapping on COM A[4]=0, Scan from COM0 to COM[N –1] [reset] A[4]=1, Scan from COM[N-1] to COM0. Where N is the multiplex ratio. A[5]=0, Disable COM Split Odd Even [reset] A[5]=1, Enable COM Split Odd Even Refer to Figure 9-6 for details. A[7:6] = 00; 256 color format A[7:6] = 01; 65k color format [RESET] A[7:6] = 10; 256k color format A[7:6] = 11; 256k color 16-bit format 2 If 9-/18-bit mode is selected, color depth will be fixed to 256k regardless of the setting. Refer to Table 7-7 for details.
0 1	A1 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display start line register by Row A[7:0]: from 00d to 131d [00d (00h)] **Note** (1) A[7:0] must be set to 0 when using A3h command.
0 1	A2 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical offset by COM A[7:0]: from 00d to 131d [00d (00h)]
0 0 0 0	A4 A5 A6 A7	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	Set Display Mode	A4h=Normal Display [reset] A5h=Entire Display ON, all pixels turn ON at GS63 A6h=Entire Display OFF, all pixels turn OFF A7h=Inverse Display

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	Set MUX ratio to N+1 Mux N = A[7:0] from 15d to 131d (i.e.16MUX -132 MUX) A[7:0] from 00d to 14d are invalid entry [reset= 131d (83h)]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	AB	1	0	1	0	1	0	1	1	Dim Mode setting	Configure dim mode setting A[7:0] = Reserved. (Set as 00h) B[7:0] = Contrast setting for Color A, valid range 0 to 255d. C[7:0] = Contrast setting for Color B, valid range 0 to 255d. D[7:0] = Contrast setting for Color C, valid range 0 to 255d. E[4:0] = Pre-charge voltage setting, valid range 0 to 31d.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[4:0]	*	*	*	E_4	E_3	E_2	E_1	E_0		
0	AC	1	0	1	0	1	1	0	0	Set Display ON/OFF	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) [reset] AFh = Display ON in normal mode Refer to Figure 9-13 for transitions between different modes
0	AE	1	0	1	0	1	1	1	0		
0	AF	1	0	1	0	1	1	1	1		
0	B1	1	0	1	1	0	0	0	1	Phase 1 and 2 period adjustment	A[3:0] : Phase 1 period in N DCLKs. 3~31 DCLKs allowed as follow: A[3:0] | Phase 1 period 0000 | invalid 0001 | 3 DCLKs 0010 | 5 DCLKs 0011 | 7 DCLKs 0100 | 9 DCLKs [reset] : | : 1111 | 31 DCLKs A[7:4] : Phase 2 period in N DCLKs. 2~15 DCLKs allowed. A[7:4] | Phase 2 period 0000 | invalid 0001 | invalid 0010 | 2 DCLKs 0011 | 3 DCLKs : | : 0111 | 7 DCLKs[reset] : | : 1111 | 15 DCLKs
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	B3	1	0	1	1	0	0	1	1	Display Clock Divider / Oscillator Frequency	A[3:0] Divider DCLK is generated from CLK divided by DIVIDER +1 (i.e., 1 to 16) [reset=0000b] A[7:4] Fosc frequency Frequency increases as setting value increases [reset=1100b]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B4	1	0	1	1	0	1	0	0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b 0 DCLKS 0001b 1 DCLKS 0010b 2 DCLKS .... 0111 7 DCLKS [reset] .... 1111 15 DCLKS
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	These 63 parameters define Gray Scale (GS) Table in terms of Gamma Setting A1[3:0]: Gamma Setting for GS1, A2[3:0]: Gamma Setting for GS2, : A62[6:0]: Gamma Setting for GS62, A63[6:0]: Gamma Setting for GS63. **Note** (1) Input 1d for Gamma Setting 1, 2d for Gamma setting 2, ... ,127d for Gamma Setting127 (2) 0 < Setting of GS1 < Setting of GS2 < Setting of GS3..... Setting 62 < Setting 63 Refer to Section 7.8 for details.
1	A1[3:0]	*	*	*	*	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	:	:	:	:	:	:	:	:	:		
1	A7[3:0]	*	*	*	*	$A7_3$	$A7_2$	$A7_1$	$A7_0$		
1	A8[4:0]	*	*	*	$A8_4$	$A8_3$	$A2_2$	$A8_1$	$A8_0$		
1	:	:	:	:	:	:	:	:	:		
1	A15[4:0]	*	*	*	$A15_4$	$A15_3$	$A15_2$	$A15_1$	$A15_0$		
1	A16[5:0]	*	*	$A16_5$	$A16_4$	$A16_3$	$A16_2$	$A16_1$	$A16_0$		
1	:	:	:	:	:	:	:	:	:		
1	A31[5:0]	*	*	$A31_5$	$A31_4$	$A31_3$	$A31_2$	$A31_1$	$A31_0$		
1	A32[6:0]	*	$A32_6$	$A32_5$	$A32_4$	$A32_3$	$A32_2$	$A32_1$	$A31_0$		
1	:	:	:	:	:	:	:	:	:		
1	A63[6:0]	*	$A63_6$	$A63_5$	$A63_4$	$A63_3$	$A63_2$	$A63_1$	$A63_0$		
0	B9	1	0	1	1	1	0	0	1	Enable Linear Gray Scale Table	Reset built in Linear Gray Scale table GS0 = Gamma Setting 0; GS1 = Gamma Setting 2 GS2 = Gamma Setting 4; GS3 = Gamma Setting 6; : GS31 = Gamma Setting 62 GS32 = Gamma Setting 65; GS33 = Gamma Setting 67; : GS62 = Gamma Setting 125; GS63 = Gamma Setting 127; Refer to Section 7.8 for details.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge level	Set pre-charge voltage level. All three colors share the same pre-charge voltage. [RESET =3Eh]
1	A[5:1]	0	0	A_5	A_4	A_3	A_2	A_1	0		

A[5:1]	Hex code	pre-charge voltage
00000	00h	0.20 x V_{CC}
:	:	:
11111	3Eh	0.60 x V_{CC}

0	BE	1	0	1	1	1	1	1	0	Set V_{COMH}	Set COM deselect voltage level [reset =3Ch] A[5:2] =
1	A[5:2]	0	0	A_5	A_4	A_3	A_2	0	0		

A[5:2]	Hex code	V_{COMH}
0000	00h	0.51 x V_{CC}
0001	04h	0.53 x V_{CC}
..	..	..
1101	34h	0.79 x V_{CC}
1110	38h	0.81 x V_{CC}
1111	3Ch	0.84 x V_{CC}

0	E2	1	1	1	0	0	0	1	0	Software Reset	Reset display circuit and stop Graphic Acceleration operations.
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation.
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[2]: MCU protection status [RESET = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [RESET] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.
1	A[2]	0	0	0	1	0	A_2	1	0		

Note
(1) "*" stands for "Don't care".

Graphic Acceleration Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	21	0	0	1	0	0	0	0	1	Draw Line	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[5:0] : Color C of the line F[5:0] : Color B of the line G[5:0] : Color A of the line **Note** (1) Please enter all 6 bits for Color setting: E[5:0], F[5:0] and G[5:0] , despite of the color format setting in command A0h
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		
1	G[5:0]	*	*	G_5	G_4	G_3	G_2	G_1	G_0		
0	22	0	0	1	0	0	0	1	0	Drawing Rectangle	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[5:0] : Color C of the line F[5:0] : Color B of the line G[5:0] : Color A of the line H[5:0] : Color C of the fill area I[5:0] : Color B of the fill area J[5:0] : Color A of the fill area **Note** (1) Please enter all 6 bits for Color setting: E[5:0], F[5:0] , G[5:0], H[5:0]. I[5:0] and J[5:0] , despite of the color format setting in command A0h (2) 0<A[7:0] < C[7:0] <159 (3) 0<B[7:0] < D[7:0]<131
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		
1	G[5:0]	*	*	G_5	G_4	G_3	G_2	G_1	G_0		
1	H[5:0]	*	*	H_5	H_4	H_3	H_2	H_1	H_0		
1	I[5:0]	*	*	I_5	I_4	I_3	I_2	I_1	I_0		
1	J[5:0]	*	*	J_5	J_4	J_3	J_2	J_1	J_0		
0	23	0	0	1	0	0	0	1	1	Copy	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[7:0] : Column Address of New Start F[7:0] : Row Address of New Start
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	24	0	0	1	0	0	1	0	0	Dim Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		

Graphic Acceleration Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1 1 1 1	25 A[7:0] B[7:0] C[7:0] D[7:0]	0 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	1 A_5 B_5 C_5 D_5	0 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	1 A_2 B_2 C_2 D_2	0 A_1 B_1 C_1 D_1	1 A_0 B_0 C_0 D_0	Clear Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End
0 1	26 A[4:0]	0 *	0 *	1 *	0 A_4	0 0	1 0	1 0	0 A_0	Fill Enable / Disable	A[0] : 0b = Disable Fill for Draw Rectangle Command [reset] 1b = Enable Fill for Draw Rectangle Command A[3:1] : 000 (Reserved values) A[4] : 0b = Disable reverse copy (reset) 1b = Enable reverse during copy command.
0 1 1 1 1 1	27 A[7:0] B[7:0] C[7:0] D[7:0] E[1:0]	0 A_7 B_7 C_7 D_7 *	0 A_6 B_6 C_6 D_6 *	1 A_5 B_5 C_5 D_5 *	0 A_4 B_4 C_4 D_4 *	0 A_3 B_3 C_3 D_3 *	1 A_2 B_2 C_2 D_2 *	1 A_1 B_1 C_1 D_1 E_1	1 A_0 B_0 C_0 D_0 E_0	Continuous Horizontal & Vertical Scrolling Setup	A[7:0]: Set number of column as horizontal scroll offset Range: 0d-131d (no horizontal scroll if equals to 0 B[7:0]: Define start row address C[7:0]: Set number of rows to be horizontal scrolled B[7:0]+C[7:0] <=132 D[7:0]: Set number of row as vertical scroll offset Range: 0d-131d (no vertical scroll if equals to 0) E[1:0]: Set time interval between each scroll step 00b 3 frames 01b 5 frames 10b 50 frames 11b 100 frames **Note**: (1) Vertical scroll run with command A3h Set Vertical Scroll Area (2) The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Deactivate horizontal scrolling. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

Graphic Acceleration Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Activate horizontal scrolling. This command activates the scrolling function according to the setting done by command 27h Continuous Horizontal & Vertical Scrolling Setup
0 1 1	A3 A[7:0] B[7:0]	1 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[7:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[7:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 132] **Note** (1) A[7:0]+B[7:0] <= MUX ratio (2) B[7:0] <= MUX ratio (3) Set Display Start Line (A1h) must be set to 0 when using A3h command. (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 132d MUX display A[7:0] = 0, B[7:0]=132 : whole area scrolls A[7:0]= 0, B[7:0] < 132 : top area scrolls A[7:0] + B[7:0] < 132 : central area scrolls A[7:0] + B[7:0] = 132 : bottom area scrolls Refer to Figure 9-19 for details.

9 COMMAND DESCRIPTIONS

9.1 Fundamental Command

9.1.1 Set Column Address (15h)

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address.

9.1.2 Write RAM Command (5Ch)

After this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

9.1.3 Read RAM Command (5Dh)

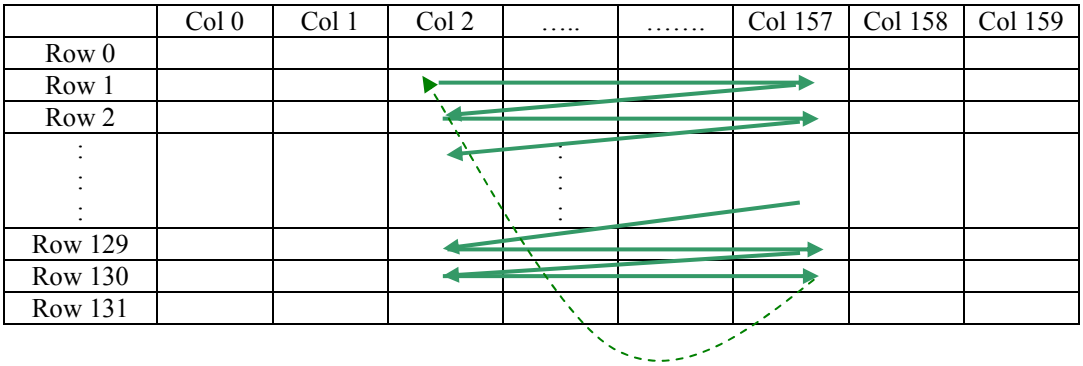
After this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

9.1.4 Set Row Address (75h)

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The figure below shows the way of column and row address pointer movement through the example: column start address is set to 2 and column end address is set to 157, row start address is set to 1 and row end address is set to 130. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 157 and from row 1 to row 130 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation *(solid line in Figure 9-1)*. Whenever the column address pointer finishes accessing the end column 157, it is reset back to column 2 and row address is automatically increased by 1 *(solid line in Figure 9-1)*. While the end row 130 and end column 157 RAM location is accessed, the row address is reset back to 1 *(dotted line in Figure 9-1)*.

Figure 9-1 : Example of Column and Row Address Pointer Movement



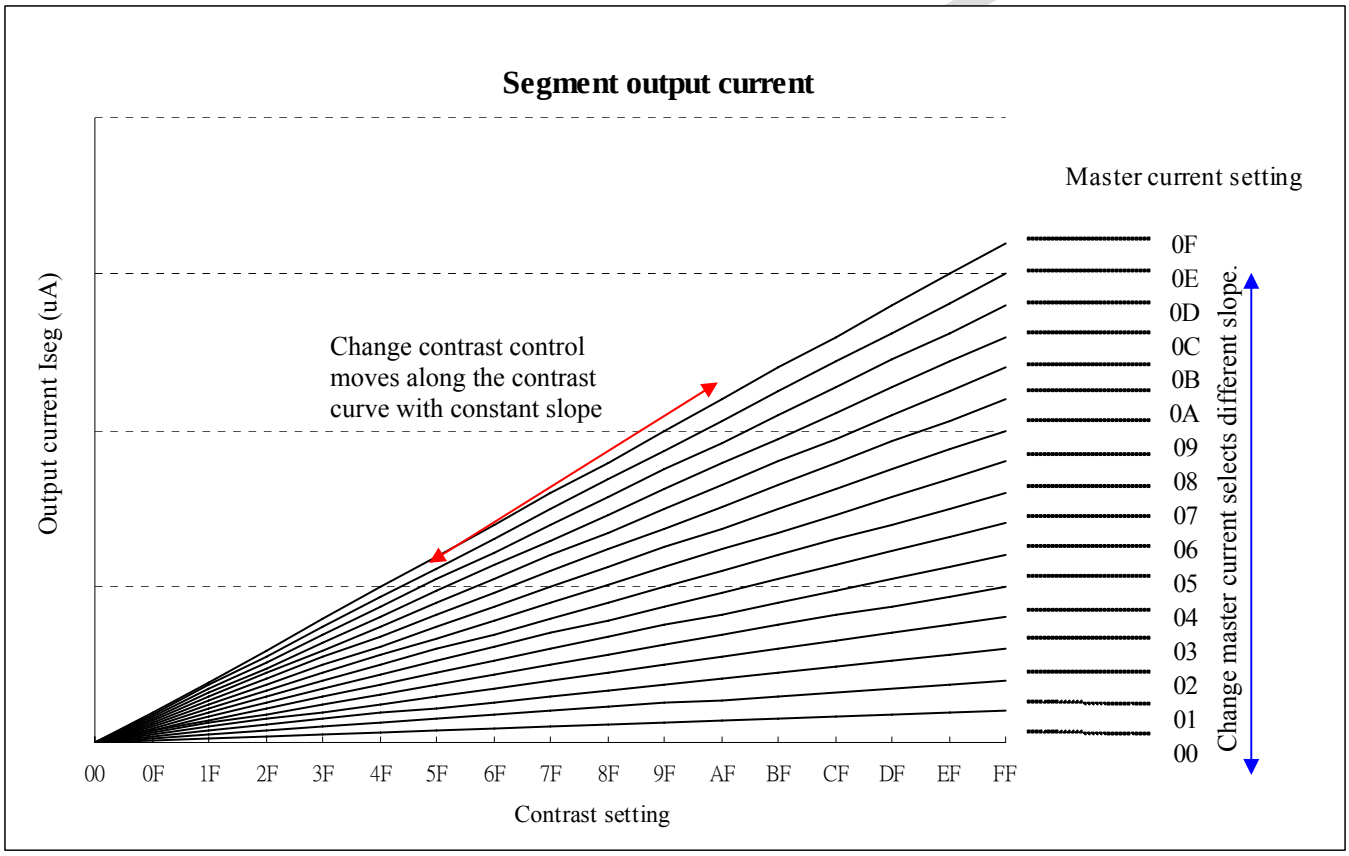
9.1.5 Set Contrast for Color A, B, C (81h, 82h, 83h)

This command is to set Contrast Setting of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter of the color. This relation is shown in Figure 9-2.

9.1.6 Master Current Control (87h)

This command is to control the segment output current by a scaling factor. This factor is common to color A, B and C. The chip has 16 master control steps. The factor is ranged from 1 [0000b] to 16 [1111b]. Reset is 16 [1111b]. The smaller the master current value, the dimmer the OLED panel display is set. For example, if original segment output current of a color is 160uA at scale factor = 16, setting scale factor to 8 to reduce the current to 80uA. Please see Figure 9-2 .

Figure 9-2 : Segment Output Current for Different Contrast Control and Master Current Setting



9.1.7 Set Second Pre-charge speed (8Ah)

This command is used to set the speed of second pre-charge in phase 3. Please refer to Table 8-1 for the details of setting.

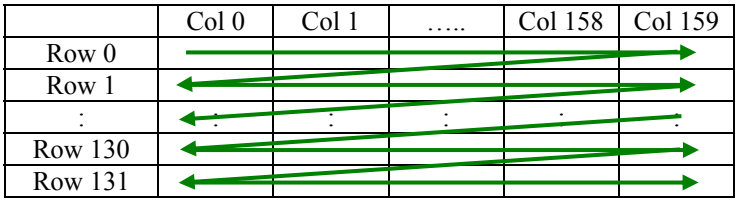
9.1.8 Set Re-map & Data Format (A0h)

This command has multiple configurations and each bit setting is described as follows.

- Address increment mode (A[0])
  When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and

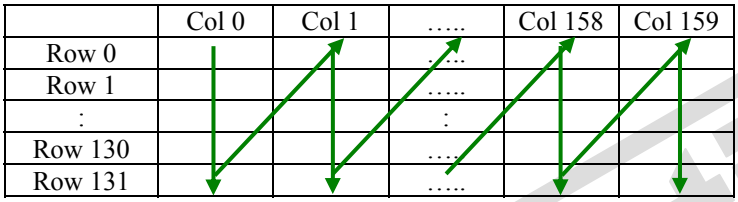
row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 9-3.

Figure 9-3 : Address Pointer Movement of Horizontal Address Increment Mode



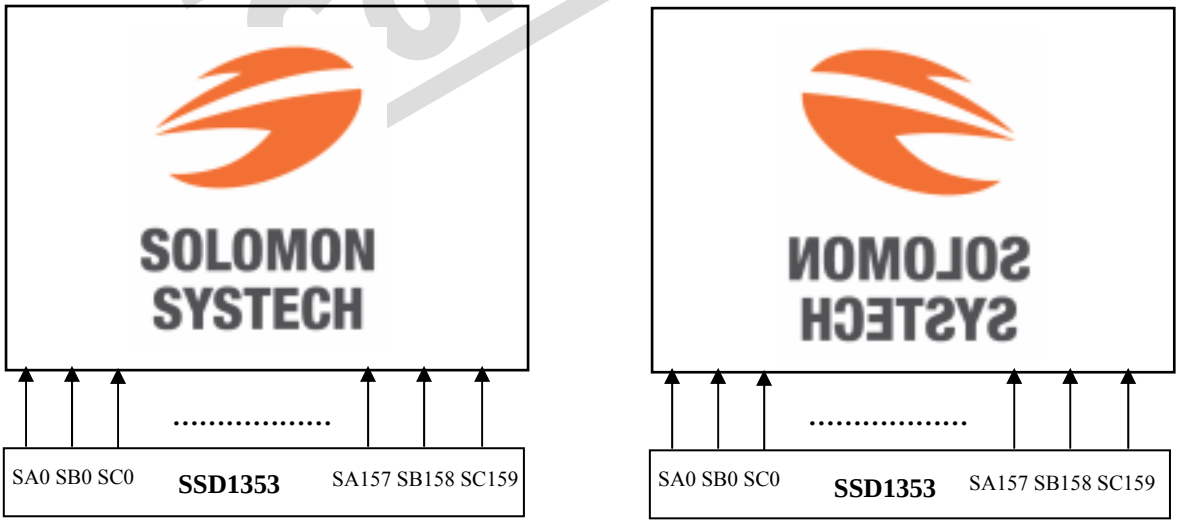
When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 9-4.

Figure 9-4 : Address Pointer Movement of Vertical Address Increment Mode



- Column Address Mapping (A[1])
  This command bit is made for flexible layout of segment signals in OLED module with segment arranged from left to right or vice versa. The display direction is either mapping display data RAM column 0 to SEG0 pin (A[1] = 0), or mapping display data RAM column 159 to SEG0 pin (A[1] = 1). The effects of both are shown in Figure 9-5.

Figure 9-5 : Example of Column Address Mapping



Column 0 maps to SEG0 pin

Column 159 maps to SEG0 pin

- RGB Mapping (A[2])
  This command bit is made for flexible layout of segment signals in OLED module to match filter design.

- COM Left / Right Remap (A[3])
  This command bit is made for flexible layout of common signals in OLED module with common 0 arranged on either left or right side. Details of pin arrangement can be found in Figure 9-6.

- COM scan direction Remap (A[4])
  This bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa. Details of pin arrangement can be found in Figure 9-6.

- Odd even split of COM pins (A[5])
  This bit can set the odd even arrangement of COM pins.
  A[5] = 0: Disable COM split odd even, pin assignment of common is in sequential as
  COM131 COM130 .... COM 67 COM66..SC159...SA0..COM0 COM1.... COM64 COM65
  A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
  COM131 COM129.... COM3 COM1..SC159..SA0..COM0 COM2.... COM128 COM130
  Details of pin arrangement can be found in Figure 9-6.

- Display color mode (A[7:6])
  Select either 65k or 256 color mode. The display RAM data format in different mode is described in section 7.3.

Figure 9-6 : COM Pins Hardware Configuration (MUX ratio: 132)

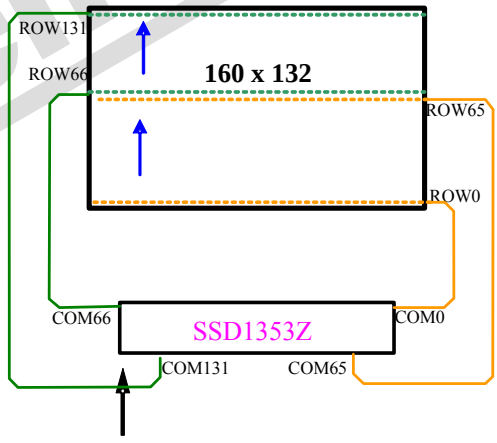
Case and Conditions

A

A[5] =0	A[4]=0	A[3]=0
Disable Odd Even Split of COM pins	COM Scan Direction : from COM0 to COM131	Disable COM Left / Right Remap

Pin name	Panel
COM 0	Row 0
COM 1	Row 1
COM 2	Row 2
… …	… …
COM 64	Row 64
COM 65	Row 65
COM 66	Row 66
COM 67	Row 67
…	… …
COM 129	Row 129
COM 130	Row 130
COM 131	Row 131

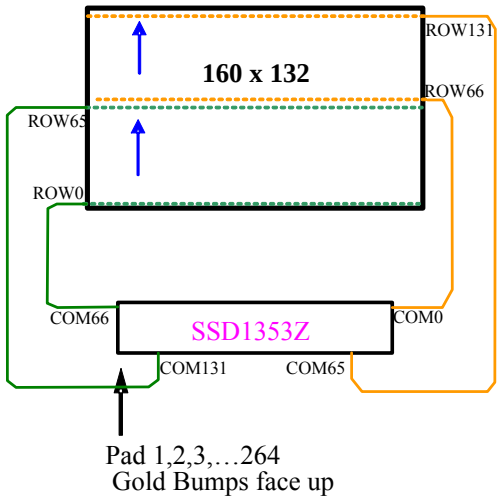
COM pins Configurations

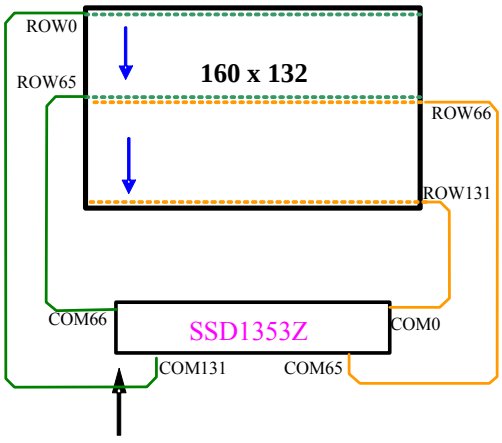
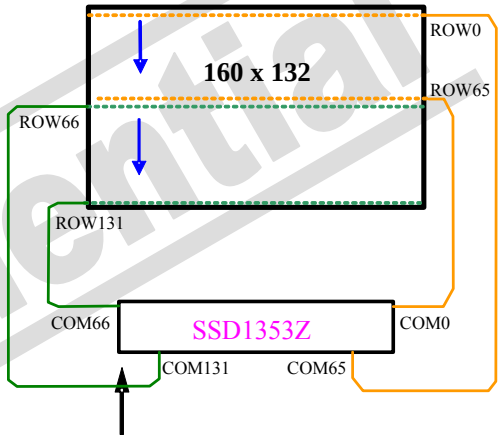
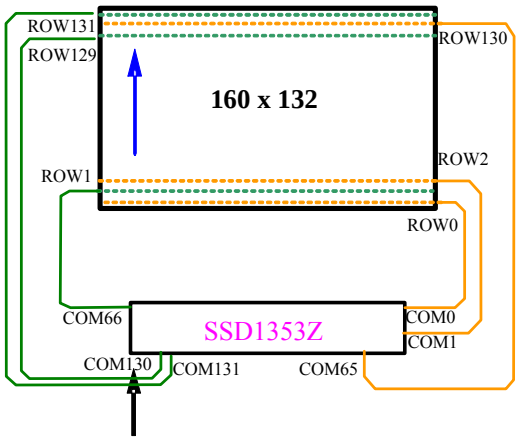


B

A[5] =0	A[4]=0	A[3]=1
Disable Odd Even Split of COM pins	COM Scan Direction : from COM0 to COM131	Enable COM Left / Right Remap

Pin name	Panel
COM 0	Row 66
COM 1	Row 67
COM 2	Row 68
… …	… …
COM 64	Row 130
COM 65	Row 131
COM 66	Row 0
COM 67	Row 1
…	… …
COM 129	Row 63
COM 130	Row 64
COM 131	Row 65

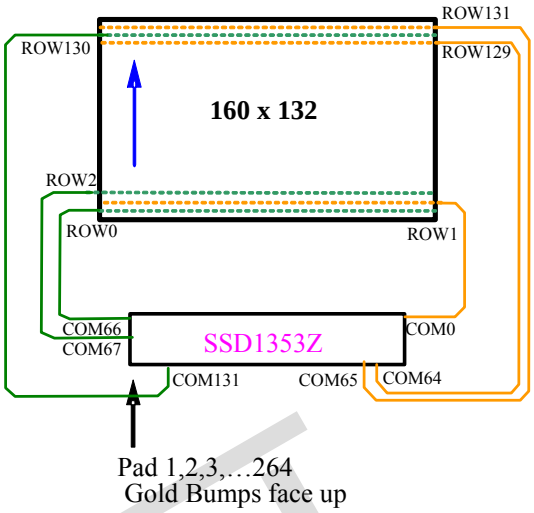


Case and Conditions	COM pins Configurations
C A[5] =0 / A[4]=1 / A[3]=0 Disable Odd Even Split of COM pins / COM Scan Direction : from COM131 to COM0 / Disable COM Left / Right Remap Pin name / Panel COM 0 Row 131 COM 1 Row 130 COM 2 Row 129 … … … … COM 64 Row 67 COM 65 Row 66 COM 66 Row 65 COM 67 Row 64 … … … COM 129 Row 2 COM 130 Row 1 COM 131 Row 0	 Pad 1,2,3,…264 Gold Bumps face up
D A[5] =0 / A[4]=1 / A[3]=1 Disable Odd Even Split of COM pins / COM Scan Direction : from COM131 to COM0 / Enable COM Left / Right Remap Pin name / Panel COM 0 Row 65 COM 1 Row 64 COM 2 Row 63 … … … … COM 64 Row 1 COM 65 Row 0 COM 66 Row 131 COM 67 Row 130 … … … COM 129 Row 68 COM 130 Row 67 COM 131 Row 66	 Pad 1,2,3,…264 Gold Bumps face up
E A[5] =1 / A[4]=0 / A[3]=0 Enable Odd Even Split of COM pins / COM Scan Direction : from COM0 to COM131 / Disable COM Left / Right Remap Pin name / Panel COM 0 Row 0 COM 1 Row 2 COM 2 Row 4 … … … … COM 64 Row 128 COM 65 Row 130 COM 66 Row 1 COM 67 Row 3 … … … COM 129 Row 127 COM 130 Row 129 COM 131 Row 131	 Pad 1,2,3,…264 Gold Bumps face up

Case and Conditions	COM pins Configurations
F	

A[5] =1	A[4]=0	A[3]=1
Enable Odd Even Split of COM pins	COM Scan Direction : from COM0 to COM131	Enable COM Left / Right Remap

Pin name	Panel
COM 0	Row 1
COM 1	Row 3
COM 2	Row 5
… …	… …
COM 64	Row 129
COM 65	Row 131
COM 66	Row 0
COM 67	Row 2
…	… …
COM 129	Row 126
COM 130	Row 128
COM 131	Row 130

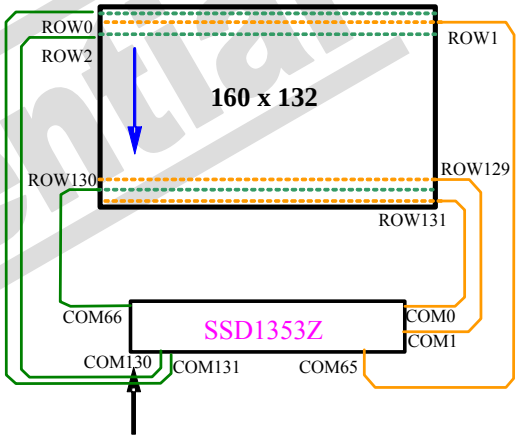


Pad 1,2,3,…264
Gold Bumps face up

G

A[5] =1	A[4]=1	A[3]=0
Enable Odd Even Split of COM pins	COM Scan Direction : from COM131 to COM0	Disable COM Left / Right Remap

Pin name	Panel
COM 0	Row 131
COM 1	Row 129
COM 2	Row 127
… …	… …
COM 64	Row 3
COM 65	Row 1
COM 66	Row 130
COM 67	Row 128
…	… …
COM 129	Row 4
COM 130	Row 2
COM 131	Row 0

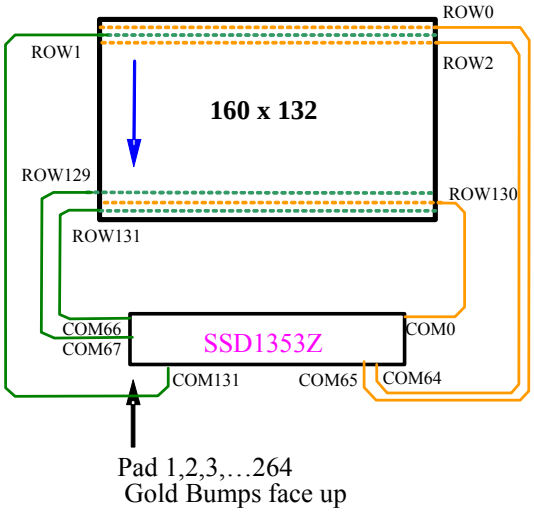


Pad 1,2,3,…264
Gold Bumps face up

H

A[5] =1	A[4]=1	A[3]=1
Enable Odd Even Split of COM pins	COM Scan Direction : from COM131 to COM0	Enable COM Left / Right Remap

Pin name	Panel
COM 0	Row 130
COM 1	Row 128
COM 2	Row 126
… …	… …
COM 64	Row 2
COM 65	Row 0
COM 66	Row 131
COM 67	Row 129
…	… …
COM 129	Row 5
COM 130	Row 3
COM 131	Row 1



Pad 1,2,3,…264
Gold Bumps face up

9.1.9 Set Display Start Line (A1h)

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 131. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 9-7 : Example of Set Display Start Line with no Remap

	132	132	100	100	MUX ratio (A8h)
COM Pin	0	32	0	32	Display start line (A1h)
COM0	Row0	Row32	Row0	Row32	
COM1	Row1	Row33	Row1	Row33	
COM2	Row2	Row34	Row2	Row34	
COM3	Row3	Row35	Row3	Row35	
COM4	Row4	Row36	Row4	Row36	
COM5	Row5	Row37	Row5	Row37	
COM6	Row6	Row38	Row6	Row38	
:	:	:	:	:	
:	:	:	:	:	
:	:	:	:	:	
:	:	:	:	:	
COM95	Row95	Row127	Row95	Row128	
COM96	Row96	Row128	Row96	Row129	
COM97	Row97	Row129	Row97	Row130	
COM98	Row98	Row130	Row98	Row131	
COM99	Row99	Row131	Row99	Row0	
COM100	Row100	Row0	-	-	
COM101	Row101	Row1	-	-	
COM102	Row102	Row2	-	-	
COM103	Row103	Row3	-	-	
COM104	Row104	Row4	-	-	
COM105	Row105	Row5	-	-	
COM106	Row106	Row6	-	-	
COM107	Row107	Row7	-	-	
COM108	Row108	Row8	-	-	
COM109	Row109	Row9	-	-	
COM110	Row110	Row10	-	-	
COM111	Row111	Row11	-	-	
COM112	Row112	Row12	-	-	
COM113	Row113	Row13	-	-	
COM114	Row114	Row14	-	-	
COM115	Row115	Row15	-	-	
COM116	Row116	Row16	-	-	
COM117	Row117	Row17	-	-	
COM118	Row118	Row18	-	-	
COM119	Row119	Row19	-	-	
COM120	Row120	Row20	-	-	
COM121	Row121	Row21	-	-	
COM122	Row122	Row22	-	-	
COM123	Row123	Row23	-	-	
COM124	Row124	Row24	-	-	
COM125	Row125	Row25	-	-	
COM126	Row126	Row26	-	-	
COM127	Row127	Row27	-	-	
COM128	Row128	Row28	-	-	
COM129	Row129	Row29	-	-	
COM130	Row130	Row30	-	-	
COM131	Row131	Row31	-	-	
Display example	 (a)	 (b)	 (c)	 (d)	 (GDDARAM)	

9.1.10 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-131. For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second command should be given by 0010000. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 9-8 : Example of Set Display Offset with no Remap

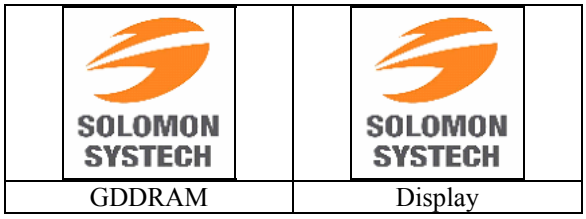
	132	132	100	100	MUX ratio (A8h)
COM Pin	0	32	0	32	Display offset (A2h)
COM0	Row0	Row32	Row0	Row32	
COM1	Row1	Row33	Row1	Row33	
COM2	Row2	Row34	Row2	Row34	
COM3	Row3	Row35	Row3	Row35	
COM4	Row4	Row36	Row4	Row36	
COM5	Row5	Row37	Row5	Row37	
COM6	Row6	Row38	Row6	Row38	
:	:	:	:	:	
:	:	:	:	:	
COM66	Row66	Row98	Row66	Row98	
COM67	Row67	Row99	Row67	Row99	
:	:	:	:	:	
:	:	:	:	:	
COM95	Row95	Row127	Row95	-	
COM96	Row96	Row128	Row96	-	
COM97	Row97	Row129	Row97	-	
COM98	Row98	Row130	Row98	-	
COM99	Row99	Row131	Row99	Row0	
COM100	Row100	Row0	-	Row1	
COM101	Row101	Row1	-	Row2	
COM102	Row102	Row2	-	Row3	
COM103	Row103	Row3	-	Row4	
COM104	Row104	Row4	-	Row5	
COM105	Row105	Row5	-	Row6	
COM106	Row106	Row6	-	Row7	
COM107	Row107	Row7	-	Row8	
COM108	Row108	Row8	-	Row9	
COM109	Row109	Row9	-	Row10	
COM110	Row110	Row10	-	Row11	
COM111	Row111	Row11	-	Row12	
COM112	Row112	Row12	-	Row13	
COM113	Row113	Row13	-	Row14	
COM114	Row114	Row14	-	Row15	
COM115	Row115	Row15	-	Row16	
COM116	Row116	Row16	-	Row17	
COM117	Row117	Row17	-	Row18	
COM118	Row118	Row18	-	Row19	
COM119	Row119	Row19	-	Row21	
COM120	Row120	Row20	-	Row20	
COM121	Row121	Row21	-	Row22	
COM122	Row122	Row22	-	Row23	
COM123	Row123	Row23	-	Row22	
COM124	Row124	Row24	-	Row24	
COM125	Row125	Row25	-	Row25	
COM126	Row126	Row26	-	Row26	
COM127	Row127	Row27	-	Row27	
COM128	Row128	Row28	-	Row28	
COM129	Row129	Row29	-	Row29	
COM130	Row130	Row30	-	Row30	
COM131	Row131	Row31	-	Row31	
Display example	 (a)	 (b)	 (c)	 (d)	 (GDDARAM)

9.1.11 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display ON, Entire Display OFF and Inverse Display.

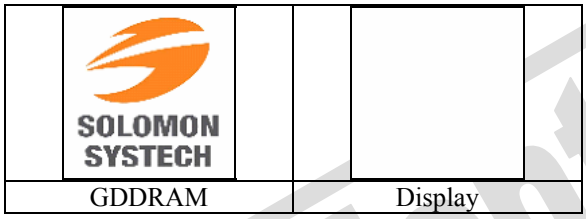
- Normal Display (A4h)
  Reset the above effect and turn the data to ON at the corresponding gray level. Figure 9-9 shows an example of Normal Display.

Figure 9-9 : Example of Normal Display



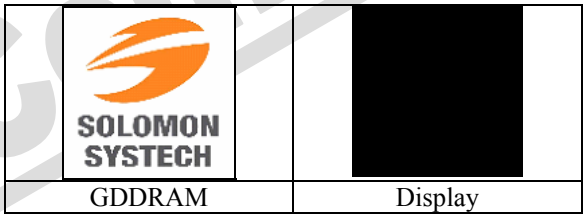
- Set Entire Display ON (A5h)
  Forces the entire display to be at "GS63" regardless of the contents of the display data RAM as shown in Figure 9-10.

Figure 9-10 : Example of Entire Display ON



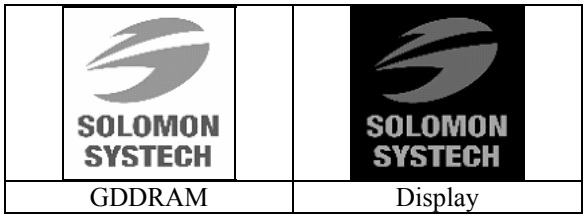
- Set Entire Display OFF (A6h)
  Forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM as shown in Figure 9-11.

Figure 9-11 : Example of Entire Display OFF



- Inverse Display (A7h)
  The gray level of display data are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", …..
  Figure 9-12 shows an example of inverse display.

Figure 9-12 : Example of Inverse Display



9.1.12 Set Multiplex Ratio (A8h)

This command switches default 1:132 multiplex mode to any multiplex mode from 16 to 132. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h. Figure 9-7 and Figure 9-8 show examples of setting the multiplex ratio through command A8h.

9.1.13 Dim mode setting (ABh)

This command contains multiple bits to configure the dim mode display parameters.
Contrast setting of color A, B, C and precharge voltage can be set different to normal mode (AFh).

9.1.14 Set Display ON/OFF (ACh / AEh / AFh)

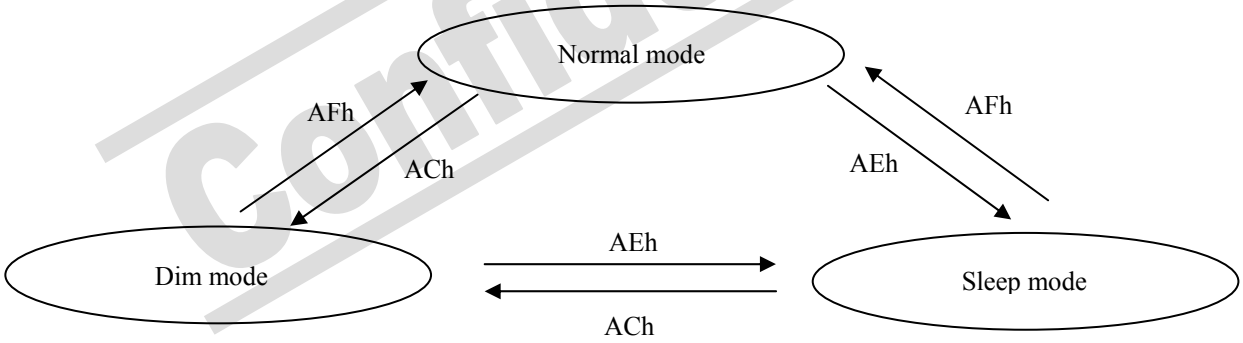
These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned off and the segment and common output are in high impedance state.

These commands set the display to one of the three states:

- ACh : Dim Mode Display ON
- AEh : Display OFF
- AFh : Normal Brightness Display ON

where the dim mode settings are controlled by command ABh.

Figure 9-13 : Transition between different modes



9.1.15 Phase 1 and 2 Period Adjustment (B1h)

This command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 3 to 31 in the unit of 2 DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 2 to 15 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P for color A, B and C.

9.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (B3h)

This command consists of two functions:

- Display Clock Divide Ratio (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to section 7.5.1 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency setting available.

9.1.17 Set Second Pre-charge period (B4h)

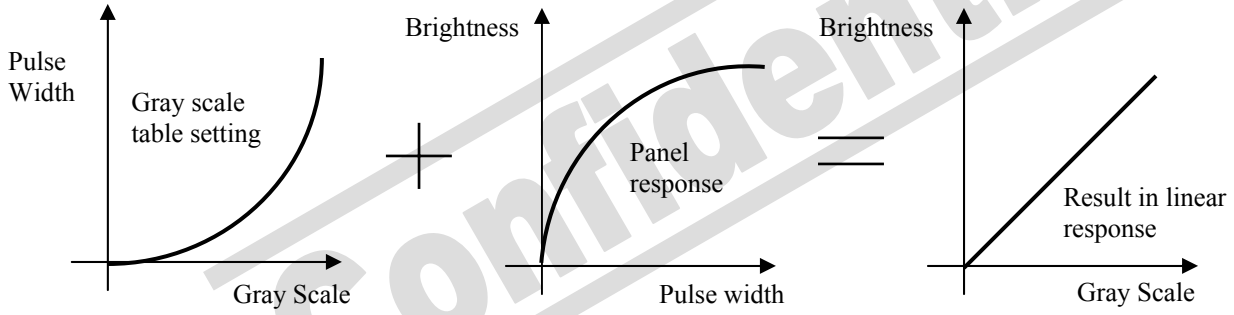
This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command B4h and it is ranged from 0 to 15 DCLK's. Please refer to Table 8-1 for the details of setting.

9.1.18 Set Gray Scale Table (B8h)

This command is used to set the Gray Scale (GS) table for the display. Except GS0, which is zero as it has no pre-charge and current drive, each entry GS level is programmed in the Gamma Setting. The larger value of Gamma Setting, the brighter is the OLED pixel when it's turned ON. Following the command B8h, the user has to set the Gamma Setting for GS1, GS2, GS3, …, GS61, GS62, GS63 one by one in sequence. Refer to Section 7.8 for details.

The setting of Gray Scale entry can perform Gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate Gray Scale table setting like example below can compensate this effect.

Figure 9-14 : Example of Gamma correction by Gamma Look Up table setting



9.1.19 Enable Linear Gray Scale Table (B9h)

This command reloads the preset linear Gray Scale table as GS0 =Gamma Setting 0, GS1 = Gamma Setting 2, GS2 = Gamma Setting 4, ..., GS31=Gamma Setting 62, GS32=Gamma Setting 65, GS33=Gamma Setting 67, …., GS62 = Gamma Setting 125, GS63 = Gamma Setting 127. Refer to Section 7.8 for details.

9.1.20 Set Pre- charge voltage (BBh)

This command sets the pre-charge voltage level of segment pins, The level of pre-charge is programmed with reference to V_{CC}.

9.1.21 Set V_{COMH} Voltage (BEh)

This command sets the high voltage level of common pins, V_{COMH}. The level of V_{COMH} is programmed with reference to V_{CC}.

9.1.22 Software Reset (E2h)

This command resets the display circuit and stops the Graphic Acceleration operations by generating an internal reset pulse.

9.1.23 NOP (E3h)

This is the no operation command.

9.1.24 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

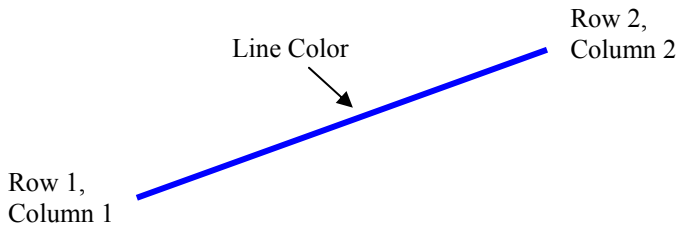
Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the “Lock” state. And the driver IC will then respond to the command and memory access.

9.2 Graphic Acceleration Command

9.2.1 Draw Line (21h)

This command draws a line by the given start, end column and row coordinates and the color of the line.

Figure 9-15 : Example of Draw Line Command



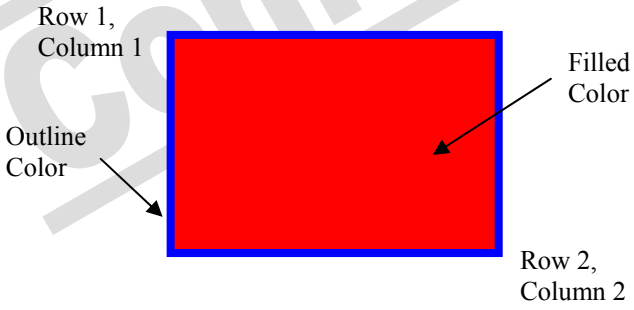
For example, the line above can be drawn by the following command sequence.

1. Enter into draw line mode by command 21h
2. Send column start address of line, column1, for example = 1h
3. Send row start address of line, row 1, for example = 10h
4. Send column end address of line, column 2, for example = 28h
5. Send row end address of line, row 2, for example = 4h
6. Send color C, B and A of line, for example = (3Fh, 0h, 0h)

9.2.2 Draw Rectangle (22h)

Given the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2), specify the outline and fill area colors, a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled (refer to command 26h Fill Enable/Disable), the enclosed area will not be filled.

Figure 9-16 : Example of Draw Rectangle Command



The following example illustrates the rectangle drawing command sequence.

1. Enter the “draw rectangle mode” by execute the command 22h
2. Set the starting column coordinates, Column 1, for example = 03h
3. Set the starting row coordinates, Row 1, for example = 02h
4. Set the finishing column coordinates, Column 2, for example = 12h
5. Set the finishing row coordinates, Row 2, for example = 15h
6. Set the outline color C, B and A, for example = (63d, 0d, 0d)
7. Set the filled color C, B and A, for example = (0d, 0d, 63d)

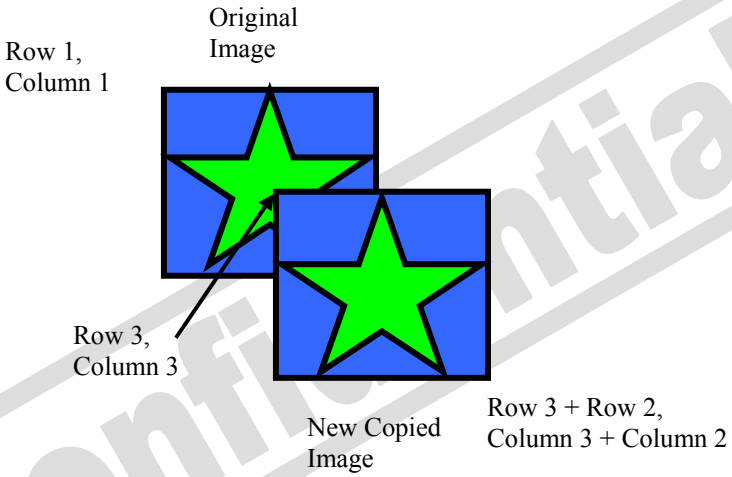
9.2.3 Copy (23h)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

1. Enter the "copy mode" by execute the command 23h
2. Set the starting column coordinates, Column 1, for example = 00h.
3. Set the starting row coordinates, Row 1, for example = 00h.
4. Set the finishing column coordinates, Column 2, for example = 05h
5. Set the finishing row coordinates, Row 2, for example = 05h
6. Set the new column coordinates, Column 3, for example = 03h
7. Set the new row coordinates, Row 3, for example = 03h

Figure 9-17 : Example of Copy Command



9.2.4 Dim Window (24h)

This command will dim the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2). After the execution of this command, the selected window area will become darker as follow.

Table 9-1 : Result of Change of Brightness by Dim Window Command

Original gray scale	New gray scale after dim window command
GS0 ~ GS15	No change
GS16 ~ GS19	GS4
GS20 ~ GS23	GS5
:	:
GS60 ~ GS63	GS15

Additional execution of this command over the same window area will not change the data content.

9.2.5 Clear Window (25h)

This command sets the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to clear the window display. The graphic display data RAM content of the specified window area will be set to zero.

This command can be combined with Copy command to make as a "move" result. The following example illustrates the copy plus clear procedure and results in moving the window object.

1. Enter the "copy mode" by execute the command 23h
2. Set the starting column coordinates, Column 1, for example = 00h.
3. Set the starting row coordinates, Row 1, for example = 00h.
4. Set the finishing column coordinates, Column 2, for example = 05h
5. Set the finishing row coordinates, Row 2, for example 05h
6. Set the new column coordinates, Column 3, for example = 06h
7. Set the new row coordinates, Row 3, for example = 06h
8. Enter the "clear mode" by execute the command 24h
9. Set the starting column coordinates, Column 1, for example = 00h.
10. Set the starting row coordinates, Row 1, for example = 00h.
11. Set the finishing column coordinates, Column 2, for example = 05h
12. Set the finishing row coordinates, Row 2, for example = 05h

Figure 9-18 : Example of Copy + Clear = Move Command

9.2.6 Fill Enable/Disable (26h)

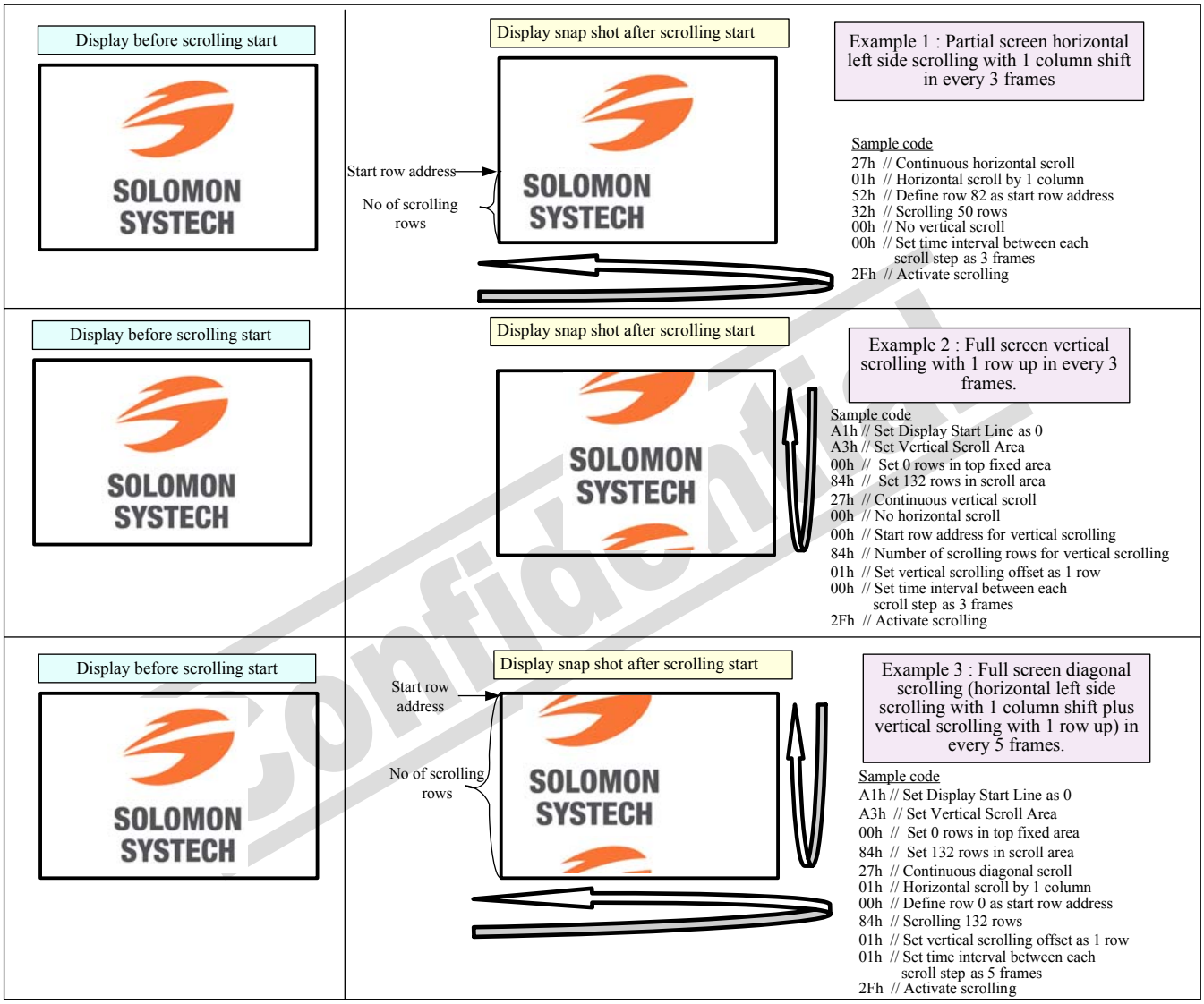
This command has two functions.

- Enable/Disable fill (A[0])
  0 = Disable filling of color into rectangle in draw rectangle command. (reset)
  1 = Enable filling of color into rectangle in draw rectangle command.
- Enable/Disable reverse copy (A[4])
  0 = Disable reverse copy (reset)
  1 = During copy command, the new image colors are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", ….

9.2.7 Horizontal Scroll Setup (27h)

This command setup the parameters required for horizontal and vertical scrolling. The parameters should not be changed after scrolling is activated

Figure 9-19 : Examples of Continuous Horizontal and Vertical Scrolling command setup



9.2.8 Deactivate Horizontal Scroll (2Eh)

This command deactivates the scrolling function. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

9.2.9 Activate Horizontal Scroll (2Fh)

This command activates the scrolling function according to the setting done by Continuous Horizontal & Vertical Scrolling Setup command 27h.

9.2.10 Set Vertical Scroll Area(A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For details please refer to Table 8-1.

10 MAXIMUM RATINGS

Table 10-1 : Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to 2.75	V
V_{CC}		-0.5 to 22.0	V
V_{DDIO}		-0.5 to V_{CI}	V
V_{CI}		-0.3 to 4.0	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	Vss-0.3 to V_{DDIO}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

11 DC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD} = 2.4 to 2.6V
V_{CI} = 2.4 to 3.5V (V_{CI} must be larger than or equal to V_{DD})
T_A = 25°C

Table 11-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	10	-	21	V
V_{DD}	Logic Supply Voltage	-	2.4	-	2.6	V
V_{CI}	Low voltage power supply	-	2.4	-	3.5	V
V_{DDIO}	Power Supply for I/O pins	-	1.6	-	V_{CI}	V
V_{OH}	High Logic Output Level	Iout =100uA	0.9*V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low Logic Output Level	Iout =100uA	0	-	0.1*V_{DDIO}	V
V_{IH}	High Logic Input Level	-	0.8*V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low Logic Input Level	-	0	-	0.2*V_{DDIO}	V
I_{SLP_VDD}	V_{DD} Sleep mode Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD}(external) = 2.5V, Display OFF, No panel attached	-	-	15	uA
I_{SLP_VDDIO}	V_{DDIO} Sleep mode Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD}(external) = 2.5V, Display OFF, No panel attached	-	-	15	uA
I_{SLP_VCI}	V_{CI} Sleep mode Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD}(external) = 2.5V, Display OFF, No panel attached	-	-	15	uA
I_{SLP_VCC}	V_{CC} Sleep mode Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD}(external) = 2.5V, Display OFF, No panel attached	-	-	15	uA
I_{DD}	V_{DD} Supply Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD} = 2.5V, V_{CC} = 21V, Display ON, No panel attached, contrast = FF	-	TBD	-	uA
I_{DDIO}	V_{DDIO} Supply Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD} = 2.5V, V_{CC} = 21V, Display ON, No panel attached, contrast = FF	-	TBD	-	uA
I_{CI}	V_{CI} Supply Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD} = 2.5V, V_{CC} = 21V, Display ON, No panel attached, contrast = FF	-	TBD	-	uA
I_{CC}	V_{CC} Supply Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD} = 2.5V, V_{CC} = 21V, Display ON, No panel attached, contrast = FF	-	TBD	-	uA
I_{SEG}	Segment Output Current Setting V_{CC}=18V, I_{REF}=10uA	Contrast = FF , GS=127	-	160	-	uA
		Contrast = 7F, GS=127	-	80	-	uA
		Contrast = 7F, GS= 63	-	40	-	uA
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} = Segment current at contrast FF	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

12 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD}=2.4 to2.6V
T_A = 25°C

Table 12-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.5V	-	1.6	-	MHz
F_{FRM}	Frame Frequency for 132 MUX Mode	160x132 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} * 1/(D*K*132) (2)	-	Hz
t_{RES}	Reset low pulse width (RES#)	-	100	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value.

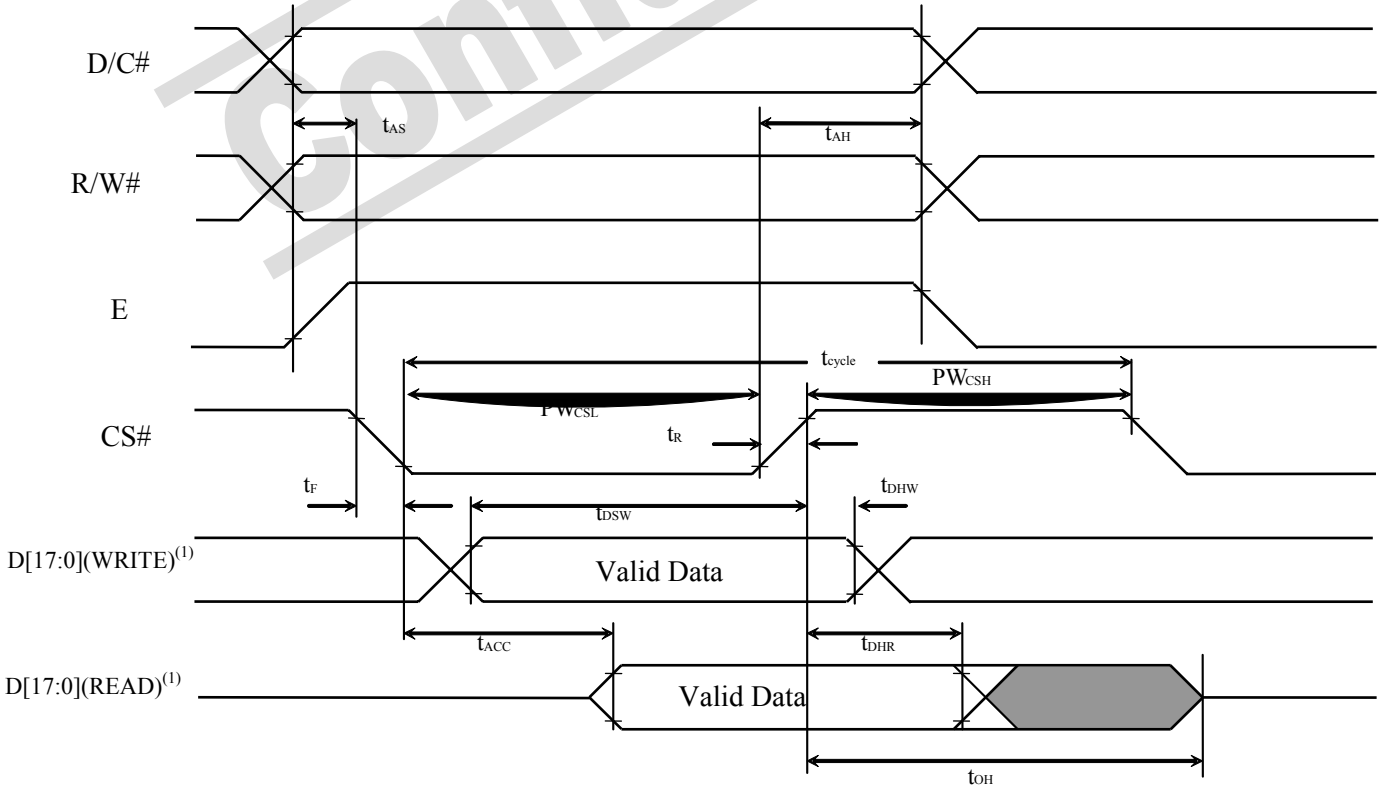
(2) D: divide ratio
K: Phase 1 period +Phase 2 period + 98

Table 12-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 12-1 : 6800-series MCU parallel interface characteristics



Note

(1) when 8 bit used: D[7:0] instead; when 9 bit used: D[8:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

Table 12-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 12-2 : 8080-series MCU parallel interface characteristics (Form 1)

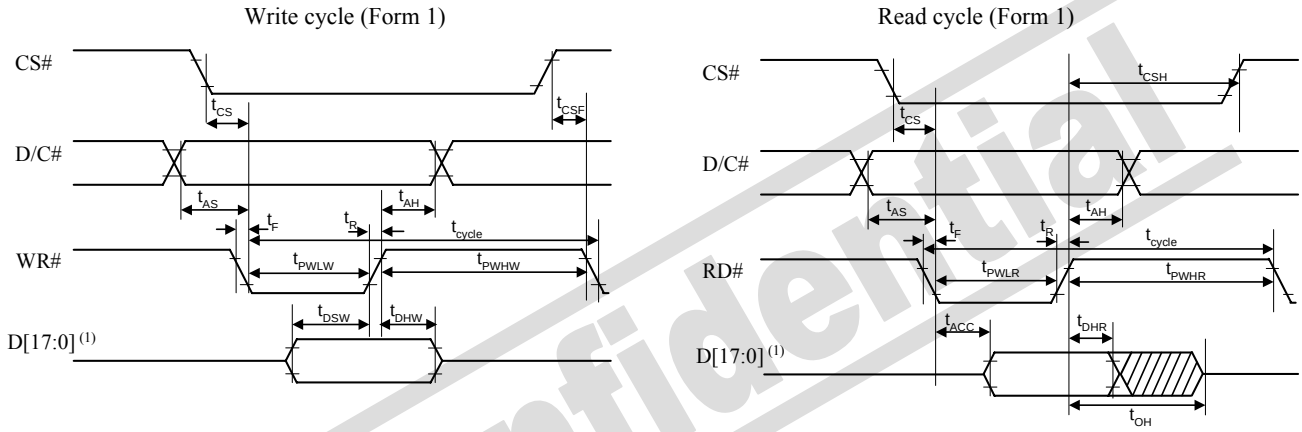
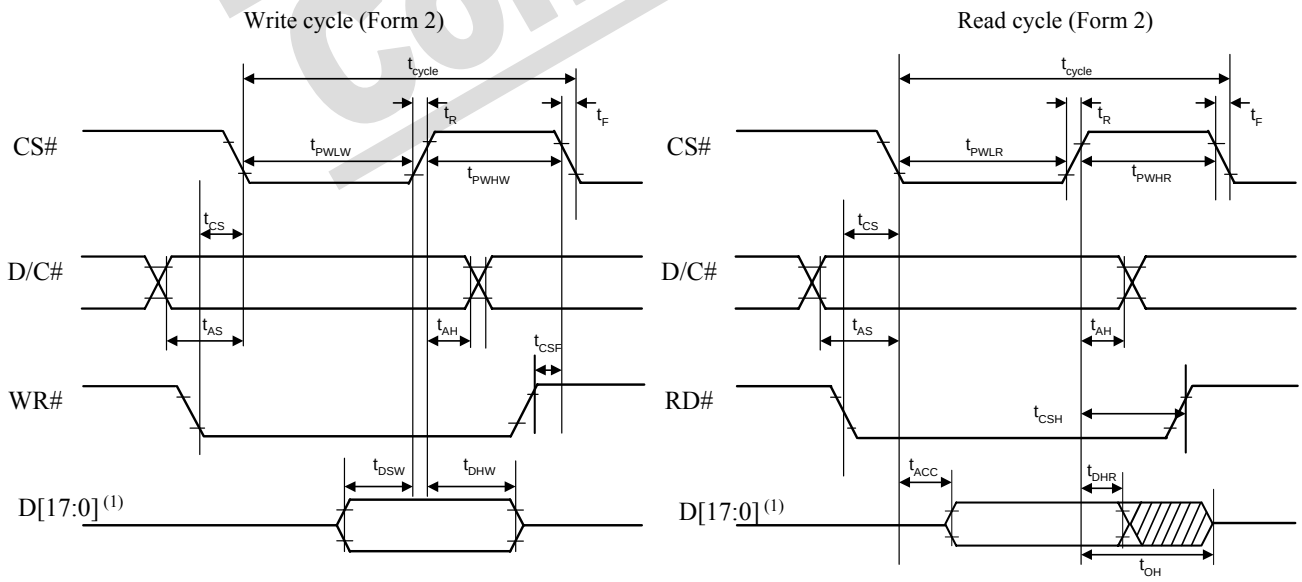


Figure 12-3 : 8080-series MCU parallel interface characteristics (Form 2)



Note

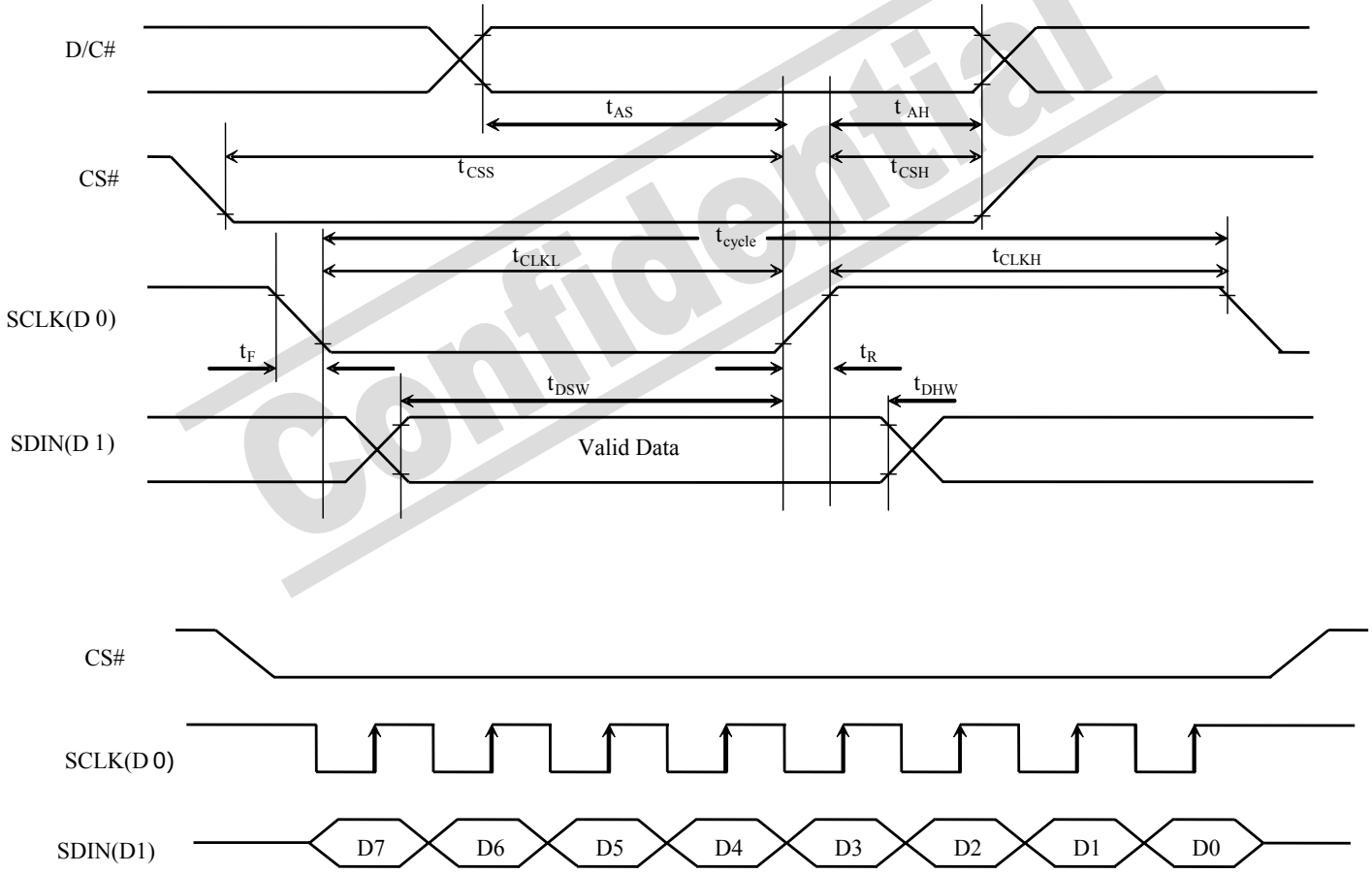
(1) when 8 bit used: D[7:0] instead; when 9 bit used: D[8:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

Table 12-4 : Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

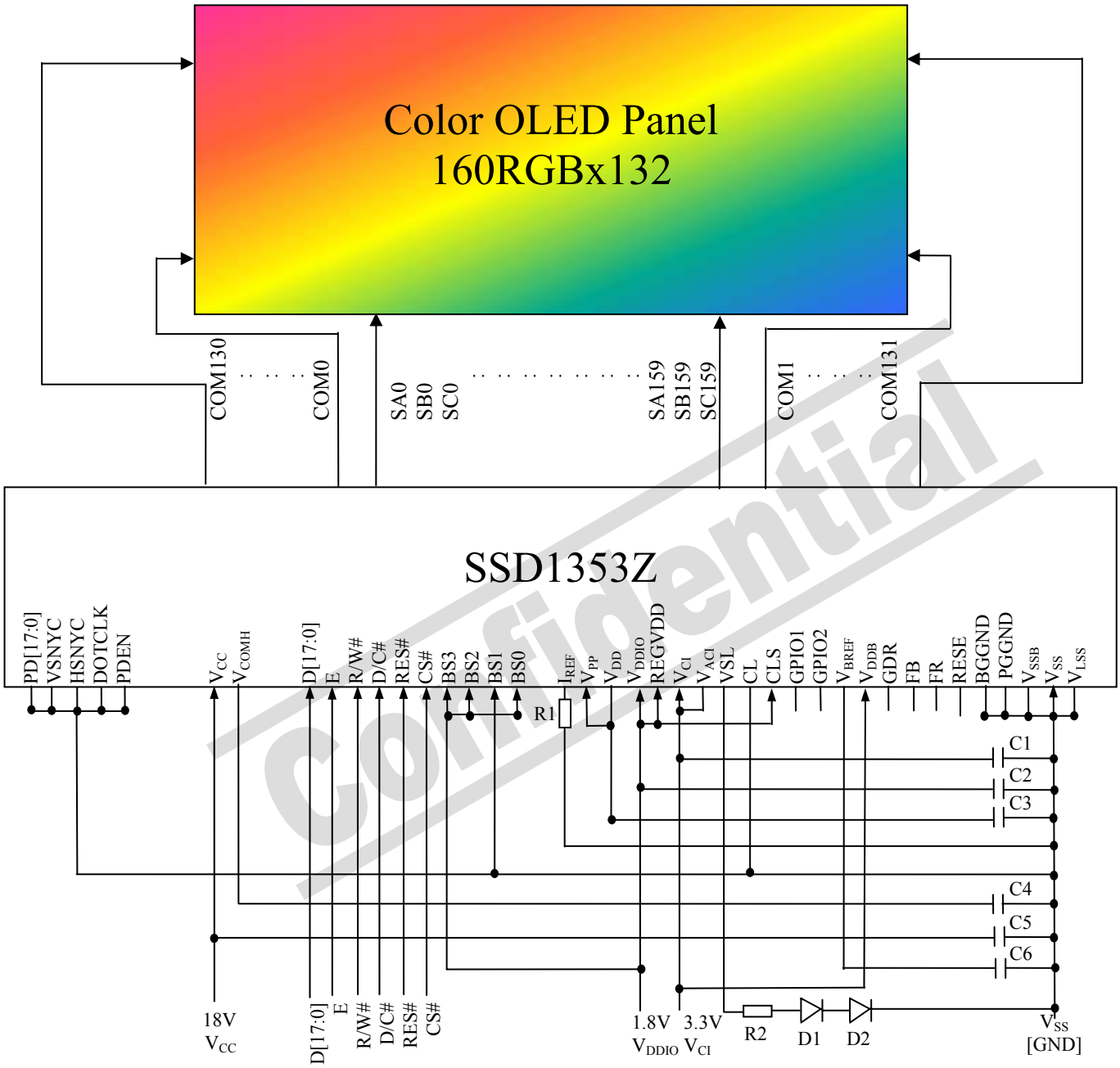
Figure 12-4 : Serial interface characteristics



13 APPLICATION EXAMPLE

Figure 13-1 : SSD1353 application example for 18-bit 6800-parallel interface mode (Internal regulated V_{DD})

The configuration for 18-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{CI} =3.3V(V_{CI} must be > 2.6V), Internal regulated V_{DD} = 2.5V, V_{DDIO} =1.8V, external V_{CC} = 18V, I_{REF} = 10uA)

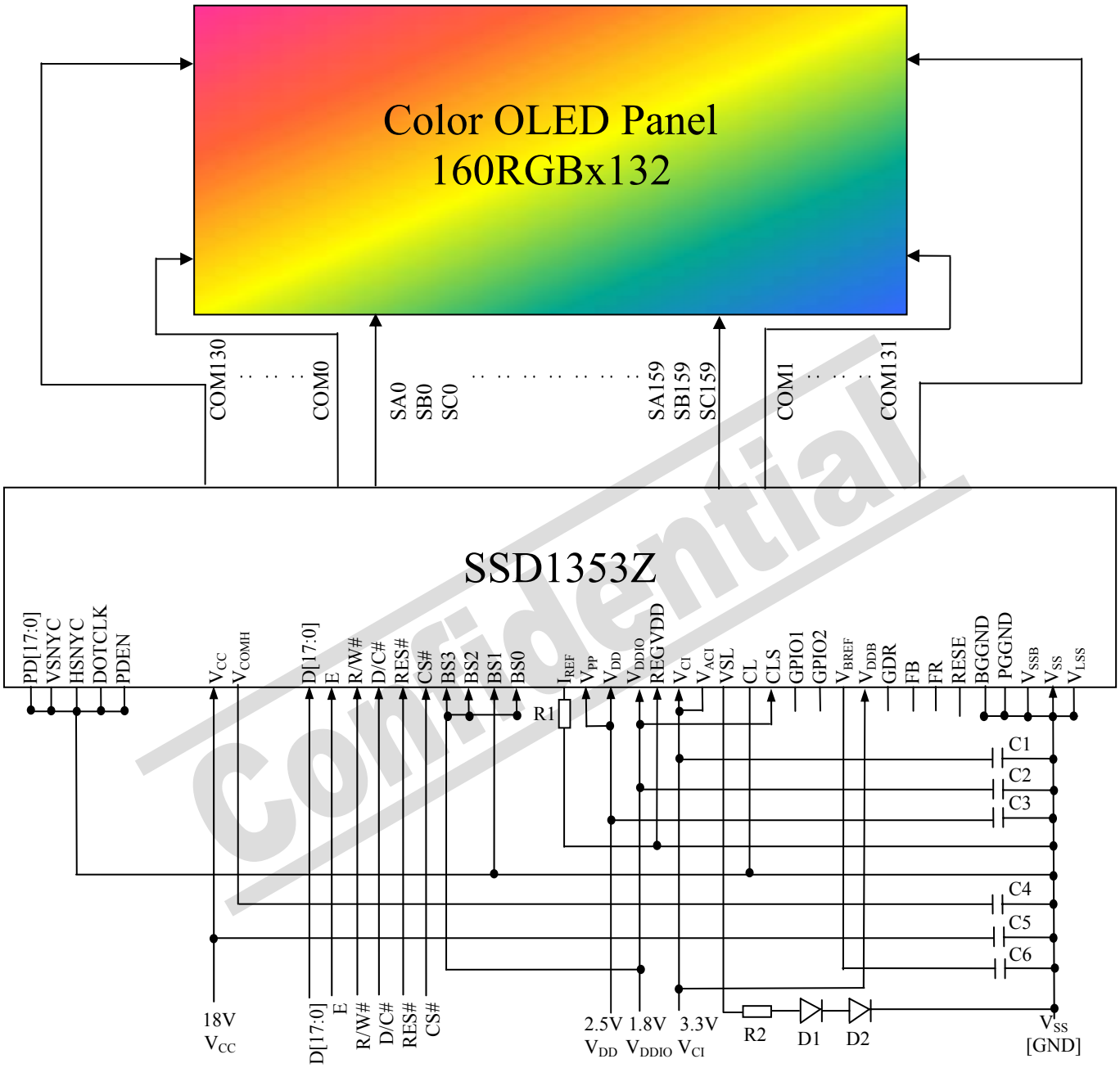


Voltage at I_{REF} = V_{CC} – 3V. For V_{CC} = 18V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (18-3)/10u
= 1.5MΩ
R2 = 50Ω, 1/8W (1)
D1-D2= V_{th}=0.7V, 1N4148 (1)
C1-C3: 1uF, C4-C5: 4.7uF , C6 : 68nF (1)

Note
(1) The value is recommended value. Select appropriate value against module application.

Figure 13-2 : SSD1353 application example for 18-bit 6800-parallel interface mode (External V_{DD})

The configuration for 18-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{CI} =3.3V (2.4V < V_{CI} <3.5V), External V_{DD} = 2.5V, V_{DDIO} =1.8V, external V_{CC} = 18V, I_{REF} = 10uA)



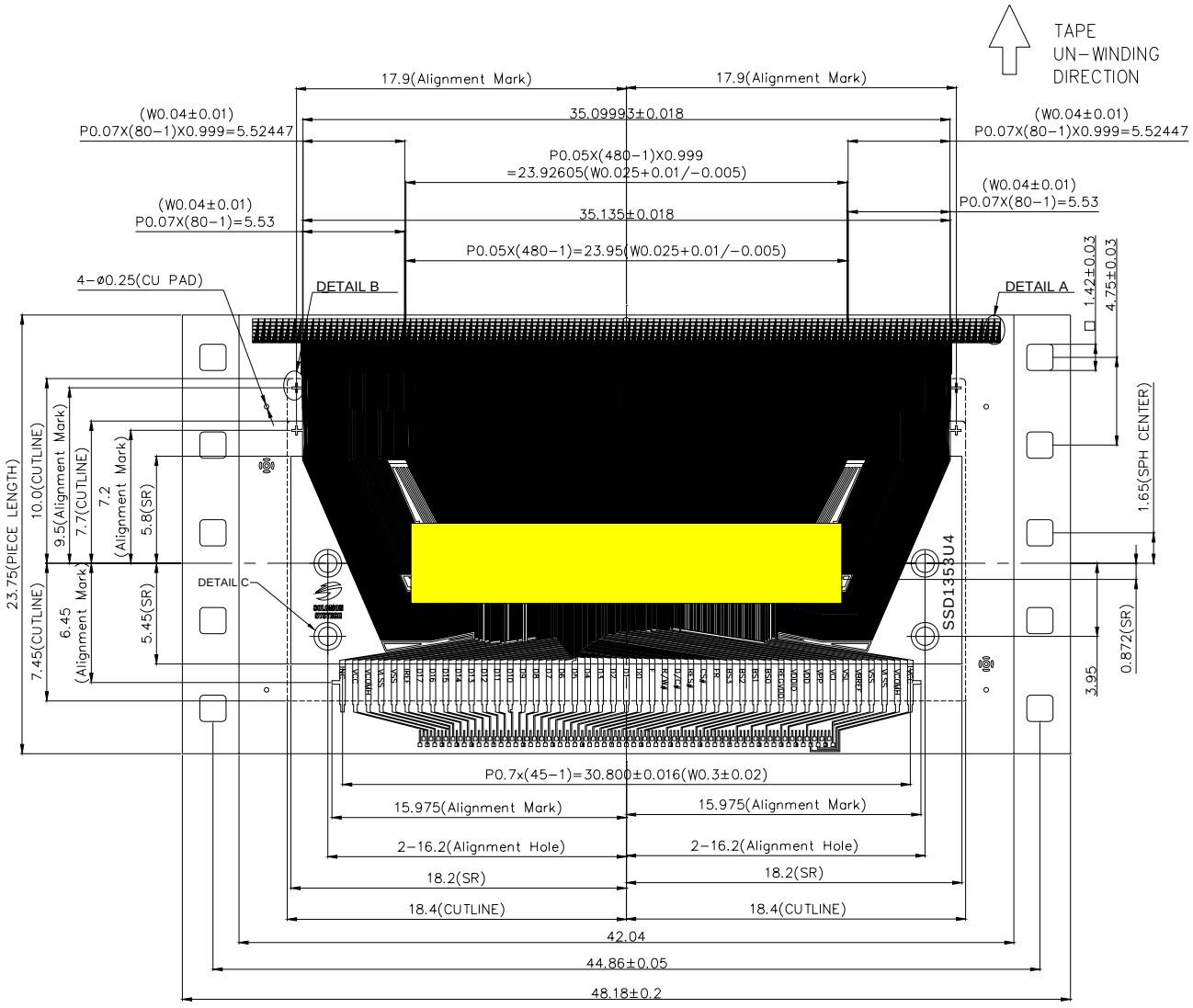
Voltage at I_{REF} = V_{CC} – 3V. For V_{CC} = 18V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (18-3)/10u
= 1.5MΩ
R2 = 50Ω, 1/8W (1)
D1-D2= V_{th}=0.7V, 1N4148 (1)
C1-C3: 1uF, C4-C5: 4.7uF , C6 : 68nF (1)

Note
(1) The value is recommended value. Select appropriate value against module application.

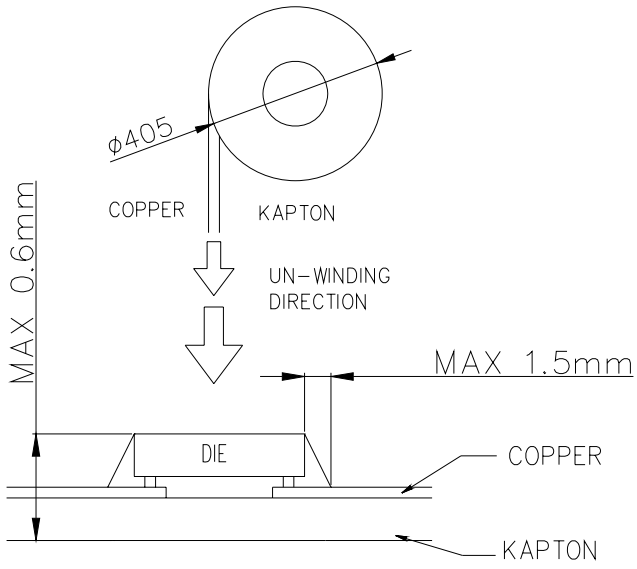
14 PACKAGE DIMENSION

14.1 SSD1353U4R1 Detail Dimension

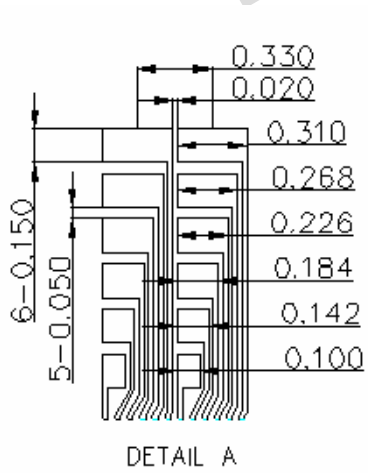
Figure 14-1: SSD1353U4R1 detail dimension



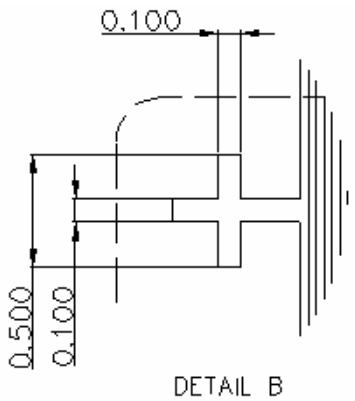
NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 15±10um
   (OTHER TOLERANCE: ±0.200mm)
3. Sn PLATING 0.23±0.050mm
4. TAPSITE: 5 SPH, 23.75mm



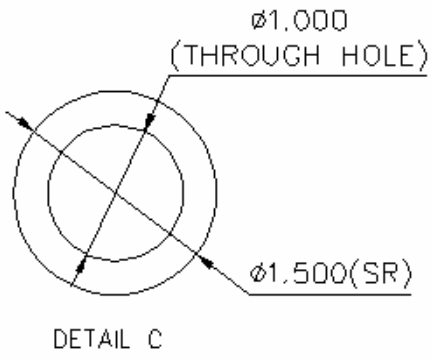
MIRROR DESIGN



DETAIL A



DETAIL B



DETAIL C

http://www.solomon-systech.com