GLOSSARY OF ACRONYMS

CD — Card Detect
CLK — Clock
CMD — Command
FET — Field-Effect Transistor
GPIO — General Purpose I/O
I/O — Input/Output
MMC — Multimedia Card
SD/SDIO — Secure Digital/Input Output
WP — Write Protect

FEATURED TECHNOLOGY | By Prasad Dhond

Interfacing a Low-voltage Processor with 3 V SD/SDIO or MMC Cards

Today's world of shrinking real estate, multiple power requirements, diverse interfaces and multiple solutions present the designer with a dizzying array of options. As processors evolve in complexity and function, they will place even more demands upon interface designs. Today, many digital baseband processors already have maximum I/O voltages restricted to as low as 1.8 V. As processors advance and I/O and core voltages continue to drop, there is a growing discrepancy between the processor and peripheral I/O voltages.

The task of interfacing voltage-disparaging devices has come to the forefront of many designers' radar screens. Modern processors have I/O supply voltage requirements of 1.8 V or lower, but many peripherals continue to operate at higher voltages.

For example, the majority of removable-flash memory cards used in today's applications are operated at 3 V. To enable error-free communication between a low-voltage processor and a 3 V memory card, for example, a voltage-level translator is used to interface the different voltage levels.

Figure 1 shows a schematic where the processor and SD/SDIO card are operating at the same voltage level. The SDIO interface consists of four data signals (DAT0-3), one CLK signal and one CMD signal. The data and command signals are bi-directional, whereas the clock signal is uni-directional. The card connector typically has mechanical WP and CD switches. These WP and CD signals are sent back to the processor to implement control functions, such as powering up certain sections of the board. Pull-up resistors to V_{DD} are connected from the data and command lines to prevent them from floating when the card is removed or when card outputs are disabled.

If the processor and SDIO peripheral are operating at different interface supply voltages, then a level translator has to be added to the system to ensure switching compatibility. There are different options to implement this level-translation scheme, and depending on application conditions, one option may be preferred over another.

In particular, the bi-directional data and command lines pose a quandary to the system designer, regarding the choice of a

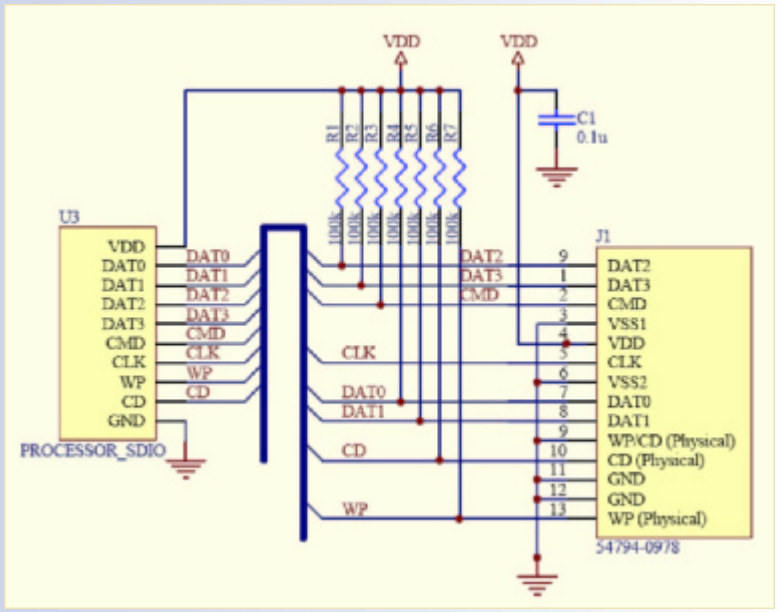

Figure 1. Typical interface between a processor and an SD/SDIO card.

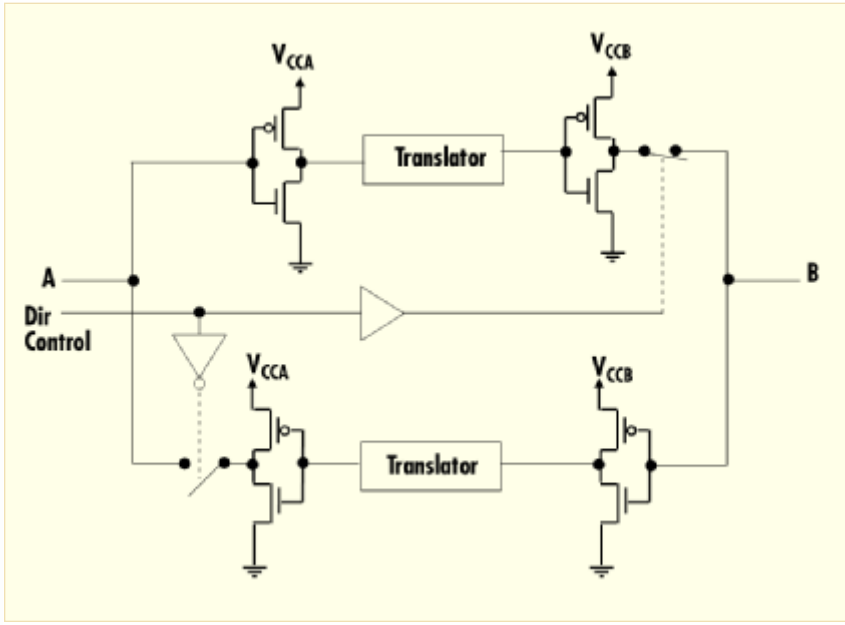

Figure 2. Fully buffered voltage translation.

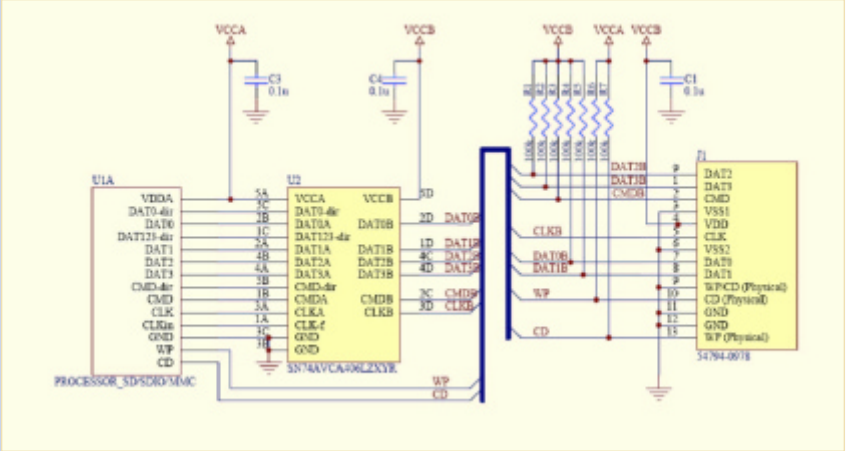

Figure 3. Using a fully buffered voltage translator between the processor and memory card.

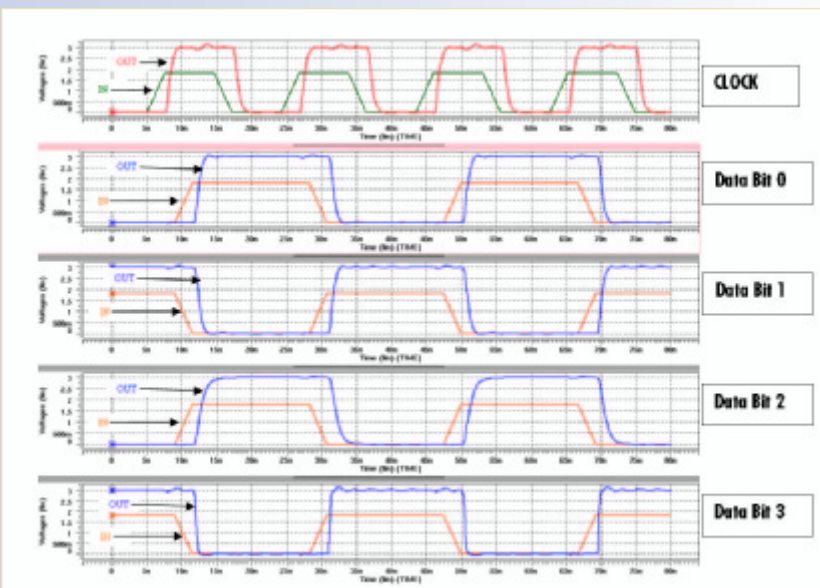

Figure 4. 52 MHz clock signal and 52 Mb/s data signals being translated from 1.8 to 3 V using a fully buffered solution.

level-translation solution in terms of how to control the flow of data and command signals from processor to card and vice-versa. There are various approaches to this problem. One option is to use a level-translating transceiver with a direction-control pin. The other option is to use a "directionless" level translator.

Option 1. A Level Translator with a Direction-control Pin

A bi-directional translator with a direction-control pin is shown in Figure 2. The output transistors are typically sized to offer several tens of mA of DC current, and the data rate is restricted only by the output capacitive load and switching speed of the transistors. This solution is called a "fully buffered" translator.

Figure 3 shows how this translator might be used in the SD/SDIO interface. One obvious drawback of this solution is the extra processor GPIOs that are needed for the direction signals (DAT0-dir, DAT123-dir and CMD-dir), which control the data and command lines as shown in Figure 3. Another disadvantage is the extra software programming that is needed in the processor to set these signals correctly.

However, there are several advantages to using a fully buffered solution in this application. Card specifications such as MMC 4.1 specify that the clock can run at a frequency as high as 52 MHz with each data bit running at a maximum rate of 52 Mb/s. SD cards can operate with a clock frequency of up to 50 MHz in the high-speed mode. These card specs also specify that edge rate of the clock signal must not be slower than 3 ns. With these

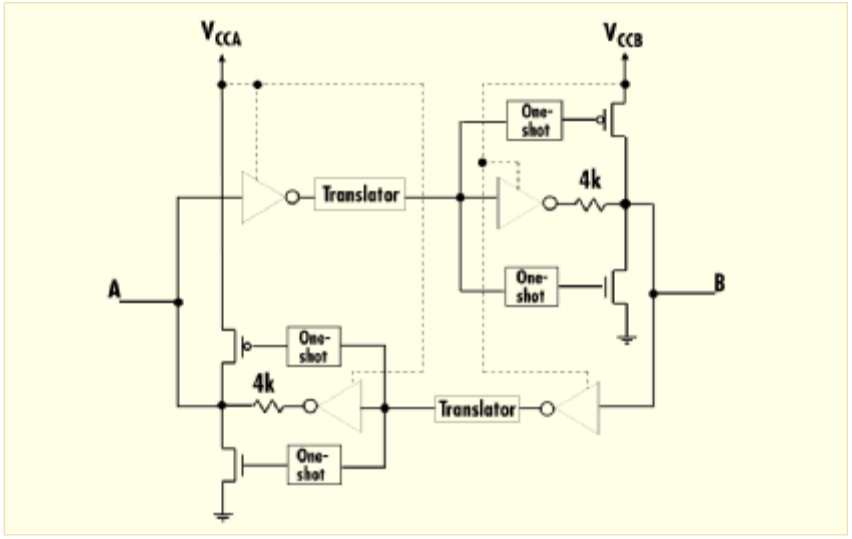

Figure 5. Auto direction-sensing voltage translator.

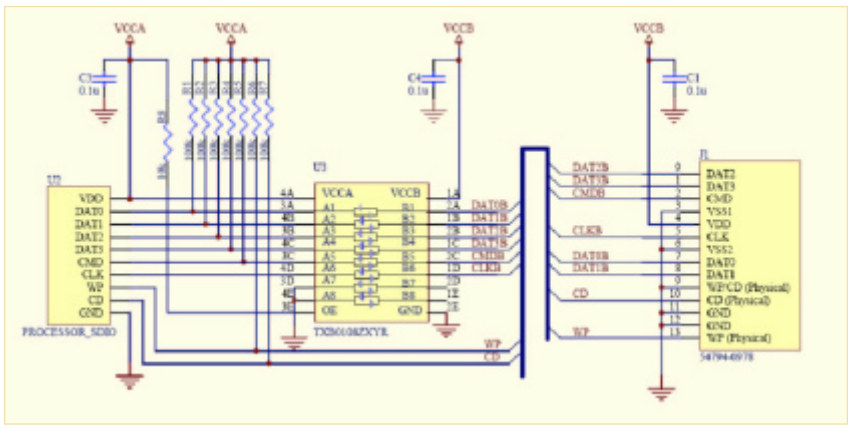

Figure 6. TXB0108 used to interface a low-voltage processor with a SD/SDIO card.

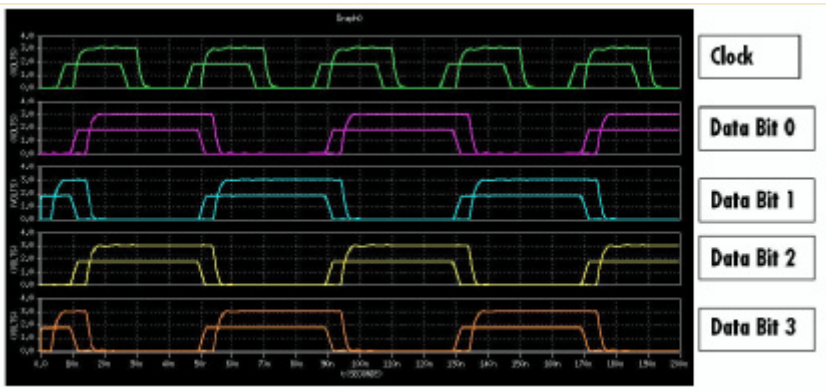

Figure 7. 25 MHz clock signal and 25 Mb/s data signals translated from 1.8 to 3 V.

requirements, it becomes necessary to consider fully buffered solutions, since other solutions have restrictions on maximum allowable frequencies, and might violate the edge-rate requirements on the clock signal. Figure 4 shows a 52 MHz clock and 52 Mb/s data signals passing through a fully buffered voltage translator.

Option 1a. A Variant of the Design Without a Directional Control Signal

These are bi-directional translators that do not require a direction-control signal. Using this type of translator between the processor and card would free up GPIOs on the processor. There are two topologies of directionless translators. One is an auto direction-sensing topology shown in

Figure 5 and another is a FET-based topology shown in Figure 8.

Option 2. The Auto Direction-sensing Translator

This translator has a restriction on the maximum DC-current load that can be connected at its outputs. In a DC state, the output drivers can maintain a high or low state with a very light-resistive or high-impedance load. The output drivers are designed to be weak, so they can be overdriven by an external driver when data starts flowing in the opposite direction. Due to its weak DC drive (typically few tens of µA), these devices must be implemented carefully in applications where pull-up or pull-down resistors are present on the data I/O lines. Output one-shots are used to provide strong AC drive to maintain fast output edge rates. The maximum

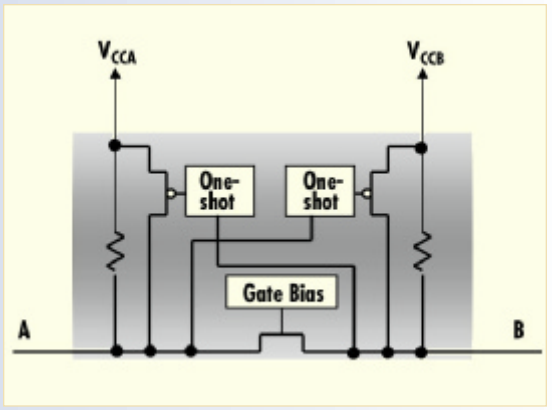

Figure 8. Internal structure of a FET-switch-based translation solution.

output frequency of these translators is restricted by the amount of time that the one-shots are designed to remain turned on. For instance, a one-shot designed to remain on for 10 ns will allow a maximum frequency equal to:

$$\frac{1}{(2)(10)ns} = 50\text{MHz}$$

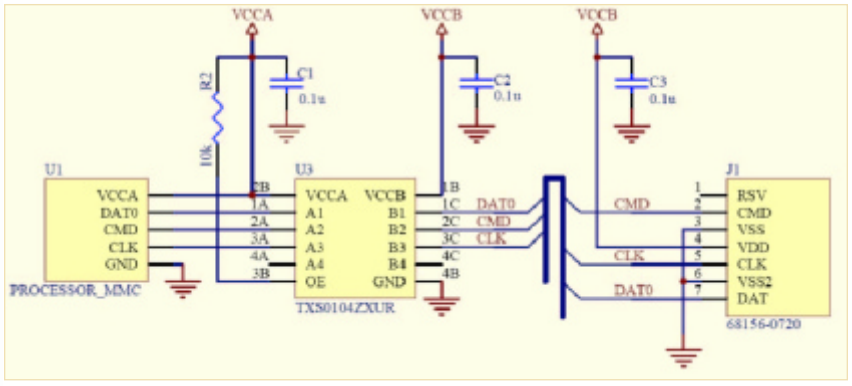

Figure 9. TXS0104 used to interface a processor with a MMC card.

Considerations When Using an Auto Direction-sensing Translator

- To prevent floating bus lines, card standards recommend adding pull-up resistors on the data and command lines. When using an auto direction-sensing translator, the value of these pull-up resistors must be kept high enough to ensure that they do not contend with the weak outputs of the translator. For card-interface applications using auto direction-sensing translators, the highest allowable pull-up resistor value of 100 kΩ must be used.
- For MMC cards, the CMD signal is initialized in an open-drain mode and later shifts into a push-pull mode. The auto direction-sensing translator is intended for use with a push-pull driver only and must not be used with open-drain drivers. The reason for this is that the auto direction-sensing devices have an input-

current requirement. When driven with an open-drain driver, the weak pull-up resistor on the bus is unable to fulfill this input-current requirement. Hence, these auto direction-sensing translators must not be used to interface with MMC cards. Fully buffered translators (Option 1) or FET-switch-based solutions (discussed later) are more appropriate options for use with MMC cards.

Figure 6 shows the schematic for using an auto direction-sensing translator to interface with a SD/SDIO card. Figure 7 shows the clock and data signals being translated from 1.8 to 3 V using an auto direction-sensing voltage translator.

Another Direction — FET-switch-based Solution

The other directionless translator uses the topology shown in Figure 8. It uses a pass transistor FET structure with internal pull-up resistors (typically 10 kΩ) on both sides. One-shots are incorporated to speed up the low-to-high signal transition. Due to their internal structure, these devices can be used with push-pull, as well as with open-drain drivers. Hence, this is a good solution to interface with a MMC card, or with a slot that is designed to accept both MMC and SD cards.

To interface with a single-data-bit MMC card, a 4-bit translator is sufficient, as shown in Figure 9. Figure 10 shows a 2.5 MHz clock signal and a 2.5 Mb/s data signal being translated from 1.8 to 3 V using a FET-switch-based translator.

Summary of Solutions

The system designer has a variety of options when choosing a level translator for the SD/SDIO or MMC interface. The SD card is available in smaller form factors such as miniSD and microSD or Trans Flash. Similarly, "reduced size MMC," or RS-MMC, is a smaller form factor of the MMC card. MMCPlus and MMCMobile are MMC cards capable of operating at higher data rates (up to 52 Mb/s). MMCPlus uses the standard MMC package, whereas MMCMobile uses the RS package.

In interfacing these cards with the processor, fully buffered translators offer high-data-rate capability and do not place restrictions on the values of pull-up or pull-down resistors connected to the data and command I/Os. However, these devices do need a direction-control signal to control the data and command flow from the processor to the card and vice-versa. Auto direction-sensing translators eliminate the need for these direction-control signals. Pull-up or pull-down resistors on the bus must be chosen carefully in order for this solution to work correctly. In addition, these translators cannot be used with open-drain drivers; hence, they are not an option when used to interface with MMC cards, since the MMC command line is initialized in an open-drain mode. FET-switch-based translators can be used to interface with MMC as well as with SD/SDIO cards. However, FET-switch-based translators currently available in the market support very low data rates, placing a restriction on the maximum operating frequency of these memory cards. The system designer must consider these trade-offs when choosing a level translator for the SD or MMC interface.

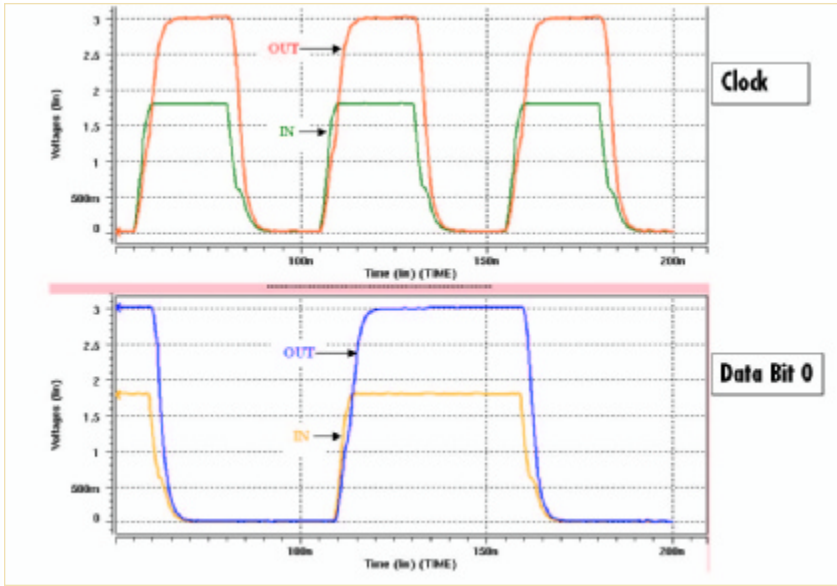

Figure 10. MMC Interface: 20 MHz clock signal and 20 Mb/s data signal translated from 1.8 to 3 V.

Cards Interfaced	Card Spec	Max Clock Speed	Most Optimal Solution for Level Translation
SD/SDIO, miniSD, microSD, TransFlash	SD 1.1	25 MHz	Fully Buffered, Auto Direction-sensing, FET-switch-based
MMC + SD/SDIO	MMC 3.xx, SD 1.1	25 MHz	Fully Buffered, FET-switch-based
MMC, RS-MMC	MMC 3.xx	20 MHz	Fully Buffered, FET-switch-based
MMCPlus, MMC Mobile	MMC 4.1	52 MHz	Fully Buffered, FET-switch-based

Figure 11. Matrix of devices and solutions.

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About the Author

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