PREPARED BY: DATE	SHARP	SPEC No. LCS4122
		FILE No.
APPROVED BY: DATE	LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION	ISSUE JAN. 31. 1994
		PAGE 24 Pages
		REPRESENTATIVE DIVISION
	SPECIFICATION	■ DUTY Panel Development Center

DEVICE SPECIFICATION for
Passive Matrix LCD Unit
(640×480 dots)

Model No.

LM64P858

□CUSTOMER'S APPROVAL

DATE 2/22/94

BY

PRESENTED BY Y. Inoue

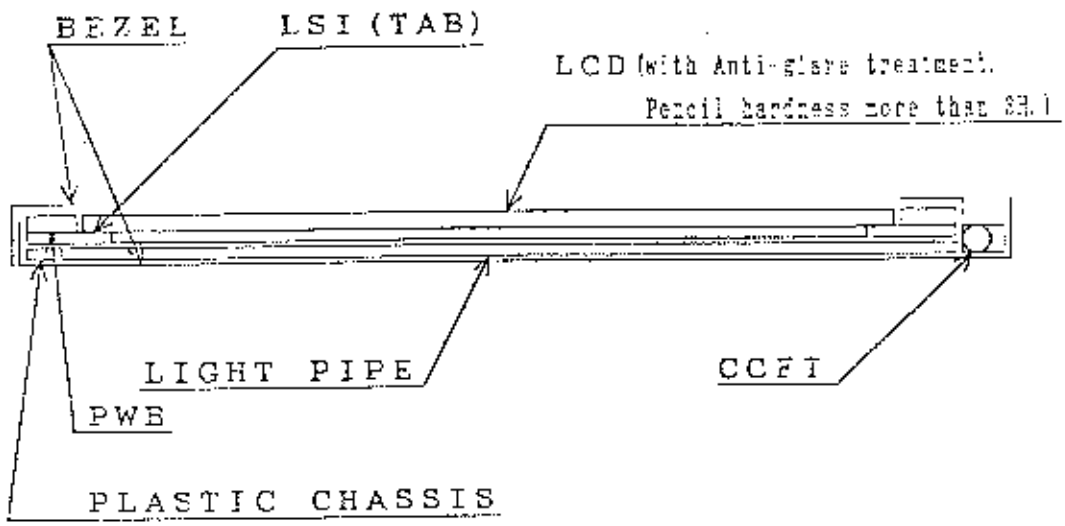
Y. Inoue
Department General Manager
Engineering Department 2
DUTY Panel Development center
SHARP CORPORATION

1. Application

This data sheet is to introduce the specification of 640×480, 0.3×0.3Pitch Passive Matrix type LCD unit.

2. Construction and Outline

Construction: 640×480 dots display unit consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto, TAB(tape automated bonding) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT backlight and bezels to fix them mechanically.



Outline : See Fig. 10

Connection : See Fig. 10 and Table 6

3. Mechanical Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions	235 (W) × 182.8 (H) × 10.5MAX (D) *1*2	mm
Effective viewing Area	196 (W) × 147.6 (H)	mm
Display format	640 (W) × 480 (H) full dot	—
Dot size	0.27×0.27	mm
Dot spacing	0.03	mm
Dot color	White*3*4	—
Background color	Black*3*4	—
Weight	Approx. 550	g

*1 Included the mounting tabs.

*2 Excluded the allowance of deformation.

*3 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*4 Negative-type display
Displayed data 'H' : Dots ON : White
Displayed data 'L' : Dots OFF: Black

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25 °C
Input voltage	V_{IN}	0	V_{DD}	V	Ta=25 °C

4-2 Environmental Conditions

Table 3

Item	Tstg MIN.	Tstg MAX.	Topr MIN.	Topr MAX.	Remark
Ambient temperature	-25 °C	+60 °C	0 °C	+40 °C	Note 4
Humidity	Note 1		Note 1		No condensation
Vibration	Note 2		Note 2		3 directions (X/Y/Z)
Shock	Note 3		Note 3		3 directions (±X±Y±Z)

Note 1) Ta≦40°C.....95% RE Max

Ta>40°C.....Absolute humidity shall be less than Ta=40 °C/95% RE.

Note 2) There test conditions are in accordance with 'IEC 68-2-6'.

Frequency	5 Hz～57 Hz	57 Hz～ 500 Hz
Vibration level	—	9.8 m/s²
Vibration width	0.075 mm	—
Interval	10 Hz～500 Hz～10 Hz/10 min	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Acceleration: 490 m/s²

Pulse width : 11 ms

3 times for each direction of ±X／±Y／±Z

Note 4) Care should be taken so that the LCD Unit may not be subjected to the temperature out of this specification.

5. Electrical Specifications

5-1 Electrical characteristics

Tabel 4 Ta=25 °C, V_{DD}=5 V±5 %

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}	Note 1) Note 2)		4.75	5.0	5.25	V
Contrast adjust voltage	V_{COM}-V_{SS}	Ta= 0 °C		0.50	-	-	V
		Ta=25 °C		-	2.05	-	V
		Ta=40 °C		-	-	2.80	V
Input signal voltage	V_{IN}	'H' level		2.0	-	V_{DD}	V
		'L' level		0	-	0.8	V
Input leakage current	I_{IL}	'H' level		-	-	250	μA
		'L' level		-250	-	-	μA
Supply current (Logic)	I_{DD}	Note 3)	V_{COM} =	-	125	180	mA
Power consumption	Pd		2.05 V	-	625	900	mW

Note 1) The viewing angle θ at which the optimum contrast is obtained can be set by adjusting V_{COM}-V_{SS}. Refer to Fig.4 for the definition of θ.

Note 2) Max. and Min. values are specified as the Max. and Min. voltage within the condition of operational temperature range (0~40 °C). Typ. values are specified as the typical voltage at 25 °C.

Note 3) Display high frequency pattern.

V_{DD} = 5 V, Frame frequency = 85 Hz, Display pattern = 1 bit checker

Display pattern

5-2 Input capacitance

Table 5

Signal	Input capacitance
S	40 pF
C21	40 pF
C23	40 pF
DC0~DC3	40 pF
DL0~DL3	40 pF
DISP	250 pF

6-3 Interface signals

Table 6

○LCD

Pin No	Symbol	Description	Level
1	Gnd	Ground potential	—
2	DL2	Display data signal (Lower half)	H(ON), L(OFF)
3	DL1		
4	DL2		
5	DL3		
6	Gnd	Ground potential	—
7	DU0	Display data signal (Upper half)	H(ON), L(OFF)
8	DU1		
9	DU2		
10	DU3		
11	Gnd	Ground potential	—
12~13	N/C	No connect	—
14~16	VCC	Power supply for logic and LCD (+5 V)	—
17~18	N/C	No connect	—
19	GND	Ground potential	—
20~23	N/C	No connect	—
24	GND	Ground potential	—
25	CP2	Data input clock signal	H→L
26	CP1	Input data latch signal	H →L
27	S	Scan start-up signal	"H"
28	DISP	Display control signal	Display on : "H"
29	Gnd	Ground potential	—
30	N/C	No connect	—
31	VCON	Contrast control	—

○CCFT

Pin No	Symbol	Description	Level
1	HV	High voltage line (from Inverter)	-
2	NC	-	-
3	LV	Ground line (from Inverter)	-

Note) Pin No. and its location are shown in Fig. 10.

○LCD

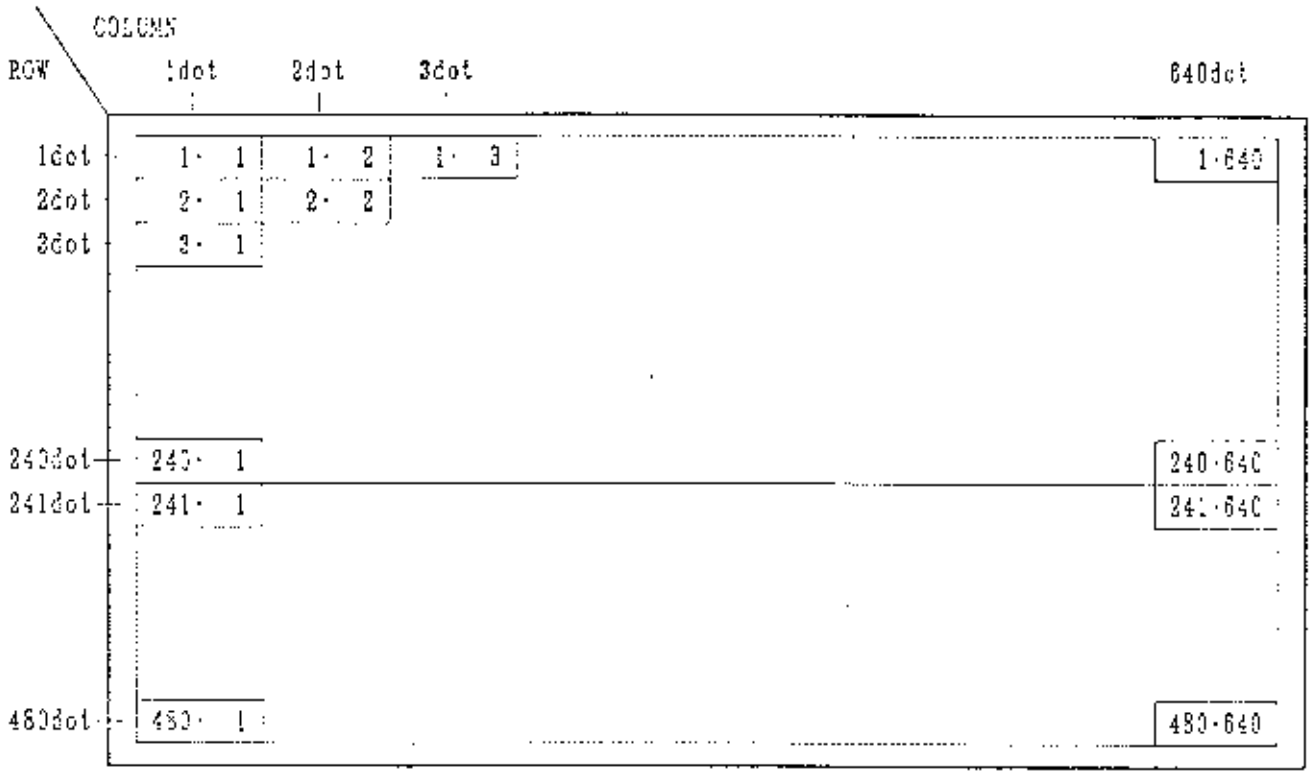
Used connector:DF9B-31P-1V(HIROSE)

Mating connector:DF9B-31S-1V(HIROSE)

○CCFT

Used connector:BHR-03VS-1 (JST)

Mating connector:SM03(4.0)B-BHS(JST)



Note) 1·2 means 1st row 2nd column dot.

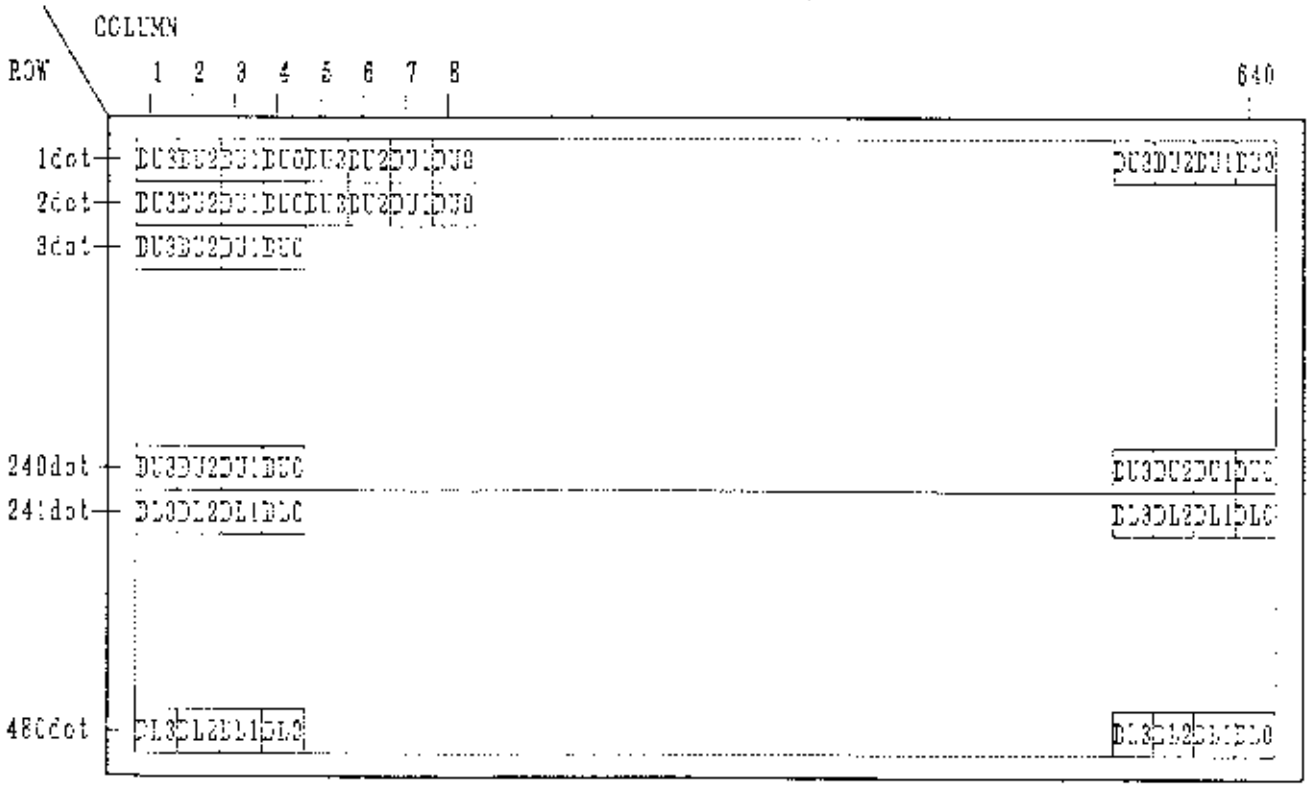


Fig. 1 Dot chart of display area

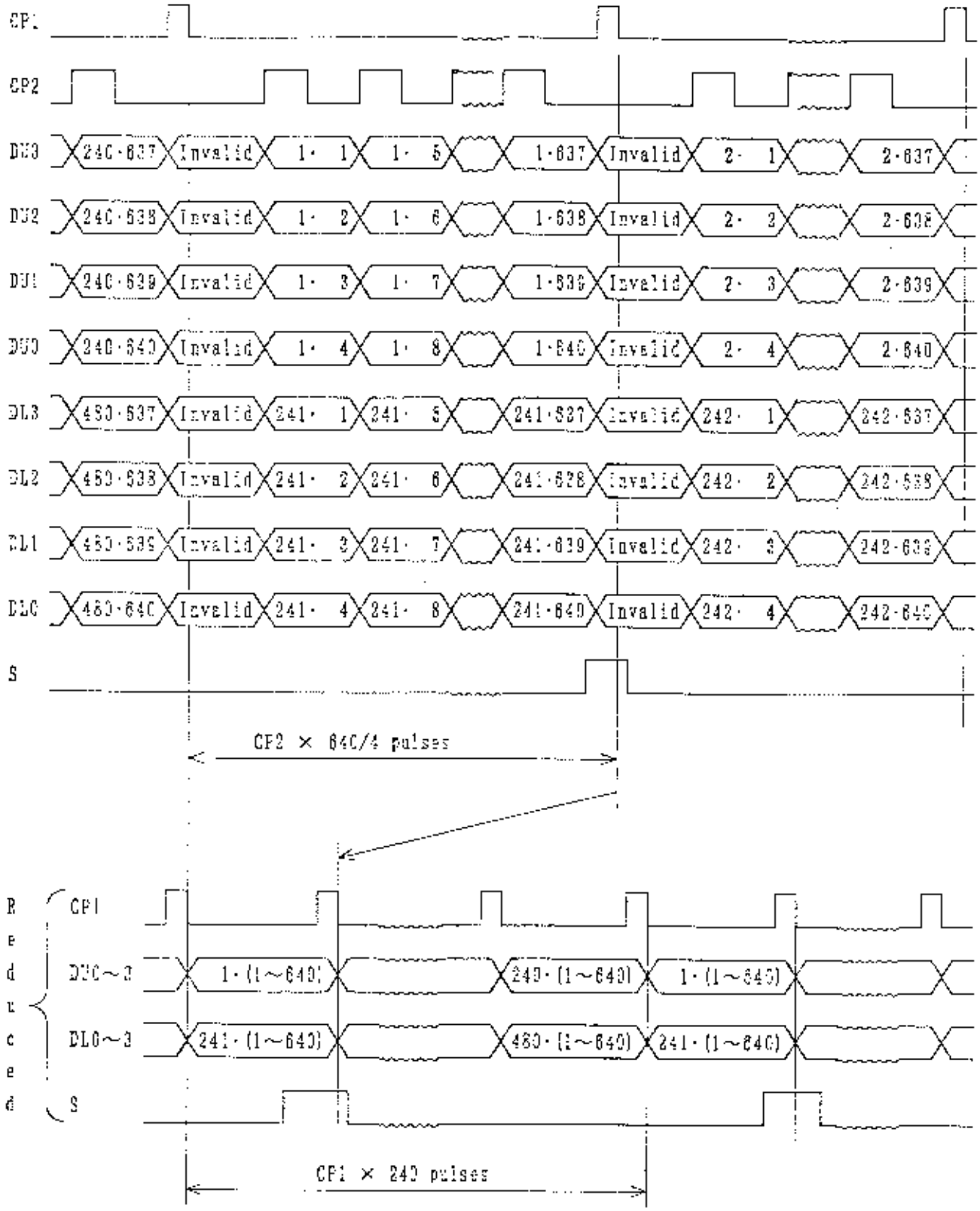


Fig.2 Data input timing

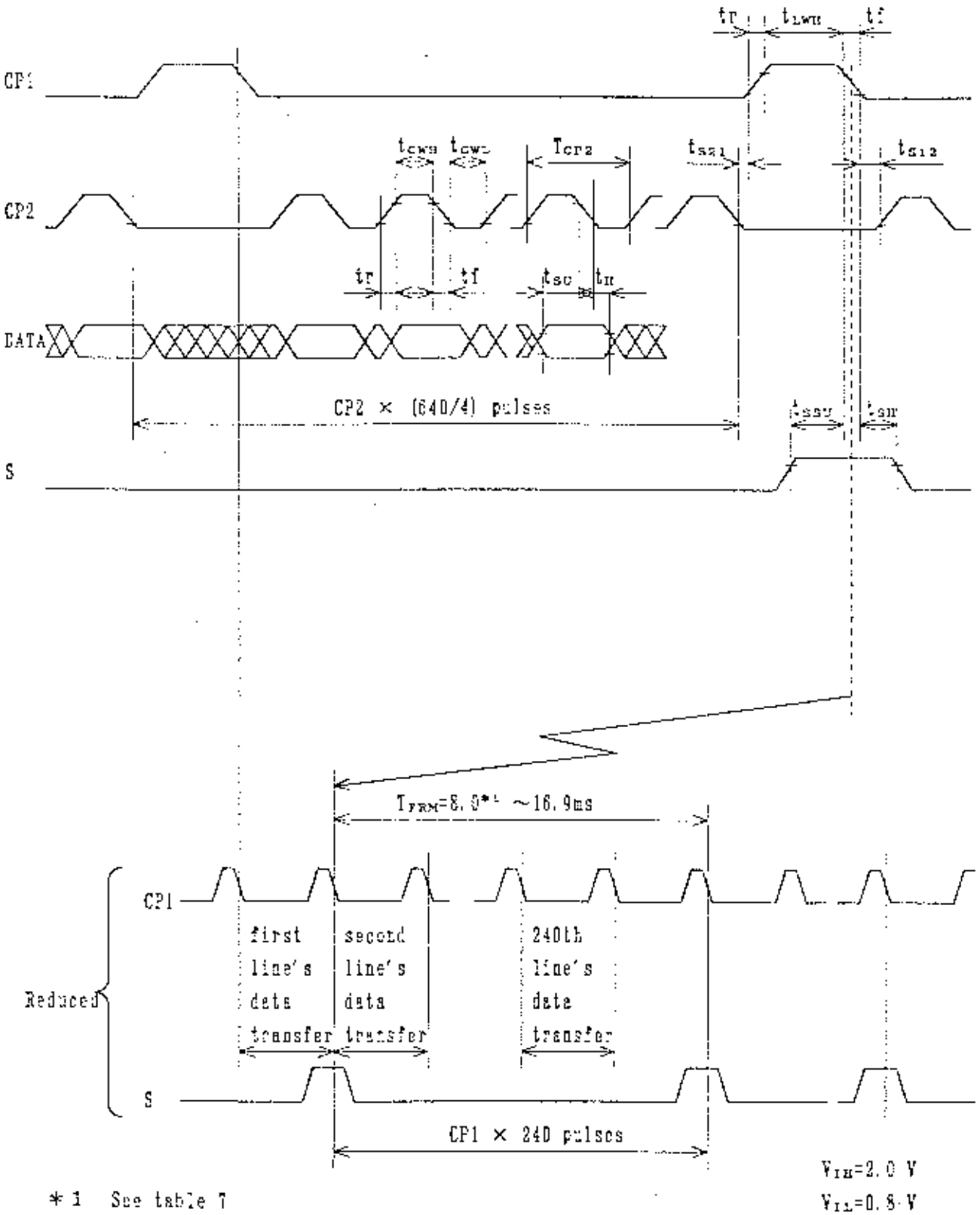


Fig.3 Interface timing chart

Table 7 Interface timing ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	T_{FRM}	8.0*1		16.9	ms
CP2 clock cycle	T_{CP2}	182			ns
'H' level clock width	t_{CWH}	86			ns
'L' level clock width	t_{CWL}	86			ns
'H' level latch clock width	t_{LWH}	70			ns
Data set up time	t_{SU}	50			ns
Data hold time	t_H	40			ns
S set up time	t_{SSU}	100			ns
S hold time	t_{SH}	100			ns
CP2↑ clock allowance time from CP1↓	t_{S21}	0			ns
CP1↑ clock allowance time from CP2↓	t_{S12}	0			ns
Clock rise/fall time	tr, tf			t_{rf}*2	ns

*1 : LCD unit functions at the minimum frame cycle of 8 ms (Maximum frame frequency of 125 Hz). Owing to the characteristics of LCD unit, 'shadowing' will become more eminent as frame frequency goes up, while flicker will be reduced.

According to our experiments, frame cycle of 11.7 ms Min. or frame frequency of 85 Hz Max. will demonstrate optimum display quality in terms of flicker and 'shadowing'. But since judgement of display quality is subjective and display quality such as 'shadowing' is pattern dependent, it is recommended that decision of frame cycle or frame frequency, to which power consumption of the LCD unit is proportional, be made based on your own through testing on the LCD unit with every possible patterns displayed on it.

*2 : t_{rf} = 50 in case $t_{cr}=[T_{CP2}-t_{CWH}-t_{CWL}]/2 \geq 50$

t_{rf} = t_{cr} in case $t_{cr}=[T_{CP2}-t_{CWH}-t_{CWL}]/2 < 50$

6. Unit Driving Method

6.1 Circuit configuration

Fig.9 shows the block diagram of the Unit's circuitry.

6.2 Display Face Configuration

The display face electrically consists of two (upper and lower) display segments so that the unit may offer higher contrast by reducing drive duty ratio. Each display segment (640×240 dots) is driven at 1/240 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits.

Display data which are externally divided into data for each row (640dots) will be sequentially transferred in the form of 4-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

When data of one row (640dots) have been input, they will be latched in the form of parallel data for 640 lines of signal electrodes by latch signal CP1. Then the corresponding drive signal will be transmitted to the 640 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of upper and lower half of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD

While the 1st rows of data are being displayed, the 2nd rows of data are entered When 640 dots of data have been transferred then latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

Such data input will be repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing method. The data input proceeds to the next display face.

Scan start-up signal S generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which will deteriorate LCD panel, drive waveform shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up as the operating frequency CP2 increases. Thus the driver LSI applies the system of tranferring 4-bits parallel data through the 4 lines of shift registers to reduce the data transfer speed CP2. Thanks to the LSI, the power consumption of the unit will be minimized.

In this circuit configuration, 4-bit display data shall be therefore input to data input pins of DU_{0-3}(upper display segment) and DL_{0-3}(lower display segment).

Furthermore the LCD unit adopts bus line system for data input to minimize the power consumption. In this system data input terminal of each driver LSI activated only when relevant data input is fed.

Data input for column electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This process is simultaneously followed at the column drivers LSI's of both the upper and the lower display segments. Thus data input for both the upper and the lower display segments must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no refresh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3 and Table 7.

7. Optical Caracteristics

Ta=25 °C,

V_{DD}-V_{EE}=Vmax

Table 8

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction ($\theta x=\theta y=0$) will be MAX.

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx		$\theta y=0$	-25	-	25	dgr.	
		θy	Co) 4.0	$\theta x=0$	-10	-	20	dgr.	Note 1
Contrast ratio		Co	$\theta x=\theta y=0$		10	18		-	Note 2
Response time	Rise	τr	$\theta x=\theta y=0$		-	200	300	ms	
	Decay	τd	$\theta x=\theta y=0$		-	150	250	ms	Note 3

Note 1) The viewing angle range is defined as shown Fig. 4.

Note 2) Contrast ratio is defined as follows:

$$Co=\frac{\text{Luminance (brightness) all pixels 'white' at Vmax}}{\text{Luminance (brightness) all pixels 'dark' at Vmax}}$$

Vmax is defined in Fig. 6.

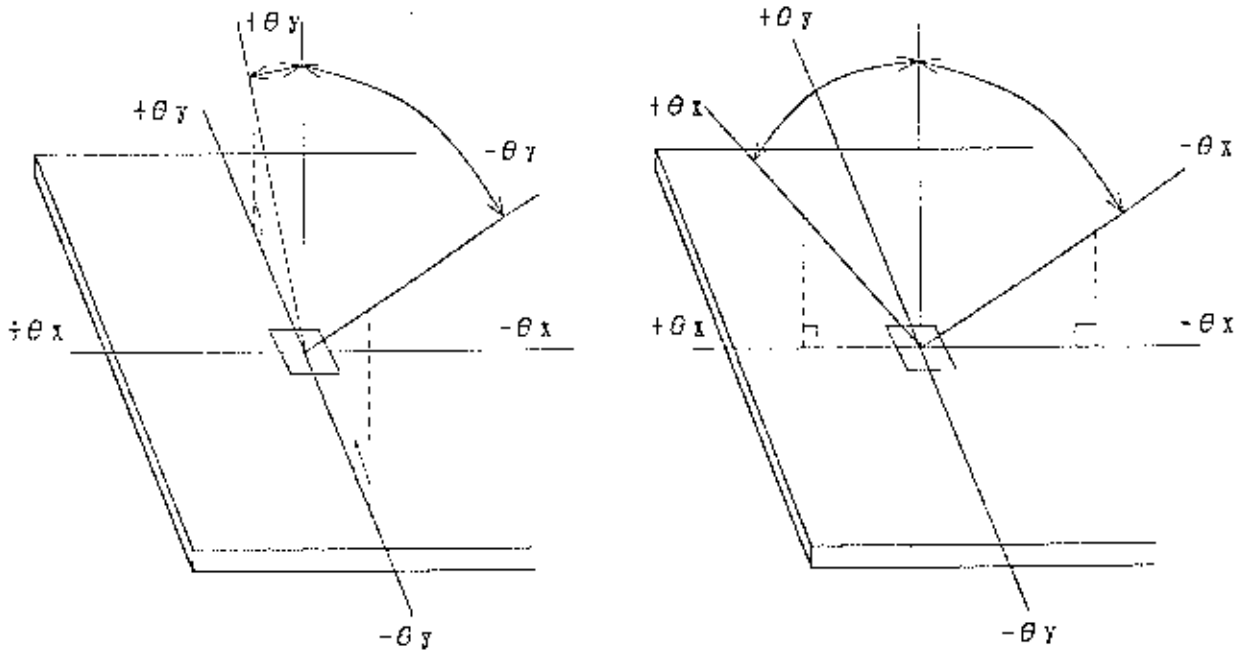
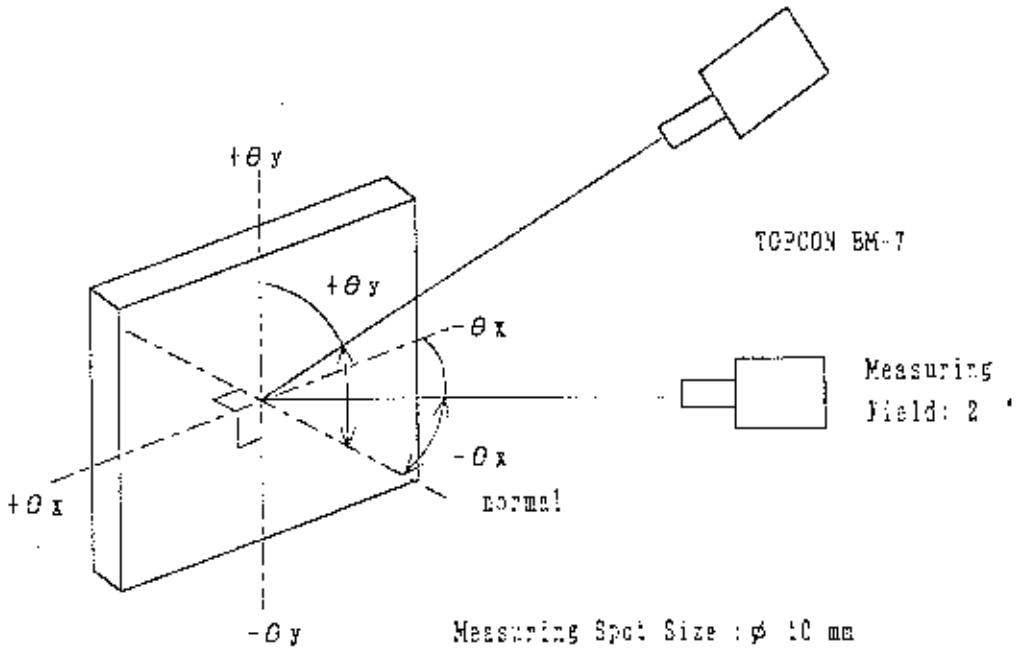


Fig. 4 Definition of Viewing Angle

Note 3) The response characteristics of photo-detector output are measured as shown in Fig. 7, assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig. 8.



Measuring Spot Size : φ 10 mm

θx : Angle from 'normal' to viewing surface rotated about the horizontal axis.

θy : Angle from 'normal' to viewing surface rotated about the vertical axis.

Fig.5 Optical Characteristics Test Method I

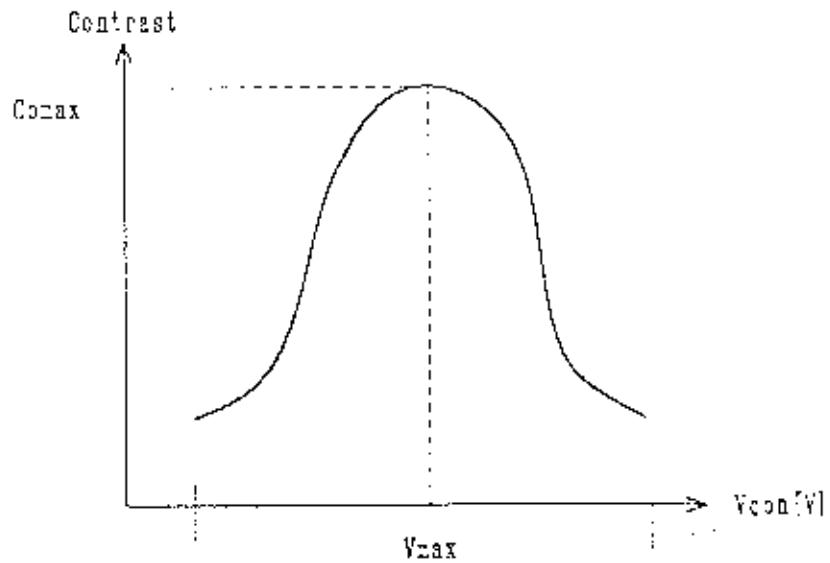
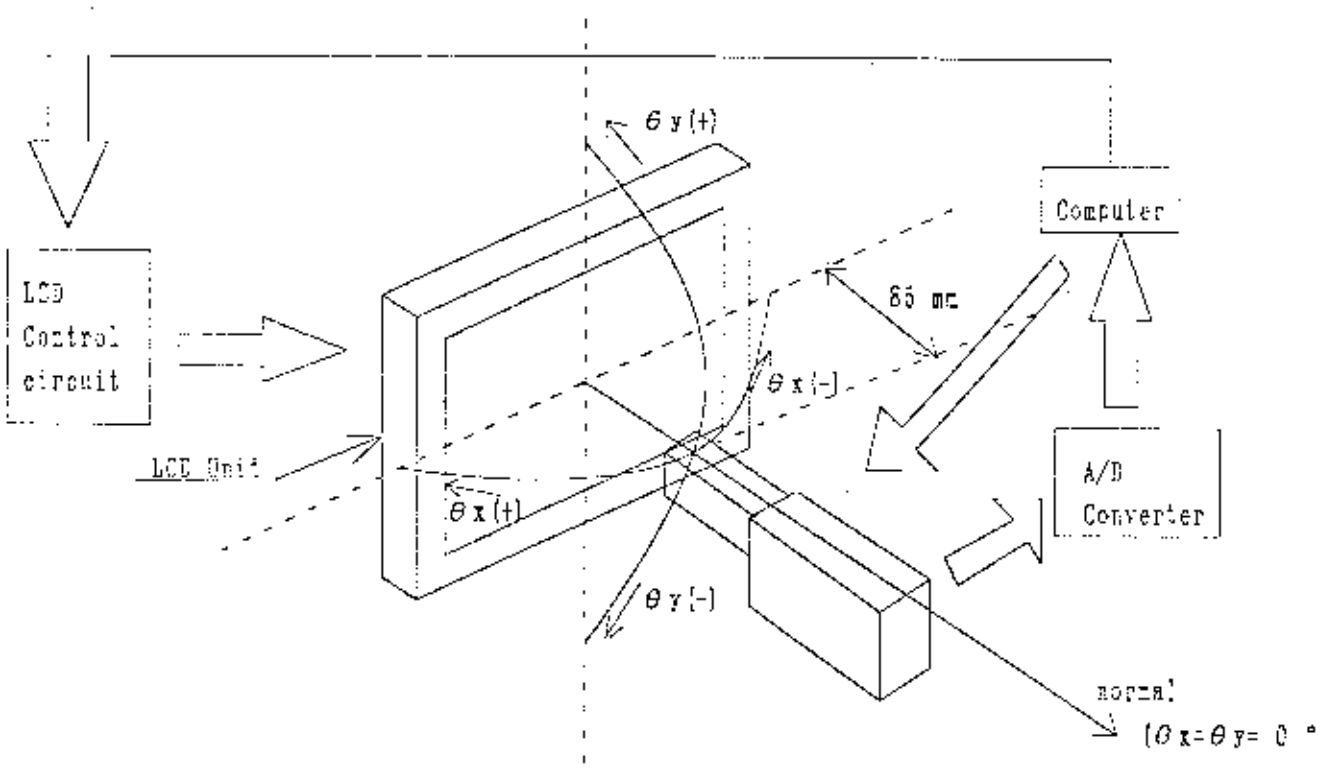


Fig.6 Definition of Vmax

(Response Measurement)
Ta=25 °C
In dark room



TOPCON BM7 + quartz fiber
(Measuring Spot Size: φ 13 mm,
Measuring Field: 2 °)

Fig.7 Optical Characteristics Test Method II

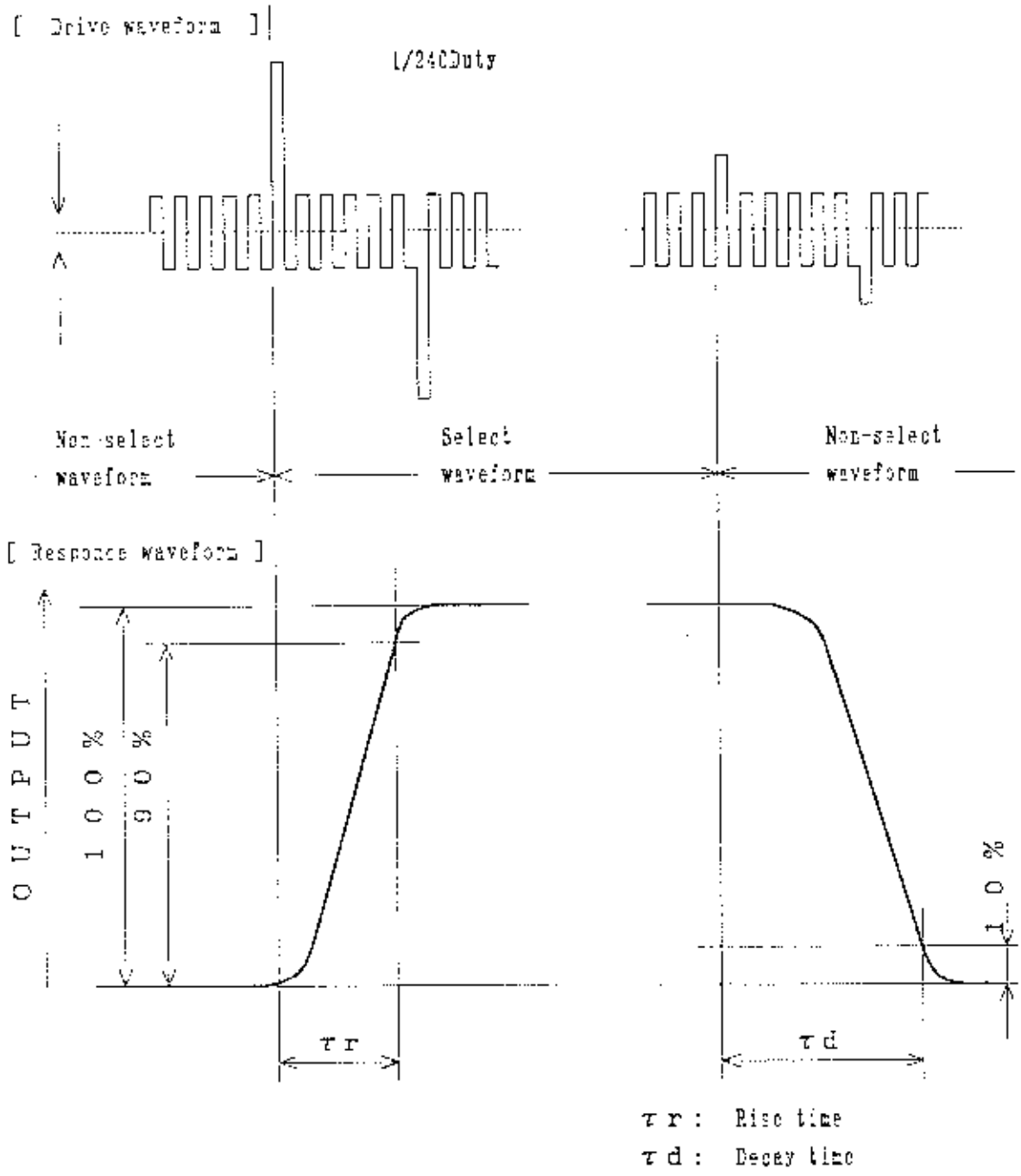


Fig.5 Difinition of Response Time

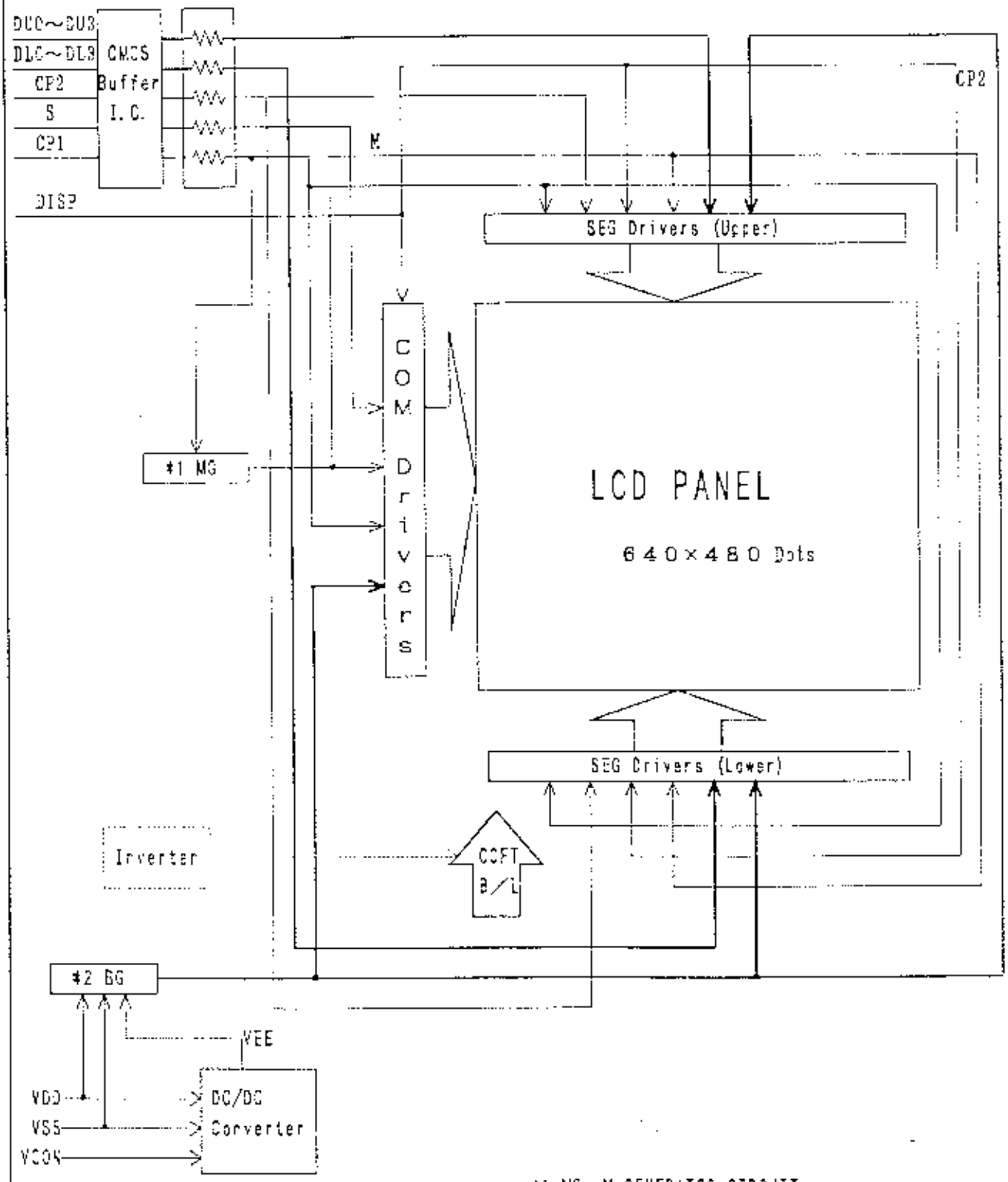


Fig. 6 Circuit block diagram

*1 MG: M GENERATOR CIRCUIT
*2 BG: BIAS GENERATOR & PROTECTION CIRCUIT

8. Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied.

1) Rating (Note)

Parameter	Min	Typ	Max	Unit
Brightness	100	130	—	cd/m²

2) Measurement circuit : CXA-M10L (TOSHIBA) (at IL=6 mArms)

3) Measurement equipment: BM-7 (TOPCON Corporation)

4) Measurement conditions

4-1 Measurement circuit voltage: DC=10.8 V, at primary side.

4-2 LCD: All digits WHITE, VDD=5 V, Vcom-Vss=Vmax, D00～D03, DL0～DL3='H' (refer Fig.8)

4-3 Ambient temperature: 25 °C

Measurement shall be executed 30 minutes after turning on.

5) Used lamp: K C218C30252FH (West electric co.LTD.)

or FLE 30216 (EMI) B-NS198 (ELEVAM co.LTD.) 1pc.

5-1 Ratings

Parameter		Max. allowable value
Circuit voltage (VS)	1 300 Vrms MIN. (*3)	
Discharging tube current (IL)	6 mArms TYP	6.5 mArms (*1)
Power consumption	2.6 W (*2)	—
Discharging tube voltage (VL)	430±43 Vrms	—
Brightness (B)	30 000 cd/m² TYP	—

Within no conductor closed.

(*1) It is recommended that IL be not more than 6 mArms so that heat radiation of CCFT backlight may least effect the display quality.

(*2) Power consumption excluded inverter loss.

(*3) The circuit voltage (VS) of the inverter should be designed to have some margin (reference value: 1 450 Vrms MIN.), because VS may be increased due to the leak current in case of the LCD unit.

5-2 Operating life

The operating life time is 10 000 hours or more at 6 mA.

(5 000 hours or more at 3.5 mA.)

(Operating life with CXA-M10L or equivalent.)

The inverter should meet the following conditions to keep the specified life time of used lamp:

-Sine, symmetric waveform without spike in positive and negative.

-Output frequency range: 25～45kHz

Make sure the operating condisions by executing the burn-in enough time.

The operating life is defined as having ended when any of the following the following conditions occur; 25±1 °C
-When the voltage required for initial discharge has reached 1 430 Vrms or when it has reached 12.0 V-DC when used an inverter.
-When the illuminence or quantity of light has decreased to 60 % of the initial value.

(NOTE) Rating are defined as the average brightness inside the viewing area specified in Fig. 11.

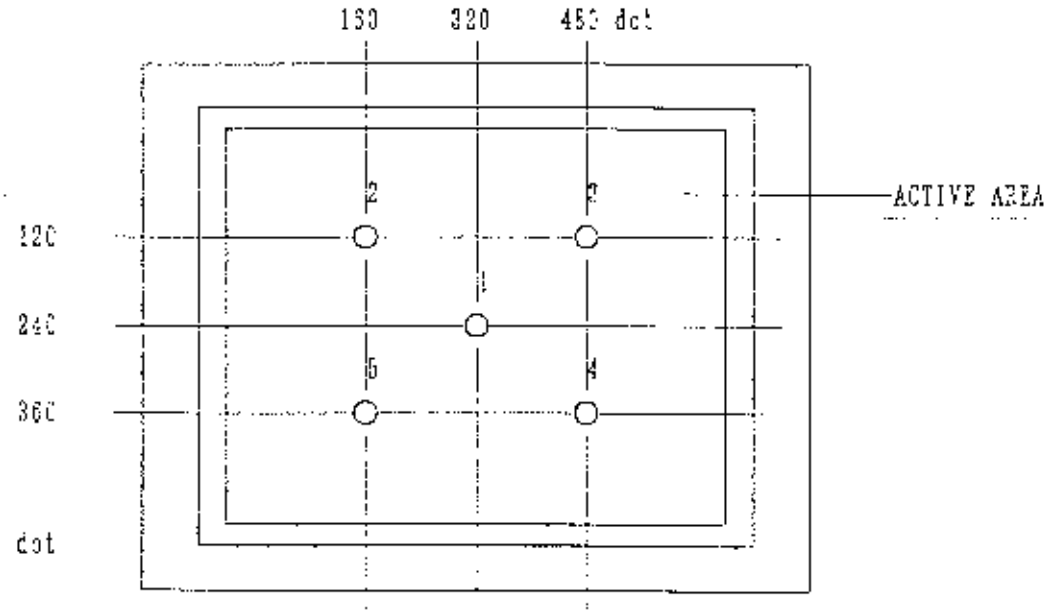


Fig. 11 Measuring points (1~5)

9. Precautions

1) Industrial (Mechanical) design of the product in which this LCD unit will be incorporated must be so made that the viewing angle characteristics of the LCD may be optimized.
This unit's viewing angle is illustrated in Fig.12.
θymin < viewing angle < θymax [θymin<0 ° θymax≧0 °]
(For the specific values of θymin, θymax, refer to the table 8.)
Please consider the optimum viewing conditions according to the purpose when installing the unit.

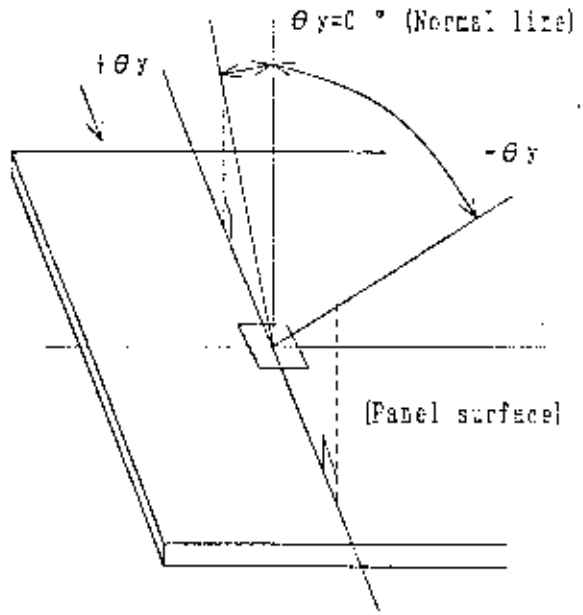


Fig.12 Dot matrix LCD viewing angle

2) This unit is installed using mounting tabs at the four corners of PCB or bezel.
When installing the unit, pay attention and handle carefully not to allow any undue stress such as twist or bend.
A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.

3) Since the front polarizer is easily damaged, please pay attention not to scratch on its face.

4) If the surface of the LCD cells needs to be cleaned, wipe it swiftly with cotton or other soft cloth. If still not completely clear, blow on it and wipe.

5) Water droplets, etc. must be wiped off immediately since they may cause color changes, staining, etc. if remained for a long time.

6) Since LCD is made of glass plates, dropping the unit or banging it against hard objects may cause cracking or fragmentation.

7) CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by earthing human body, etc. Take the following measures, to protect the unit from the electric discharge via mounting tabs from the main system the electrified with static electricity.

(1) Earth the metallic case of the main system (contact of the unit and main system).

(2) Insulate the unit and main system by attaching insulating washers made of bakelite or nylon, etc.

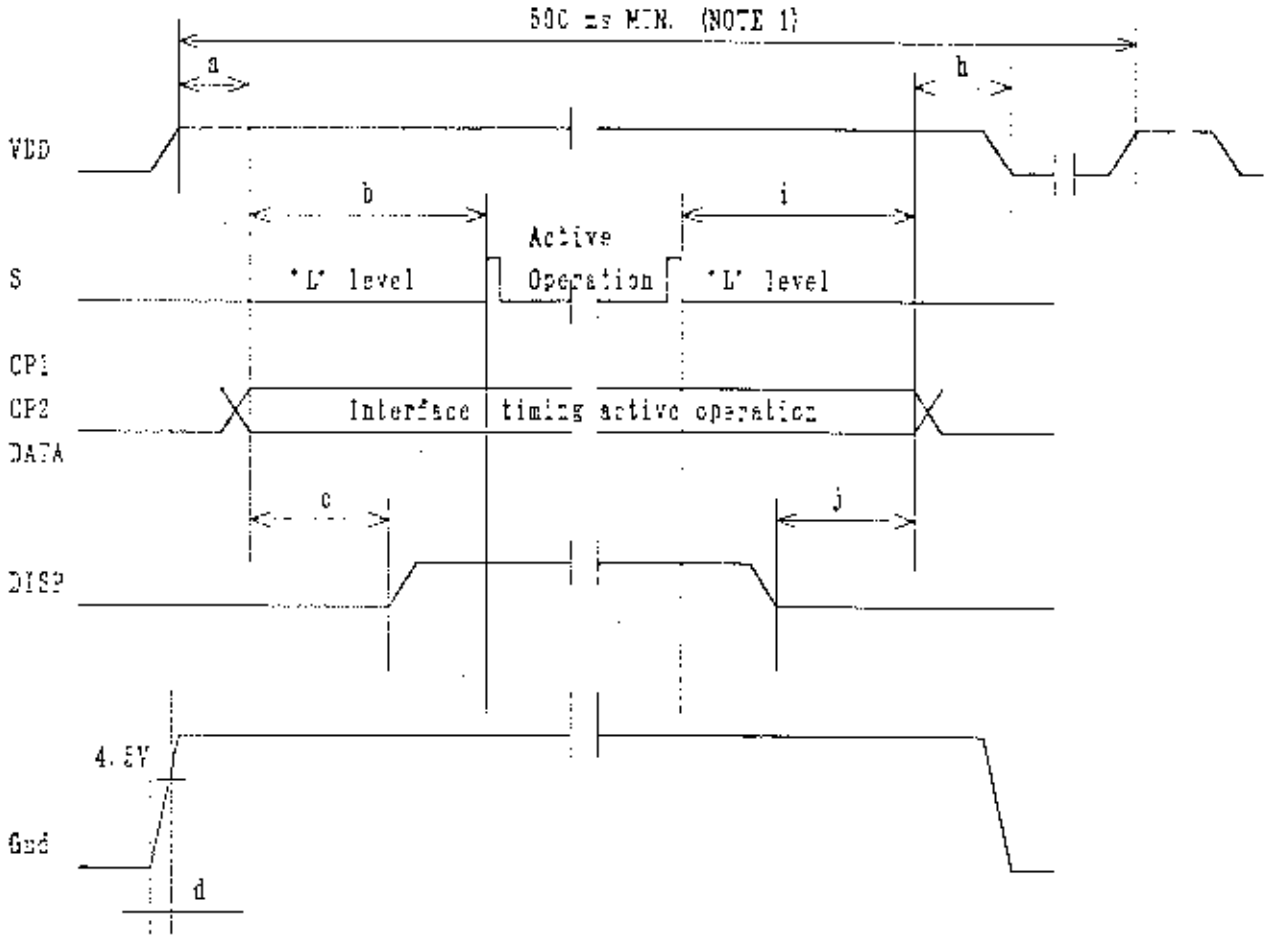
8) The unit should be driven according to the specified ratings to avoid malfunction of permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continous application of the signal M. Especially the power ON/OFF sequence shown on next page shall be followed to avoid latch-up of driver LSIs and application of DC voltage to LCD panel.

9) Avoid to expose the unit to the direct sun-light, strong ultra-violet light, etc. for a long time.

10) If stored at temperatures below specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orientation of the LC may change to that of a liquid, and they may not return to their original state.

11) Disassembling the LCD unit can cause permanent damage and should be strictly avoided.

Supply voltage sequence condition



POWER ON	
SYMBOL	Allowanble value
a	0 ms MIN.
b	0 ms MIN.
c	LP×260 ms MIN.
d	10 ms MAX

POWER OFF	
SYMBOL	Allowanble value
h	0 ms MIN.
i	0 ms MIN.
j	LP×260 ms MIN.

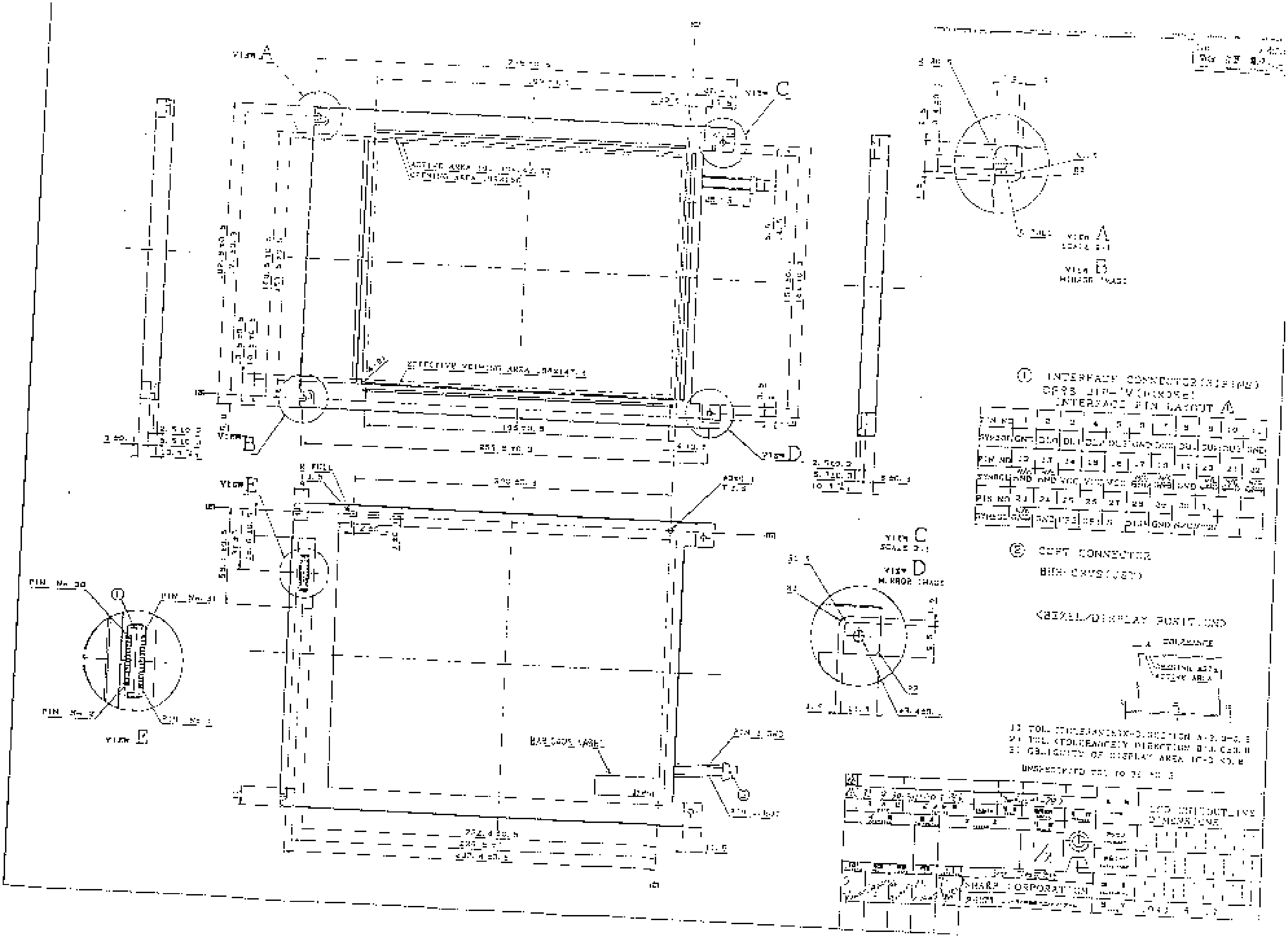
(Note 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

10. Applicable inspection standard
    The LCD unit shall meet the following inspection standard
    : S-U-A04

11. This specification describes display quality in case of no gray scale.
    Since display quality can be affected by gray scale methods, display quality shall be carefully evaluated for the usability of the LCD UNIT in case gray scale is displayed on the LCD UNIT.

WARNING

DON'T USE ANY MATERIALS WHICH EMIT FOLLOWING GAS FROM EPOXY RESIN (AMINES' HARDENER) AND SILICONE ADHESIVE AGENT (DEALCOHOL OR DEOXYM) TO PREVENT CHANGE POLARIZER COLOR OWING TO GAS.


VIEW A
VIEW B
VIEW C
VIEW D
VIEW E
VIEW F
EFFECTIVE VIEWING AREA
BAR CODE LABEL
INTERFACE PIN LAYOUT
COFT CONNECTOR
SHARP CORPORATION
LCD UNIT OUTLINE DIMENSIONS