HD66773

132 x 176 dot Graphics Controller Driver for TFT 260,000-color Displays

HITACHI

Rev.1.0-1
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<NOTICE: This document may, wholly or partially be subject to change without notice>

Description

The HD66773, controller driver LSI, displays 132RGB-by-176 dot graphics on TFT displays in 260,000 colors. The HD66773's bit-operation functions, 18-bit high-speed bus interface, and high-speed RAM-write functions enable efficient data transfer and high-speed rewriting of data to the graphic RAM.

HD66773 has a low-voltage operation 2.2V min, and it is equipped with internal operation circuits for TFT gate and source. Also HD66773 has the internal booster that generates the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. And HD66773 can compose a LCM only with an external capacitor and resistor. In addition, precise power control can be achieved by combining these hardware functions with software functions, such as an 8-color display and standby and sleep mode. This LSI is suitable for any medium-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bi-directional pagers, and small PDAs.

Features

- 132RGB x 176-dot graphics display LCD controller/driver for 260,000 TFT colors.
- 18-/16-/9-/8-bit high-speed bus interface and serial peripheral interface (SPI)
- High-speed burst-RAM write function
- Writing to a window-RAM address area by using a window-address function
- Internal bit-operation functions for graphics processing:
  - — Write-data mask function in bit units
  - — Logical operation in pixel unit and conditional write function
- Various color-display control functions:
  - — 260,000 colors can be displayed at the same time (gamma adjust included)
  - — Vertical scroll display function in raster-row units

- Low-power operation supports:
  - ― Vcc = 2.2 to 3.3 V (low-voltage range)
  - ― Vci = 2.5 to 3.3 V (internal reference voltage)
  - ― Power-save functions such as the standby mode and sleep mode
  - ― Partial LCD drive of two screens in any position
  - ― Internal power supply circuit
  - ― Internal equalize function
- Structure for TFT-display retention volume Cst/Cadd structure
- Internal power supply circuit
  - ― Step-up circuit: Five to nine times, positive-polarity inversion
  - ― Alternating functions for TFT-display counter-electrode power supply
  - ― N-line alternating drive of Vcom (Vgoff is also available for N-line alternating drive for Cadd)
  - ― Adjustment of Vcom (Vgoff) amplitude: internal 22-level digital potentiometer
- Output power-supply voltage
  - ― For the TFT-display counter electrode: Vcom amplitude = 6V (max), VcomH-GND =VREG1OUT (max), VcomL-GND= Vci + 1.0V to –Vci+0.5V (max)
- Internal RAM capacity: 46,464 bytes
- Internal operation circuit of liquid crystal display
  Source signal: 396
  Gate signal: 176
- n-raster-row inversion drive
  (It is possible to invert the polarity in every selected raster-row.)
- Internal oscillation and hardware reset
- Shift change of source/gate driver
- Available to COG with setting gate on both edge on one chip

HD66773 Block Diagram Description

TBD

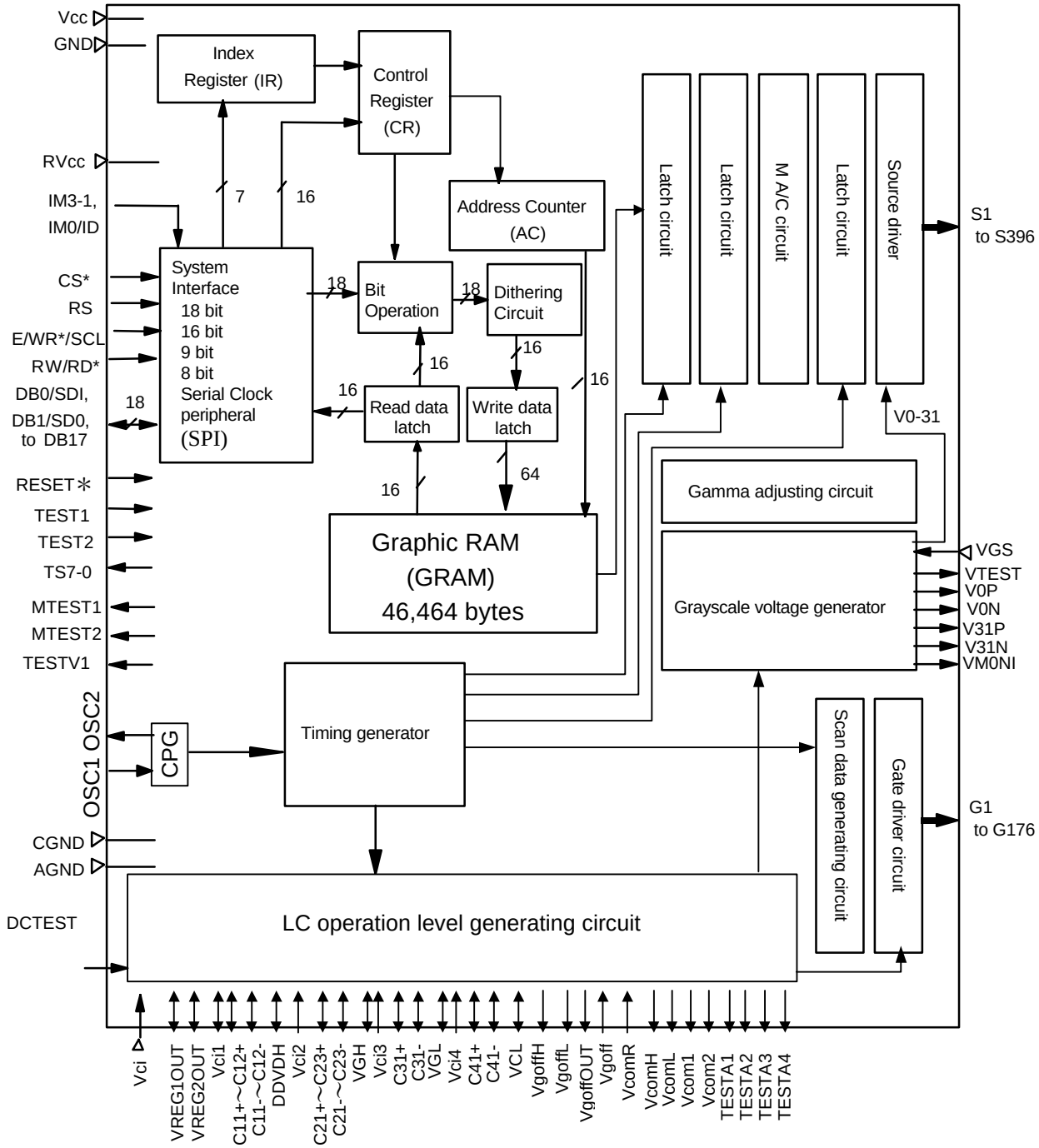


Figure 1: HD66773 Block Diagram Description

Figure 2 HD66773 Pad Arrangement

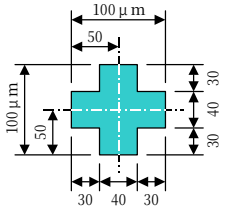
-Chip size: 20.69mm×2.47mm
-Chip thickness: 400 μm(typ.)
-Pad Coordinate: Pad Center
-Coordinate Origin: Chip center

-Au bump size:
(1) 80 μm×80 μm
Corner dummy:
No.1,No195,No.239,No.742

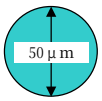
(2) 54 μm×100 μm
Input side
No.2 to No.194

(3) 36 μm×70 μm
Laced liquid crystal output side:
No.196 to No.238
No.240 to No.741
No.743 to No.786

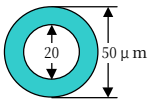
-Au bump pitch: Refer to Pad Coordinate
-Au bump height: 15 μm(typ.)
- Numbers in figure 2 refer to numbers in Pad coordinate
- Alignment Mark
(1) Assignment: 2places
Coordinate (X, Y) = (±10135,935)



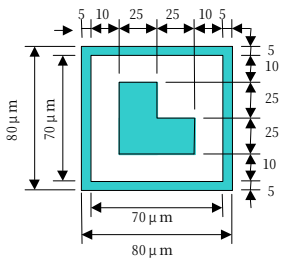
(2-a) Coordinate (X, Y) = (-10119, 1100)



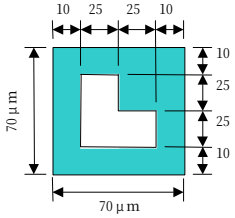
(2-b) Coordinate (X, Y) = (10119,1100)



(3-a) Coordinate (X, Y) = (-10029, 1100)



(3-b) Coordinate (X, Y) = (10029, 1100)



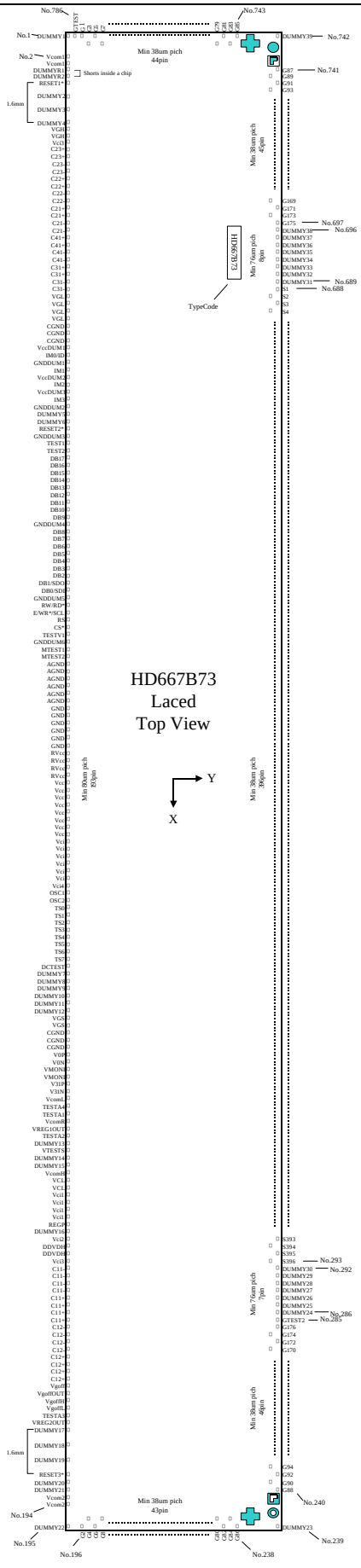


Table 1 HD667B73 PAD Coordinate (Laced)

No.	pad name	X	Y
1	DUMMY1	-10209	-1099
2	Vcom1	-10041	-1089
3	Vcom1	-9961	-1089
4	DUMMYR1	-9859	-1089
5	DUMMYR2	-9768	-1089
6	RESET1*	-9650	-1089
7	DUMMY2	-9116	-1089
8	DUMMY3	-8582	-1089
9	DUMMY4	-8048	-1089
10	VGH	-7947	-1089
11	VGH	-7867	-1089
12	Vci3	-7765	-1089
13	C23+	-7685	-1089
14	C23+	-7605	-1089
15	C23-	-7525	-1089
16	C23-	-7445	-1089
17	C22+	-7365	-1089
18	C22+	-7284	-1089
19	C22-	-7204	-1089
20	C22-	-7124	-1089
21	C21+	-7044	-1089
22	C21+	-6964	-1089
23	C21-	-6884	-1089
24	C21-	-6803	-1089
25	C41+	-6723	-1089
26	C41+	-6643	-1089
27	C41-	-6563	-1089
28	C41-	-6483	-1089
29	C31+	-6403	-1089
30	C31+	-6323	-1089
31	C31-	-6242	-1089
32	C31-	-6162	-1089
33	VGL	-6029	-1089
34	VGL	-5949	-1089
35	VGL	-5869	-1089
36	VGL	-5789	-1089
37	CGND	-5687	-1089
38	CGND	-5607	-1089
39	CGND	-5527	-1089
40	VccDUM1	-5447	-1089
41	IM0/ID	-5356	-1089
42	GNDDUM1	-5237	-1089
43	IM1	-5146	-1089
44	VccDUM2	-5028	-1089
45	IM2	-4936	-1089
46	VccDUM3	-4818	-1089
47	IM3	-4727	-1089
48	GNDDUM2	-4608	-1089
49	DUMMY5	-4528	-1089
50	DUMMY6	-4448	-1089
51	RESET2*	-4357	-1089
52	GNDDUM3	-4238	-1089
53	TEST1	-4147	-1089
54	TEST2	-4067	-1089
55	DB17	-3987	-1089
56	DB16	-3907	-1089
57	DB15	-3826	-1089
58	DB14	-3746	-1089
59	DB13	-3666	-1089
60	DB12	-3586	-1089
61	DB11	-3506	-1089
62	DB10	-3426	-1089
63	DB9	-3346	-1089
64	GNDDUM4	-3227	-1089
65	DB8	-3136	-1089
66	DB7	-3056	-1089
67	DB6	-2976	-1089
68	DB5	-2895	-1089
69	DB4	-2815	-1089
70	DB3	-2735	-1089
71	DB2	-2655	-1089
72	DB1/SDO	-2575	-1089
73	DB0/SDI	-2495	-1089
74	GNDDUM5	-2376	-1089
75	RW/RD*	-2285	-1089
76	E/WR*/SCL	-2205	-1089
77	RS	-2125	-1089
78	CS*	-2045	-1089
79	TESTV1	-1964	-1089
80	GNDDUM6	-1846	-1089
81	MTEST1	-1755	-1089
82	MTEST2	-1675	-1089
83	AGND	-1525	-1089
84	AGND	-1445	-1089
85	AGND	-1343	-1089
86	AGND	-1263	-1089
87	AGND	-1161	-1089
88	AGND	-1081	-1089
89	GND	-948	-1089
90	GND	-868	-1089
91	GND	-767	-1089
92	GND	-687	-1089
93	GND	-585	-1089
94	GND	-505	-1089
95	RVcc	-372	-1089
96	RVcc	-292	-1089
97	RVcc	-212	-1089
98	RVcc	-131	-1089
99	Vcc	-51	-1089
100	Vcc	29	-1089
101	Vcc	109	-1089
102	Vcc	189	-1089
103	Vcc	269	-1089
104	Vcc	349	-1089
105	Vcc	430	-1089
106	Vcc	510	-1089
107	Vci	590	-1089
108	Vci	670	-1089
109	Vci	750	-1089
110	Vci	830	-1089
111	Vci	911	-1089
112	Vci	991	-1089
113	Vci4	1129	-1089
114	OSC1	1257	-1089
115	OSC2	1337	-1089
116	TS0	1418	-1089
117	TS1	1498	-1089
118	TS2	1578	-1089
119	TS3	1658	-1089
120	TS4	1738	-1089
121	TS5	1818	-1089
122	TS6	1898	-1089
123	TS7	1979	-1089
124	DCTEST	2059	-1089
125	DUMMY7	2177	-1089
126	DUMMY8	2257	-1089
127	DUMMY9	2337	-1089
128	DUMMY10	2418	-1089
129	DUMMY11	2498	-1089
130	DUMMY12	2578	-1089
131	VGS	2685	-1089
132	VGS	2765	-1089
133	CGND	2872	-1089
134	CGND	2952	-1089
135	CGND	3032	-1089
136	V0P	3139	-1089
137	V0N	3219	-1089
138	VMONI	3299	-1089
139	VMONI	3380	-1089
140	V31P	3460	-1089
141	V31N	3540	-1089
142	VcomL	3657	-1089
143	TESTA4	3737	-1089
144	TESTA1	3854	-1089
145	VcomR	3934	-1089
146	VREG1OUT	4014	-1089
147	TESTA2	4094	-1089
148	DUMMY13	4201	-1089
149	VTESTS	4308	-1089
150	DUMMY14	4415	-1089
151	DUMMY15	4495	-1089
152	VcomH	4602	-1089
153	VCL	4740	-1089
154	VCL	4820	-1089
155	Vci1	4959	-1089
156	Vci1	5039	-1089
157	Vci1	5119	-1089
158	Vci1	5199	-1089
159	REGP	5343	-1089
160	DUMMY16	5450	-1089
161	Vci2	5557	-1089
162	DDVDH	5695	-1089
163	DDVDH	5776	-1089
164	Vci3	5909	-1089
165	C11-	6047	-1089
166	C11-	6127	-1089
167	C11-	6207	-1089
168	C11-	6287	-1089
169	C11+	6368	-1089
170	C11+	6448	-1089
171	C11+	6528	-1089
172	C11+	6608	-1089
173	C12-	6688	-1089
174	C12-	6768	-1089
175	C12-	6848	-1089
176	C12-	6929	-1089
177	C12+	7009	-1089
178	C12+	7089	-1089
179	C12+	7169	-1089
180	C12+	7249	-1089
181	Vgoff	7388	-1089
182	VgoffOUT	7468	-1089
183	VgoffH	7601	-1089
184	VgoffL	7681	-1089
185	TESTA3	7814	-1089
186	VREG2OUT	7947	-1089
187	DUMMY17	8048	-1089
188	DUMMY18	8582	-1089
189	DUMMY19	9116	-1089
190	RESET3*	9650	-1089
191	DUMMY20	9768	-1089
192	DUMMY21	9859	-1089
193	Vcom2	9961	-1089
194	Vcom2	10041	-1089
195	DUMMY22	10209	-1099
196	G2	10214	-801
197	G4	10104	-763
198	G6	10214	-725
199	G8	10104	-687
200	G10	10214	-649
201	G12	10104	-610
202	G14	10214	-572
203	G16	10104	-534
204	G18	10214	-496
205	G20	10104	-458
206	G22	10214	-420
207	G24	10104	-382
208	G26	10214	-343
209	G28	10104	-305
210	G30	10214	-267
211	G32	10104	-229
212	G34	10214	-191
213	G36	10104	-153
214	G38	10214	-114
215	G40	10104	-76
216	G42	10214	-38
217	G44	10104	0
218	G46	10214	38
219	G48	10104	76
220	G50	10214	114
221	G52	10104	153
222	G54	10214	191
223	G56	10104	229
224	G58	10214	267
225	G60	10104	305
226	G62	10214	343
227	G64	10104	382
228	G66	10214	420
229	G68	10104	458
230	G70	10214	496
231	G72	10104	534
232	G74	10214	572
233	G76	10104	610
234	G78	10214	649
235	G80	10104	687
236	G82	10214	725
237	G84	10104	763
238	G86	10214	801
239	DUMMY23	10209	1099
240	G88	9919	1104
241	G90	9881	994
242	G92	9843	1104
243	G94	9805	994
244	G96	9766	1104
245	G98	9728	994
246	G100	9690	1104
247	G102	9652	994
248	G104	9614	1104
249	G106	9576	994
250	G108	9538	1104
251	G110	9499	994
252	G112	9461	1104
253	G114	9423	994
254	G116	9385	1104
255	G118	9347	994
256	G120	9309	1104
257	G122	9270	994
258	G124	9232	1104
259	G126	9194	994
260	G128	9156	1104
261	G130	9118	994
262	G132	9080	1104
263	G134	9042	994
264	G136	9003	1104
265	G138	8965	994
266	G140	8927	1104
267	G142	8889	994
268	G144	8851	1104
269	G146	8813	994
270	G148	8775	1104
271	G150	8736	994
272	G152	8698	1104
273	G154	8660	994
274	G156	8622	1104
275	G158	8584	994
276	G160	8546	1104
277	G162	8507	994
278	G164	8469	1104
279	G166	8431	994
280	G168	8393	1104
281	G170	8355	994
282	G172	8317	1104
283	G174	8279	994
284	G176	8240	1104
285	GTEST2	8164	1104
286	DUMMY24	8088	1104
287	DUMMY25	8012	1104
288	DUMMY26	7935	1104
289	DUMMY27	7859	1104
290	DUMMY28	7783	1104
291	DUMMY29	7706	1104
292	DUMMY30	7630	1104
293	S396	7554	994
294	S395	7516	1104
295	S394	7477	994
296	S393	7439	1104
297	S392	7401	994
298	S391	7363	1104
299	S390	7325	994
300	S389	7287	1104
301	S388	7249	994
302	S387	7210	1104
303	S386	7172	994
304	S385	7134	1104
305	S384	7096	994
306	S383	7058	1104
307	S382	7020	994
308	S381	6981	1104
309	S380	6943	994
310	S379	6905	1104
311	S378	6867	994
312	S377	6829	1104
313	S376	6791	994
314	S375	6753	1104
315	S374	6714	994
316	S373	6676	1104
317	S372	6638	994
318	S371	6600	1104
319	S370	6562	994
320	S369	6524	1104
321	S368	6486	994
322	S367	6447	1104
323	S366	6409	994
324	S365	6371	1104
325	S364	6333	994
326	S363	6295	1104
327	S362	6257	994
328	S361	6218	1104
329	S360	6180	994
330	S359	6142	1104
331	S358	6104	994
332	S357	6066	1104
333	S356	6028	994
334	S355	5990	1104
335	S354	5951	994
336	S353	5913	1104
337	S352	5875	994
338	S351	5837	1104
339	S350	5799	994
340	S349	5761	1104
341	S348	5723	994
342	S347	5684	1104
343	S346	5646	994
344	S345	5608	1104
345	S344	5570	994
346	S343	5532	1104
347	S342	5494	994
348	S341	5455	1104
349	S340	5417	994
350	S339	5379	1104
351	S338	5341	994
352	S337	5303	1104
353	S336	5265	994
354	S335	5227	1104
355	S334	5188	994
356	S333	5150	1104
357	S332	5112	994
358	S331	5074	1104
359	S330	5036	994
360	S329	4998	1104
361	S328	4960	994
362	S327	4921	1104
363	S326	4883	994
364	S325	4845	1104
365	S324	4807	994
366	S323	4769	1104
367	S322	4731	994
368	S321	4692	1104
369	S320	4654	994
370	S319	4616	1104
371	S318	4578	994
372	S317	4540	1104
373	S316	4502	994
374	S315	4464	1104
375	S314	4425	994
376	S313	4387	1104
377	S312	4349	994
378	S311	4311	1104
379	S310	4273	994
380	S309	4235	1104
381	S308	4197	994
382	S307	4158	1104
383	S306	4120	994
384	S305	4082	1104
385	S304	4044	994
386	S303	4006	1104
387	S302	3968	994
388	S301	3929	1104
389	S300	3891	994
390	S299	3853	1104
391	S298	3815	994
392	S297	3777	1104
393	S296	3739	994
394	S295	3701	1104
395	S294	3662	994
396	S293	3624	1104
397	S292	3586	994
398	S291	3548	1104
399	S290	3510	994
400	S289	3472	1104

Table 1 HD667B73 PAD Coordinate (Laced) cont.

No.	pad name	X	Y
401	S288	3434	994
402	S287	3395	1104
403	S286	3357	994
404	S285	3319	1104
405	S284	3281	994
406	S283	3243	1104
407	S282	3205	994
408	S281	3166	1104
409	S280	3128	994
410	S279	3090	1104
411	S278	3052	994
412	S277	3014	1104
413	S276	2976	994
414	S275	2938	1104
415	S274	2899	994
416	S273	2861	1104
417	S272	2823	994
418	S271	2785	1104
419	S270	2747	994
420	S269	2709	1104
421	S268	2671	994
422	S267	2632	1104
423	S266	2594	994
424	S265	2556	1104
425	S264	2518	994
426	S263	2480	1104
427	S262	2442	994
428	S261	2403	1104
429	S260	2365	994
430	S259	2327	1104
431	S258	2289	994
432	S257	2251	1104
433	S256	2213	994
434	S255	2175	1104
435	S254	2136	994
436	S253	2098	1104
437	S252	2060	994
438	S251	2022	1104
439	S250	1984	994
440	S249	1946	1104
441	S248	1908	994
442	S247	1869	1104
443	S246	1831	994
444	S245	1793	1104
445	S244	1755	994
446	S243	1717	1104
447	S242	1679	994
448	S241	1640	1104
449	S240	1602	994
450	S239	1564	1104
451	S238	1526	994
452	S237	1488	1104
453	S236	1450	994
454	S235	1412	1104
455	S234	1373	994
456	S233	1335	1104
457	S232	1297	994
458	S231	1259	1104
459	S230	1221	994
460	S229	1183	1104
461	S228	1145	994
462	S227	1106	1104
463	S226	1068	994
464	S225	1030	1104
465	S224	992	994
466	S223	954	1104
467	S222	916	994
468	S221	877	1104
469	S220	839	994
470	S219	801	1104
471	S218	763	994
472	S217	725	1104
473	S216	687	994
474	S215	649	1104
475	S214	610	994
476	S213	572	1104
477	S212	534	994
478	S211	496	1104
479	S210	458	994
480	S209	420	1104
481	S208	382	994
482	S207	343	1104
483	S206	305	994
484	S205	267	1104
485	S204	229	994
486	S203	191	1104
487	S202	153	994
488	S201	114	1104
489	S200	76	994
490	S199	38	1104
491	S198	-38	1104
492	S197	-76	994
493	S196	-114	1104
494	S195	-153	994
495	S194	-191	1104
496	S193	-229	994
497	S192	-267	1104
498	S191	-305	994
499	S190	-343	1104
500	S189	-382	994
501	S188	-420	1104
502	S187	-458	994
503	S186	-496	1104
504	S185	-534	994
505	S184	-572	1104
506	S183	-610	994
507	S182	-649	1104
508	S181	-687	994
509	S180	-725	1104
510	S179	-763	994
511	S178	-801	1104
512	S177	-839	994
513	S176	-877	1104
514	S175	-916	994
515	S174	-954	1104
516	S173	-992	994
517	S172	-1030	1104
518	S171	-1068	994
519	S170	-1106	1104
520	S169	-1145	994
521	S168	-1183	1104
522	S167	-1221	994
523	S166	-1259	1104
524	S165	-1297	994
525	S164	-1335	1104
526	S163	-1373	994
527	S162	-1412	1104
528	S161	-1450	994
529	S160	-1488	1104
530	S159	-1526	994
531	S158	-1564	1104
532	S157	-1602	994
533	S156	-1640	1104
534	S155	-1679	994
535	S154	-1717	1104
536	S153	-1755	994
537	S152	-1793	1104
538	S151	-1831	994
539	S150	-1869	1104
540	S149	-1908	994
541	S148	-1946	1104
542	S147	-1984	994
543	S146	-2022	1104
544	S145	-2060	994
545	S144	-2098	1104
546	S143	-2136	994
547	S142	-2175	1104
548	S141	-2213	994
549	S140	-2251	1104
550	S139	-2289	994
551	S138	-2327	1104
552	S137	-2365	994
553	S136	-2403	1104
554	S135	-2442	994
555	S134	-2480	1104
556	S133	-2518	994
557	S132	-2556	1104
558	S131	-2594	994
559	S130	-2632	1104
560	S129	-2671	994
561	S128	-2709	1104
562	S127	-2747	994
563	S126	-2785	1104
564	S125	-2823	994
565	S124	-2861	1104
566	S123	-2899	994
567	S122	-2938	1104
568	S121	-2976	994
569	S120	-3014	1104
570	S119	-3052	994
571	S118	-3090	1104
572	S117	-3128	994
573	S116	-3166	1104
574	S115	-3205	994
575	S114	-3243	1104
576	S113	-3281	994
577	S112	-3319	1104
578	S111	-3357	994
579	S110	-3395	1104
580	S109	-3434	994
581	S108	-3472	1104
582	S107	-3510	994
583	S106	-3548	1104
584	S105	-3586	994
585	S104	-3624	1104
586	S103	-3662	994
587	S102	-3701	1104
588	S101	-3739	994
589	S100	-3777	1104
590	S99	-3815	994
591	S98	-3853	1104
592	S97	-3891	994
593	S96	-3929	1104
594	S95	-3968	994
595	S94	-4006	1104
596	S93	-4044	994
597	S92	-4082	1104
598	S91	-4120	994
599	S90	-4158	1104
600	S89	-4197	994
601	S88	-4235	1104
602	S87	-4273	994
603	S86	-4311	1104
604	S85	-4349	994
605	S84	-4387	1104
606	S83	-4425	994
607	S82	-4464	1104
608	S81	-4502	994
609	S80	-4540	1104
610	S79	-4578	994
611	S78	-4616	1104
612	S77	-4654	994
613	S76	-4692	1104
614	S75	-4731	994
615	S74	-4769	1104
616	S73	-4807	994
617	S72	-4845	1104
618	S71	-4883	994
619	S70	-4921	1104
620	S69	-4960	994
621	S68	-4998	1104
622	S67	-5036	994
623	S66	-5074	1104
624	S65	-5112	994
625	S64	-5150	1104
626	S63	-5188	994
627	S62	-5227	1104
628	S61	-5265	994
629	S60	-5303	1104
630	S59	-5341	994
631	S58	-5379	1104
632	S57	-5417	994
633	S56	-5455	1104
634	S55	-5494	994
635	S54	-5532	1104
636	S53	-5570	994
637	S52	-5608	1104
638	S51	-5646	994
639	S50	-5684	1104
640	S49	-5723	994
641	S48	-5761	1104
642	S47	-5799	994
643	S46	-5837	1104
644	S45	-5875	994
645	S44	-5913	1104
646	S43	-5951	994
647	S42	-5990	1104
648	S41	-6028	994
649	S40	-6066	1104
650	S39	-6104	994
651	S38	-6142	1104
652	S37	-6180	994
653	S36	-6218	1104
654	S35	-6257	994
655	S34	-6295	1104
656	S33	-6333	994
657	S32	-6371	1104
658	S31	-6409	994
659	S30	-6447	1104
660	S29	-6486	994
661	S28	-6524	1104
662	S27	-6562	994
663	S26	-6600	1104
664	S25	-6638	994
665	S24	-6676	1104
666	S23	-6714	994
667	S22	-6753	1104
668	S21	-6791	994
669	S20	-6829	1104
670	S19	-6867	994
671	S18	-6905	1104
672	S17	-6943	994
673	S16	-6981	1104
674	S15	-7020	994
675	S14	-7058	1104
676	S13	-7096	994
677	S12	-7134	1104
678	S11	-7172	994
679	S10	-7210	1104
680	S9	-7249	994
681	S8	-7287	1104
682	S7	-7325	994
683	S6	-7363	1104
684	S5	-7401	994
685	S4	-7439	1104
686	S3	-7477	994
687	S2	-7516	1104
688	S1	-7554	994
689	DUMMY31	-7630	1104
690	DUMMY32	-7706	1104
691	DUMMY33	-7783	1104
692	DUMMY34	-7859	1104
693	DUMMY35	-7935	1104
694	DUMMY36	-8012	1104
695	DUMMY37	-8088	1104
696	DUMMY38	-8164	1104
697	G175	-8240	1104
698	G173	-8279	994
699	G171	-8317	1104
700	G169	-8355	994
701	G167	-8393	1104
702	G165	-8431	994
703	G163	-8469	1104
704	G161	-8507	994
705	G159	-8546	1104
706	G157	-8584	994
707	G155	-8622	1104
708	G153	-8660	994
709	G151	-8698	1104
710	G149	-8736	994
711	G147	-8775	1104
712	G145	-8813	994
713	G143	-8851	1104
714	G141	-8889	994
715	G139	-8927	1104
716	G137	-8965	994
717	G135	-9003	1104
718	G133	-9042	994
719	G131	-9080	1104
720	G129	-9118	994
721	G127	-9156	1104
722	G125	-9194	994
723	G123	-9232	1104
724	G121	-9270	994
725	G119	-9309	1104
726	G117	-9347	994
727	G115	-9385	1104
728	G113	-9423	994
729	G111	-9461	1104
730	G109	-9499	994
731	G107	-9538	1104
732	G105	-9576	994
733	G103	-9614	1104
734	G101	-9652	994
735	G99	-9690	1104
736	G97	-9728	994
737	G95	-9766	1104
738	G93	-9805	994
739	G91	-9843	1104
740	G89	-9881	994
741	G87	-9919	1104
742	DUMMY39	-10209	1099
743	G85	-10214	801
744	G83	-10104	763
745	G81	-10214	725
746	G79	-10104	687
747	G77	-10214	649
748	G75	-10104	610
749	G73	-10214	572
750	G71	-10104	534
751	G69	-10214	496
752	G67	-10104	458
753	G65	-10214	420
754	G63	-10104	382
755	G61	-10214	343
756	G59	-10104	305
757	G57	-10214	267
758	G55	-10104	229
759	G53	-10214	191
760	G51	-10104	153
761	G49	-10214	114
762	G47	-10104	76
763	G45	-10214	38
764	G43	-10104	0
765	G41	-10214	-38
766	G39	-10104	-76
767	G37	-10214	-114
768	G35	-10104	-153
769	G33	-10214	-191
770	G31	-10104	-229
771	G29	-10214	-267
772	G27	-10104	-305
773	G25	-10214	-343
774	G23	-10104	-382
775	G21	-10214	-420
776	G19	-10104	-458
777	G17	-10214	-496
778	G15	-10104	-534
779	G13	-10214	-572
780	G11	-10104	-610
781	G9	-10214	-649
782	G7	-10104	-687
783	G5	-10214	-725
784	G3	-10104	-763
785	G1	-10214	-801
786	GTEST1	-10214	-877

Alignment mark	X	Y
Cross	-10135	935
	10135	935
Circle (Positive)	-10119	1100
Circle (Negative)	10119	1100
L (Positive)	-10029	1100
L (Negative)	10029	1100

Pin Functions

Table 2 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM3-1, IM0/ID	4	I	GND or V_{CC}	Selects the MPU interface mode: IM3 IM2 IM1 IM0/ID MPU interface mode DB pins "GND" "GND" "GND" "GND" 68-system 16-bits bus interface DB17-10, 8-1 "GND" "GND" "GND" "Vcc" 68-system 8-bit bus interface DB17-10 "GND" "GND" "Vcc" "GND" 80-system 16-bit bus interface DB17-10, 8-1 "GND" "GND" "Vcc" "Vcc" 80-system 8-bit bus interface DB17-10 "GND" "Vcc" "GND" ID Serial peripheral interface (SPI) DB1-0 "GND" "Vcc" "Vcc" * Setting inhibited "Vcc" "GND" "GND" "GND" 68-system 18-bit bus interface DB17-0 "Vcc" "GND" "GND" "Vcc" 68-system 9-bit bus interface DB17-9 "Vcc" "GND" "Vcc" "GND" 80-system 18-bit bus interface DB17-0 "Vcc" "GND" "Vcc" "Vcc" 80-system 9-bit bus interface DB17-9 "Vcc" "Vcc" * * Setting inhibited When a serial interface is selected, the IM0 pin is used as the ID setting for a device code.
CS*	1	I	MPU	Selects the HD66773: Low: HD66773 is selected and can be accessed High: HD66773 is not selected and cannot be accessed Must be fixed at GND level when not in use.
RS	1	I	MPU	Selects the register. Low: Index/status High: Control When using SPI, fix it to Vcc or GND level.
E/WR*/SCL	1	I	MPU	For a 68-system bus interface, serves as an enable signal to activate data read/write operation. For an 80-system bus interface, serves as a write strobe signal, and writes data at the low level. For a synchronous clock interface, serves as the synchronous clock signal.
RW/RD*	1	I	MPU	For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read For an 80-system bus interface, serves as a read strobe signal, and reads data at the low level. When using SPI, fix it to Vcc or GND level.
DB0/SDI	1	I/O	MPU	Serves as a 18-bit bi-directional data bus. 8-bit bus interface: DB17-10 9-bit bus interface: DB17-9 16-bit bus interface: DB17-10, 8-1 18-bit bus interface: DB17-0 Fix unused pins to the Vcc or GND level as they are used for data transfer. For a clock-synchronous serial interface, serves as the serial data input pin (SDI). The input level is read on the rising edge of the SCL signal.

(Continue to the Next page)

Signals	Number of Pins	I/O	Connected to	Functions
DB1/SDO	1	I/O	MPU	Serves as a 18-bit bi-directional data bus. 8-bit bus interface: DB17-10 9-bit bus interface: DB17-9 16-bit bus interface: DB17-10. 8-1 18-bit bus interface: DB17-0 Fix unused pins to the Vcc or GND level as they used for data transfer. For a clock-synchronous serial interface, serves as a serial data output pin (SDO). Successive bit values are output on the falling edge of the SCL signal.
DB2-DB17	16	I/O	MPU	Serves as a 18-bit bi-directional data bus. 8-bit bus interface: DB17-10 9-bit bus interface: DB17-9 16-bit bus interface: DB17-10, 8-1 18-bit bus interface: DB17-0 Fix unused pins to the to the Vcc or GND level as they used for data transfer.
OSC1, OSC2	2	I/O	Oscillation-resistor	Connect an external resistor for R-C oscillation. When input the clock from outside, input to OSC1, and open OSC2.
RESET1* RESET2* RESET3*	3	I	MPU or Reset generating circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on. Input data from either one of RESET pins, and leave other unused pins open.
TEST1	1	I	GND	Test pin. Must be fixed to GND level.
TEST2	1	I	GND	Test pin. Must be fixed to GND level.
Vcc, GND	2	-	Power supply	Logic Vcc: +2.2V to +3.3V, Logic ground GND: 0V
RVcc	1	-	Power supply	Vcc power supply for an internal RAM. Supply same level as Vcc.
AGND	1	-	Power supply	Analogue for ground side, AGND: 0 V
CGND	1	O	Opposed GND of external parts	Outputs GND level. Can be used as opposed GND of external parts.
Vci	1	I	Vcc or power supply	Power supply for analogue circuit. Connect to an external power supply 2.5V to 3.3V.
Vci1	1	I/O	Capacitor for stabilization or power supply	Output internal reference voltage generated between Vci and GND. Reference voltage of step-up circuit1. When not using an internal reference voltage, connect an external power supply lower than 2.75V.
DDVDH	1	I/O	Capacitor for stabilization or open	Pressure up the voltage generated between Vci and GND two to three times through the step-up circuit 1, and outputs the pressured up voltage. Pressure up magnification can be set at an internal register. Connect a capacitor for stabilixation. When not using a step-up circuit 1, leave it open.
Vci2	1	I	DDVDH or power supply	Reference voltage for step-up circuit 2. Connect to DDVDH. When not using DDVDH, connect an external power supply lower than 5.5V.
VGH	1	I/O	Capacitor for stabilization or power supply	Pressure up the voltage generated between DDVDH and GND two to four times through the step-up circuit 2, and outputs the pressured up voltage. Connect a capcitor for stabilization. When not using the step-up circuit 2, connect an external power supply lower than 16.5V.
Vci3	1	I	VGH or power supply	Reference voltage for the step-up circuit 3. Conect to VGH. When not using VGH, connect an external power upply lower than 16.5V.

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Signals	Number of Pins	I/O	Connected to	Functions
VGL	1	I/O	Capacitor for stabilization or power supply	Outputs voltage generated between VGH and GND as same amount of negative voltage through the step-up circuit 3. Connect a capacitor for stabilization. When not usign the step-up circuit 3, connect an external power supply higher than –16.5V.
Vci4	1	I	Vcc, or Vci1, or power supply	Reference voltage for a step-up circuit 4. Supply Vci or external power supply 2.5 to 3.3 V
VCL	1	I/O	Capacitor for stabilization or power supply	Outputs voltage generated between Vci4 and GND as same amount of negative voltage through the step-up circuit 4. Connect a capacitor for stabilization and VCL pin. A power supply for generating VcomL. When using external power supply while VcomL is negative, connect an external power supply more than –3.3V. When VcomL is higher than GND, stop step-up circuit 4 and connect GND.
VREG1OUT	1	I/O	Capacitor for stabilization or power supply	This pin generates and outputs a reference voltage for VREG1 between DDVDH and GND from the reference voltage between Vci and GND that is internally generated. The step-up factor can be set in an internal register. Connect a capacitor for stabilization. As it is the reference voltage for generating Vcom, connect a nexternal power supply lower than DDVDH whnenot using the amplifier circuit 1.
VREG2OUT	1	I/O	Capacitor for stabilization or power supply	This pin generates and outputs a reference voltage for VREG2 between GND and VGL from the reference voltage between Vci and GND that is internally generated. The step-up factor can be set in an internal register. Connect a capacitor for stabilization. As it is the reference voltage for generating VgoffOUT, connect an external power supply more than VGL when not using the amplifier circuit 2.
C11+, C11- to C23+,C23-	10	—	Step-up capacitor	Connect the step-up capacitors according to the step-up factor. When the internal step-up circuit is not used, leave this pin open.
C31+, C31-	2	—	Step-up capacitor	Connect a step-up capacitor for generating the VGL level from the VGH and GND levels. When the internal step-up circuit is not used, leave these pins open.
C41+, C41-	2	—	Step-up capacitor	Connect a step-up capacitor for generating the –Vci4 level from the Vci4 and GND levels. When the internal step-up circuit is not used, leave these pins open.
Vcom1 Vcom2	3	O	TFT-display counter electrode	A power supply for the TFT-display counter electrode. When the reversing Vcom alternation is not driven, the amplitude between VcomH and VcomL is output. The alternating cycle can be set by the M pin. Connect this pin to the TFT-display counter electrode.
VcomR	1	I	Variable resistor or open	A reference voltage of VcomH. When VcomH is externally adjusted, halt the internal adjuster of VcomH by setting the register and insert a variable resistor between VREG1OUT and GND. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register.
VcomH	1	O	Capacitor for stabilization	This pin indicates a high level of Vcom generated in driving the Vcom alternation. Connect this pin to the capacitor for stabilization.

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Signals	Number of Pins	I/O	Connected to	Functions
VcomL	1	O	Capacitor for stabilization or Open	The Vcom voltage when the Vcom alternation is not driven. When the Vcom alternation is driven, this pin indicates a low level of Vcom. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VcomL output stops and a capacitor for stabilization is not needed.
VgoffOUT	1	O	Vgoff or Open	An output power supply for driving the gate line of the gate driver. Alternation can be driven by synchronizing Vcom with the setting of the internal register. Set the internal register according to the structure of the TFT-display retention volume. For the amplitude at the alternation driving. this pin outputs a voltage between VcomH and VcomL with the VgoffL reference voltage.
Vgoff	1	I	VgoffOUT or power supply	This pin is a negative voltage at the TFT-gate off level. Connect VgoffOUT. When not using VgoffOUT, connect an external power supply which voltage is higher than VGL.
VgoffH	1	O	Capacitor for stabilization or Open	When the Vgoff alternation is driven, this pin indicates a high level of VgoffOUT. Connect this pin to a capacitor for stabilization. When the CAD bit is low, the VgoffH output stops and a capacitor for stabilization is not needed.
VgoffL	1	O	Capacitor for stabilization	The Vgoff voltage when the Vgoff alternation is not driven. When the Vgoff alternation is driven, this pin indicates a low level of VgoffOUT. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization.
V0P V31P	2	I/O	Capacitor for stabilization	When an internal operation amplifier is ON, they output voltage from internal operation amplifier for positive polarity. Connect a capacitor for stabilization.
V0N V31N	2	I/O	Capacitor for stabilization	When an internal operation amplifier in ON, they output voltage form internal operation amplifier for negative polarity. Connect a capacitor for stabilization.
VGS	1	I	GND or external resistor	Reference voltage for grayscale voltage generating circuit. When adjusting level by each panel, connect an external variable resister.
S1–S396	396	O	LCD	Output signals for gate wiring. The SS bit can change the shift direction of the source signal. For example, if SS = 0, RAM address 0000 is output from S1. If SS = 1, it is output from S528. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G1-176	176	O	LCD	They are the gate wiring output signals. Gate wiring selecting level, VGH, and the gate wiring non-selecting level, Vgoff.
GTEST1-2	2	O	LCD or Open	They are the dummy gate wring output signals. When CAD = High, gate wiring selecting level: output VGH and the gate wiring non-selecting level, Vgoff. When CAD bit = low, gate wiring selecting level output Vgoff level. When not using these pins, leave them open.

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Signals	Number of Pins	I/O	Connected to	Functions
TESTA1	1	I/O	Test pin	A test pin for the VcomH output. Leave it open or connect a capacitor for stabilization according to the display quality.
TESTA2	1	I/O	Test pin	A test pin for the VcomL output. Leave it open or connect a capacitor for stabilization according to the display quality.
TESTA3	1	I/O	Test pin	A test pin for the VgoffH output. Leave it open or connect a capacitor for stabilization according to the display quality.
TESTA4	1	I/O	Test pin	A test pin for the VcomL output. Leave it open or connect a capacitor for stabilization according to the display quality.
DCTEST	1	I	GND	A test pin. Must be connected to GND.
MTEST1 MTEST2	2	O	Test pin	A test pin. Must be lift open.
VTESTS	1	I/O	Test pin	A test pin. Must be left open.
TS0-TS7	8	O	Test pin	A test pin. Must be left open.
VMONI	1	O	Test pin	A test pin. Must be left open.
TESTV1	1	I	Test pin	A test pin. Must be connected to GND.
REGP	1	I/O	Test pin	A test pin of VREG1OUT. Must be left open.

Block Function Description

System Interface

The HD66773 has three high-speed system interfaces: a 68-system, an 80-system 18-/16-/9-/8-bit bus, and a clock synchronous serial (SPI: Serial Peripheral Interface). The interface mode is selected by the setting of IM3-0 pins.
The HD66773 has three 16-bit registers: an index register (IR) 16-bit, a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal.
Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 3 Register Selection (8/9/16/18 Parallel Interface)

80-system		68-system	RS	Operation
WR*	RD*	R/W		
0	1	0	0	Writes indexes into IR
1	0	1	0	Reads internal status
0	1	0	1	Writes into control registers and GRAM through WDR
1	0	1	1	Reads from GRAM through RDR

Table 4 Register Selection (Clock Peripheral Serial Interface)

Start bytes		
R/W Bits	**RS Bits**	**Operations**
0	0	Writes indexes into IR
1	0	Reads internal status
0	1	Writes into control registers and GRAM through WDR
1	1	Reads from GRAM through RDR

Bit Operation

The HD66773 supports the following functions: a write data mask function that selects and writes data into the GRAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the compare register and writes into the GRAM. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assigns address to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.
After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

Hard dithering circuit

HD66773 is equipped with the circuit which transforms 18-bit into 16-bit for 1 pixel data.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has 16 bits/pixel and stores the bit-pattern data of 132 x 176 words.

Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma-adjusting resistor. 262,144 possible colors can be displayed when 1 byte = 18 bit. For details, see the gamma-adjusting resistor.

Power supply circuit for LCD operation

It generates the voltage of V0P, V0N, V31P, V31N, VGH, VGL, VgoffOUT, and Vcom level which are necessary for operating the LCD.

Oscillation Circuit (OSC)

The HD66773 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 396 source drivers (S1 to S396), and 176 gate driver (G1 to G176). Display pattern data is latched when 396-bit data has arrived. The latched data then enables the source drivers to generate drive waveform outputs. The shift direction of 396-bit data can be changed by the SS bit by selecting an appropriate direction for the device-mounting configuration.

Table 5: Relationship between GRAM address and display position (SS = “0”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB17 .... DB0			DB17 .... DB0			DB17 .... DB0			DB17 .... DB0				DB17 .... DB0			DB17 .... DB0			DB17 .... DB0			DB17 .... DB0		
G1	G176	"0000"H			"0001"H			"0002"H			"0003"H			.....	"0080"H			"0081"H			"0082"H			"0083"H		
G2	G175	"0100"H			"0101"H			"0102"H			"0103"H			.....	"0180"H			"0181"H			"0182"H			"0183"H		
G3	G174	"0200"H			"0201"H			"0202"H			"0203"H			.....	"0280"H			"0281"H			"0282"H			"0283"H		
G4	G173	"0300"H			"0301"H			"0302"H			"0303"H			.....	"0380"H			"0381"H			"0382"H			"0383"H		
G5	G172	"0400"H			"0401"H			"0402"H			"0403"H			.....	"0480"H			"0481"H			"0482"H			"0483"H		
G6	G171	"0500"H			"0501 H			"0502"H			"0503"H			.....	"0580"H			"0581 H			"0582"H			"0583"H		
G7	G170	"0600"H			"0601"H			"0602"H			"0603"H			.....	"0680"H			"0681"H			"0682"H			"0683"H		
G8	G169	"0700"H			"0701"H			"0702"H			"0703"H			.....	"0780"H			"0781"H			"0782"H			"0783"H		
G9	G168	"0800"H			"0801"H			"0802"H			"0803"H			.....	"0880"H			"0881"H			"0882"H			"0883"H		
G10	G167	"0900"H			"0901"H			"0902"H			"0903"H			.....	"0980"H			"0981"H			"0982"H			"0983"H		
G11	G166	"0A00"H			"0A01"H			"0A02"H			"0A03"H			.....	"0A80"H			"0A81"H			"0A82"H			"0A83"H		
G12	G165	"0B00"H			"0B01"H			"0B02"H			"0B03"H			.....	"0B80"H			"0B81"H			"0B82"H			"0B83"H		
G13	G164	"0C00"H			"0C01"H			"0C02"H			"0C03"H			.....	"0C80"H			"0C81"H			"0C82"H			"0C83"H		
G14	G163	"0D00"H			"0D01"H			"0D02"H			"0D03"H			.....	"0D80"H			"0D81"H			"0D82"H			"0D83"H		
G15	G162	"0E00"H			"0E01"H			"0E02"H			"0E03"H			.....	"0E80"H			"0E81"H			"0E82"H			"0E83"H		
G16	G161	"0F00"H			"0F01"H			"0F02"H			"0F03"H			.....	"0F80"H			"0F81"H			"0F82"H			"0F83"H		
G17	G160	"1000"H			"1001"H			"1002"H			"1003"H			.....	"1080"H			"1081"H			"1082"H			"1083"H		
G18	G159	"1100"H			"1101"H			"1102"H			"1103"H			.....	"1180"H			"1181"H			"1182"H			"1183"H		
G19	G158	"1200"H			"1201"H			"1202"H			"1203"H			.....	"1280"H			"1281"H			"1282"H			"1283"H		
G20	G157	"1300"H			"1301"H			"1302"H			"1303"H			.....	"1380"H			"1381"H			"1382"H			"1383"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G169	G8	"A800"H			"A801"H			"A802"H			"A803"H			.....	"A880"H			"A881"H			"A882"H			"A883"H		
G170	G7	"A900"H			"A901"H			"A902"H			"A903"H			.....	"A980"H			"A981"H			"A982"H			"A983"H		
G171	G6	"AA00"H			"AA01"H			"AA02"H			"AA03"H			.....	"AA80"H			"AA81"H			"AA82"H			"AA83"H		
G172	G5	"AB00"H			"AB01"H			"AB02"H			"AB03"H			.....	"AB80"H			"AB81"H			"AB82"H			"AB83"H		
G173	G4	"AC00"H			"AC01"H			"AC02"H			"AC03"H			.....	"AC80"H			"AC81"H			"AC82"H			"AC83"H		
G174	G3	"AD00"H			"AD01"H			"AD02"H			"AD03"H			.....	"AD80"H			"AD81"H			"AD82"H			"AD83"H		
G175	G2	"AE00"H			"AE01"H			"AE02"H			"AE03"H			.....	"AE80"H			"AE81"H			"AE82"H			"AE83"H		
G176	G1	"AF00"H			"AF01"H			"AF02"H			"AF03"H			.....	"AF80"H			"AF81"H			"AF82"H			"AF83"H		

18-bit interface & hard dithering mode

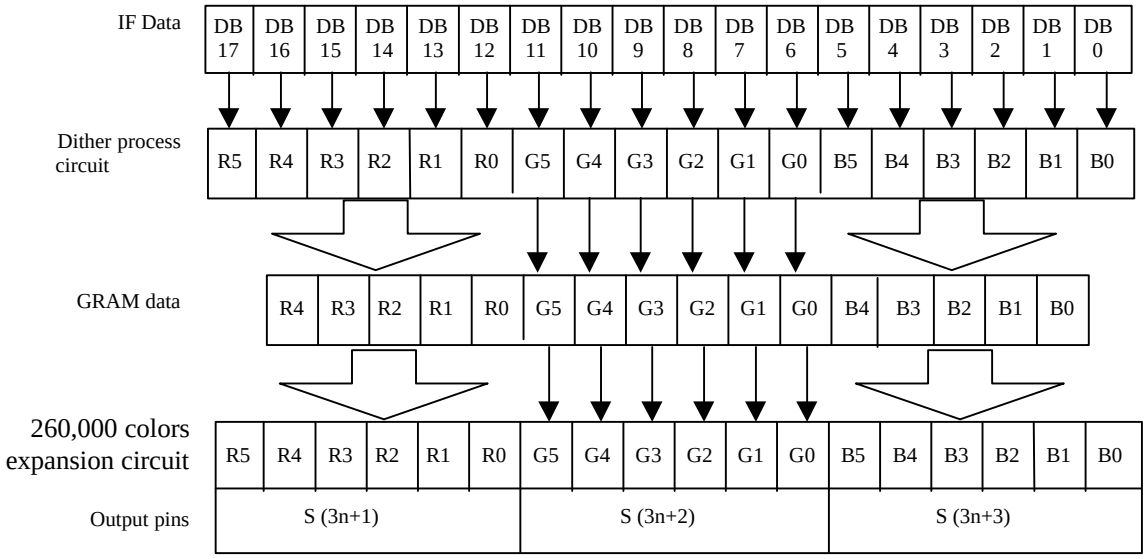
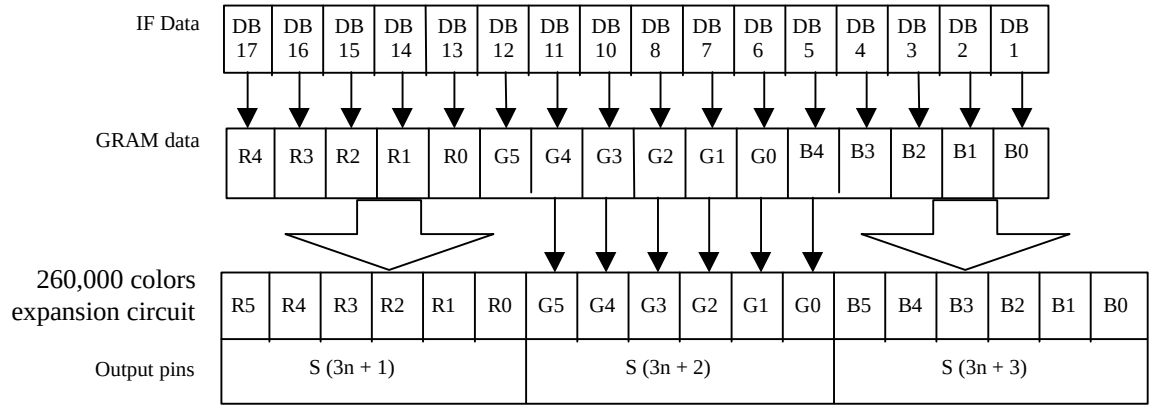


Figure 3 Note: n = lower eight bit of address (0 to 132)

16-bit interface



Note: n = lower eight bit of address (0 to 132)

Figure 4

9-bit interface & hard dither mode

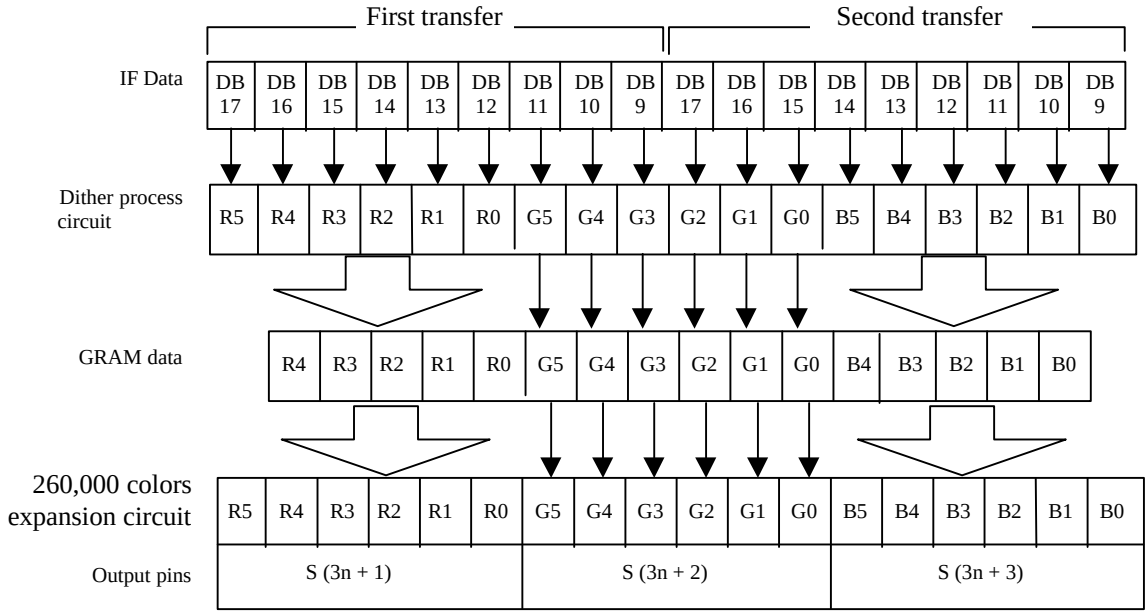


Figure 5 Note: n = lower eight bit of address (0 to 132)

8-bit interface / SPI

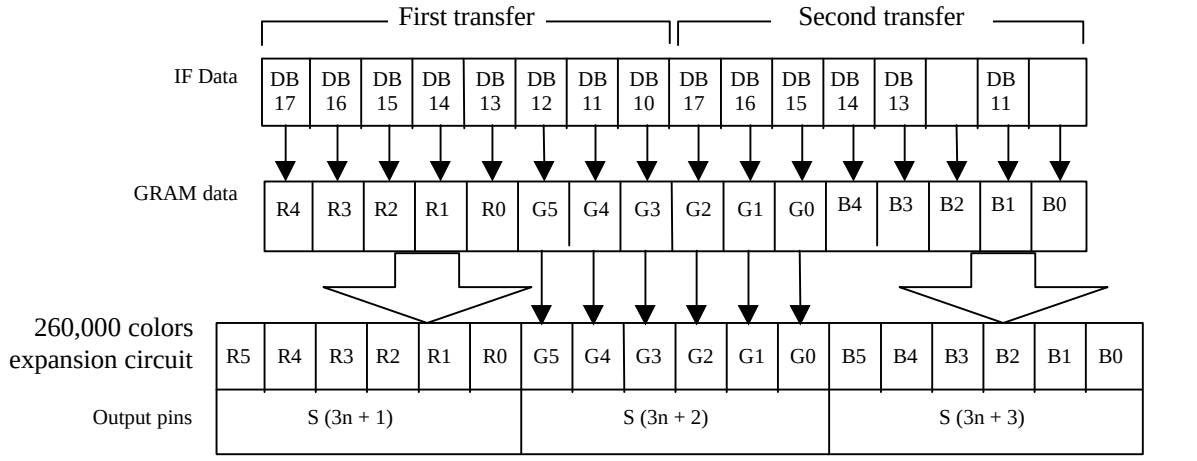


Figure 6 Note: n = lower eight bite of address (0 to 132)

Table 6: Relationship between GRAM address and display position (SS = “1”, BGR= “1”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB0 ... DB17			DB0 ... DB17			DB0 ... DB17			DB0 ... DB17				DB0 ... DB17			DB0 ... DB17			DB0 ... DB17			DB0 ... DB17		
G1	G176	"0083"H			"0082"H			"0081"H			"0080"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	G175	"0183"H			"0182"H			"0181"H			"0180"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	G174	"0283"H			"0282"H			"0281"H			"0280"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	G173	"0383"H			"0382"H			"0381"H			"0380"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	G172	"0483"H			"0482"H			"0481"H			"0480"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	G171	"0583"H			"0582"H			"0581 H			"0580"H			.....	"0503"H			"0502"H			"0501 H			"0500"H		
G7	G170	"0683"H			"0682"H			"0681"H			"0680"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	G169	"0783"H			"0782"H			"0781"H			"0780"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	G168	"0883"H			"0882"H			"0881"H			"0880"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	G167	"0983"H			"0982"H			"0981"H			"0980"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	G166	"0A83"H			"0A82"H			"0A81"H			"0A80"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	G165	"0B83"H			"0B82"H			"0B81"H			"0B80"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	G164	"0C83"H			"0C82"H			"0C81"H			"0C80"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	G163	"0D83"H			"0D82"H			"0D81"H			"0D80"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	G162	"0E83"H			"0E82"H			"0E81"H			"0E80"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	G161	"0F83"H			"0F82"H			"0F81"H			"0F80"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	G160	"1083"H			"1082"H			"1081"H			"1080"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	G159	"1183"H			"1182"H			"1181"H			"1180"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	G158	"1283"H			"1282"H			"1281"H			"1280"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	G157	"1383"H			"1382"H			"1381"H			"1380"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
⋮		⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G169	G8	"A883"H			"A882"H			"A881"H			"A880"H			.....	"A803"H			"A802"H			"A801"H			"A800"H		
G170	G7	"A983"H			"A982"H			"A981"H			"A980"H			.....	"A903"H			"A902"H			"A901"H			"A900"H		
G171	G6	"AA83"H			"AA82"H			"AA81"H			"AA80"H			.....	"AA03"H			"AA02"H			"AA01"H			"AA00"H		
G172	G5	"AB83"H			"AB82"H			"AB81"H			"AB80"H			.....	"AB03"H			"AB02"H			"AB01"H			"AB00"H		
G173	G4	"AC83"H			"AC82"H			"AC81"H			"AC80"H			.....	"AC03"H			"AC02"H			"AC01"H			"AC00"H		
G174	G3	"AD83"H			"AD82"H			"AD81"H			"AD80"H			.....	"AD03"H			"AD02"H			"AD01"H			"AD00"H		
G175	G2	"AE83"H			"AE82"H			"AE81"H			"AE80"H			.....	"AE03"H			"AE02"H			"AE01"H			"AE00"H		
G176	G1	"AF83"H			"AF82"H			"AF81"H			"AF80"H			.....	"AF03"H			"AF02"H			"AF01"H			"AF00"H		

18-bit interface & hard dither mode

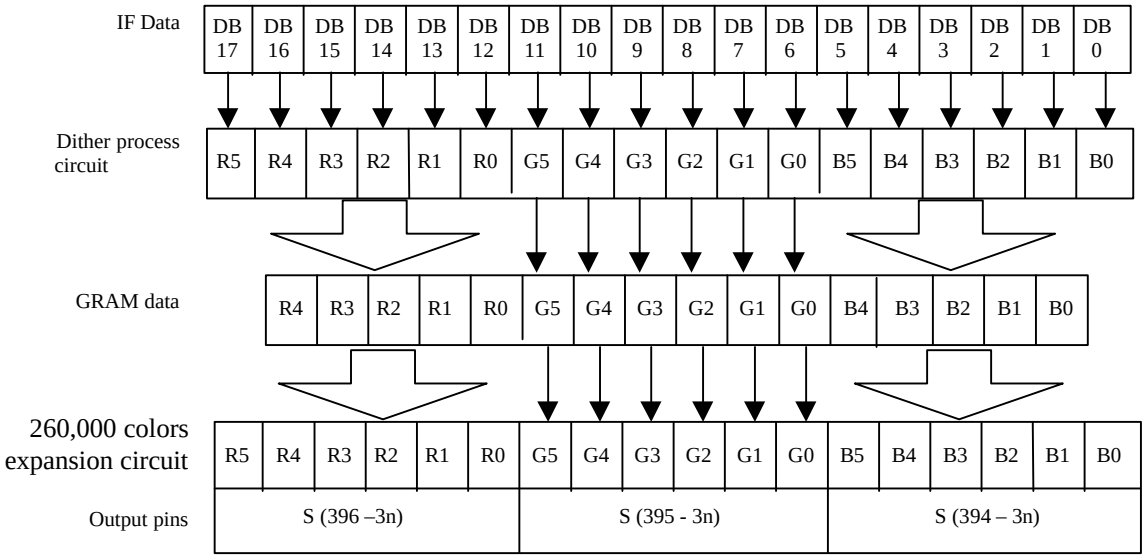


Figure 7 Note: n = lower eight bite of address (0 to 132)

16-bit interface

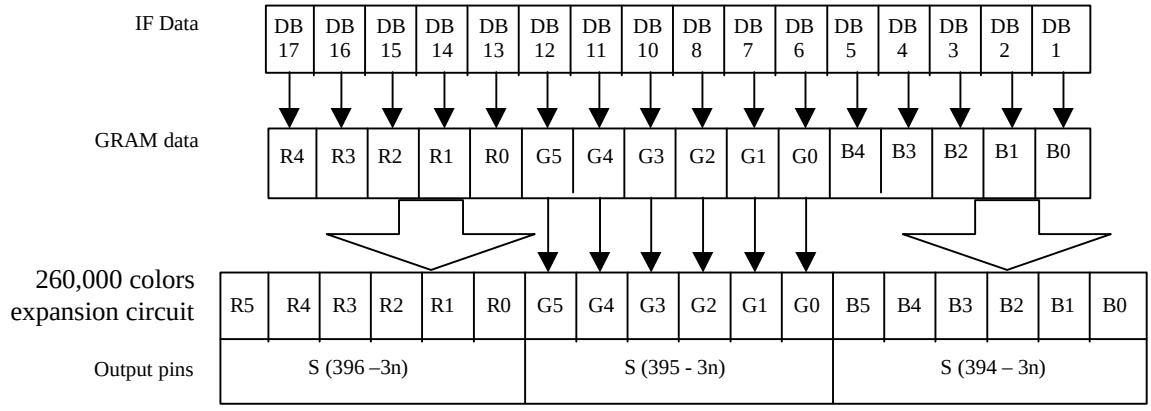


Figure 8 Note: n = lower eight bite of address (0 to 132)

9-bit interface & hard dither mode

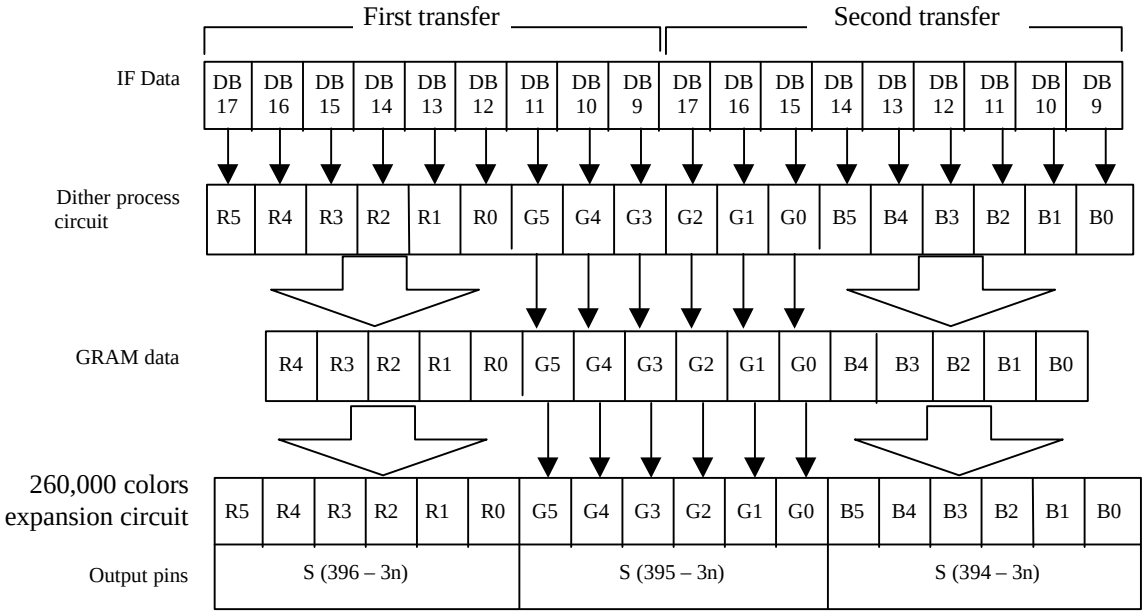


Figure 9

8-bit interface / SPI

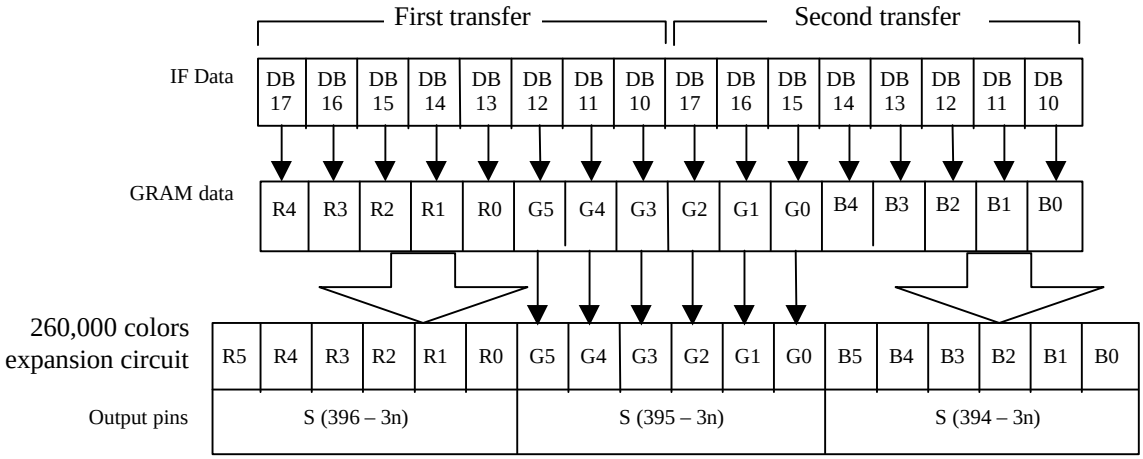


Figure 10

Note: n = lower eight bite of address (0 to 132)

Instructions

Outline

The HD66773 uses the 18-bit bus architecture. Before the internal operation of the HD66773 starts, control information of 18-/16-/9-/8-bit is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66773 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (IB15 to IB0), make up the HD66773 instructions. When using an internal RAM, HD66773 selects 18-bit. There are eight categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale gamma adjustment

Normally, instructions that write data are used most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load. Because instructions are executed in 0 cycles, data could be written in succession.

As indicated below, assignment to 16-bit instruction ()B15-0) depends on its instruction. Follow the data format of the interface used and execute the instruction.

18-bit interface

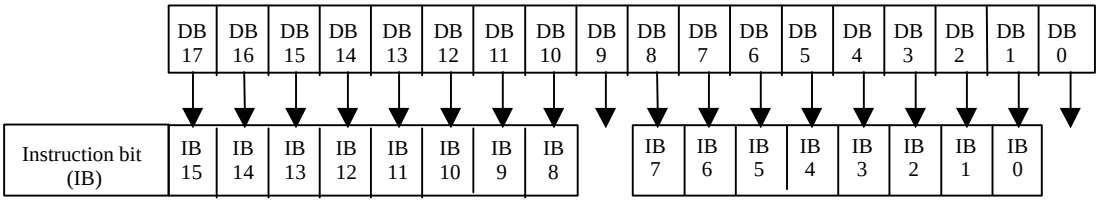


Figure 11

16-bit interface

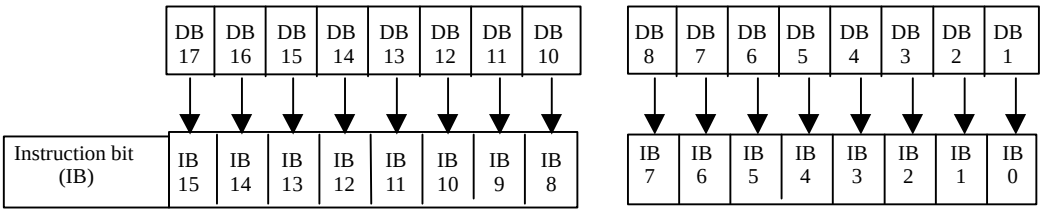


Figure 12

9-bit interface

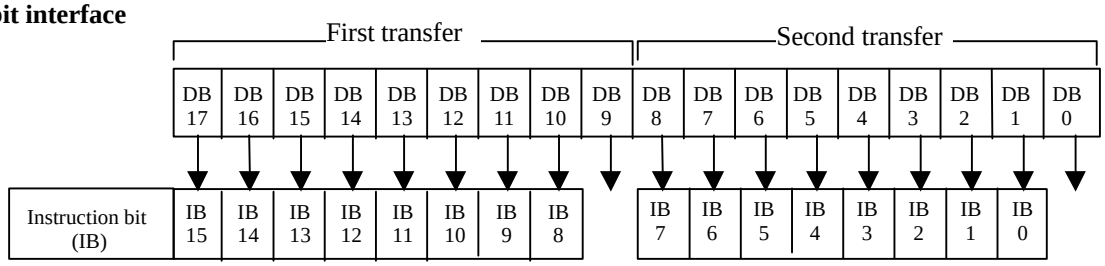


Figure 13

8-bit interface/SPI (transfer two times/pixel)

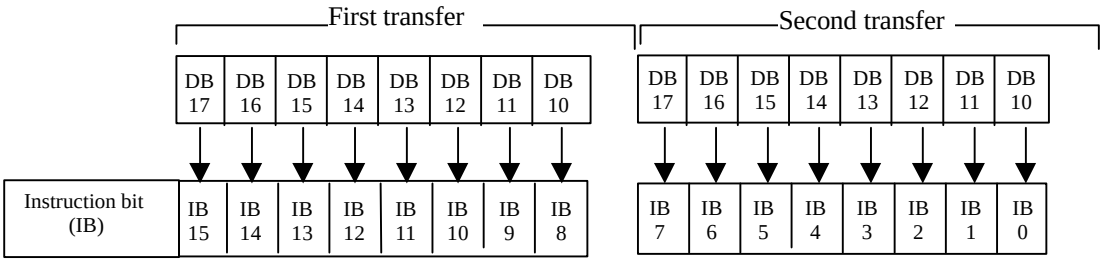


Figure 14

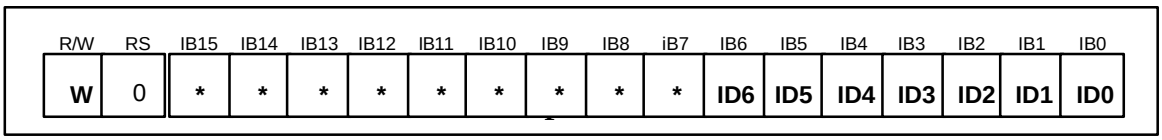
Detail description

Please be noticed that instructions description indicated below are descriptions for instruction bit (IB15-0) mounted on each interface.

Index / Status / Display control Instruction

Index (IR)

The index instruction specifies the RAM control indexes (R00h to R3Bh). It sets the register number in the range of 000000 to 111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

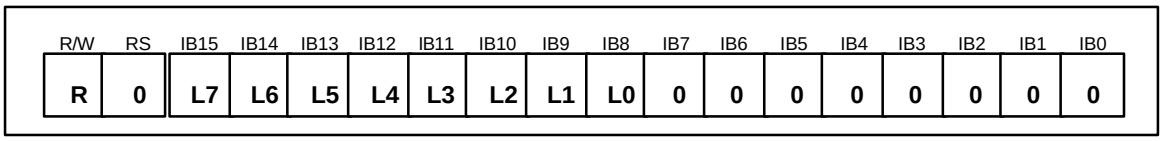


R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	iB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 15 Index Instruction

Status Read (SR)

The status read instruction reads the internal status of the HD66773.
L7–0: Indicates the driving raster-row position where the liquid crystal display is being driven.

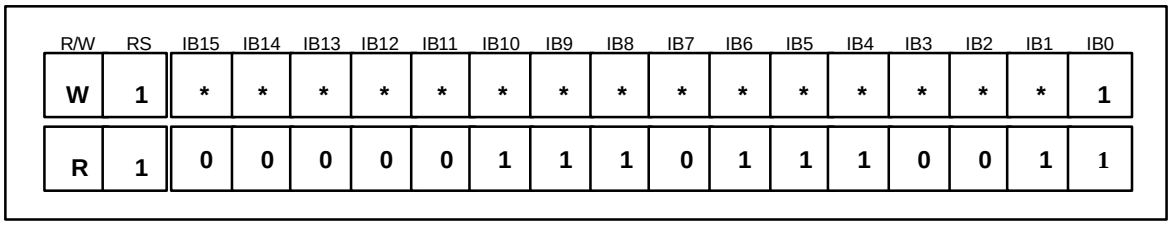


R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 16 Status Read Instruction

Start Oscillation (R00 h)

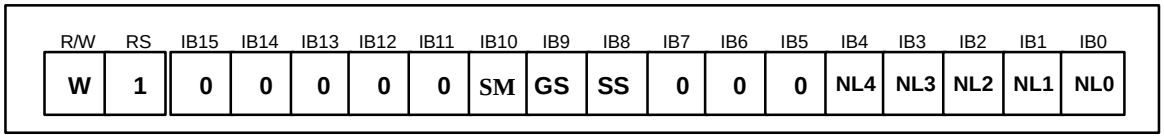
The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)
If this register is read forcibly, *0773H is read.



R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	1	1

Figure 17 Start Oscillation Instruction

Driver Output Control (R01 h)



R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 18 Driver Output Control Instruction

GS: Selects the output shift direction of the gate driver. When GS = 0, G1 shifts to G176. When GS = 1, G176 shifts to G1. ‘

SM: Change scan order of gate driver. Select the order according to the mounting method. See “Scan Mode Setting” for details see the page 76.

SS: Selects the output shift direction of the source driver. When SS = “0”, S1 shifts to S396. When SS = “1”, S396 shifts to S1. When SS = “0”, <R><G><B> color is assigned from S1. Set SS bit and BGR bit when changing the dot order of R, G and B. When SS = 1, <R><G><B> color is assigned from S396. Re-write the RAM when intending to change the SS bit or RGB bit.

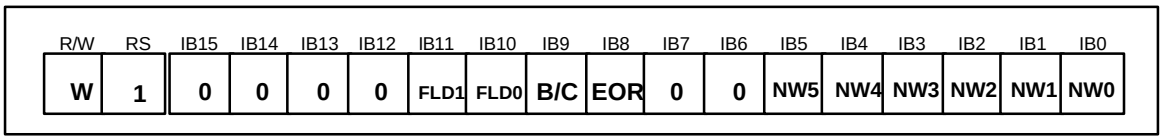
NL4–0: Specify number of lines for the LCD drive. Number of lines for the LCD drive can be adjusted for every eight raster-rows. GRAM address mapping does not depend on the setting value of the drive duty ratio. Select the set value for the panel size or higher.

Table 7: NL Bits and Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size	Number of LCD Driver Lines	Gate Driver Used
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	396 x 16 dots	16	G1 to G16
0	0	0	1	0	396 x 24 dots	24	G1 to G24
0	0	0	1	1	396 x 32 dots	32	G1 to G32
0	0	1	0	0	396 x 40 dots	40	G1 to G40
0	0	1	0	1	396 x 48 dots	48	G1 to G48
0	0	1	1	0	396 x 56 dots	56	G1 to G56
0	0	1	1	1	396 x 64 dots	64	G1 to G64
0	1	0	0	0	396 x 72 dots	72	G1 to G72
0	1	0	0	1	396 x 80 dots	80	G1 to G80
0	1	0	1	0	396 x 88 dots	88	G1 to G88
0	1	0	1	1	396 x 96 dots	96	G1 to G96
0	1	1	0	0	396 x 104 dots	104	G1 to G104
0	1	1	0	1	396 x 112 dots	112	G1 to G112
0	1	1	1	0	396 x 120 dots	120	G1 to G120
0	1	1	1	1	396 x 128 dots	128	G1 to G128
1	0	0	0	0	396 x 136 dots	136	G1 to G136
1	0	0	0	1	396 x 144 dots	144	G1 to G144
1	0	0	1	0	396 x 152 dots	152	G1 to G152
1	0	0	1	1	396 x 160 dots	160	G1 to G160
1	0	1	0	0	396 x 168 dots	168	G1 to G168
1	0	1	0	1	396 x 176 dots	176	G1 to G176

Note: Blank period (when all gates output Vgoff level) of 8H period will be inserted to the gates after all gates are scanned.

LCD-Driving-Waveform Control (R02 h)



R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 19 LCD-Driving-Waveform Control Instruction

FLD1-0: Set number of the field that the n field inter-laced driving. For details, see the “Inter-laced” drive section. (P76)

FLD1	FLD0	Number of field
0	0	Setting disabled
0	1	1 field
1	0	Setting disabled
1	1	3 field

Table 8

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a n raster-row waveform is generated and alternates in each raster-row specified by bits EOR and NW5–NW0 in the LCD-driving-waveform control register. For details, see the “n-raster-row Reversed AC Drive” section. (P75)

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the number of the LCD drive raster-row and the “n raster-row”. For details, see the “n-raster-row Reversed AC Drive” section.

NW5–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW5–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

Power Control 1 (R03h)

Power Control 2 (R04h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB
W	1	CAD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20 Power Control Instruction

BT2–0: The output factor of step-up circuit is selected. Adjust scale factor of the step-up circuit by the voltage used. Lower amplification of the step-up circuit consumes less current.

DC2-0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP2–0: The amount of fixed current from operational amplifier for the power supply is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when AP2-0 = “000”, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

SLP: When SLP = 1, the HD66773 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption.
During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66773 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section. Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = “0”)

b. Start oscillation

During the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled. Serial transfer to the common driver is possible when it is in standby mode. Transfer the data again after it has been released from standby mode.

CAD: Set up based on retention capacitor configuration of the TFT panel.

CAD = “0” Set this up when use Cst composition.

CAD = “1” Set this up when use Cadd composition.

Table 9 BT Bits and DDVDH and VGH Outputs

BT2	BT1	BT0	DDVDH Output	VGH Output	Notes*	Capacitor connect pin
0	0	0	2 x Vci1	3 x Vci2	VGH = Vci1 x 6	DDVDH, VGH, VGL, VCL, C11±, C21±, C22±, C31±, C41±
0	0	1	2 x Vci1	4 x Vci2	VGH = Vci1 x 8	DDVDH, VGH, VGL, VCL, C11±, C21±, C22±, C23±, C31±, C41±
0	1	0	3 x Vci1	3 x Vci2	VGH = Vci1 x 9	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±, C31±, C41±
0	1	1	3 x Vci1	2 x Vci2	VGH = Vci1 x 6	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±, C31±, C41±
1	0	0	2 x Vci1	Vci1 + 2 x Vci2	VGH = Vci1 x 5	DDVDH, VGH, VGL, VCL, C11±, C21±, C22±, C31±, C41±
1	0	1	2 x Vci1	Vci1 + 3 x Vci2	VGH = Vci1 x 7	DDVDH, VGH, VGL, VCL, C11±, C21±, C22±, C23±, C31±, C41±
1	1	0	Step-up stopped	3 x Vci2	VGH = Vci2 x 3	DDVDH, VGH, VGL, VCL, C21±, C22±, C31±, C41±
1	1	1	Setting prohibited	Setting prohibited	Setting prohibited	—

Note: The step-up factors of VGH are derived from Vci1 when DDVDH and Vci2 are shorted. The conditions of DDVDH ≤ 5.5 V and VGH ≤ 16.5 V must be satisfied.

Table 10 DC Bits and Step-up Cycle

DC2	DC1	DC0	Step-up Cycle in Step-up Circuit 1	Step-up Cycle in Step-up Circuits 2/3/4
0	0	0	DCCLK divided by 15	DCCLK divided by 60
0	0	1	DCCLK divided by 30	DCCLK divided by 60
0	1	0	DCCLK divided by 60	DCCLK divided by 60
0	1	1	DCCLK divided by 30	DCCLK divided by 240
1	0	0	DCCLK divided by 15	DCCLK divided by 120
1	0	1	DCCLK divided by 30	DCCLK divided by 120
1	1	0	DCCLK divided by 60	DCCLK divided by 120
1	1	1	DCCLK divided by 60	DCCLK divided by 240

Table 11 AP Bits and Amount of Current in Operational Amplifier

AP2	AP1	AP0	Amount of Current in Operational Amplifier
0	0	0	Operation of the operational amplifier and step-up circuit stops.
0	0	1	Small
0	1	0	Small or medium
0	1	1	Medium
1	0	0	Medium or large
1	0	1	Large
1	1	0	Setting inhibited
1	1	1	Setting inhibited

Power Control 3 (R0Ch)
Power Control 4 (R0Dh)
Power Control 5 (R0Eh)

R/W	RS	IB15	IDB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
W	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 21

VC2-0: Adjust reference voltage of VREG1OUT, VREG2OUT and VciOUT to optional rate of Vci. Also, when VC2-0 = "111", it is possible to stop the internal reference voltage generator. It is possible to apply any voltage.

VRL3-0: Set magnification of amplification for VREG2OUT voltage (voltage for the reference while generating Vgoff.) It allows magnify the amplification of Vci output voltage from –1.5 to -6.5 times.

PON: This is an operation starting bit for the booster circuit 3. PON = 0 is to stop and PON = 1 to start operation.

VRH3-0: Set magnification of amplification for VREG1OUT voltage (VCOM, reference voltage for gryascale voltage) It allows magnify the amplification of REGP from 1.33 to 2.775 times.

VCOMG: When VCOMG = 1, VcomL voltage can output to negative voltage (-5V).
When VCOMG = 0, VcomL voltage becomes GND and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished. Also, When VCOMG = 0, setting of the VDV4-0 is invalid. In this case, adjustment of Vcom/Vgoff A/C amplitude must be adjusted with VcomH using VCM4-0.

VDV4-0: Sets amplification factors for Vcom and Vgoff while Vcom AC drive is being performed. It is possible to set up from 0.6 to 1.23 times of VREG1. When VCOMG = 0, the set up is invalid.

VCM4-0: Set VcomH voltage (voltage of higher side when Vcom is driven in A/C.) It is possible to amplify from 0.4 to 0.98 times of VREG1 voltage. Also, when setting up VCM4-0 = "11111", stop the internal volume adjustment and adjust VcomH with external resistance from VcomR.

Table 12 VC Settings and Internal Reference Voltage

VC2	VC1	VC0	Internal Reference Voltage (REGP) of VREG1OUT and Vci1
0	0	0	Vci
0	0	1	0.92 x Vci
0	1	0	0.87 x Vci
0	1	1	0.83 x Vci
1	0	0	0.76 x Vci
1	0	1	0.73 x Vci
1	1	0	0.68 x Vci
1	1	1	Vci1: Hi-Z REGP: GND

Note: Leave these settings open because the voltage other than that for halting the internal circuit is output for REGP.

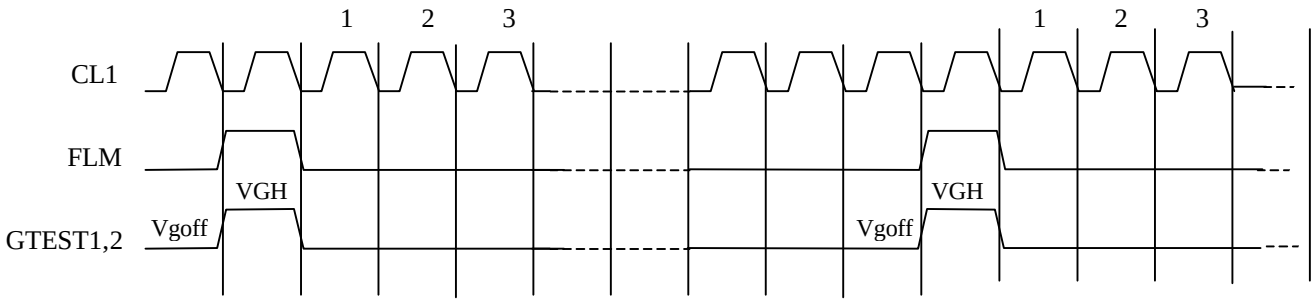


Figure 22 Output timing of GTEST1, and 2

Table 13 VRH Bits and VREG1OUT Voltage

VRH3	VRH2	VRH1	VRH0	VREG1OUT Voltage
0	0	0	0	REGP x 1.33 times
0	0	0	1	REGP x 1.45 times
0	0	1	0	REGP x 1.55 times
0	0	1	1	REGP x 1.65 times
0	1	0	0	REGP x 1.75 times
0	1	0	1	REGP x 1.80 times
0	1	1	0	REGP x 1.85 times
0	1	1	1	Stopped
1	0	0	0	REGP x 1.9000 times
1	0	0	1	REGP x 2.175 times
1	0	1	0	REGP x 2.325 times
1	0	1	1	REGP x 2.475 times
1	1	0	0	REGP x 2.625 times
1	1	0	1	REGP x 2.700 times
1	1	1	0	REGP x 2.775 times
1	1	1	1	Stopped

Notes: 1. Adjust VC2-0 and VRH3-0 so that the VREG1OUT voltage is lower than 5.0 V.

Table 14 VRL Bits and VREG2OUT Voltage

VRL3	VRL2	VRL1	VRL0	VREG2OUT Voltage
0	0	0	0	Vci x –1.5
0	0	0	1	Vci x– 2.0 times
0	0	1	0	Vci x – 2.5 times
0	0	1	1	Vci x – 3.0 times
0	1	0	0	Vci x– 3.5 times
0	1	0	1	Vci x –4.0 times
0	1	1	0	Vci x –4.5 times
0	1	1	1	Stopped
1	0	0	0	Vci x –5.0 times
1	0	0	1	Vci x –5.5 times
1	0	1	0	Vci x –6.0times
1	0	1	1	Vci x –6.5 times
1	1	0	0	Setting inhibited
1	1	0	1	Setting inhibited
1	1	1	0	Setting inhibited
1	1	1	1	Stopped

Notes: 1. Adjust Vci and VRL3-0 so that the VREG2OUT voltage is higher than –16.0 V.

Table 15 VCM4-0 Bits and VcomH Voltage

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH Voltage
0	0	0	0	0	VREG1OUT x 0.40
0	0	0	0	1	VREG1OUT x 0.42
0	0	0	1	0	VREG1OUT x 0.44
:	:	:	:	:	
0	1	1	0	0	VREG1OUT x 0.64
0	1	1	0	1	VREG1OUT x 0.66
0	1	1	1	0	VREG1OUT x 0.68
0	1	1	1	1	The internal volume stops, and VcomH can be adjusted from VcomR by an external variable resistor.
1	0	0	0	0	VREG1OUT x 0.70
1	0	0	0	1	VREG1OUT x 0.72
1	0	0	1	0	VREG1OUT x 0.74
:	:	:	:	:	
1	1	1	0	0	VREG1OUT x 0.94
1	1	1	0	1	VREG1OUT x 0.96
1	1	1	1	0	VREG1OUT x 0.98
1	1	1	1	1	The internal volume stops, and VcomH can be adjusted from VcomR by an external variable resistor.

Note: Adjust VREG1OUT and VCM4-0 so that the VcomH voltage is lower than VDH.

Table 16 VDV4-0 Bits and Vcom Amplitude

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom Amplitude
0	0	0	0	0	VREG1OUT x 0.60 times
0	0	0	0	1	VREG1OUT x 0.63 times
0	0	0	1	0	VREG1OUT x 0.66 times
:	:	:	:	:	
0	1	1	0	0	VREG1OUT x 0.96 times
0	1	1	0	1	VREG1OUT x 0.99 times
0	1	1	1	0	VREG1OUT x 1.02 times
0	1	1	1	1	Setting inhibited
1	0	0	0	0	VREG1OUT x 1.05 times
1	0	0	0	1	VREG1OUT x 1.08 times
1	0	0	1	0	VREG1OUT x 1.11 times
1	0	0	1	1	VREG1OUT x 1.14 times
1	0	1	0	0	VREG1OUT x 1.17 times
1	0	1	0	1	VREG1OUT x 1.20 times
1	0	1	1	0	VREG1OUT x 1.23 times
1	0	1	1	1	Setting inhibited
1	1	*	*	*	

Note: Adjust VREG1OUT and VDV4-0 so that the Vcom and Vgoff amplitudes are lower than 6.0 V.

Entry Mode (R05h)

Compare Register (R06h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DIT	0	0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Figure 23

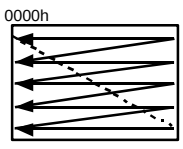
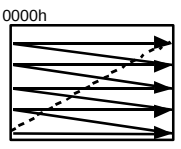
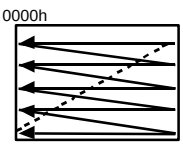
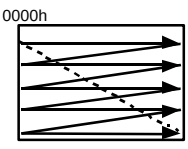
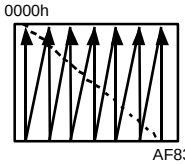
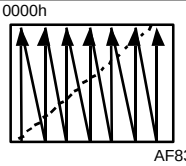
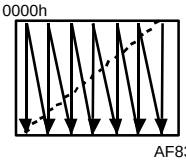
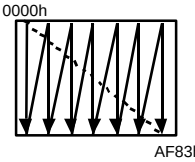
The write data sent from the microcomputer is modified in the HD66773 written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section. (See page 64.)

HWM: When HWM= “1”, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after writing to RAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see High Speed RAM Write Mode section. (See page 58)

I/D1-0: When I/D1-0 = “1”, the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D1-0 = “0”, the AC is automatically decremented by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter by I/D1-0 is done independently for the upper (AD15-8) and lower (AD7-0) addresses. The direction of moving through the addresses when the GRAM is written to is set by the AM bit.

AM: Set the automatic update method of the AC after the data is written to the GRAM. When AM = “0”, the data is continuously written horizontally. When AM = “1”, the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

DIT: Hard dither mode is selected when DIT= “1”.Use hard dither mode when 18-/9-bit or I/F mode is selected.

	I/D1-0="00" Horizontal: decrement Vertical: decrement	I/D1-0="01" Horizontal: increment Vertical: decrement	I/D1-0="10" Horizontal: decrement Vertical: increment	I/D1-0="11" Horizontal: increment Vertical: increment
AM="0" Horizontal				
AM="1" Vertical				

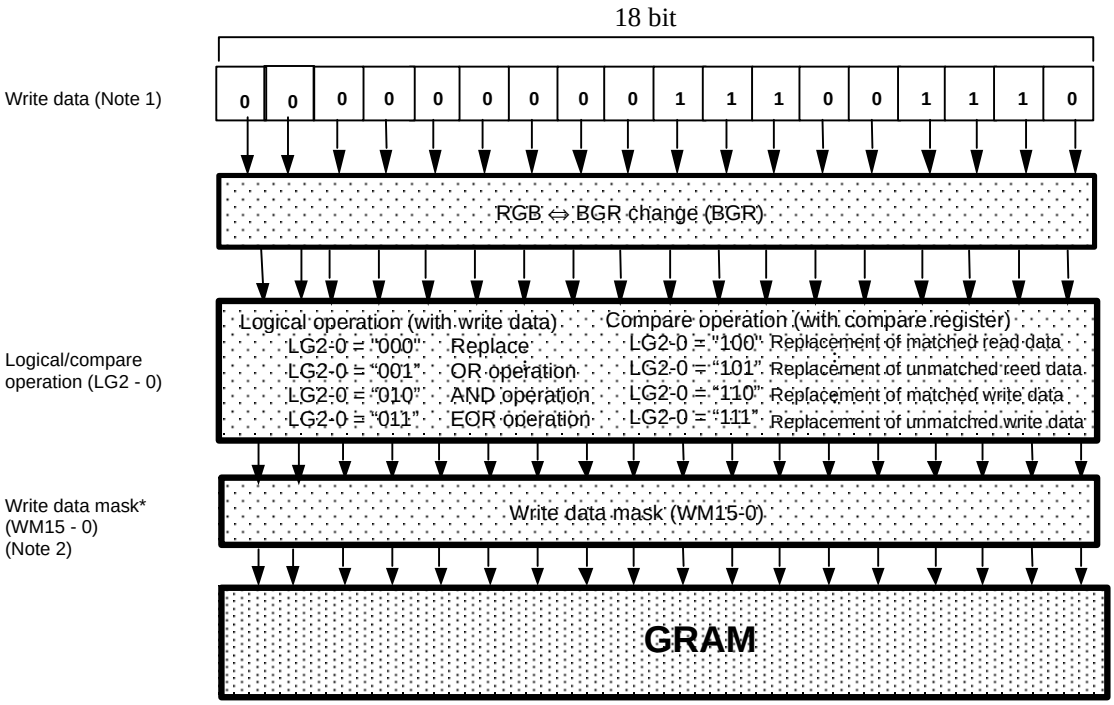
Note: When a window address range has been set the GRAM can only be written to within that range.

Figure 24 Address Direction Settings

LG2–0: Compare the data read from the GRAM or write data written from the microcomputer with the compare registers (CP15–0) by a compare/logical operation and write the results to GRAM. For details, see the "Graphic Operation function".

CP15–0: Sets the compare register for the compare operation with the data read from the GRAM or written by the microcomputer. *This function can not be used when using 18-/9-bit interface. Set LG2-0 = "000" when using 18-/9-bit interface.

BGR: In the writing of 18 bits of data to RAM, this bit may be used to reverse the it order from R, G, and B to B, G, and R. Please be aware that setting BGR to 1 will convert the order of the CP15-0 and WM15-0 bits in the same way.

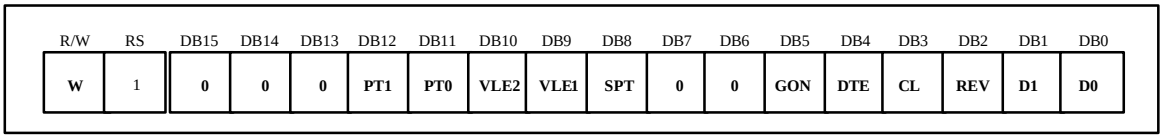


Note1) Data processing when it is not LG2-0 = "000", is available only when using 8-/16-bit interface. For the bit assignment for each interface, see the section parallel transfer.

2) The write data mask (WM15-0) is set by the register in the RAM write data mask section. Write data mask operation is available only with 8-/16-bit interface.

Figure 25

Display Control (R07h)



R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0

Figure 26 Display Control Instruction

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven. For details, see the Screen-division Driving Function section.

VLE2–1: When VLE1 = "1", a vertical scroll is performed in the 1st screen. When VLE2 = "1", a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens cannot be controlled at the same time.

VLE2	VLE1	2nd Screen	1st Screen
0	0	Fixed display	Fixed display
0	1	Fixed display	Scroll display
1	0	Scroll display	Fixed display
1	1	Setting disabled	

Table 17

CL: When CL = "1", HD66773 selects 8-color mode. For details, see the 8-color Display Mode section.

CL	Number of Display Colors
0	65,536
1	8

Table 18

SPT: When SPT = "1", the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally-white and normally-black panels. Source output level is indicated below.

REV	GRAM data	Source output level							
		Display area		non-display area					
				PT1-0 = (0.*)		PT1-0= (1.0)		PT1-0 = (1.1)	
		VCOM = "L"	VCOM ="H"	VCOM = "L"	VCOM ="H"	VCOM = "L"	VCOM ="H"	VCOM = "L"	VCOM ="H"
0	16'h0000 ⋮ 16'hFFFF	V31 ⋮ V0	V0 ⋮ V31	V31	V0	GND	GND	Hi-z	Hi-z
1	16'h0000 ⋮ 16'hFFFF	V0 ⋮ V31	V31 ⋮ V0	V31	V0	GND	GND	Hi-z	Hi-z

Figure 27

REV	GRAM data	Source output level							
		D1-0 = (1.1)		D1-0 = (1.0)		D1-0 = (0.1)		D1-0 = (0.0)	
		VCOM = "L"	VCOM ="H"	VCOM = "L"	VCOM ="H"	VCOM = "L"	VCOM ="H"	VCOM = "L"	VCOM ="H"
0	16'h0000 ⋮ 16'hFFFF	V31 ⋮ V0	V0 ⋮ V31	V31	V0	GND	GND	GND	GND
1	16'h0000 ⋮ 16'hFFFF	V0 ⋮ V31	V31 ⋮ V0	V31	V0	GND	GND	GND	GND

Figure 28

GON: Gate off level becomes VGH when GON = "0".

D1–0: Display is on when D1 = "1" and off when D1 = "0". When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = "1". When D1= "0", the display is off with all of the source outputs set to the GND level. Because of this, the HD66773 can control the charging current for the LCD with AC driving.

When D1–0 = "01", the internal display of the HD66773 is performed although the display is off. When D1-0 = "00", the internal display operation halts and the display is off.

Control the display on/off while control GON and DTE. For details, see the Instruction Set Up Flow.

Table 19 Bits and Operation

GON	DTE	D1	D0	HD66773 Internal Display Operation	Source output	Gate output
0	0	0	0	Halt	GND	VGH
0	0	0	1	Operate	GND	VGH
1	0	0	1	Operate	GND	VGOFF
1	0	1	1	Operate	Grayscale level output	VGOFF
1	1	1	1	Operate	Grayscale level output	Gate selective line:VGH, Gate non-selective line: VGOFF

Notes: 1. Writing from the microcomputer to the GRAM is independent from the state of D1–0.

2. When it is the standby mode, D1–0 = "00". However, the register contents of D1–0 are not modified.

Frame Cycle Control (R0Bh)

R/W	RS	iB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

Figure 29

RTN3-0: Set the 1H period.

DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks which frequency are divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the 1H period (RTN3-0). When changing drive line count, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

EQ1-0: Sets equalinzing period.

Table 20

RTN3	RTN2	RTN1	RTN0	Clock cycles per Rster-row
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
⋮				⋮
1	1	1	0	30
1	1	1	1	31

Table 21

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc/1
0	1	2	fosc/2
1	0	4	fosc/4
1	1	8	fosc/8

*fosc = R-C oscillation frequency

Table 22

EQ1	EQ2	EQ period
0	0	No EQ
0	1	1 clock cycle
1	0	2 clock cycle
1	1	3 clock cycle

Formula for the fram frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row x division ratio x (Line + 8)}} \text{ [Hz]}$$

fosc: CR oscillation frequency
Line: Number of drive raster-row (NL bits)
Division ratio: DIV bit
Clock cycles per raster-row: RTN bits

Note) Equalization is available only when VcomL is larger than 0V. Set EQ = “00”, when VcomL is smaller than 0V.

SDT1-0: Set delay amount from the gate output signal falling edge of the source outputs.

Table 23

SDT1	SDT0	Delay amount of the source output
0	**0**	1 clock cycle
0	**1**	2 clock cycle
1	**0**	3 clock cycle
1	**1**	4 clock cycle

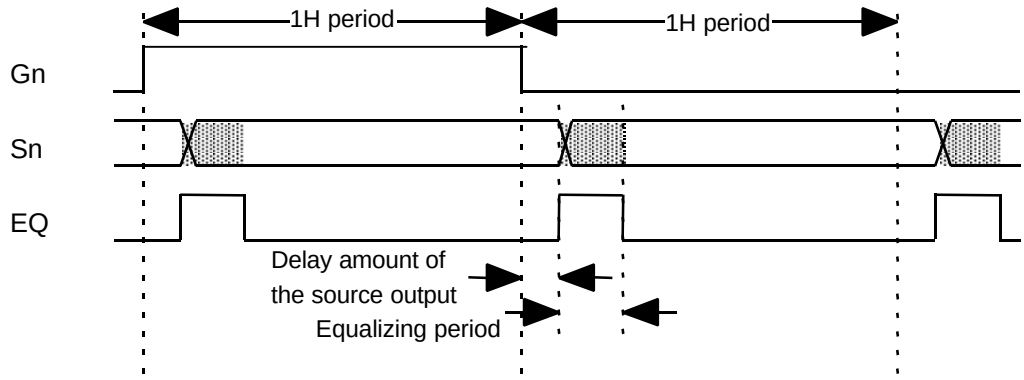


Figure 30

NO1-0: Sets amount of non-overlap of the gate output.

Table 24

NO1	NO0	Amount of non-overlap
0	**0**	0 clock cycle
0	**1**	4 clock cycle
1	**0**	6 clock cycle
1	**1**	8 clock cycle

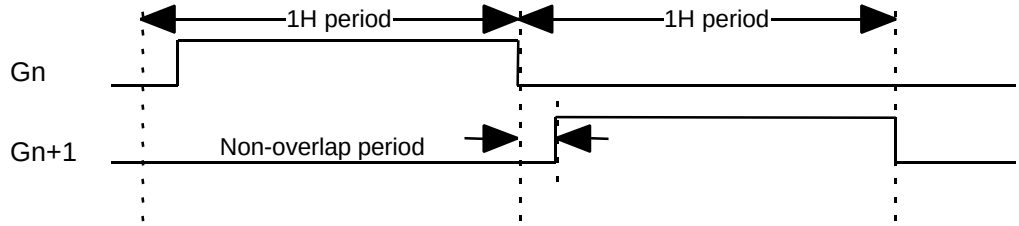


Figure 31

Gate Scan Position (R0Fh)

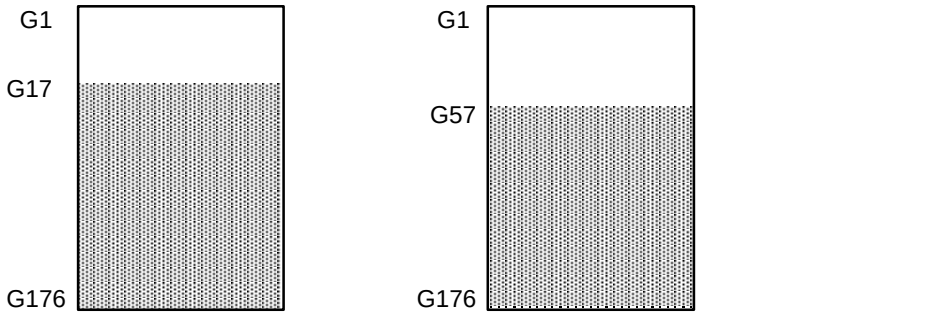
R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 32

SCN4-0: Set the scanning starting position of the gate driver.

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning start position When GS=0	Scanning start position When GS=1
0	0	0	0	0	G1	G176
0	0	0	0	1	G9	G169
0	0	0	1	0	G17	G161
⋮					⋮	⋮
1	0	1	0	0	G161	G17
1	0	1	0	1	G169	G9

Table 25



GS=0
NL=10011
SCN4-0=00010

GS=0
NL=10101
SCN4-0=01110

Note: Do not set over NL = 176 for the gate scan ending position..

Figure 33: Relationship between NL and SCN set up value

Vertical Scroll Control (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

Figure 34

VL7-0: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 176th can be scrolled for the number of the raster-row. After 176th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL7-0) is valid when VLE1 = "1" or VLE2 = "1". The raster-row display is fixed when VLE2-1 = "00".

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scroll length
0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	1	0	2 raster-row
				⋮				⋮
1	0	1	0	1	1	1	0	174 raster-row
1	0	1	0	1	1	1	1	175 raster-row

Note: Do not set any higher raster-row than 175 ("AF"H)

Table 26

1st Screen Driving Position (R14h)

2nd Screen Driving Position (R15h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 35

SS17–0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the set value + 1 gate driver.

SE17–0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the set value + 1 gate driver. For instance, when SS17–10 = "07"H and SE17–10 = "10"H are set, the LCD driving is performed from G8 to G17, and non-selection driving is performed for G1 to G7, G18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ AFH. For details, see the Screen-division Driving Function section.

SS27–0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the set value + 1 gate driver. The second screen is driven when SPT = "1".

SE27–0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the set value + 1 gate driver. For instance, when SPT = "1", SS27–20 = "20"H, and SE27–20 = "4F"H are set, the LCD driving is performed from G33 to G80. Ensure that SS17–10 ≤ SE17–10 ≤ SS27–20 ≤ SE27–20 ≤ "AF"H. For details, see the Screen-division Driving Function section.

Horizontal RAM Address Position (R16h)

Vertical RAM Address Position (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 36 Horizontal/Vertical RAM Address Position Instruction

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA7-0 from the address specified by HSA7-0. Note that an address must be set before RAM is written to. Ensure "00"h ≤ HSA7-0 ≤ HEA7-0 ≤ "83"h.

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written to. Ensure "00"h ≤ VSA7-0 ≤ VEA7-0 ≤ "AF"h.

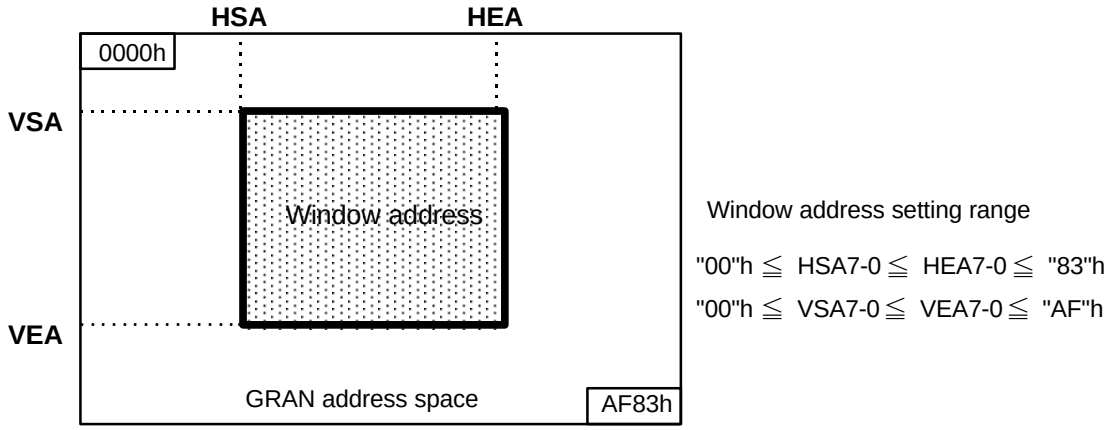


Figure 37 Window Address Setting Range

Note: 1. Ensure that the window address area is within the GRAM address space.
2. In high-speed write mode, data are written to GRAM in four-words. Thus, dummy write operations should be inserted depending on the window address area. For details, see the High-Speed Burst RAM Write Function section.
3. Set RAM address within the window address area. In high-speed write mode, set RAM address within the area containing dummy area. For details, see the High-Speed RAM Write Function section.

RAM Write Data Mask (R20h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0

Figure 38 RAM Write Data Mask Instruction

WM15–0: In writing to the GRAM, these bits mask writing in a bit unit. This function is useful only when using 8- or 16-bit interface. When WM15 = "1", this bit masks the write data of WD15 and does not write to the GRAM. Similarly, the WM14 to 0 bits mask the write data of WD14 to WD0 in a bit unit. For details, see the Graphics Operation Function section.

RAM Address Set (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 39 RAM Address Set Instruction

AD15–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address.

Table 27 GRAM Address Range in Eight-grayscale Mode

AD15 to AD0	GRAM Setting
"0000"H to "0083"H	Bitmap data for G1
"0100"H to "0183"H	Bitmap data for G2
"0200"H to "0283"H	Bitmap data for G3
"0300"H to "0383"H	Bitmap data for G4
⋮	⋮
"AC00"H to "AC83"H	Bitmap data for G173
"AD00"H to "AD83"H	Bitmap data for G174
"AE00"H to "AE83"H	Bitmap data for G175
"AF00"H to "AF83"H	Bitmap data for G176

Write Data to GRAM (R22h)

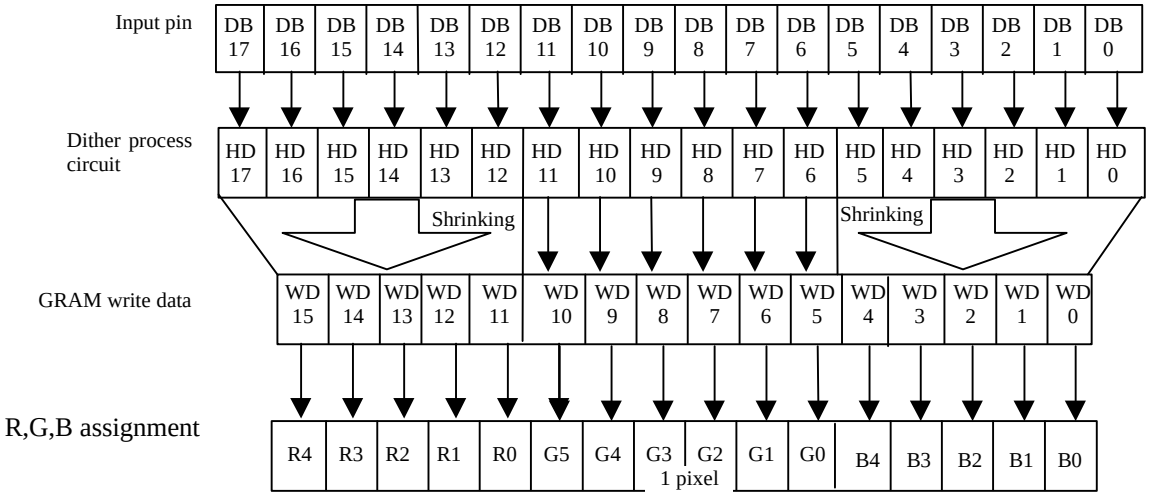
R/W	RS																		
W	1	RAM write data (WD17-0) *Allocation according to DB17-0 pin depends on interface. (Indicated below)																	
		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0

Figure 40

WD17–0: Transforms all the GRAM data into 18-bit, and writes the data. Format for trnasforming data into 18-bit depends on the interface used.

HD66773 selects the grayscale level according to the GRAM data. After writing data to GRAM, address is automatically updated according to AM bit and I/D bit. Access to GRAM during stand-by mode is not available. When using 18/9-bit interface, write data to GRAM after enable an internal hardware dither process circuit (DIT bit = “1”).

18-bit interface 262,144 colors available



Note: Write data into GAM after setting DIT = “1”.

Figure 41

16-bit interface 65,536 colors available

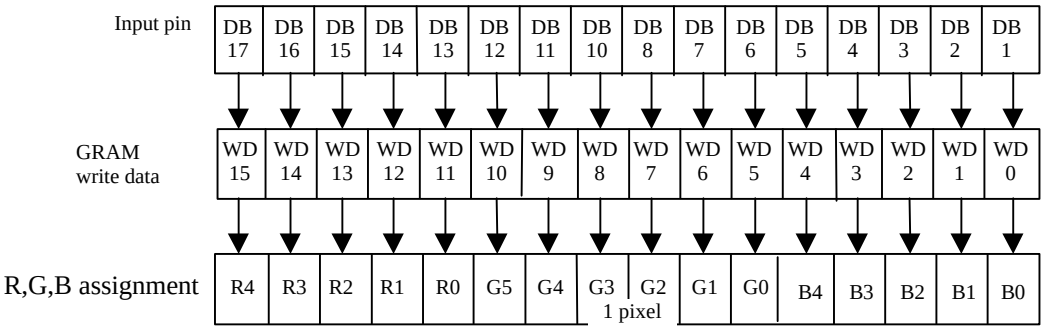


Figure 42

9-bit interface 262,144 colors available

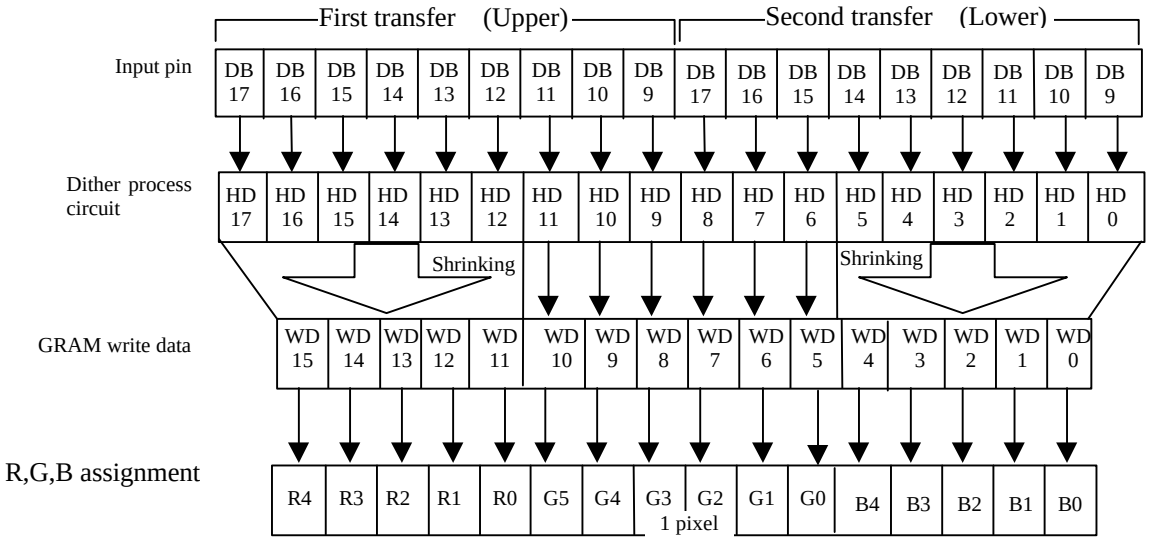


Figure 43 Note: Write data into GAM after setting DIT = "1".

8-bit interface 65,536 colors available

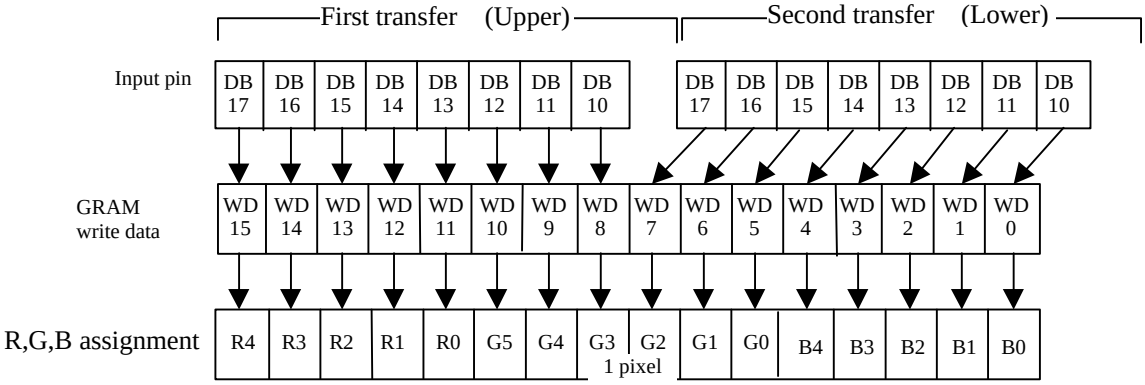


Figure 44

Table 28 GRAM Data and Grayscale Level

GRAM Data Set-up G	R/B	Selected Grayscale N	P
000000	00000	V0	V31
000001	-	V0 – V1	V31 - V30
000010	00001	V1	V30
000011	-	V1 –V2	V30 – V29
000100	00010	V2	V29
000101	-	V2 – V3	V29 – V28
000110	00011	V3	V28
000111	-	V3 – V4	V28 – V27
001000	00100	V4	V27
001001	-	V4 – V5	V27 – V26
001010	00101	V5	V26
001011	-	V5 – V6	V26 – V25
001100	00110	V6	V25
001101	-	V6 – V7	V25 – V24
001110	00111	V7	V24
001111	-	V7 – V8	V24 – V23

GRAM Data Set-up G	R/B	Selected Grayscal N	P
010000	01000	V8	V23
010001	-	V8 – V9	V23 – V22
010010	01001	V9	V22
010011	-	V9 –V10	V22 – V21
010100	01010	V10	V22
010101	-	V10 – V11	V21 – V20
010110	01011	V11	V20
010111	-	V11 – V12	V20 – V19
011000	01100	V12	V19
011001	-	V12 – V13	V19 – V18
011010	01101	V13	V18
011011	-	V13 – V14	V18 – V17
011100	01110	V14	V17
011101	-	V14 – V15	V17 – V16
011110	01111	V15	V16
011111	-	V15 – V16	V16 – V15

GRAM Data Set-up G	R/B	Selected Grayscal N	P
100000	10000	V16	V15
100001	-	V16 – V17	V15 – V14
100010	10001	V17	V14
100011	-	V17 –V18	V14 – V13
100100	10010	V18	V13
100101	-	V18 – V19	V13 – V12
100110	10011	V19	V12
100111	-	V19 – V20	V12 – V11
101000	10100	V20	V11
101001	-	V20 – V21	V11 – V10
101010	10101	V21	V10
101011	-	V21 – V22	V10 – V9
101100	10110	V22	V9
101101	-	V22 – V23	V9 – V8
101110	10111	V23	V8
101111	-	V23 – V24	V8 – V7

GRAM Data Set-up G	R/B	Selected Grayscal N	P
110000	11000	V24	V7
110001	-	V24 – V25	V7 – V6
110010	11001	V25	V6
110011	-	V25 –V26	V6 – V5
110100	11010	V26	V5
110101	-	V26 – V27	V5 – V4
110110	11011	V27	V4
110111	-	V27 – V28	V4 – V3
111000	11100	V28	V3
111001	-	V28 – V29	V3 – V2
111010	11101	V29	V2
111011	-	V29 – V30	V2 – V1
111100	11110	V30	V1
111101	-	V30 – V31	V1 – V0
111110	11111	V31	V0
111111	-	V31	V0

"N" = Negative level
"P" = Positive level

Read Data from GRAM (R22h)

R/W	RS	
R	1	RAM read data (WD15-0) *Allocation according to DB17-0 pin depends on interface. (Indicated below)

Figure 45 Read Data from GRAM Instruction

RD15–0: Read 16-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed within the HD66773, only one read can be processed since the latched data in the first word is used. Data read function and logical operation function are usable only when using 8-/16-bit interface. When using 9-/18-bit interface, this function can not be used.

16-bit interface

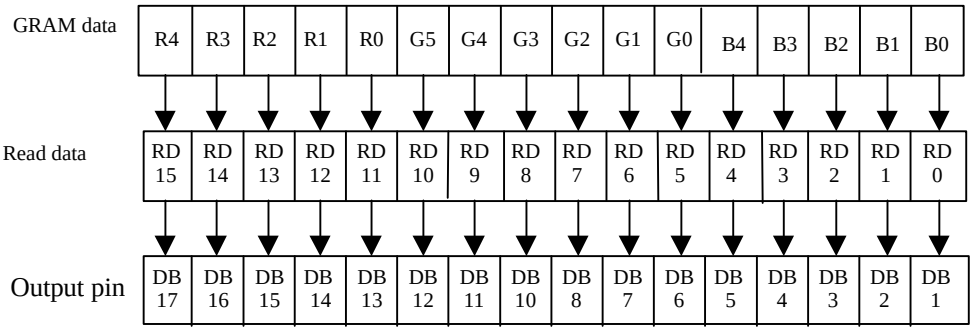


Figure 46

8-bit interface / Interface SPI

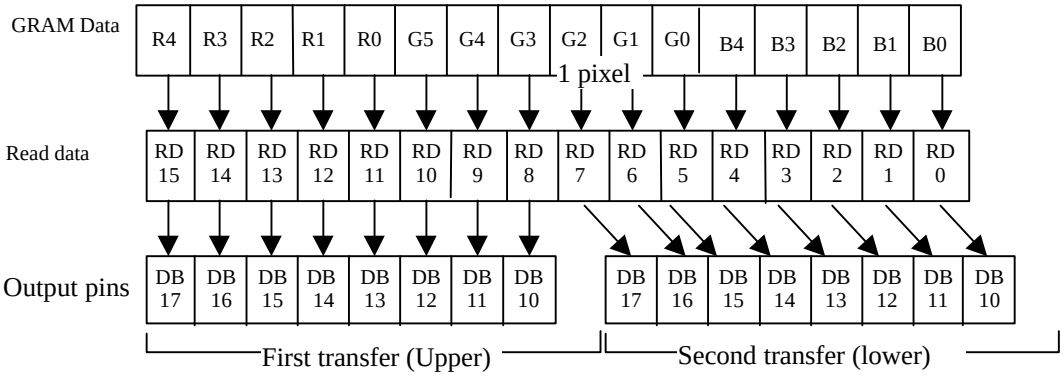


Figure 47

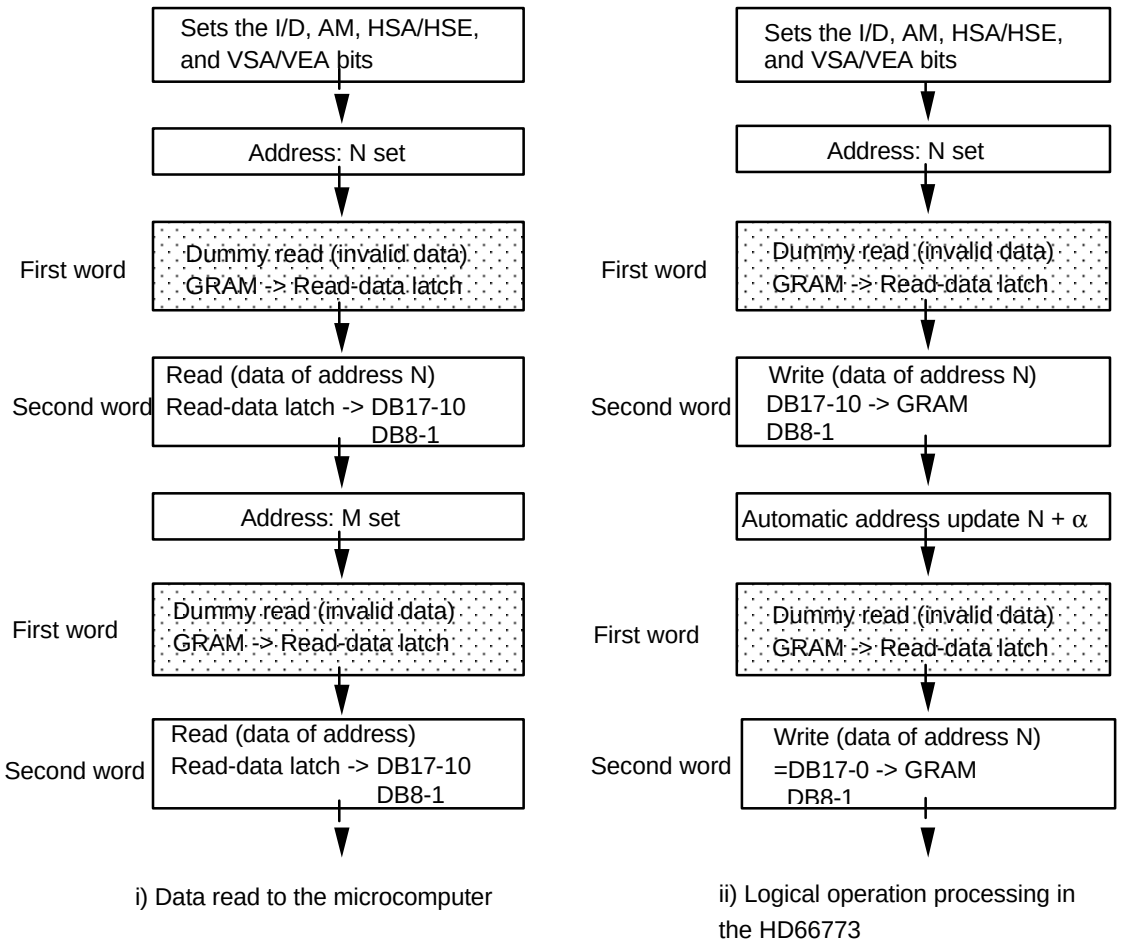


Figure 48 GRAM Read Sequence

Gamma Control (R30h to R3Bh)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31	W	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32	W	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33	W	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34	W	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35	W	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36	W	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37	W	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3A	W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3B	W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

Table 29

PKP52–00: Gamma micro adjustment register for the positive polarity output

PRP12-00: Gradient adjustment register for the positive polarity output

VRP14-00: Adjustment register for amplification adjustment of the positive polarity output

PKN52-00: Gamma micro adjustment register for the negative polarity output

PRN12-00: Gradient adjustment register for the negative polarity output

VRN14-0: Adjustment register for the amplification adjustment of the negative polarity output.

For details, see the Gamma Adjustment Function.

Table 30

Register No.	Register	R/W	RS	Upper Code IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	Lower Code IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Instructions
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Sets the index register value.
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	Reads the driving raster-row position (L7-0).
R00h	Oscillation Start	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode while stand-by period.
	Device code read	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	1	1	Reads "0773"H.
R01h	Driver output control	0	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0	Sets the gate driver shitg direction (GS), source driver shift direction (SS), and number of driving lines (NL4-0).
R02h	LCD drive AC control	0	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	Sets the LCD drive AC waveform (B/C), number of interfaced field (FLD1-0), EOR output (DOR)m and the number of n-raster-rows (NW5-0) at C-pattern
R03h	Power control (1)	0	1	0	0	0	0	0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB	Sets the stadby mode (STB), LCD power on (AP2-0), sleep mode (SLP), boosting cycle DC2-0, boosting output multiplying factor (BT3-0).
R04h	Power control (2)	0	1	CAD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Sets the configuration of retention bolume (CAD).
R05h	Entry mode	0	1	DIT	0	0	BGR	0	0	HWM	0	0	0	VD1	VD0	AM	LG2	LG1	LG0	Specifies the logical operation (LG2-0), AC counter mode (AM), increment/decrement mode (I/D1-0), high-speed-wirite mode (HWM),BGR mode, and hard dither mode (DIT).
R06h	Compare register	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	Sets the compare regiser (CP15-0).
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0	Specifies display on (D1-0), reversed display (REV), number of display colors (CL), DISPTMG enable (DTE), gate output on (GON), screen division driving (ST/PT)), and verticla scrol (VLE2-1), and source output condition (PT1-0).
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0	Sets the 1H period (RTN3-0) and operating clock grequency-division ratio (DV1-0), the equalizing period (EQ1-0), delay volume of the source output (STD1-0), non-overlap volume of the gate output (NO1-0).
R0Ch	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0	Sets an adjustment factor for the Vci voltage (VC2-0).
R0Dh	Power control (4)	0	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0	Sets the amplification factor for VREGOUT1 voltage (VRH4-0) and for VREGOUT2 voltage (VRL3-0). Step-up circuit 3 starts operation (VCM4-0).
R0Eh	Power control (5)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0	Sets VcomH voltage (VCM4-0), AC-cycle oscillation of Vcom and Vgoff (VDV4-0) and voltage fo VCOM (VCOMG).
R0Fh	Gate scan starting position	0	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0	Sets the scanning starting position (SCN4-0) of the gate driver.
R11h	vertical scroll control	0	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Specifies the screen display scroll volume (VL7-0).
R14h	First display drive position	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	Sets 1st-screen driving start (SS17-10) and end (SE17-10).
R15h	Second display drive position	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	Sets 2nd-screen driving start (SS27-10) and end (SE27-10).
R16h	Horizontal RAM address position	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	Sets the start (HSA7-0) and end (HEA7-0) of the horizontal RAM address
R17h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	Sets the start (VSA7-0) and end (VEA7-0) fo the vertical RAM address range.
R20h	RAM write data mask	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	Specifies write data mask (WM15-0) at RAM write.
R21h	RAM address set	0	1	AD15-8 (Upper)								AD7-0 (Lower)								Initially sets the RAM address to the address counter (AC).
R22h	RAM data write	0	1	Write Data (Upper)								Write Data (Lower)								Write data to RAM.
	RAM data read	1	1	Read Data (Upper)								Read Data (Lower)								Read data to RAM.
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00	Adjust the Gamma control.
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20	Adjust the Gamma control.
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40	Adjust the Gamma control.
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00	Adjust the Gamma control.
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00	Adjust the Gamma control.
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN02	PKN20	Adjust the Gamma control.
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40	Adjust the Gamma control.
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00	Adjust the Gamma control.
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	PRP 12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00	Adjust the Gamma control.
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN 12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00	Adjust the Gamma control.

Note1: "*" means "Don't care".
Note2: High-speed write mode is available only for RAM write.

Reset Function

The HD66773 is internally initialized by RESET input. While resetting, inside of HD66773 is busy and it does not accept instructions from MPU or data access from GRAM. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4–0 = “10101”, SS = “0”, CS = “0”)
3. LCD driving AC control (FLD1-0 = “01”, B/C = “0”, EOR = “0”, NW5–0 = “00000”)
4. Power control 1 (BT2-0 = “000”, DC2–0 = “000”, AP2–0 = “000”: LCD power off, SLP = “0”, STB = “0”: Standby mode off)
5. Power control 2 (CAD = “0”)
6. Entry mode set (DIT = “0”, BGR = “0”, HWM = “0”, I/D1-0 = “11”: Increment by 1, AM = “0”: Horizontal move, LG2–0 = “000”: Replace mode)
7. Compare register (CP15–0: “0000000000000000”)
8. Display control (PT1-0 = “00”, VLE2–1 = “00”: No vertical scroll, SPT = “0”, GON = “0”, DTE = “0”, CL = “0”: 260,000 color mode, REV = “0”, D1–0 = “00”: Display off)
9. Frame cycle control (NO1-0 = “00”, SDT1-0 = “00”, EQ1-0 = “00”: no equalizer, DIV1-0 = “00”: 1-divided clock, RTN3-0 = “0000”: 16 clock cycle in 1H period)
10. Power control 3 (VC2-0 = “000”)
11. Power control 4 (VRL3-0 = “0000”, PON= “0”, VRH3-0= “00000”)
12. Power control 5 (VCOMG = “0”, VDV4-0 = “00000”, VCM4-0 = “00000”
13. Gate scanning starting position (SCN4-0 = “00000”)
14. Vertical scroll (VL7–0 = “0000000”)
15. 1st screen division (SE17-10 = “11111111”, SS17-10 = “00000000”)
16. 2nd screen division (SE27-20 = “11111111”, SS27-20 = “00000000”)
17. Horizontal RAM address position (HEA7-0 = “10000011”, HSA7-0 = “00000000”)
18. Vertical RAM address position (VEA7-0 = “10101111”, VSA7-0 = “00000000”)
19. RAM write data mask (WM15–0 = “0000H”: No mask)
20. RAM address set (AD15–0 = “0000H”)
21. Gamma control
    (PKP02–00 = “000”, PKP12–10 = “000”, PKP22–20 = “000”, PKP32–30 = “000”,
    PK42–40 = “000”, PKP52–50 = “000”, PRP02–00 = “000”, PRP12–10 = “000”)
    (PKN02–00 = “000”, PKN12–10 = “000”, PKN22–20 = “000”, PKN32–30 = “000”,
    PKN42–40 = “000”, PKN52–50 = “000”, PRN02–00 = “000”, PRN12–10 = “000”)
    (VRP03-00 = “0000”, VRP14-10 = “0000”, VRN03-00 = “0000”, VRN14-10 = “0000”)

GRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D1–0 = 00).

Output Pin Initialization:

1. LCD driver output pins (Source output): Output GND level
   LCD driver output pins (Gate outputs): Output VGH level
2. Oscillator output pin (OSC2): Outputs oscillation signal

System Interface

The following interfaces are available as system interface. It is determined by setting bits of IM3-0. Instructions and RAM accesses can be performed via the system interface.

Table 31 IM bits

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin
0	0	0	0	68-system 16-bit interface	DB17 to 10, 8 to 1
0	0	0	1	68-system 8-bit interface	DB17 to 10
0	0	1	0	80-system 16-bit interface	DB17 to 10 8 to 1
0	0	1	1	80-system 8-bit interface	DB17 to 10
0	1	0	*	Clocked serial peripheral interface (SPI)	DB1 to 0
0	1	1	*	Setting inhibited	—
1	0	0	0	68-system 18-bit interface	DB17-0
1	0	0	1	68-system 9-bit interface	DB17-9
1	0	1	0	80-system 18-bit interface	DB17-0
1	0	1	1	80-system 9-bit interface	D17-9
1	1	*	*	Setting inhibited	—

1) 18-bit Bus Interface

Setting the IM3/2/1/0 (interface mode) to the Vcc/GND/GND/GND level allows 68-system 18-bit parallel data transfer. Setting the IM3/2/1/0 to the Vcc/GND/Vcc/GND level allows 80-system 18-bit parallel data transfer. Only in write mode these data transfer is valid.

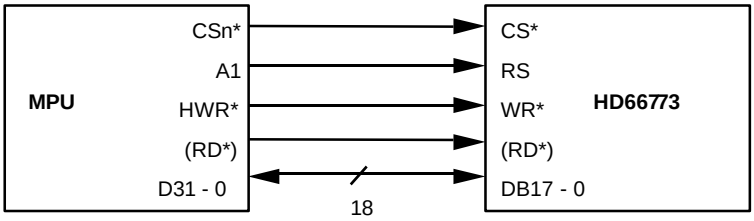


Figure 49 18-bit microcomputer and interface

Data format for 18-bit interface

Instruction

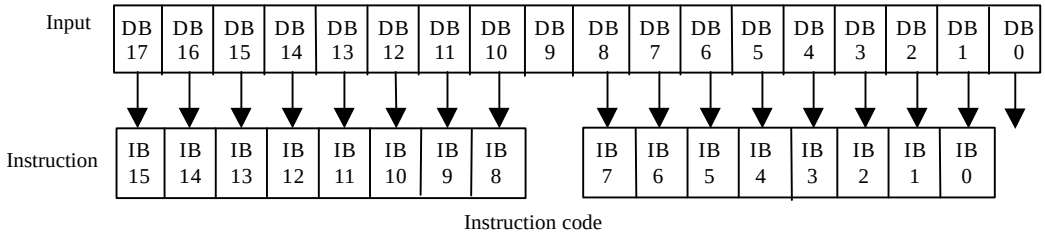
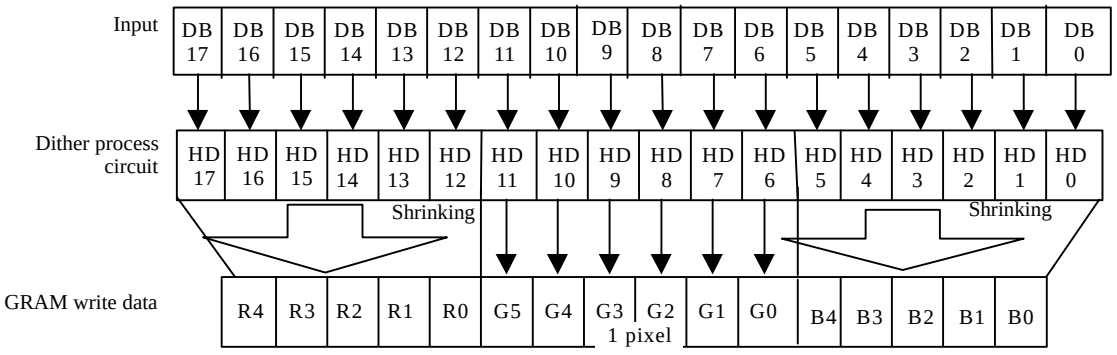


Figure 50

RAM data write



Note: With 18-bit system interface, 262,144 colors display is available when DIT bit is set "1".

Figure 51

2) 16-bit Bus Interface

Setting the IM3/2/1/0 (interface mode) to the GND/GND/GND/GND level allows 68-system 18-bit parallel data transfer. Setting the IM3/2/1/0 to the GND/GND/Vcc/GND level allows 80-system 16-bit parallel data transfer.

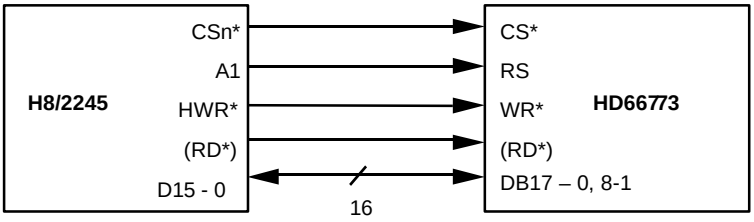


Figure 52 16-bit microcomputer and interface

Data format for 16-bit interface

Instruction

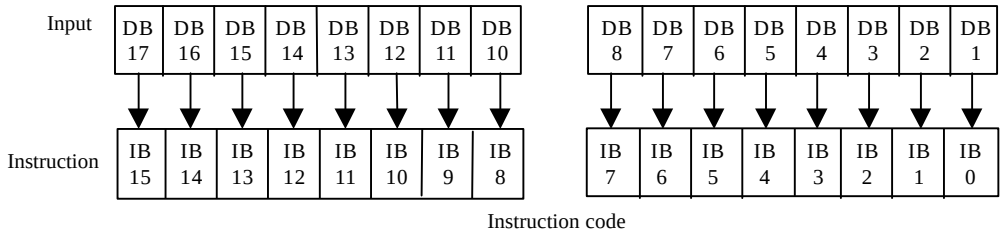
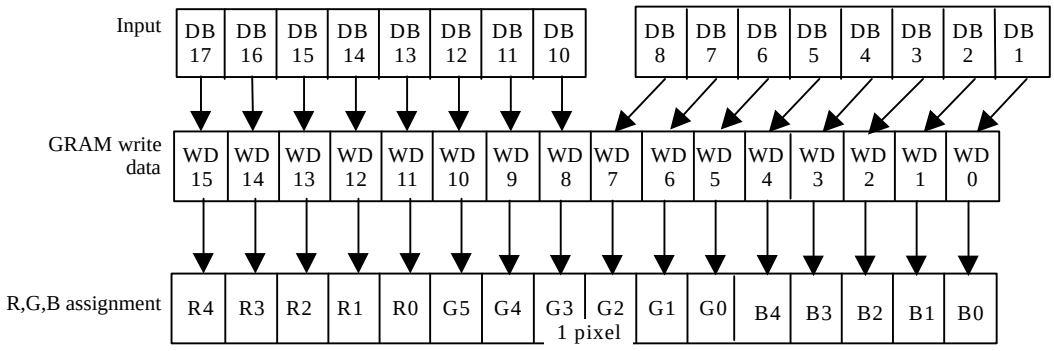


Figure 53

RAM data write



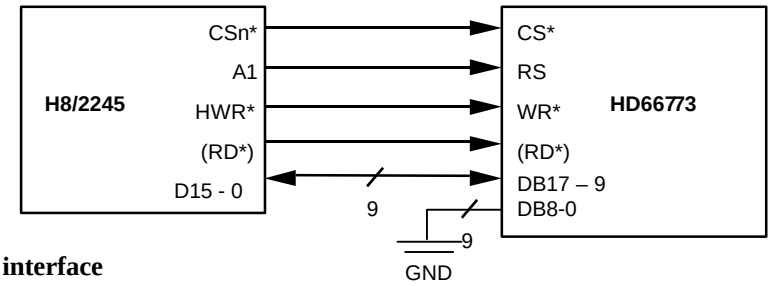
Note: With 16-bit system interface, real 65,536 color display is available.
Do not set DIT bit = "1".

Figure 54

3) 9-bit Bus Interface

Setting the IM3/2/1/0 to the Vcc/GND/GND/Vcc level allows 68-system 9-bit parallel data transfer using pins DB17–DB9. Setting the IM3/2/1/0 to the Vcc/GND/Vcc/Vcc level allows 80-system 9-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB8–DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register is written to. This transfer mode is available only for write mode.

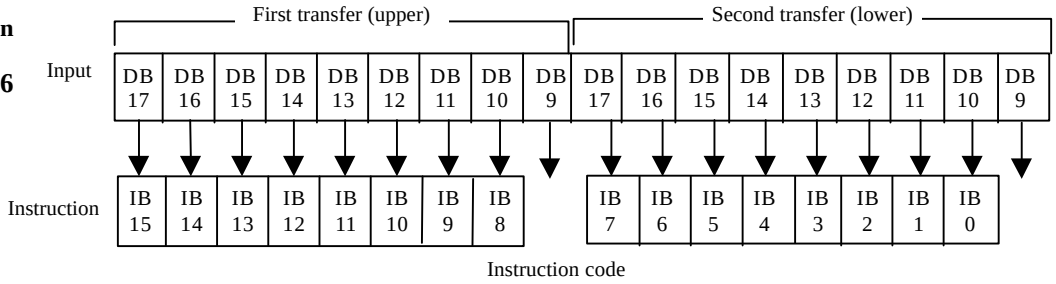
Figure 55



Data format for 9-bit interface

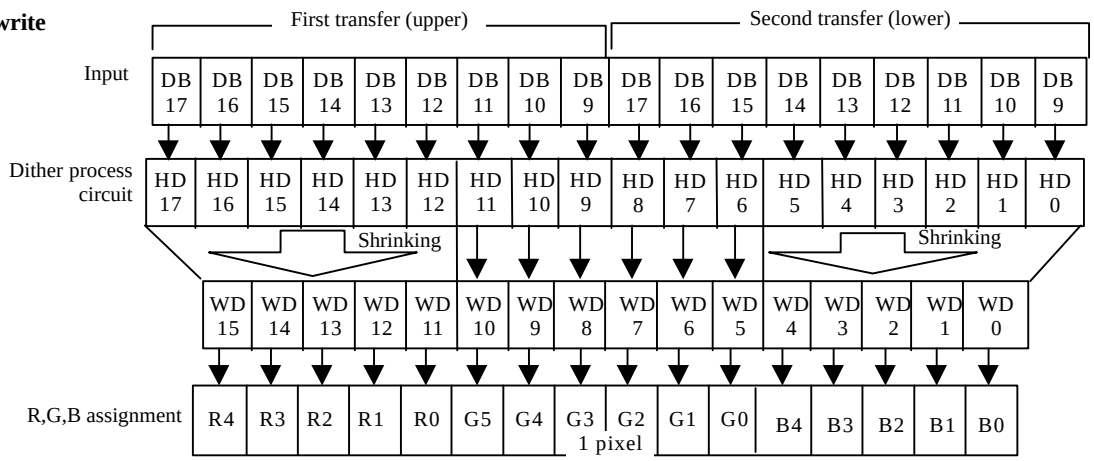
Instruction

Figure 56



RAM data write

Figure 57

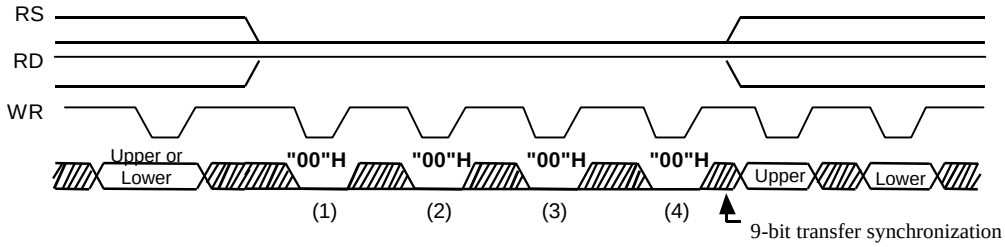


Note: With 9-bit system interface, real 262,144 color display is available.
Set DIT bit = "1".

Note: Transfer synhronization function for an 9-bit bus interface

The HD66773 supporrts the transfer synchronization function that resets the upper/lower counter to count upper/lower 9-bit data transfer in the 9-bit interface. Noise causing transfer mismatch between the upper/ lower bits can be corrected by a reset triggered by consecutively writing a "00"H instruction four times. The next transfer starts from the upper 9 bits. Executing synchronizationn function periodically can recover any runaway in the display system.

Figure 58



4) 8-bit Bus Interface

Setting the IM3/2/1/0 to the GND/GND/GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB17–DB10. Setting the IM3/2/1/0 to the GND/GND/Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB9–DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register is written to.

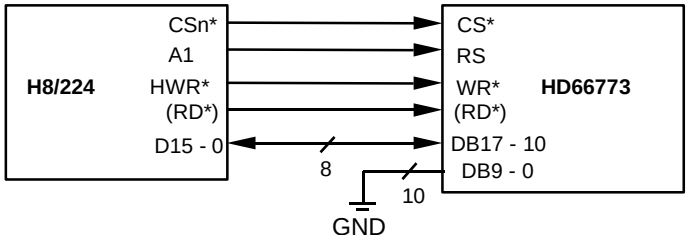
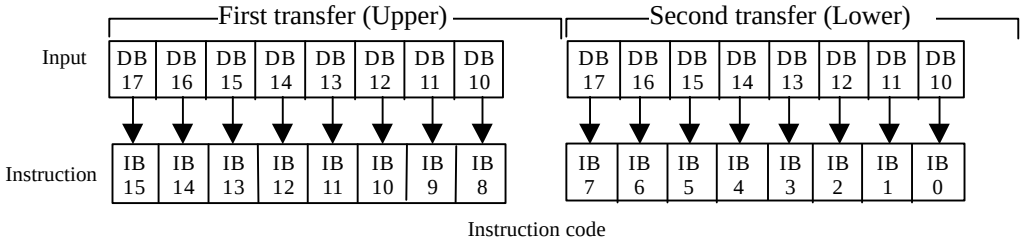


Figure 59 Interface to 8-bit Microcomputer

Data format for 8-bit interface

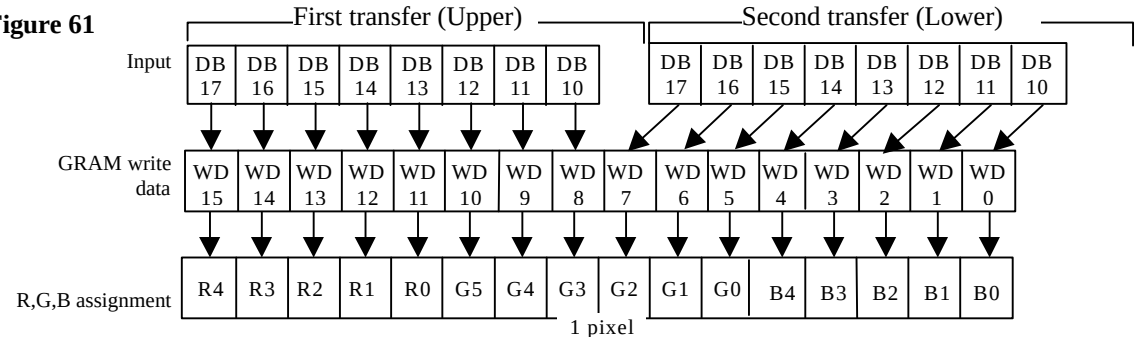
Instruction

Figure 60



RAM data write

Figure 61

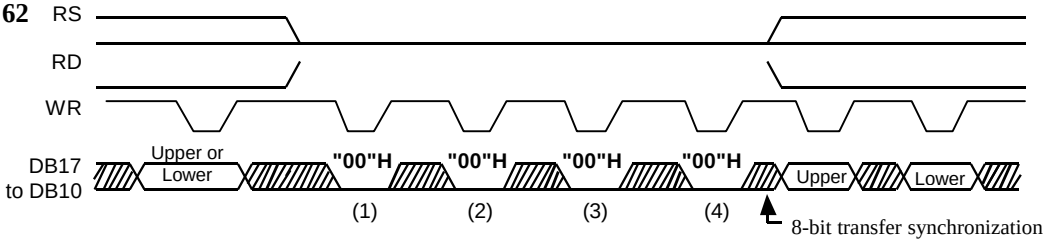


Note: With 8-bit system interface, real 65,536 colors display is available.
Do not set DIT bit = "1".

Note: Transfer synchronization function for an 8-bit bus interface

The HD66773 supports the transfer synchronization function that resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

Figure 62



Clock synchronized serial interface (SPI)

Setting the IM3/2/1 to the GND/Vcc/DNF level allows clock-synchronized serial data (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB17-2 pins which are not used must be fixed at Vcc or GND.

The HD66773 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66773 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66773. The HD66773, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be “01110”. Two different chip addresses must be assigned to a single HD66773, because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = “0”, data can be written to the index register or status can be read, and when RS = “1”, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the HD66773 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All HD66773 instructions are 16 bits. Two bytes are received with the MSB first (DB15 to 0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction.

Four bytes of RAM read data after the start byte are invalid. The HD66773 starts to read correct RAM data from the fifth byte.

Table 32 Start Byte Format

Transfer Bit	**S**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

Table 33 RS and R/W Bit Function

RS	**R/W**	**Function**
0	0	Sets index register
0	1	Reads status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

Data format for serial interface

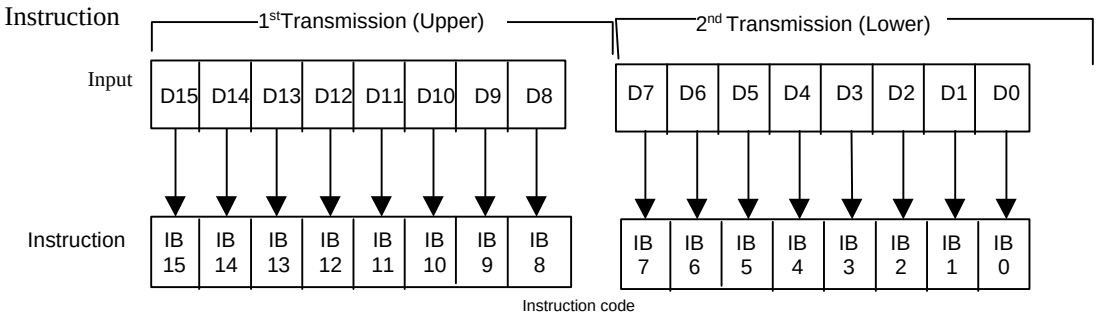
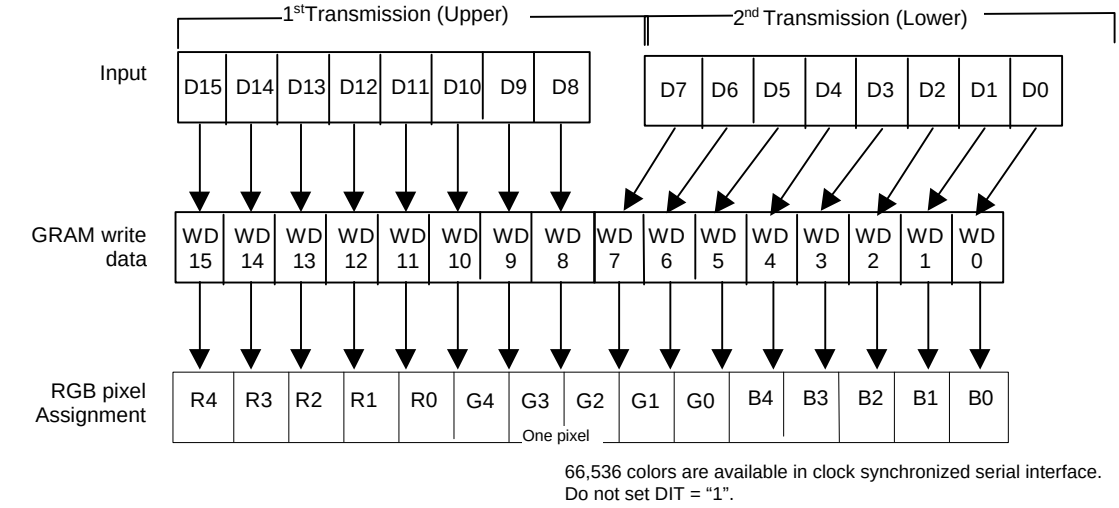


Figure63

RAM data write



66,536 colors are available in clock synchronized serial interface.
Do not set DIT = “1”.

Figure 64

a) Timing Basic Data Transfer through Clock Synchronized Serial Bus Interface

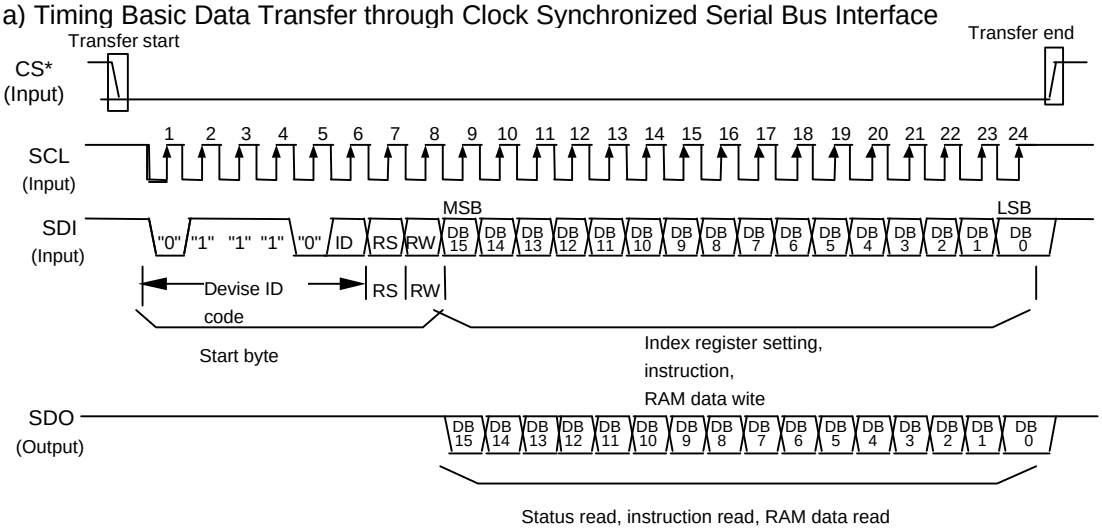
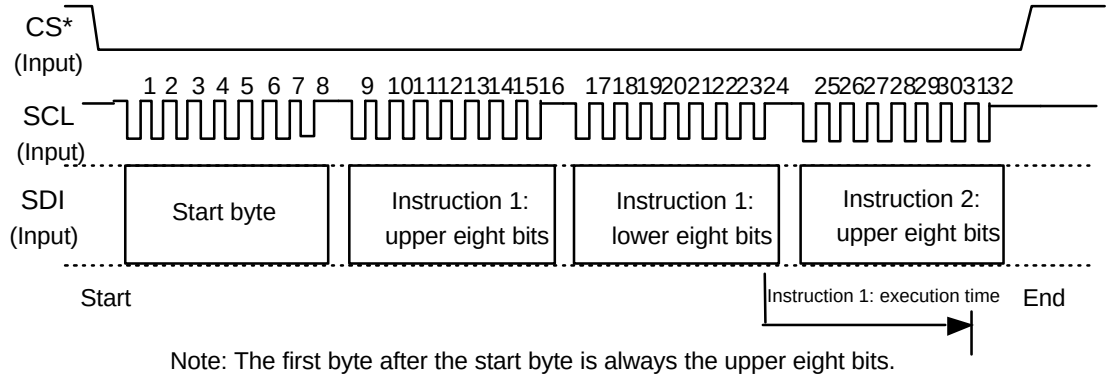


Figure 65

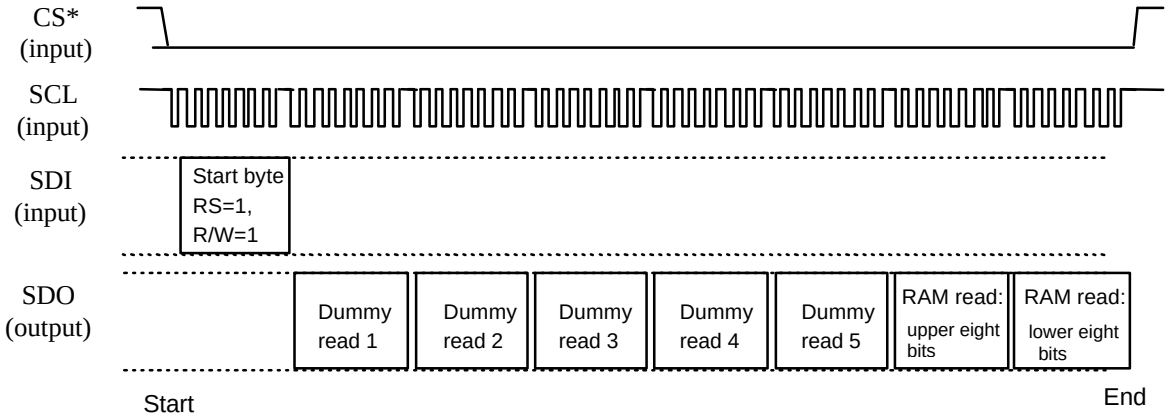
b) Timing of Consecutive Data-Transfer through Clock-synchronized serial Bus Interface



Note: The first byte after the start byte is always the upper eight bits.

Figure 66

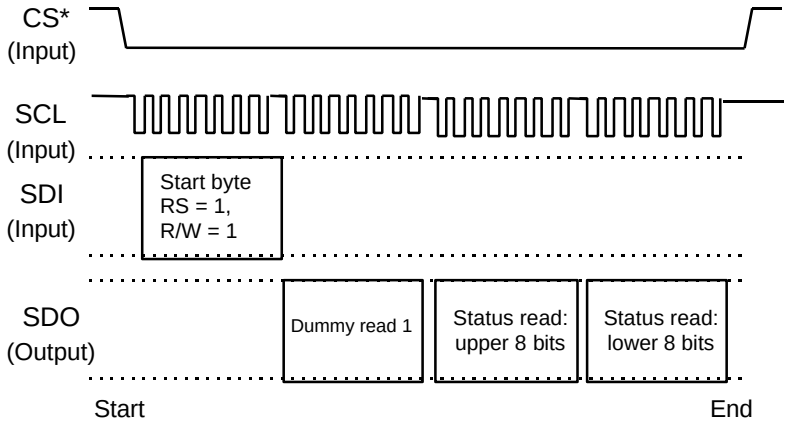
c) RAM-Data Read-Transfer Timing



Note: Five bytes of the RAM read data after the start byte are invalid. The HD66773 starts to read the correct RAM data from the sixth byte.

Figure 67

d) Status Read / Instruction Read



Note: Two byte of the read data after the start byte is invalid.
The HD66773 starts to read the correct data from the second byte.

Figure 68: Procedure for Transfer on Clock-Synchronized Serial Bus Interface (2)

High-Speed Burst RAM Write Function

The HD66773 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications that require the high-speed rewriting of the display data, for example, display of color animations, etc.

When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the HD66773 internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

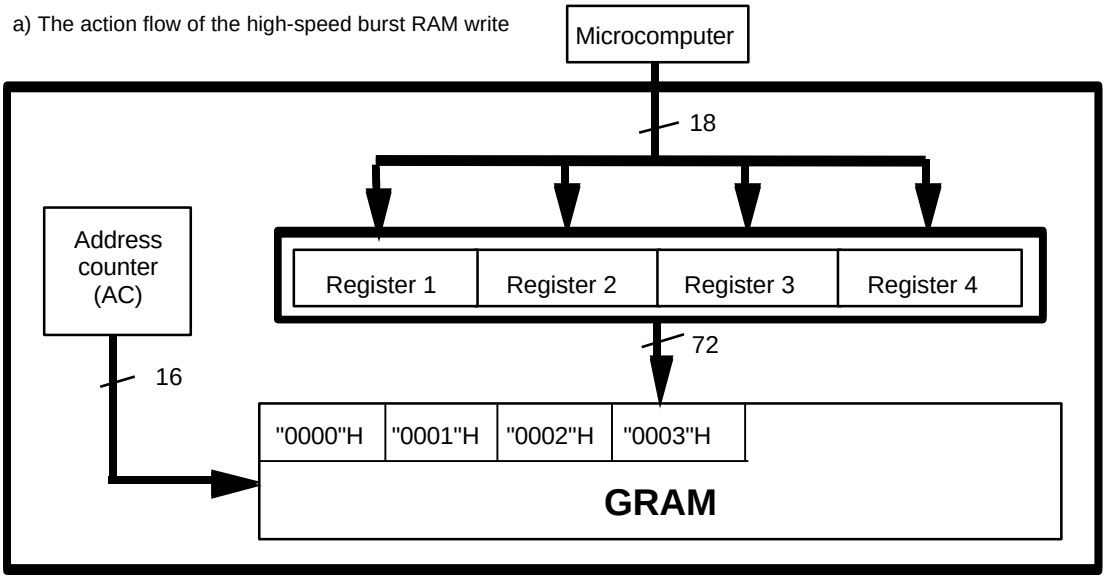
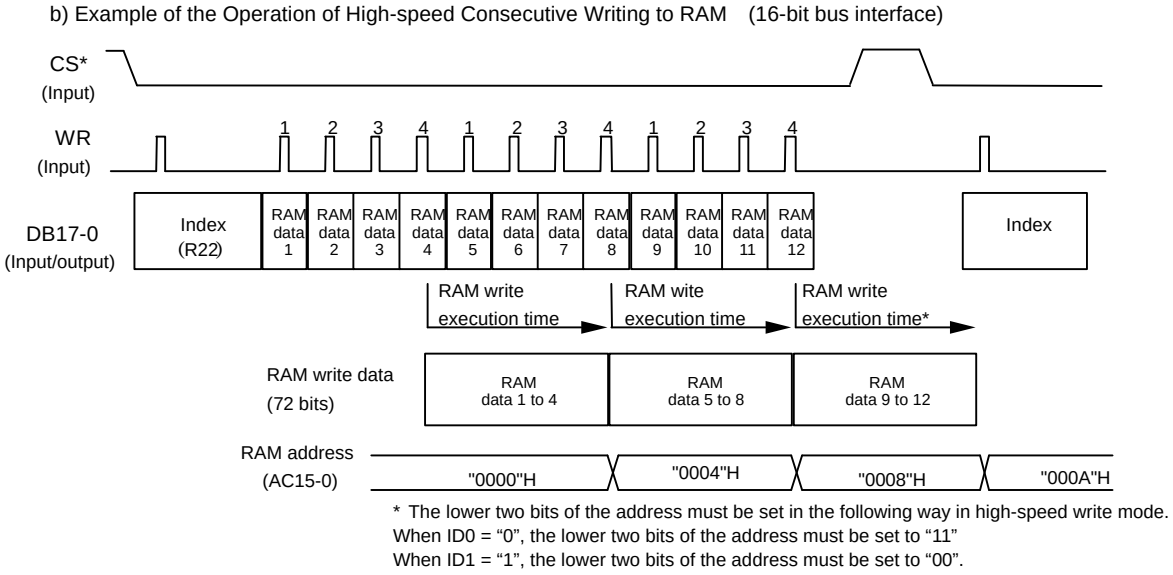


Figure 69 Flow of Operation in High-Speed Consecutive Writing to RAM

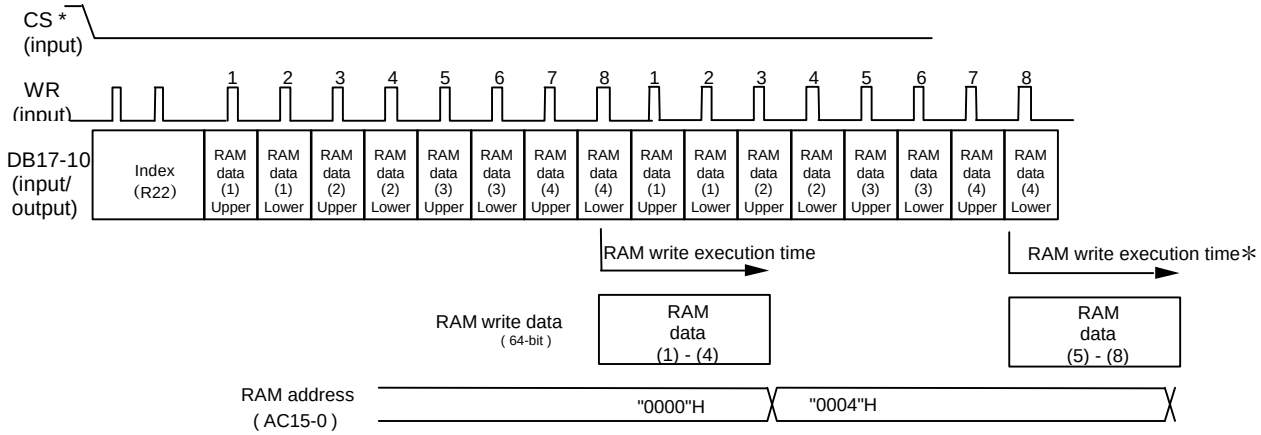


* The lower two bits of the address must be set in the following way in high-speed write mode.
When ID0 = "0", the lower two bits of the address must be set to "11"
When ID1 = "1", the lower two bits of the address must be set to "00".

Note: When a high-speed RAM write is canceled, the next instruction must only be executed after the RAM write execution time has elapsed.

Figure 70

C) Example of the Operation of High-Speed Consecutive Writing to RAM (8-bit bus interface)



* The lower two bits of the address must be set in the following way in high-speed write mode.
When ID0 = “0”, the lower two bits of the address must be set to “11”.
When ID1 = “0”, the lower two bits of the address must be set to “00”.

By using high-speed burst RAM write function, data is written to RAM each four words. Therefore when using 8-bit bus interface, data will be stored 8 times to internal register before written to RAM

Figure 71

When high-speed RAM write mode is used, note the following.

Notes: 1. The logical and compare operations cannot be used.

2. Data is written to RAM each four words. When an address is set, the lower two bits in the address must be set to the following values.

   *When ID0 = "0", the lower two bits in the address must be set to "11" and be written to RAM.

   *When ID0 = "1", the lower two bits in the address must be set to "00" and be written to RAM.

3. Data is written to RAM each four words. If less than four words of data is written to RAM, the last data will not be written to RAM.
4. When the index register and RAM data write (R22h) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to "0" while RAM is being read.
5. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.
6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

Table 34 Comparison between Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM = "0")	**High-Speed RAM Write (HWM = "1")**
Logical operation function	Can be used (Available only with 8-16-bit interface)	Cannot be used
Compare operation function	Can be used (Available only with 8-/16-bit interface)	Cannot be used
BGR function	Can be used	Can be used
Write mask function	Can be used (Available only with 8-/16-bit interface)	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word (Available only with 8-/16-bit interface)	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address-range specification
Window address	Can be set by word	Horizontal area (HAS/HSE): more than four words The number of horizontal writing: 4 x n times (N>2)
External display interface	Can be used	Can be used
AM setting	AM = 1/0	AM = 0

High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become 4N as shown in the tables below.
Dummy write operations may have to be inserted as the first and last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). Number of dummy write operations of a row must be 4N.

Table 35 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

HSA1	HSA0	Number of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2
1	1	3

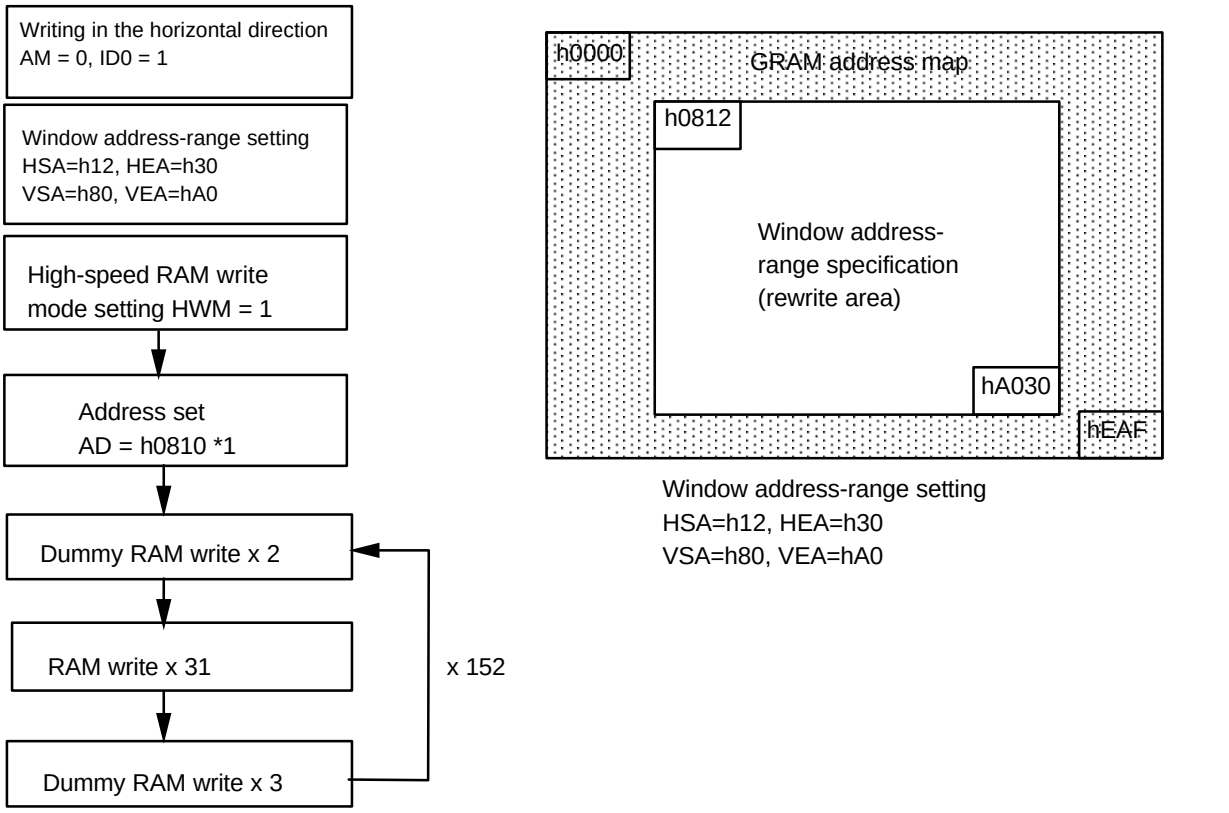
Table 36 Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

HEA1	HEA0	Number of Dummy Write Operations to be Inserted at the End of a Row
0	0	3
0	1	2
1	0	1
1	1	0

Each row of access must consist of $4 \times N$ operations, including the dummy writes.
Horizontal access count =first dummy write count + write data count + last dummy write count = $4 \times N$

An example of high-speed RAM write with a window address-range specified is shown below.

The window address-range can be rewritten to consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1 to 0=10, HEA1 to 0=00).



Note: The address set for the high-speed RAM write must be “00” or “11” according to the value of the ID0 bit. Only RAM in the specified window address-range will be over written.

Figure 72: Example of the High-Speed RAM Write with a Window Address-Range Specification

Window Address Function

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA7-0) or the vertical address register (start: VSA7-0, end: VEA7-0) can be written to consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.

The window must be specified to be within the GRAM address area described below. Addresses must be set within the window address.

[Restriction on window address-range settings]
(horizontal direction) “00”H ≤ HSA7-0 ≤ HEA7-0 ≤ “83”H
(vertical direction) “00”H ≤ VSA7-0 ≤ VEA7-0 ≤ “AF”H
[Restriction on address settings during the window address]
(RAM address) HSA7 to 0 ≤ AD7-0 ≤ HEA7-0
VSA7-0 ≤ AD15-8 ≤ VEA7-0
Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.
ID0=0: The lower two bits of the address must be set to “11”.
ID0=1: The lower two bits of the address must be set to “00”.

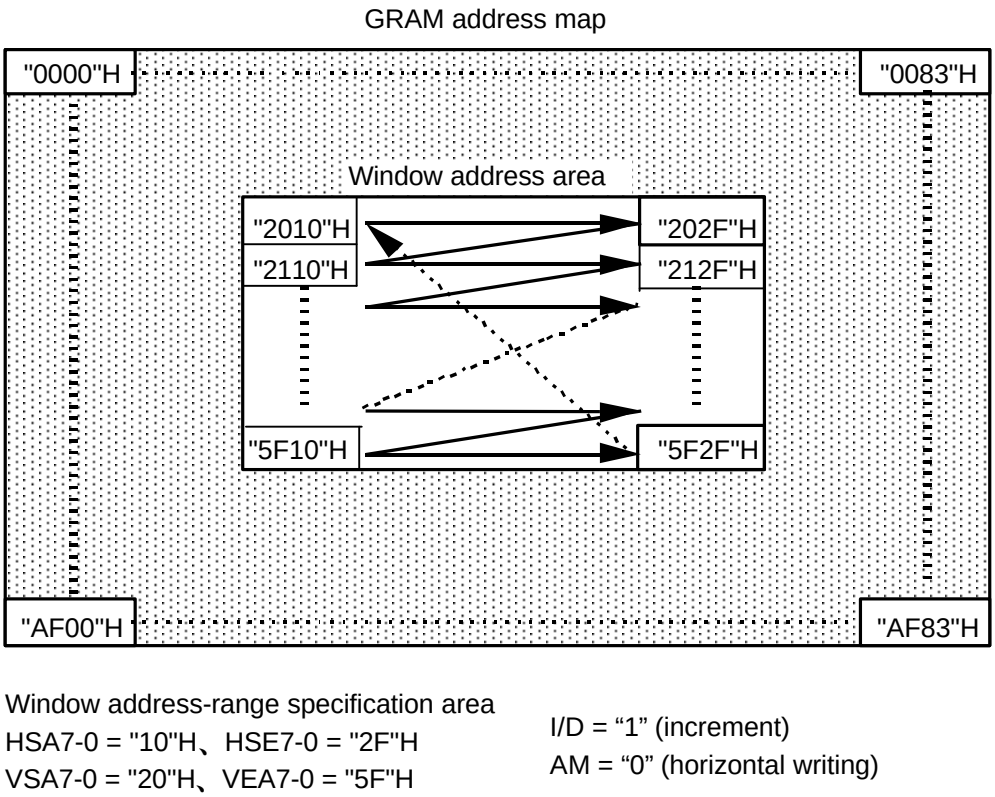


Figure 73 Example of Address Operation in the Window Address Specification

Graphics Operation Function

The HD66773 can greatly reduce the load of the microcomputer graphics software processing through the internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
2. A logical operation writes function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
3. A conditional write function that compares the original RAM data or write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match. Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten. The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Table 37 Graphics Operation

	Bit Setting			
Operation Mode	**I/D**	**AM**	**LG2–0**	**Operation and Usage**
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001 010 011	Horizontal data write with logical operation, horizontal-border drawing
Read/write mode 2	0/1	1	001 010 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100 101	Conditional horizontal data replacement, horizontal-border drawing
Read/write mode 4	0/1	1	100 101	Conditional vertical data replacement, vertical-border drawing

Note: When using 18-/9-bit bus interface, only write mode 1 and 2 are available.
When using 16-/8-bit bus interface, all the operation modes are usable.

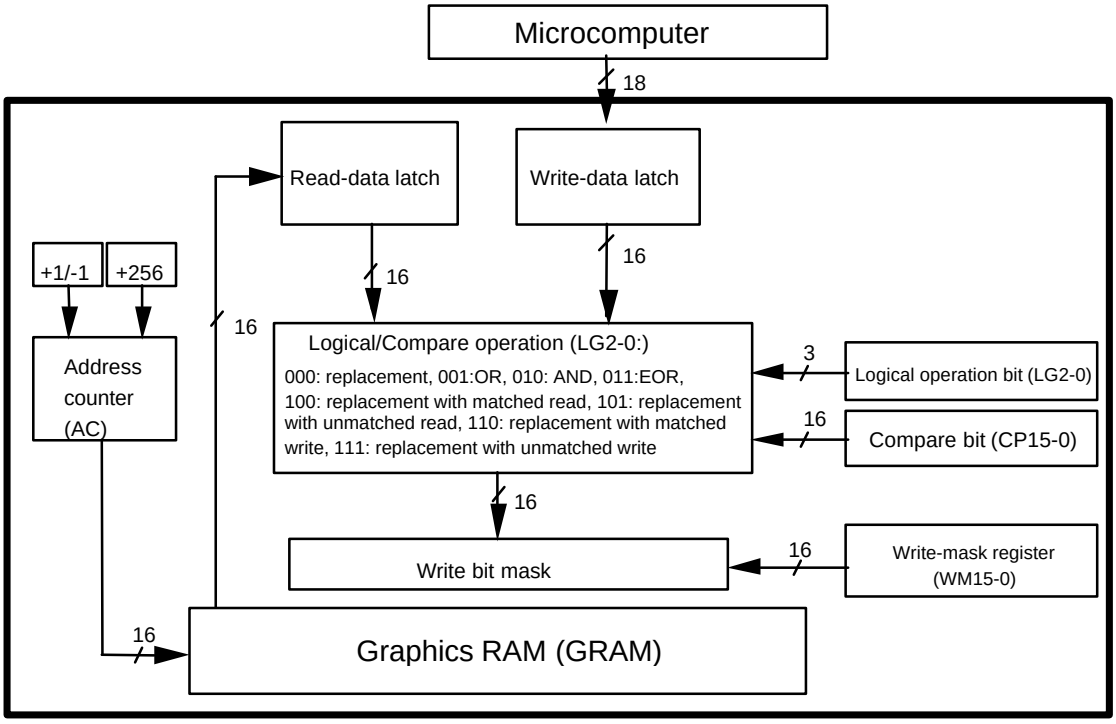
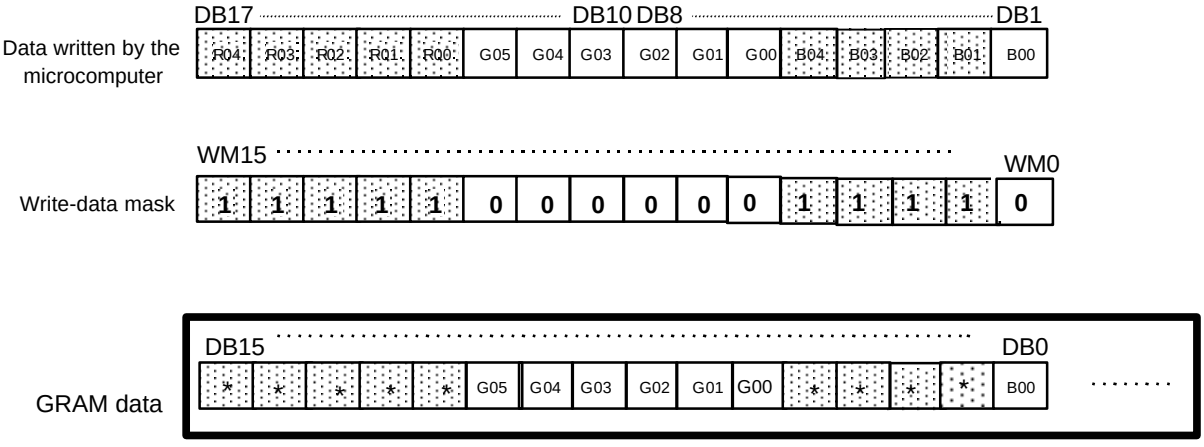


Figure 74 Data Processing Flow of the Graphic Operation

Write-data Mask Function

The HD66773 has a bit-wise write-data mask function that controls writing the 16-bit data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM15–0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.



Note) Write data function is available only when using 8-/16-bit system interface.

Figure 75 Example of Write-data Mask Function Operation

Graphics Operation Processing

1. Write mode 1: AM = “0”, LG2–0 = “000”

   This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = “1”) or decrements by 1 (I/D = “0”), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

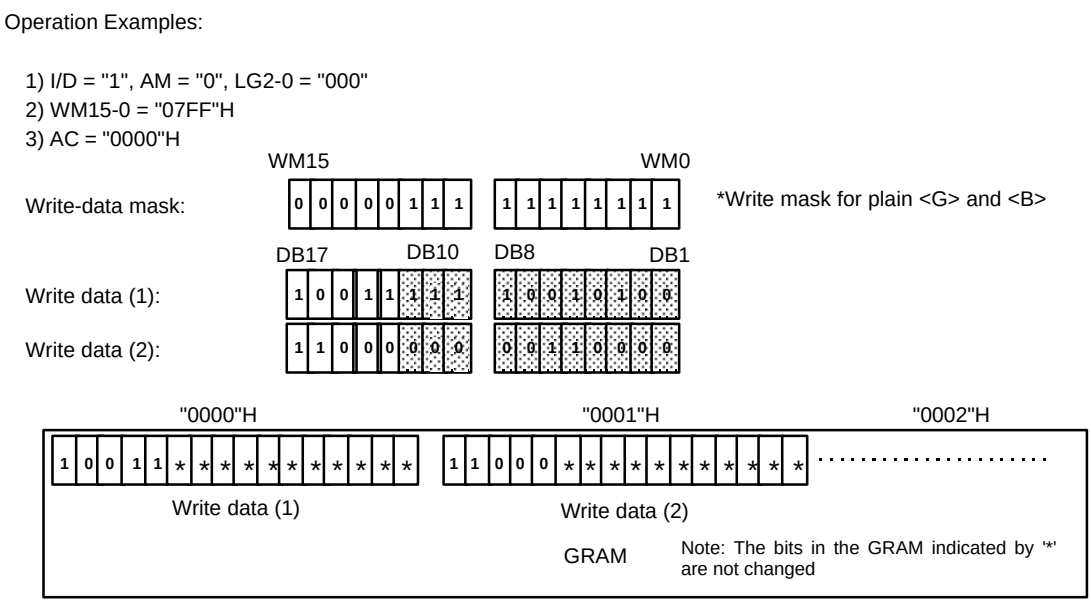


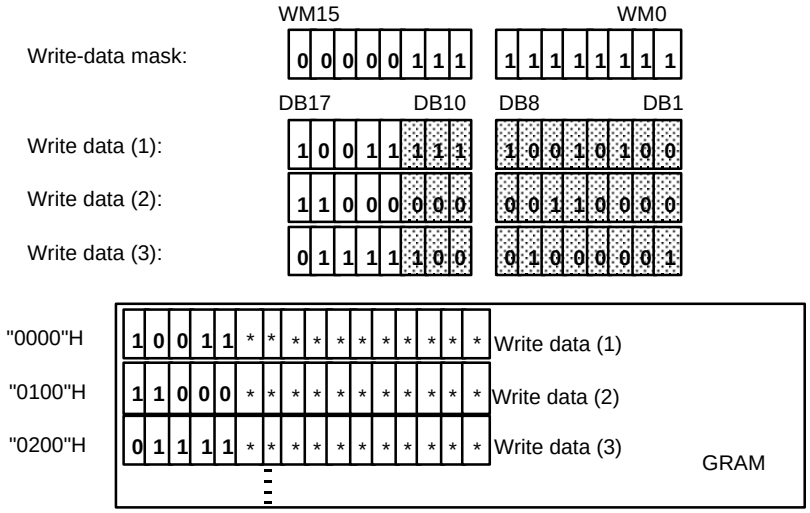
Figure 76 Writing Operation of Write Mode 1

2. Write mode 2: AM = “1”, LG2–0 = “000”

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM11–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = “1”) or upper-left edge (I/D = “0”) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I/D = "1", AM = "1", LG2-0 = "000"
2) WM15-0 = "07FF"H
3) AC = "0000"H



Note: 1. The bits in the GRAM indicated by '*' are not changed.
2. After writing to address "AF00"H, the AC jumps to "000"H.

Figure 77 Writing Operation of Write Mode 2

3. Write mode 3: AM = “0”, LG2–0 = “110”/”111”

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP15–0). When the result of the comparison in a word unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM15–0) is also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = “1”) or decrements by 1 (I/D = “0”), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

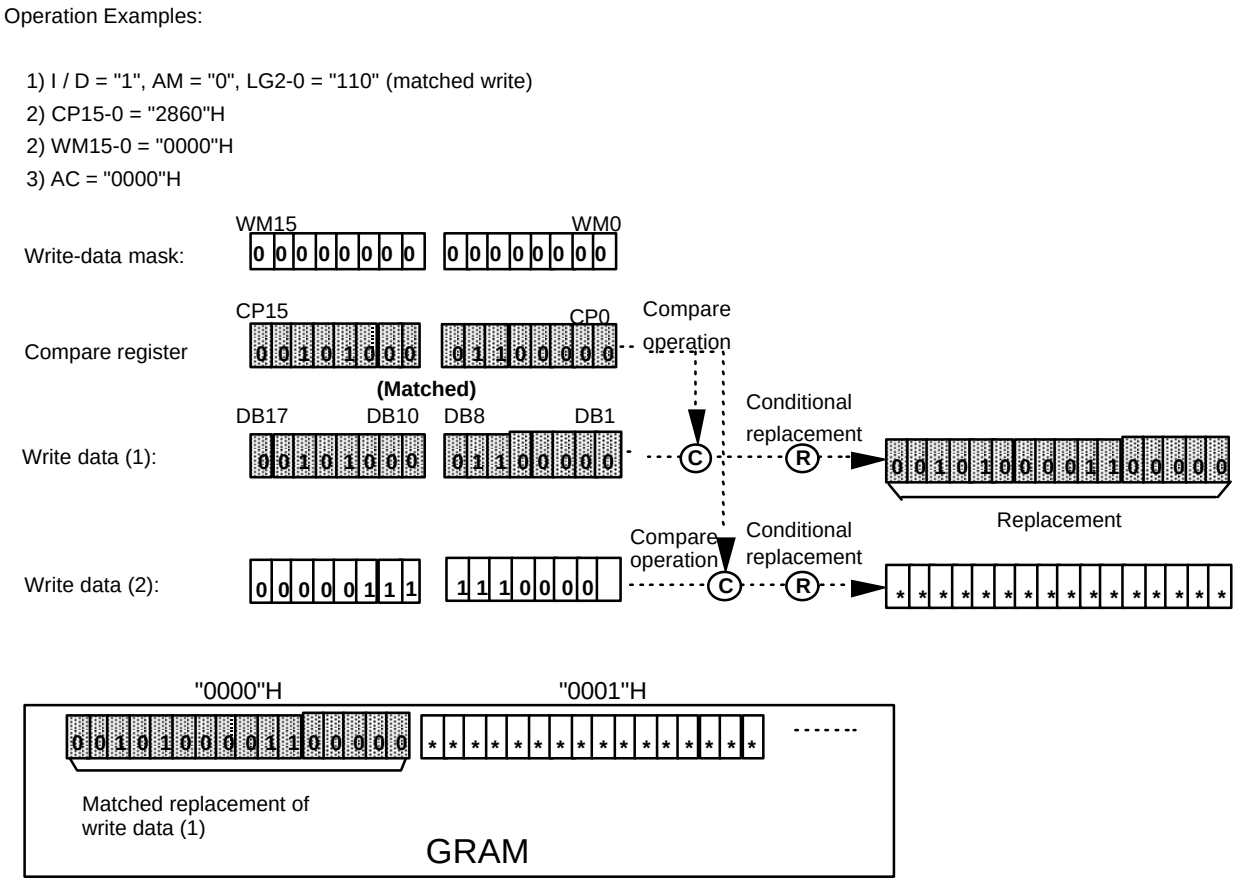


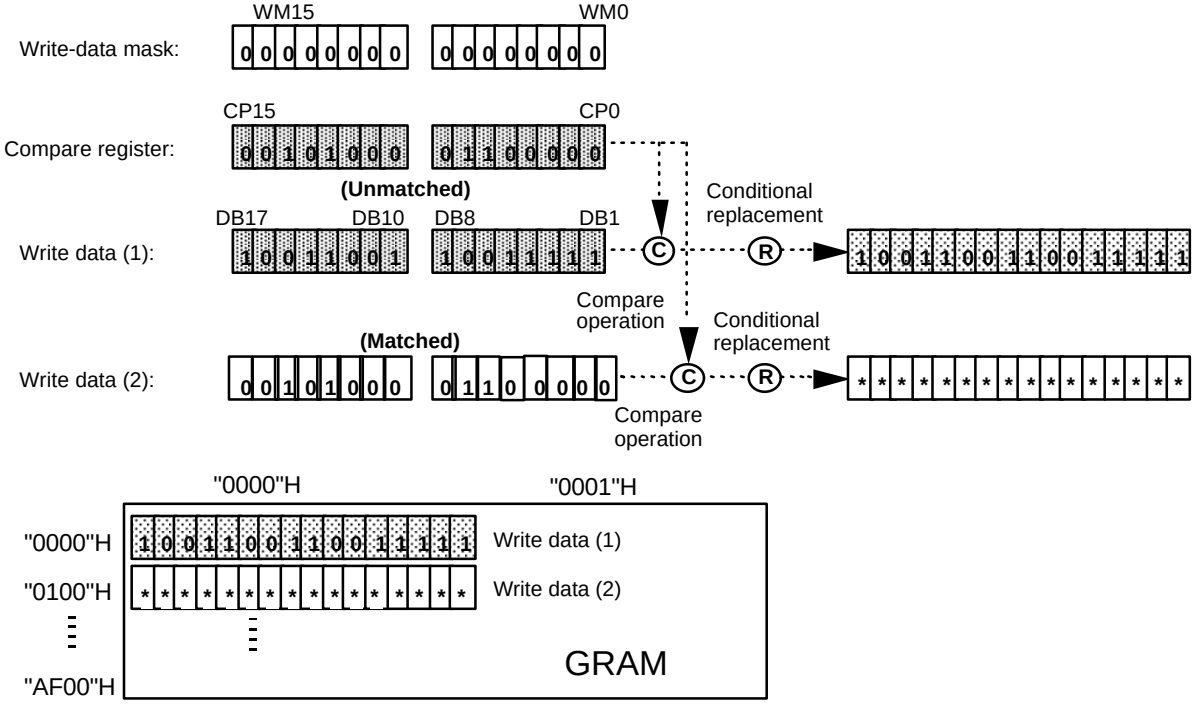
Figure 78 Writing Operation of Write Mode

4. Write mode 4: AM = “1”, LG2–0 = “110”/ “111”

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP15–0) to write the data. When the result by the comparison in a word unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM15–0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = “1”) or upper-left edge (I/D = “0”) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I/D = "1", AM = "1", LG2-0 = "111" (unmatched write)
2) CP15-0 = "2860"H
2) WM15-0 = "0000"H
3) AC = "0000"H



Note: 1. The bits in the GRAM indicated by '*' are not changed.
2. After writing to address "AF00"H, the AC jumps to "0001"H.

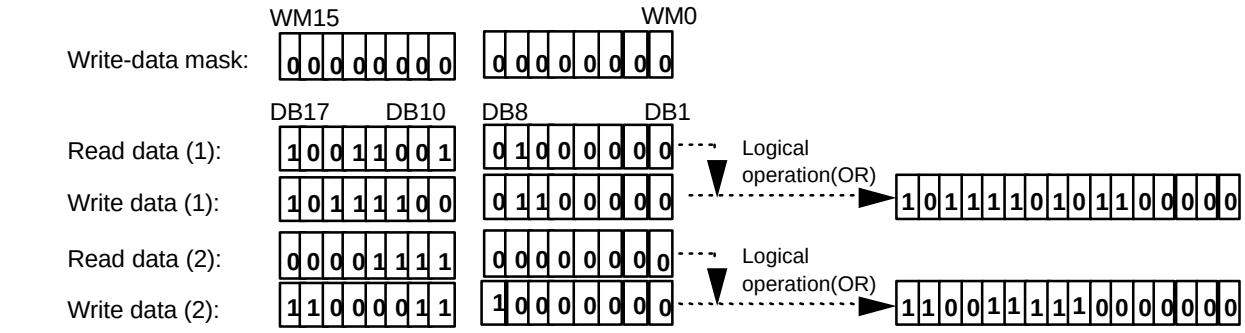
Figure 79 Writing Operation of Write Mode 4

5. Read/Write mode 1: AM = “0”, LG2–0 = “001”/ “010” / “011”

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = “1”) or decrements by 1 (I/D = “0”), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

Operation Examples:

1) I/D = "1", AM = "0", LG2-0 = "001"(OR)
2) WM15-0 = "0000"H
3) AC = "0000"H



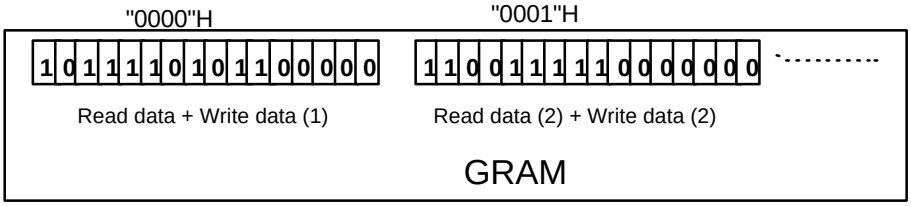
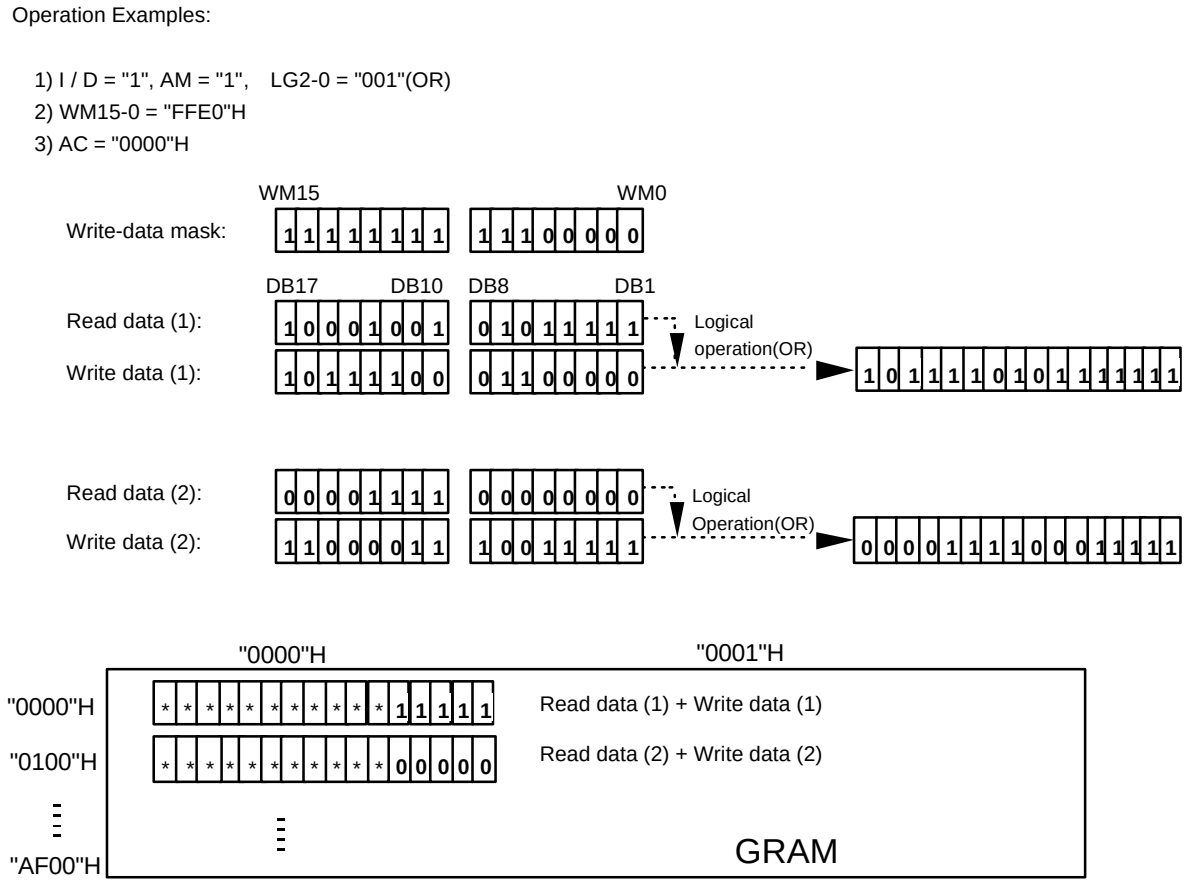


Figure 80 Writing Operation of Read/Write Mode 1

6. Read/Write mode 2: AM = “1”, LG1–0 = “001”/ “010” / “011”

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode can read the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = “1”) or upper-left edge (I/D = “0”) following the I/D bit after it has reached the lower edge of the GRAM.



Note: 1. The bits in the GRAM indicated by '*' are not changed.
2. After writing to address "AF00"H, the AC jumps to "0001"H.

Figure 81 Writing Operation of Read/Write Mode 2

7. Read/Write mode 3: AM = 0, LG2–0 = “100”/”101”

This mode is used when the data is horizontally written by comparing the original data and the set value of compare register (CP15–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = “1”) or decrements by 1 (I/D = “0”), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

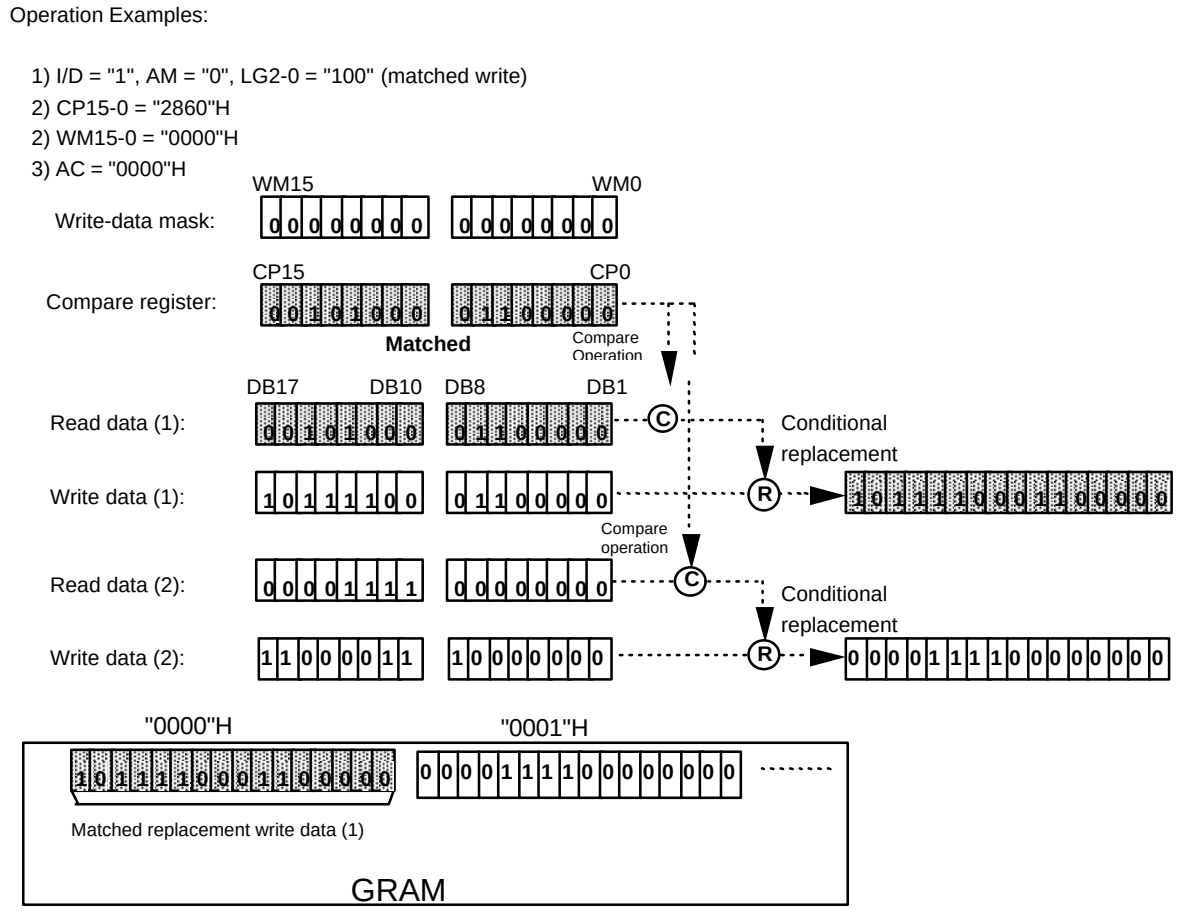


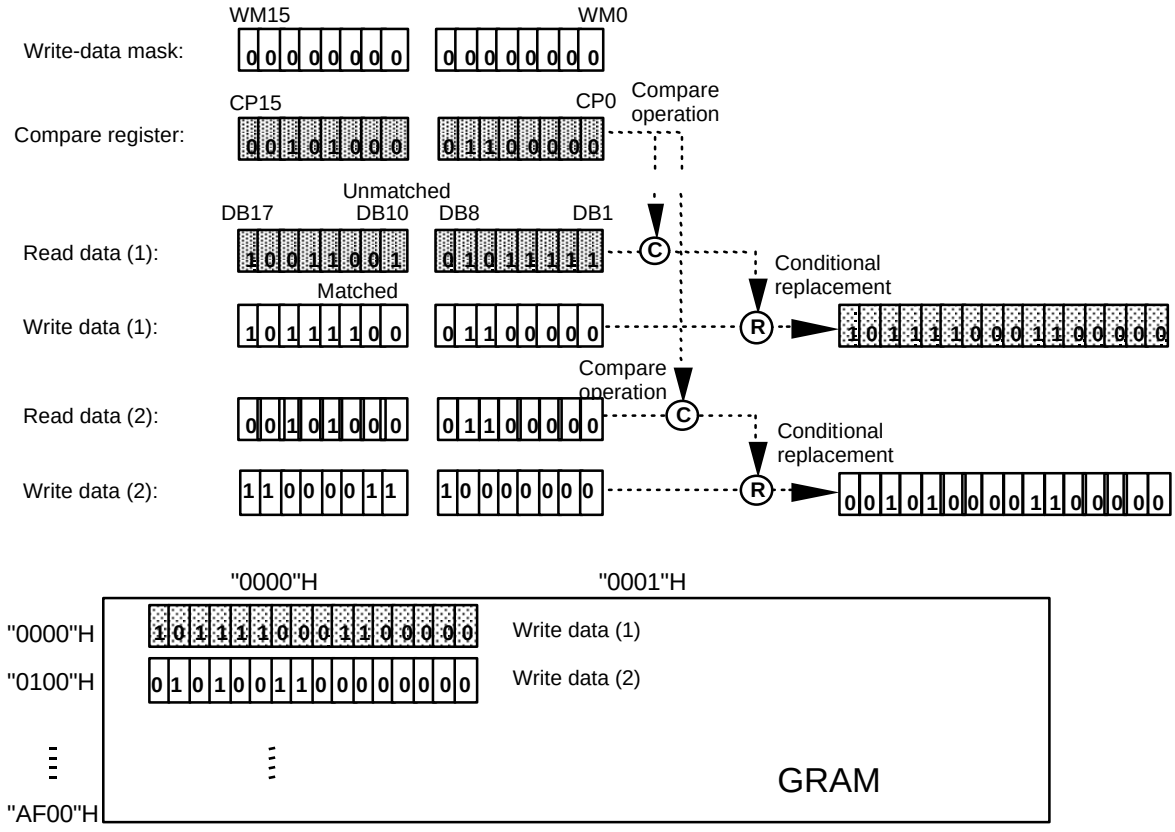
Figure 82 Writing Operation of Read/Write Mode 3

8. Read/Write mode 4: AM = “1”, LG2–0 = “100” / “101”

This mode is used when the data is vertically written by comparing the original data and the set value of the compare register (CP15–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the compare operation satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = “1”) or upper-left edge (I/D = “0”) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I / D = "1", AM = "1", LG2-0 = "101" (unmatched write)
2) CP15-0 = "2860"H
2) WM15-0 = "0000"H
3) AC = "0000"H



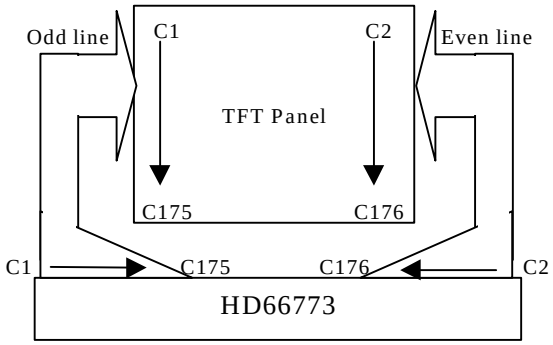
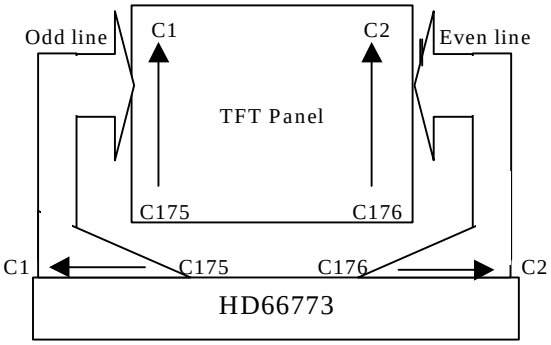
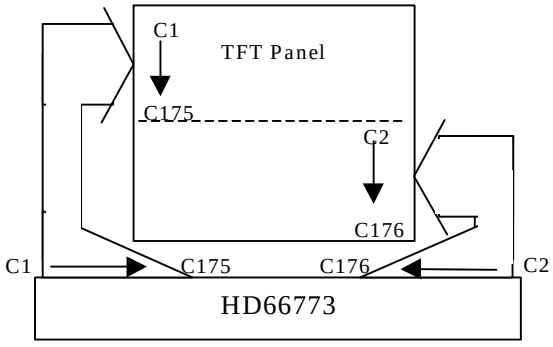
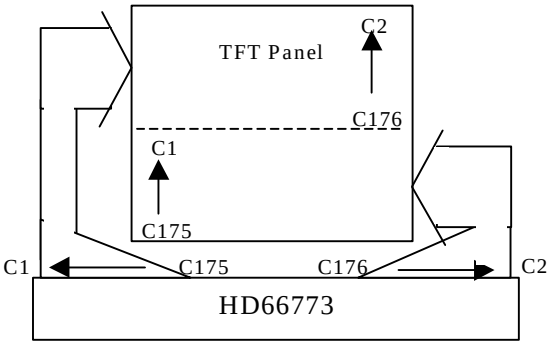
Note: 1. The bits in the GRAM indicated by '*' are not changed.
2. After writing to address "AF00"H, the AC jumps to "0001"H.

Figure 83 Writing Operation of Read/Write Mode 4

Setting scan mode

Shift direction of gate signal can be changed by SM bit and GS bit setting. By conbination of these bit setting, LCD panel and HD66773 can be connected in many ways.

Figure 84 Scan mode setting

SM	GS	Scan direction	
0	0		G1→G2→G3→ G4→···→G173→ G174→G175→G176
0	1		G176→G175→G174→ →173→···→G4→ G3→G2→G1
1	0		G1→G3→ G5→···→G173→G175 G2→G4→ G6→···→G174→G176
1	1		G176→G174→ G172→···G4→G2 G175→G173→ G171→···→G3→G1

Gamma Adjustment Function

The HD66773 incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment is implemented by deciding the 8-grayscale level with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

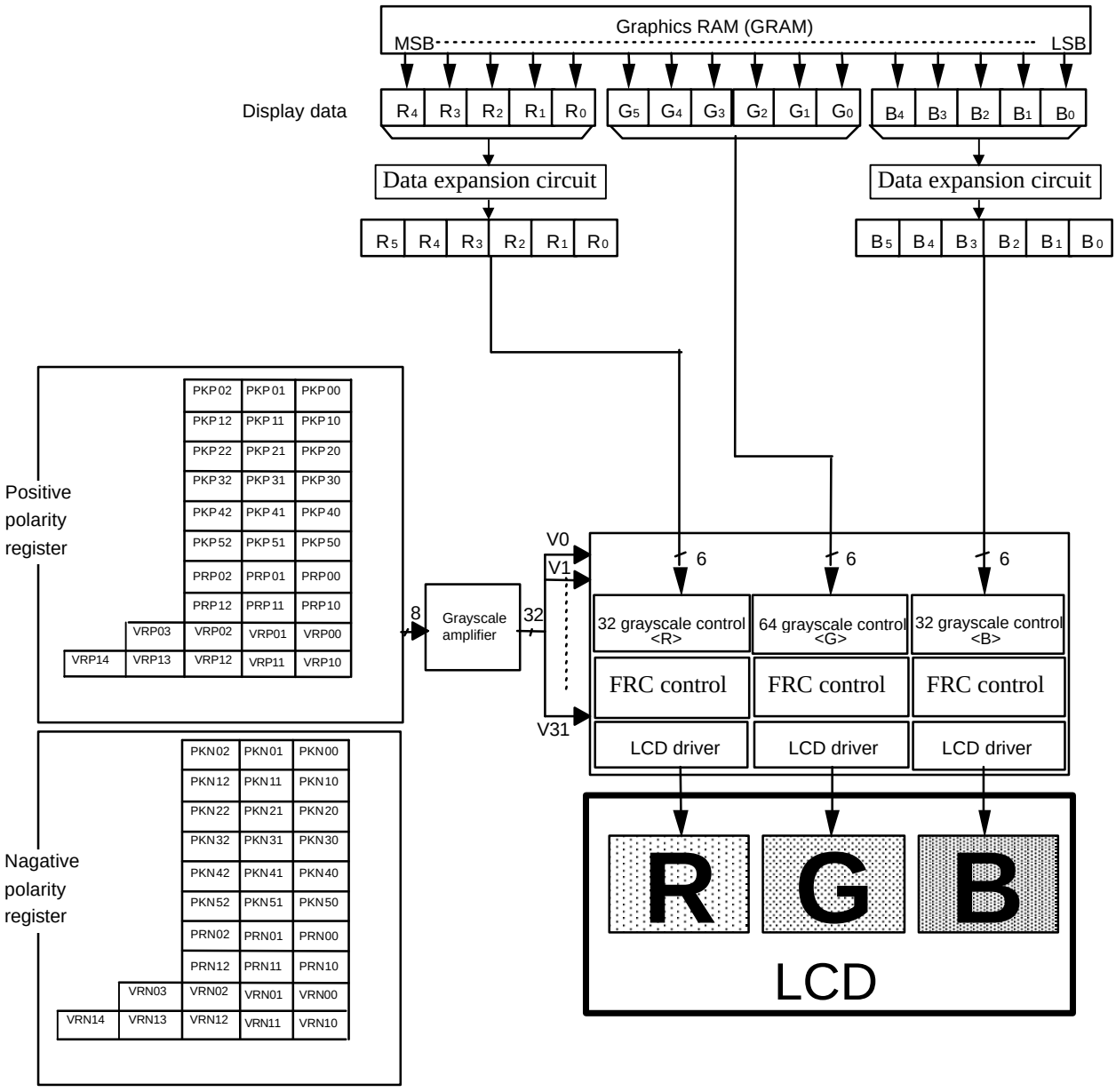


Figure 85: Gamma Adjustment Function

Structure of Grayscale Amplifier

Indicating structure of the grayscale amplifier as below. Determine 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V31.

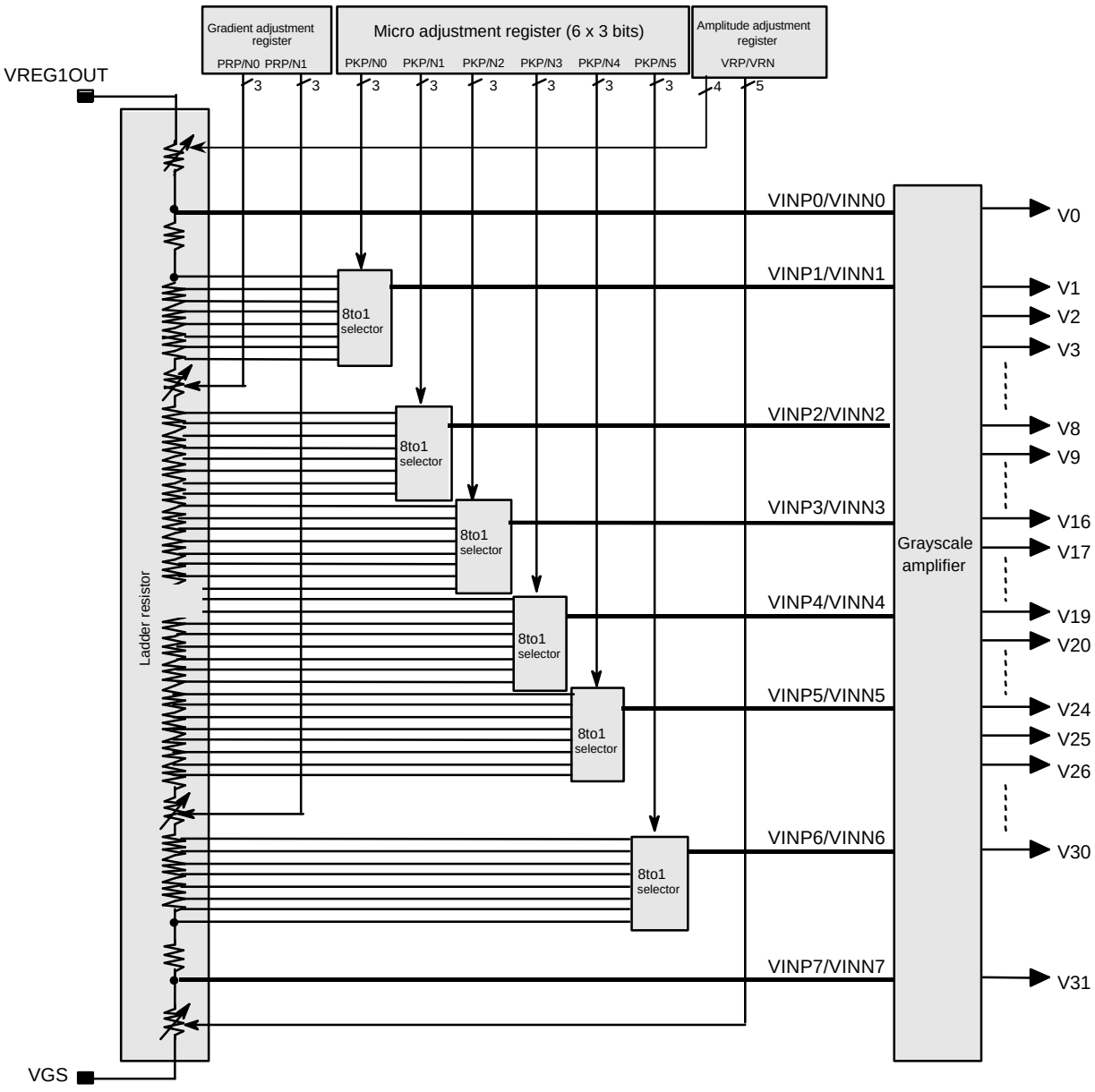


Figure 86: Structure of Grayscale Amplifier

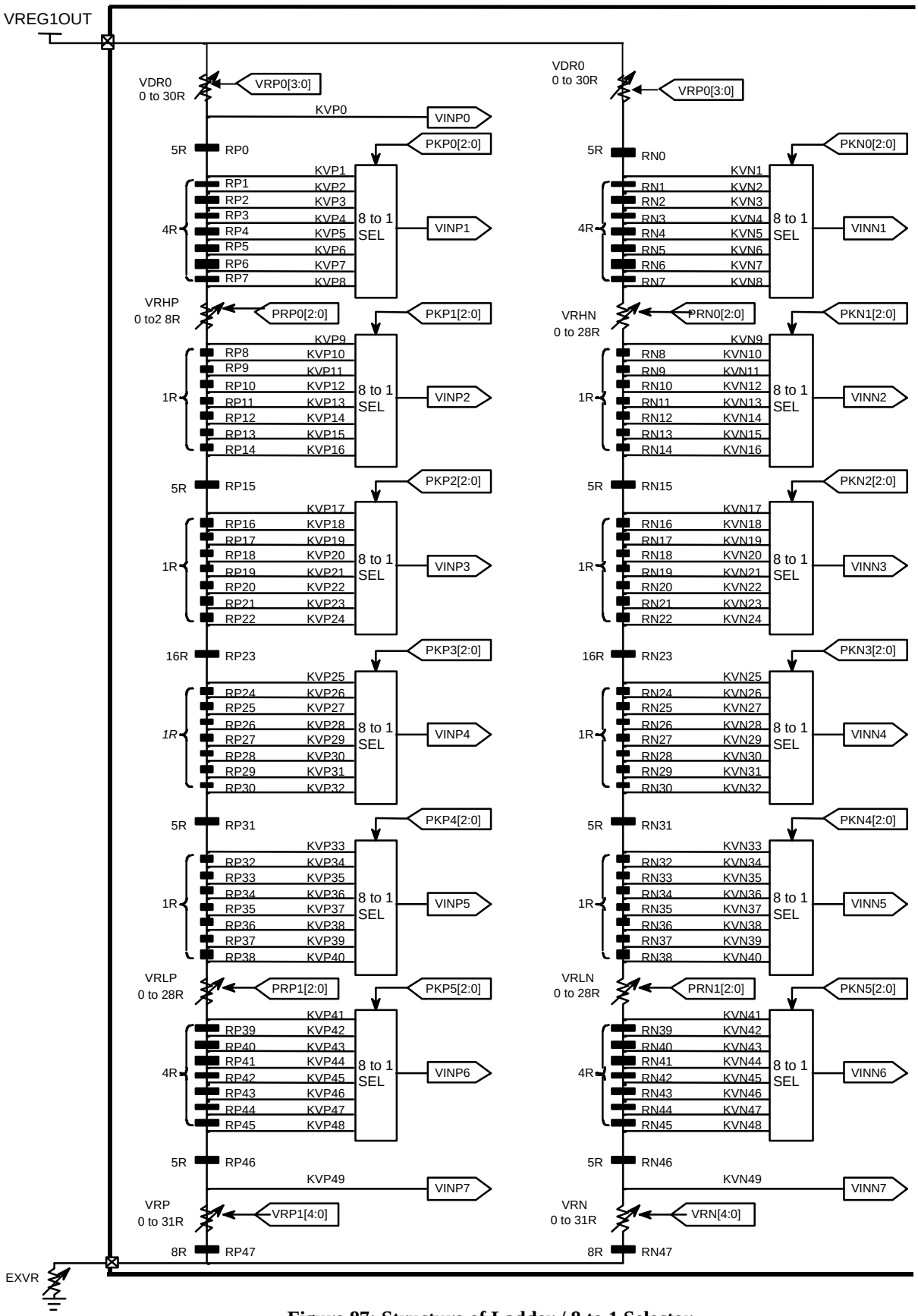


Figure 87: Structure of Ladder / 8 to 1 Selector

Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.

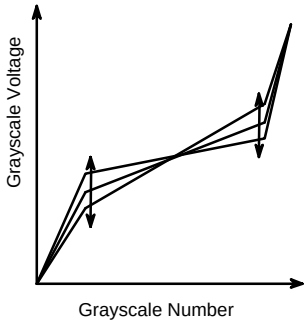


Figure 88 Gradient Adjustment

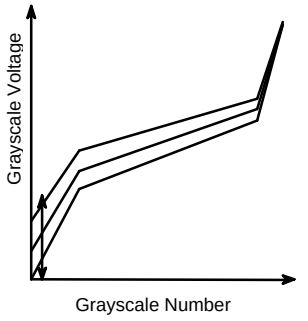


Figure 89 Amplitude Adjustment

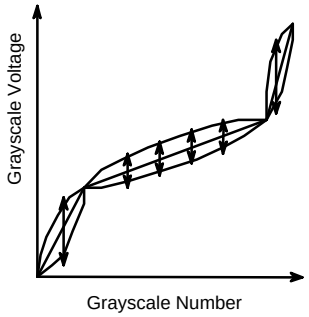


Figure 90 Micro-adjustment

1. Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRP (N) / VRL (N)) of the ladder resistor for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

2. Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP (N)0 /VRP(N)1) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor. (Adjust upper side by input VDH level.) Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

3. Micro-adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

Output signal list

Resistor Classification	For Positive Polarity	For Negative Polarity	Set-up Contents
Gradient Adjustment	PRP0[2:0]	PRN0[2:0]	Variable Resistor VR HP
	PRP1[2:0]	PRN1[2:0]	Variable Resistor VR LP
Amplitude Adjustment	VRP0[3:0]	VRN0[3:0]	Variable Resistor VRP 0
	VRP1[4:0]	VRN1[4:0]	Variable Resistor VRP 1
Micro-adjustment	PKP0[2:0]	PKN0[2:0]	8 to 1 selector voltage level for the grayscale 1
	PKP1[2:0]	PKN1[2:0]	8 to 1 selector voltage level for the grayscale 8
	PKP2[2:0]	PKN2[2:0]	8 to 1 selector voltage level for the grayscale 20
	PKP3[2:0]	PKN3[2:0]	8 to 1 selector voltage level for the grayscale 43
	PKP4[2:0]	PKN4[2:0]	8 to 1 selector voltage level for the grayscale 55
	PKP5[2:0]	PKN5[2:0]	8 to 1 selector voltage level for the grayscale 62

Table 38: Output Signal List

Ladder Resistor / 8 to 1 Selector

Block configuration

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors. Also, there are pins that connect to the external variable resistor. And it allows compensating the dispersion of length between one panel to another.

Variable Resistor

There are 2 types of the variable resistors that is for the gradient adjustment (VRHP (N) / VRLP (N)), for the amplitude adjustment (VRP (N)0/VRP(N)1). The ohmic value is set by the gradient adjustment and amplitude adjustment resistor as below.

Table 39:
Gradient Adjustment (1)

Register Value PRP (N)0[2.0]	Resistance Value VRHP(N)
000	0R
001	4R
010	8R
011	12R
101	20R
110	24R
111	28R

Table 40
Gradient Adjustment (2)

Register Value PRP (N)1[2.0]	Resistance Value VRLP (N)
000	0R
010	1R
011	2R
100	16R
101	20R
110	24R
111	28R

Table 41
Amplitude Adjustment (1)

Register Value VRP (N)0[3:0]	Resistance Value VRP (N) 0
0000	0R
0001	2R
0010	4R
⋮	⋮
1101	26R
1110	28R
1111	30R

Table42
Amplitude Adjustment (2)

Register Value PRP (N)[4.0]	Resistance Value VRP (N) 1
00000	0R
00001	1R
00010	2R
⋮	⋮
11101	29R
11110	30R
11111	31R

The 8 to 1 Selector

In the 8 to 1 selector, the voltage level can be selected from the levels which are generated by ladder resistors. And output the six types of the reference voltage, the VIN1- to VIN6. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Register Value	Selected Voltage					
PKP (N) [2:0]	VINP (N) 1	VINP (N) 2	VINP (N) 3	VNIP (N) 4	VNIP (N) 5	VINP (N) 6
000	KVP (N) 1	KVP (N) 9	KVP (N) 17	KVP (N) 25	KVP (N) 33	KVP (N) 41
001	KVP (N) 2	KVP (N) 10	KVP (N) 18	KVP (N) 26	KVP (N) 34	KVP (N) 42
010	KVP (N) 3	KVP (N) 11	KVP (N) 19	KVP (N) 27	KVP (N) 35	KVP (N) 43
011	KVP (N) 4	KVP (N) 12	KVP (N) 20	KVP (N) 28	KVP (N) 36	KVP (N) 44
100	KVP (N) 5	KVP (N) 13	KVP (N) 21	KVP (N) 29	KVP (N) 37	KVP (N) 45
101	KVP (N) 6	KVP (N) 14	KVP (N) 22	KVP (N) 30	KVP (N) 38	KVP (N) 46
110	KVP (N) 7	KVP (N) 15	KVP (N) 23	KVP (N) 31	KVP (N) 39	KVP (N) 47
111	KVP (N) 8	KVP (N) 16	KVP (N) 24	KVP (N) 32	KVP (N) 40	KVP (N) 48

Table 43

Table 44 Voltage formula (positive polarity)

Pins	Formula	Micro-adjsting register value	Reference voltage
KVP0	VREG1OUT-△V*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT-△V*(VRP0+5R)/SUMRP	PKP02-00 = "000"	VINP1
KVP2	VREG1OUT-△V*(VRP0+9R)/SUMRP	PKP02-00 = "001"	
KVP3	VREG1OUT-△V*(VRP0+13R)/SUMRP	PKP02-00 = "010"	
KVP4	VREG1OUT-△V*(VRP0+17R)/SUMRP	PKP02-00 = "011"	
KVP5	VREG1OUT-△V*(VRP0+21R)/SUMRP	PKP02-00 = "100"	
KVP6	VREG1OUT-△V*(VRP0+25R)/SUMRP	PKP02-00 = "101"	
KVP7	VREG1OUT-△V*(VRP0+29R)/SUMRP	PKP02-00 = "110"	
KVP8	VREG1OUT-△V*(VRP0+33R)/SUMRP	PKP02-00 = "111"	
KVP9	VREG1OUT-△V*(VRP0+33R+VRHP)/SUMRP	PKP12-10 = "000"	VINP2
KVP10	VREG1OUT-△V*(VRP0+34R+VRHP)/SUMRP	PKP12-10 = "001"	
KVP11	VREG1OUT-△V*(VRP0+35R+VRHP)/SUMRP	PKP12-10 = "010"	
KVP12	VREG1OUT-△V*(VRP0+36R+VRHP)/SUMRP	PKP12-10 = "011"	
KVP13	VREG1OUT-△V*(VRP0+37R+VRHP)/SUMRP	PKP12-10 = "100"	
KVP14	VREG1OUT-△V*(VRP0+38R+VRHP)/SUMRP	PKP12-10 = "101"	
KVP15	VREG1OUT-△V*(VRP0+39R+VRHP)/SUMRP	PKP12-10 = "110"	
KVP16	VREG1OUT-△V*(VRP0+40R+VRHP)/SUMRP	PKP12-10 = "111"	
KVP17	VREG1OUT-△V*(VRP0+45R+VRHP)/SUMRP	PKP22-20 = "000"	VINP3
KVP18	VREG1OUT-△V*(VRP0+46R+VRHP)/SUMRP	PKP22-20 = "001"	
KVP19	VREG1OUT-△V*(VRP0+47R+VRHP)/SUMRP	PKP22-20 = "010"	
KVP20	VREG1OUT-△V*(VRP0+48R+VRHP)/SUMRP	PKP22-20 = "011"	
KVP21	VREG1OUT-△V*(VRP0+49R+VRHP)/SUMRP	PKP22-20 = "100"	
KVP22	VREG1OUT-△V*(VRP0+50R+VRHP)/SUMRP	PKP22-20 = "101"	
KVP23	VREG1OUT-△V*(VRP0+51R+VRHP)/SUMRP	PKP22-20 = "110"	
KVP24	VREG1OUT-△V*(VRP0+52R+VRHP)/SUMRP	PKP22-20 = "111"	
KVP25	VREG1OUT-△V*(VRP0+68R+VRHP)/SUMRP	PKP32-30 = "000"	VINP4
KVP26	VREG1OUT-△V*(VRP0+69R+VRHP)/SUMRP	PKP32-30 = "001"	
KVP27	VREG1OUT-△V*(VRP0+70R+VRHP)/SUMRP	PKP32-30 = "010"	
KVP28	VREG1OUT-△V*(VRP0+71R+VRHP)/SUMRP	PKP32-30 = "011"	
KVP29	VREG1OUT-△V*(VRP0+72R+VRHP)/SUMRP	PKP32-30 = "100"	
KVP30	VREG1OUT-△V*(VRP0+73R+VRHP)/SUMRP	PKP32-30 = "101"	
KVP31	VREG1OUT-△V*(VRP0+74R+VRHP)/SUMRP	PKP32-30 = "110"	
KVP32	VREG1OUT-△V*(VRP0+75R+VRHP)/SUMRP	PKP32-30 = "111"	
KVP33	VREG1OUT-△V*(VRP0+80R+VRHP)/SUMRP	PKP42-00 = "000"	VINP5
KVP34	VREG1OUT-△V*(VRP0+81R+VRHP)/SUMRP	PKP42-40 = "001"	
KVP35	VREG1OUT-△V*(VRP0+82R+VRHP)/SUMRP	PKP42-40 = "010"	
KVP36	VREG1OUT-△V*(VRP0+83R+VRHP)/SUMRP	PKP42-40 = "011"	
KVP37	VREG1OUT-△V*(VRP0+84R+VRHP)/SUMRP	PKP42-40 = "100"	
KVP38	VREG1OUT-△V*(VRP0+85R+VRHP)/SUMRP	PKP42-40 = "101"	
KVP39	VREG1OUT-△V*(VRP0+86R+VRHP)/SUMRP	PKP42-40 = "110"	
KVP40	VREG1OUT-△V*(VRP0+87R+VRHP)/SUMRP	PKP42-40 = "111"	
KVP41	VREG1OUT-△V*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP52-50 = "000"	VINP6
KVP42	VREG1OUT-△V*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP52-50 = "001"	
KVP43	VREG1OUT-△V*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP52-50 = "010"	
KVP44	VREG1OUT-△V*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP52-50 = "011"	
KVP45	VREG1OUT-△V*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP52-50 = "100"	
KVP46	VREG1OUT-△V*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP52-50 = "101"	
KVP47	VREG1OUT-△V*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP52-50 = "110"	
KVP48	VREG1OUT-△V*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP52-50 = "111"	
KVP49	VREG1OUT-△V*(VRP0+120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128 R + VRHP + VRLP + VRP0 + VRP1

SUMRN: Total of the negative polarity ladder resistance = 128 R + VRLN + VRNL + VRHN0 + VRN1

ΔV: Voltage difference between VREG1OUT - VGS

TBD

Table 45: Voltage Formula (Positive Polarity)

grayscale voltage	Formula
V0	VINP0
V1	V3D+(VINP1-V3D)*(8/24)
V2	V4+(V3D-V4)*(16/24)
V3	V4+(V3D-V4)*(8/24)
V4	VINP2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V10+(V4-V10)*(4/24)
V10	VINP3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINP4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINP5
V28	VINP6+(V27-VINP6)*(780/960)
V29	VINP6+(V27-VINP6)*(600/960)
V30	VINP6+(V27-VINP6)*(280/960)
V31	VINP7

V3D: V3D = V4+(VINP1-V4)+(540/960)

TBD

Table 46: Voltage Formula (Negative Polarity)

Pins	Formula	Micro-adjsting register value	Reference voltage
KVN0	VREG1OUT-△V*VRN0/SUMRN	-	VINN0
KVN1	VREG1OUT-△V*(VRN0+5R)/SUMRN	PKN02-00 = "000"	VINN1
KVN2	VREG1OUT-△V*(VRN0+9R)/SUMRN	PKN02-00 = "001"	
KVN3	VREG1OUT-△V*(VRN0+13R)/SUMRN	PKN02-00 = "010"	
KVN4	VREG1OUT-△V*(VRN0+17R)/SUMRN	PKN02-00 = "011"	
KVN5	VREG1OUT-△V*(VRN0+21R)/SUMRN	PKN02-00 = "100"	
KVN6	VREG1OUT-△V*(VRN0+25R)/SUMRN	PKN02-00 = "101"	
KVN7	VREG1OUT-△V*(VRN0+29R)/SUMRN	PKN02-00 = "110"	
KVN8	VREG1OUT-△V*(VRN0+33R)/SUMRN	PKN02-00 = "111"	
KVN9	VREG1OUT-△V*(VRN0+33R+VRHN)/SUMRN	PKN12-10 = "000"	VINN2
KVN10	VREG1OUT-△V*(VRN0+33R+VRHN)/SUMRN	PKN12-10 = "001"	
KVN11	VREG1OUT-△V*(VRN0+35R+VRHN)/SUMRN	PKN12-10 = "010"	
KVN12	VREG1OUT-△V*(VRN0+36R+VRHN)/SUMRN	PKN12-10 = "011"	
KVN13	VREG1OUT-△V*(VRN0+37R+VRHN)/SUMRN	PKN12-10 = "100"	
KVN14	VREG1OUT-△V*(VRN0+38R+VRHN)/SUMRN	PKN12-10 = "101"	
KVN15	VREG1OUT-△V*(VRN0+39R+VRHN)/SUMRN	PKN12-10 = "110"	
KVN16	VREG1OUT-△V*(VRN0+40R+VRHN)/SUMRN	PKN12-10 = "111"	
KVN17	VREG1OUT-△V*(VRN0+45R+VRHN)/SUMRN	PKN22-20 = "000"	VINN3
KVN18	VREG1OUT-△V*(VRN0+46R+VRHN)/SUMRN	PKN22-20 = "001"	
KVN19	VREG1OUT-△V*(VRN0+47R+VRHN)/SUMRN	PKN22-20 = "010"	
KVN20	VREG1OUT-△V*(VRN0+48R+VRHN)/SUMRN	PKN22-20 = "011"	
KVN21	VREG1OUT-△V*(VRN0+49R+VRHN)/SUMRN	PKN22-20 = "100"	
KVN22	VREG1OUT-△V*(VRN0+50R+VRHN)/SUMRN	PKN22-20 = "101"	
KVN23	VREG1OUT-△V*(VRN0+51R+VRHN)/SUMRN	PKN22-20 = "110"	
KVN24	VREG1OUT-△V*(VRN0+52R+VRHN)/SUMRN	PKN22-20 = "111"	
KVN25	VREG1OUT-△V*(VRN0+68R+VRHN)/SUMRN	PKN32-30 = "000"	VINN4
KVN26	VREG1OUT-△V*(VRN0+69R+VRHN)/SUMRN	PKN32-30 = "001"	
KVN27	VREG1OUT-△V*(VRN0+70R+VRHN)/SUMRN	PKN32-30 = "010"	
KVN28	VREG1OUT-△V*(VRN0+71R+VRHN)/SUMRN	PKN32-30 = "011"	
KVN29	VREG1OUT-△V*(VRN0+72R+VRHN)/SUMRN	PKN32-30 = "100"	
KVN30	VREG1OUT-△V*(VRN0+73R+VRHN)/SUMRN	PKN32-30 = "101"	
KVN31	VREG1OUT-△V*(VRN0+74R+VRHN)/SUMRN	PKN32-30 = "110"	
KVN32	VREG1OUT-△V*(VRN0+75R+VRHN)/SUMRN	PKN32-30 = "111"	
KVN33	VREG1OUT-△V*(VRN0+80R+VRHN)/SUMRN	PKN42-00 = "000"	VINN5
KVN34	VREG1OUT-△V*(VRN0+81R+VRHN)/SUMRN	PKN42-00 = "001"	
KVN35	VREG1OUT-△V*(VRN0+82R+VRHN)/SUMRN	PKN42-00 = "010"	
KVN36	VREG1OUT-△V*(VRN0+83R+VRHN)/SUMRN	PKN42-00 = "011"	
KVN37	VREG1OUT-△V*(VRN0+84R+VRHN)/SUMRN	PKN42-00 = "100"	
KVN38	VREG1OUT-△V*(VRN0+85R+VRHN)/SUMRN	PKN42-00 = "101"	
KVN39	VREG1OUT-△V*(VRN0+86R+VRHN)/SUMRN	PKN42-00 = "110"	
KVN40	VREG1OUT-△V*(VRN0+87R+VRHN)/SUMRN	PKN42-00 = "111"	
KVN41	VREG1OUT-△V*(VRN0+87R+VRHN+VRLN)/SUMRN	PKN52-50 = "000"	VINN6
KVN42	VREG1OUT-△V*(VRN0+91R+VRHN+VRLN)/SUMRN	PKN52-50 = "001"	
KVN43	VREG1OUT-△V*(VRN0+95R+VRHN+VRLN)/SUMRN	PKN52-50 = "010"	
KVN44	VREG1OUT-△V*(VRN0+99R+VRHN+VRLN)/SUMRN	PKN52-50 = "011"	
KVN45	VREG1OUT-△V*(VRN0+103R+VRHN+VRLN)/SUMRN	PKN52-50 = "100"	
KVN46	VREG1OUT-△V*(VRN0+107R+VRHN+VRLN)/SUMRN	PKN52-50 = "101"	
KVN47	VREG1OUT-△V*(VRN0+111R+VRHN+VRLN)/SUMRN	PKN52-50 = "110"	
KVN48	VREG1OUT-△V*(VRN0+115R+VRHN+VRLN)/SUMRN	PKN52-50 = "111"	
KVN49	VREG1OUT-△V*(VRN0+120R+VRHN+VRLN)/SUMRN	-	VINN7

SUMRP: Total of the positive polarity ladder resistance = 128 R + VRHP + VRLP + VRP0 + VRP1

SUMRN: Total of the negative polarity ladder resistance = 128 R + VRLN + VRNL + VRHN0 + VRN1

ΔV: Voltage difference between VREG1OUT - VGS

TBD

Table 47 Voltage Formula (Negative Polarity)

grayscale voltage	Formula
V0	VINP0
V1	V3D+(VINP1-V3D)*(8/24)
V2	V4+(V3D-V4)*(16/24)
V3	V4+(V3D-V4)*(8/24)
V4	VINP2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V10+(V4-V10)*(4/24)
V10	VINP3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINP4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINP5
V28	VINP6+(V27-VINP6)*(780/960)
V29	VINP6+(V27-VINP6)*(600/960)
V30	VINP6+(V27-VINP6)*(280/960)
V31	VINP7

V3D: V3D = V4+(VINP1-V4)+(540/960)

TBD

Relationship between RAM Data and Output

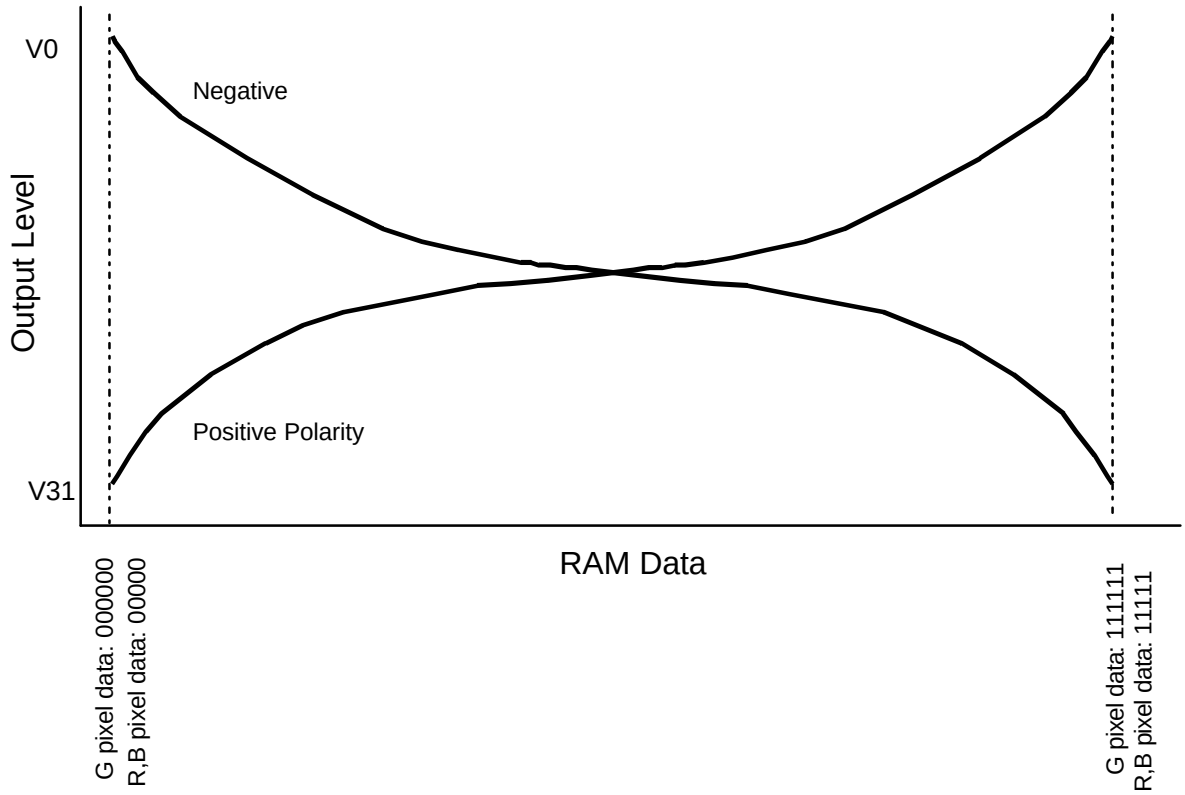


Figure 91: Relationship between RAM Data and Output Voltage

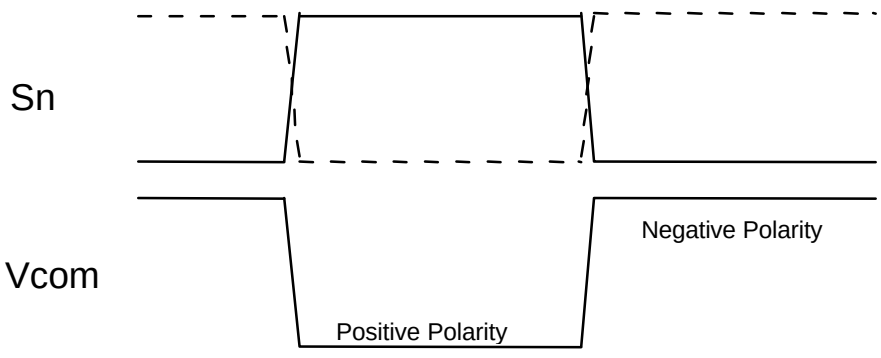


Figure 92: Relationship between Source Output and Vcom

The 8-color Display Mode

The HD66773 carries 8-color display mode. Using grayscale levels are V0 and V31 and all other level (V1 to V30) power supplies are halt. So that it attempts to lower power consumption. Also, during the 8-color mode, the Gamma micro adjustment register, PKP00-PKP52 and PKN00-PKN52 are invalid. Rewrite the data of GRAM R/B to 00000 or 11111, G to 000000 or 111111 before set the mode in order to select V0/V31. The level power supply (V1-V30) is in OFF condition during the 8-color mode.

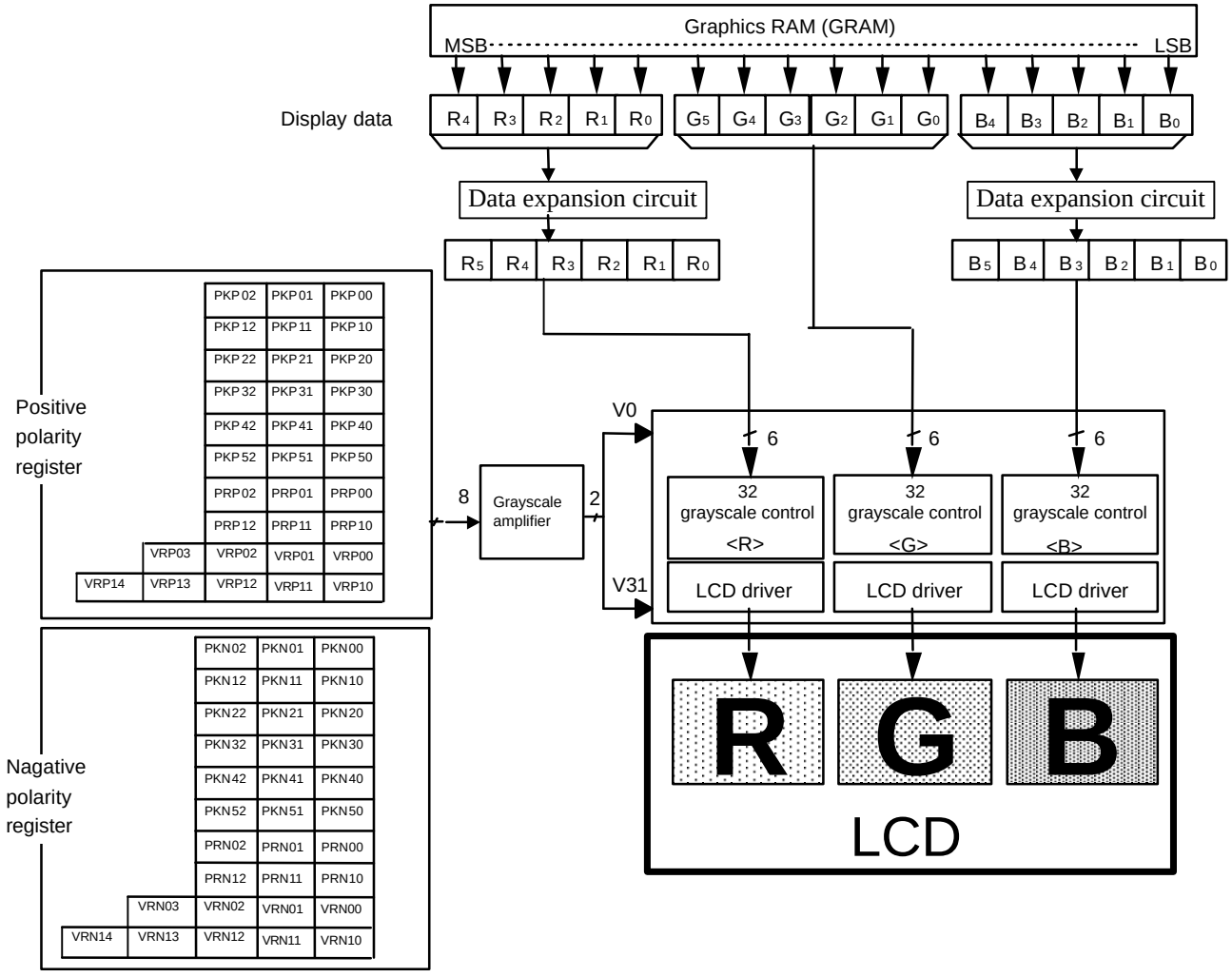


Figure 93: Grayscale Control

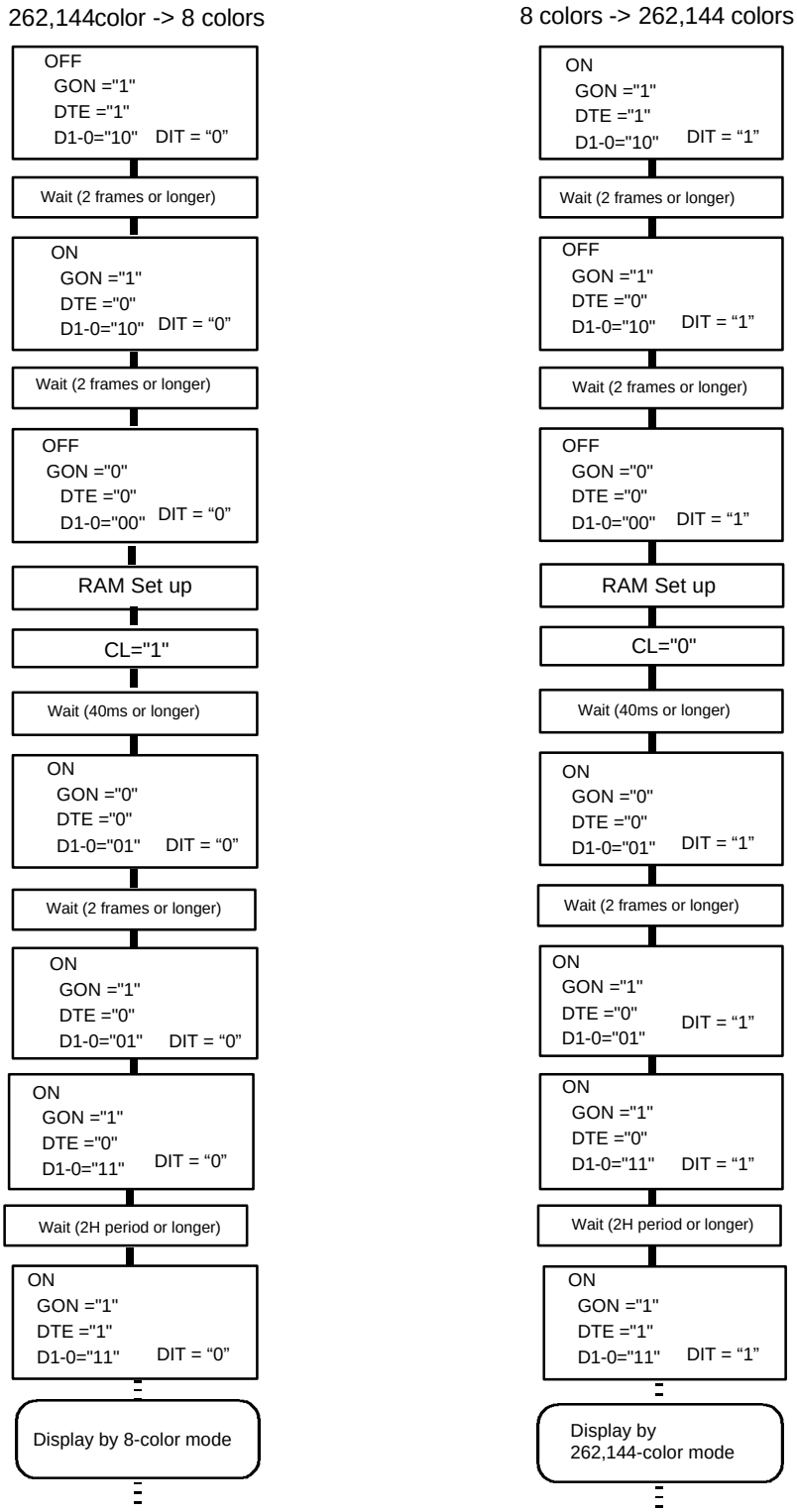

262,144color -> 8 colors
OFF
GON ="1"
DTE ="1"
D1-0="10" DIT = “0”
Wait (2 frames or longer)
ON
GON ="1"
DTE ="0"
D1-0="10" DIT = “0”
Wait (2 frames or longer)
OFF
GON ="0"
DTE ="0"
D1-0="00" DIT = “0”
RAM Set up
CL="1"
Wait (40ms or longer)
ON
GON ="0"
DTE ="0"
D1-0="01" DIT = “0”
Wait (2 frames or longer)
ON
GON ="1"
DTE ="0"
D1-0="01" DIT = “0”
ON
GON ="1"
DTE ="0"
D1-0="11" DIT = “0”
Wait (2H period or longer)
ON
GON ="1"
DTE ="1"
D1-0="11" DIT = “0”
Display by 8-color mode
8 colors -> 262,144 colors
ON
GON ="1"
DTE ="1"
D1-0="10" DIT = “1”
Wait (2 frames or longer)
OFF
GON ="1"
DTE ="0"
D1-0="10" DIT = “1”
Wait (2 frames or longer)
OFF
GON ="0"
DTE ="0"
D1-0="00" DIT = “1”
RAM Set up
CL="0"
Wait (40ms or longer)
ON
GON ="0"
DTE ="0"
D1-0="01" DIT = “1”
Wait (2 frames or longer)
ON
GON ="1"
DTE ="0"
D1-0="01" DIT = “1”
ON
GON ="1"
DTE ="0"
D1-0="11" DIT = “1”
Wait (2H period or longer)
ON
GON ="1"
DTE ="1"
D1-0="11" DIT = “1”
Display by
262,144-color mode

Figure 94

Instruction Setting Flow

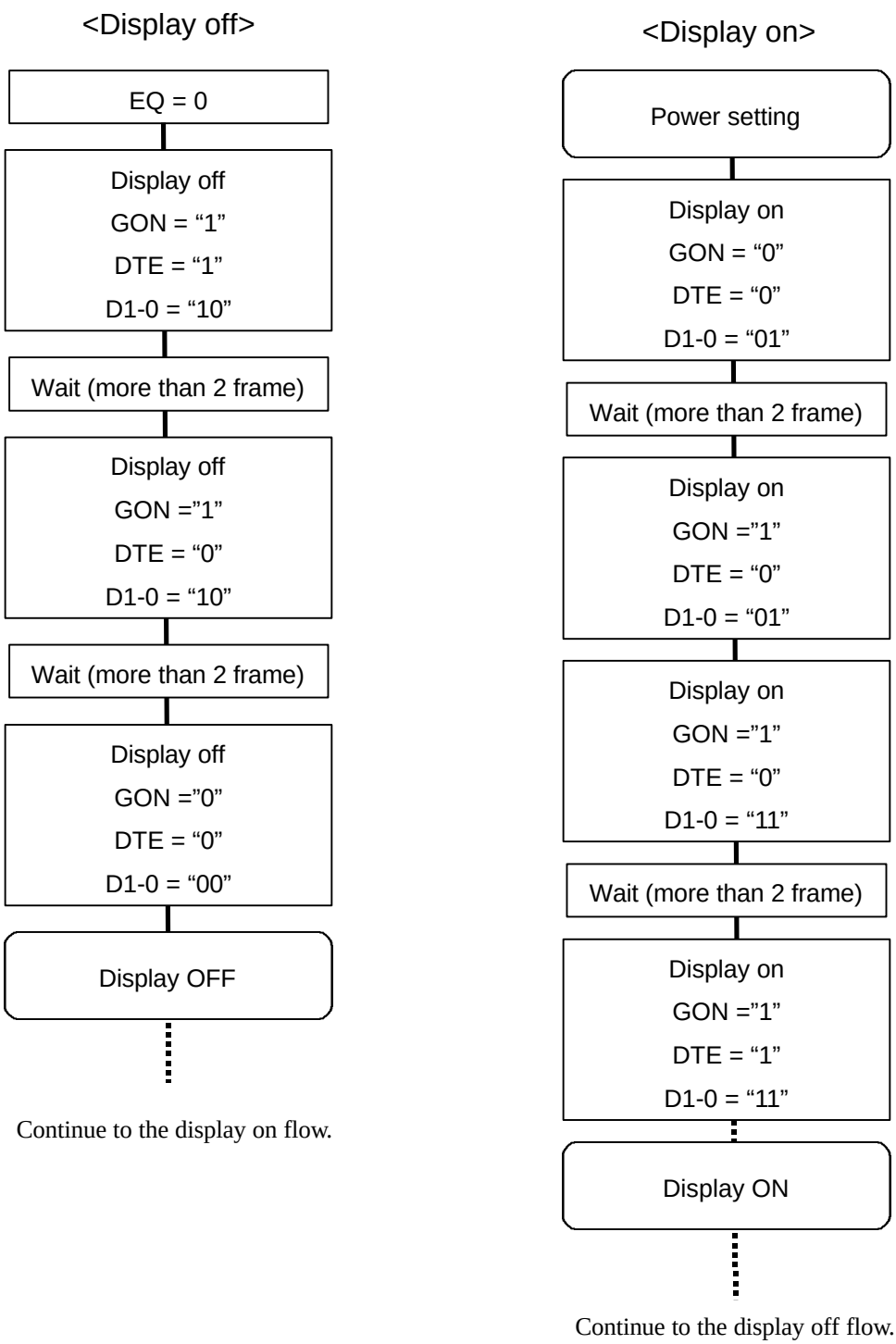


Figure 95

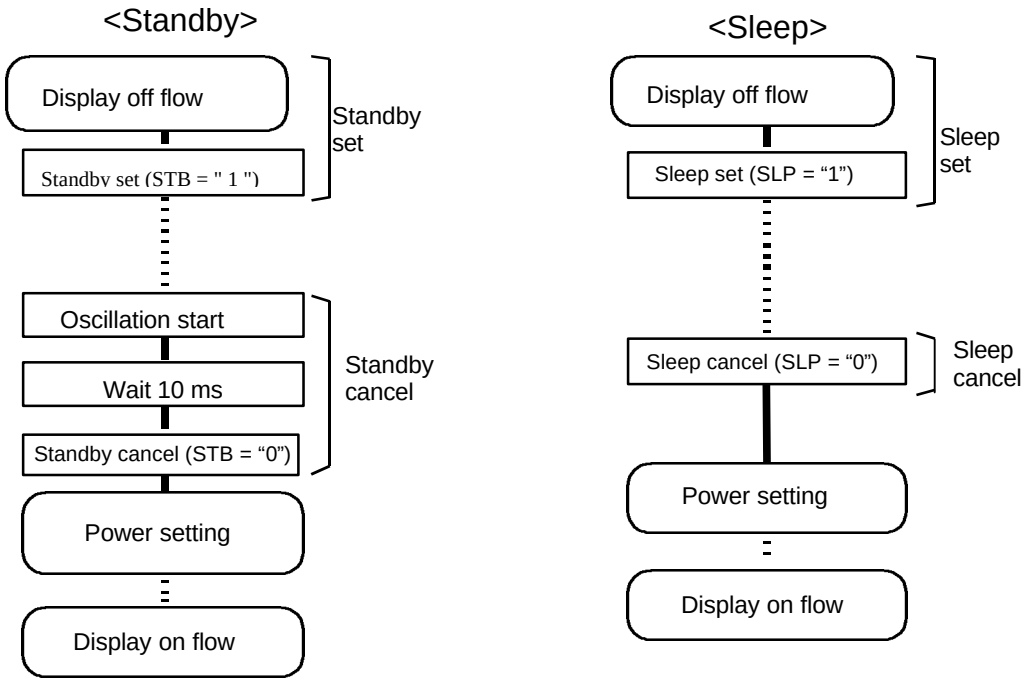

<Standby>
Display off flow
Standby set (STB = " 1 ")
Standby set
Oscillation start
Wait 10 ms
Standby cancel (STB = “0”)
Standby cancel
Power setting
Display on flow
<Sleep>
Display off flow
Sleep set (SLP = “1”)
Sleep set
Sleep cancel (SLP = “0”)
Sleep cancel
Power setting
Display on flow

Figure 96

Flow of Power-Supply Setting

Apply the power in a sequence as shown in figure 103. Stabilizing time of oscillation circuit and stabilizing time of step-up circuit and operation amplifier depend on the external resistor and external capacity.

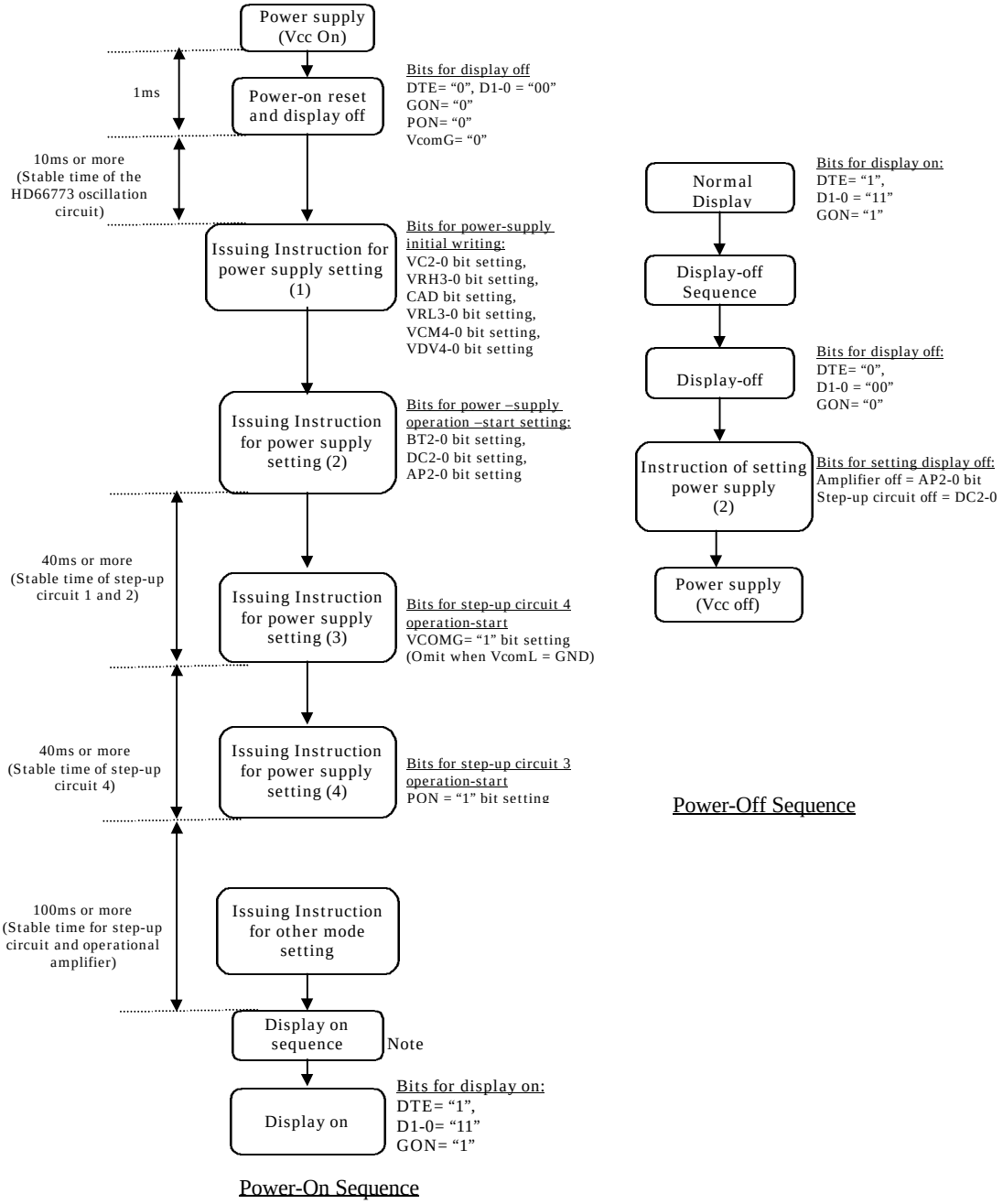
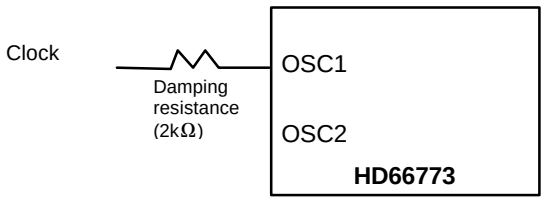


Figure 97 Flow of Power-Supply Setting

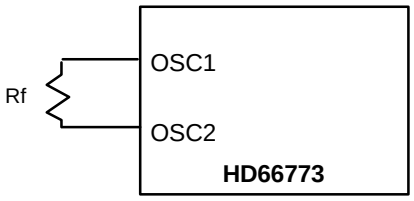
Oscillation Circuit

The HD66773 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

1) External Clock Mode



2) External resistance oscillation mode



Note: The Rf resistance must be located near the OSC1/OSC2 pin on the master side. And other signals must not run across between OSC1 and OSC2.

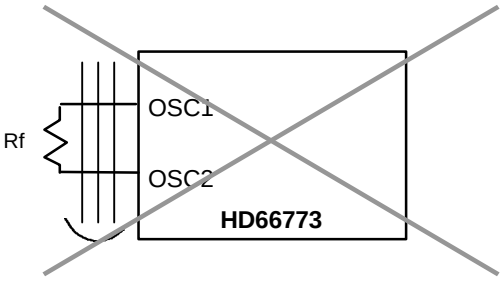
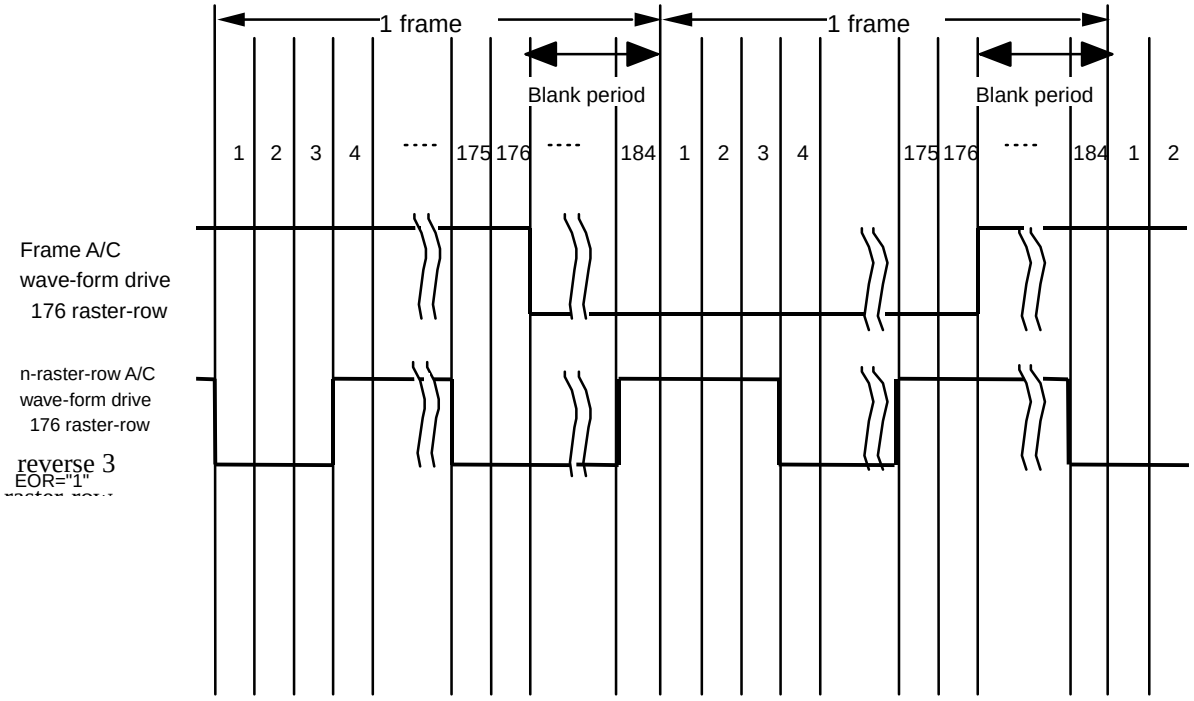


Figure 98: Oscillation Circuits

n-raster-row Reversed AC Drive

The HD66773 supports not only the LCD reversed AC drive in a one-frame unit but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster-rows. When a problem affecting display quality occurs, the n-raster-row reversed AC drive can improve the quality.

Determine the number of the raster-rows n (NW bit set value +1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-row is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Note: In an n-raster-row driving EOR should be “1” so that DC bias voltage is not applied.

Figure99: Example of an AC Signal under n-raster-row Reversed AC Drive

Interlace Drive

HD66773 supports the interlace drive to protect from the display flicker. It splits one frame into n fields and drives. Determine the n fields (FLD bit stetting value) after confirming on the actual LCD display. Following table indicates n fields: the gate selecting position when it is 1 or 3. And the diagram below indicates the output waveform when the 3-field interlace drive is active.

Table 53

GS = "0"

FLD1-0: Setting Value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G1	○	○		
G2	○		○	
G3	○			○
G4	○	○		
G5	○		○	
G6	○			○
G7	○	○		
G8	○		○	
G9	○			○
⋮	⋮	⋮	⋮	⋮
G173	○		○	
G174	○			○
G175	○	○		
G176	○		○	

GS = "1"

FLD1-0: Setting Value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G176	○	○		
G175	○		○	
G174	○			○
G173	○	○		
G172	○		○	
G171	○			○
G170	○	○		
G169	○		○	
G168	○			○
⋮	⋮	⋮	⋮	⋮
G4	○		○	
G3	○			○
G2	○	○		
G1	○		○	

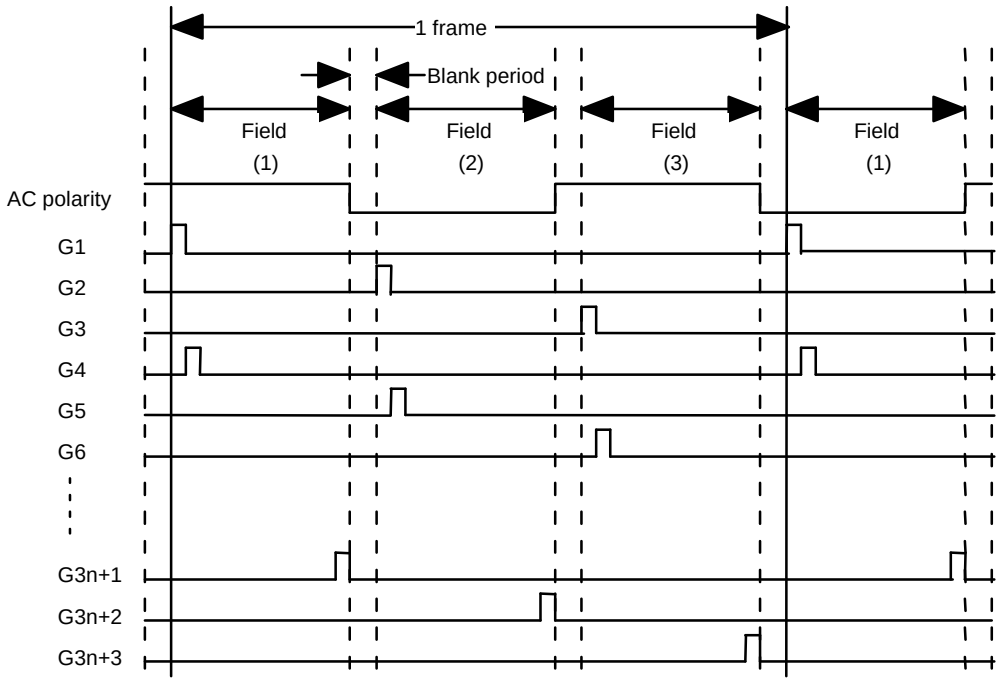


Figure 100: Gate output Timing on the 3 Field Interlace

AC Drive Timing

Following diagram indicates the timing of changing polarity on the each A/C drive method. LCD drive polarity is changed after every frame. After the A/C this timing, the blank (all outputs from the gate: Vgoff output) in 8H period is inserted. Also, LCD drive polarity is change after every field when it is on the interlace drive and a blank is inserted in every timing. The amount of blanking periods becomes 8H in a frame. When the reversed n-raster-row is driving, a blank period of the 8H period is inserted after all screens are drawn

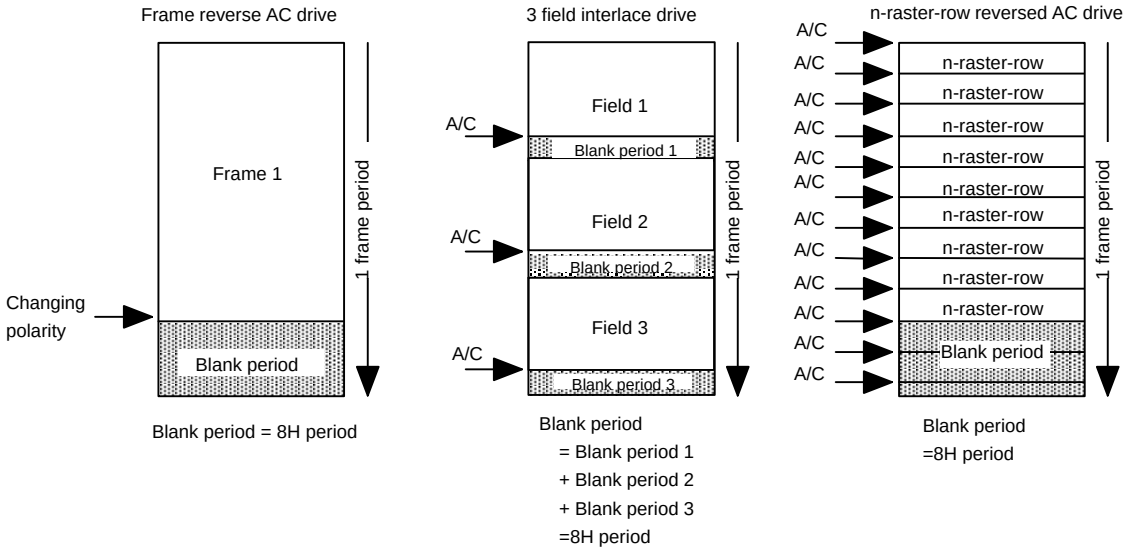


Figure 101

Frame Frequency Adjusting Function

The HD66773 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD driver as the oscillation frequency is always same.
If the oscillation frequency is set to high, animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display, etc. is required, the frame frequency can be set high.

Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the 1H period adjusting bit (RTN) and in the operation clock division bit (DIV) by the instruction.

(Formula for the frame frequency)

$$\text{Frame Frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row x division ratio x (Line+8)}} \text{ [Hz]}$$

fosc: R-C oscillation frequency
Line: Numbers of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit

Example of Calculation

In case of maximum frame frequency = 60 Hz;
Driver raster-row: 176
1H period: 16 clock (RTN3 to 0 = “0000”)
Operation clock division ratio: 1 division

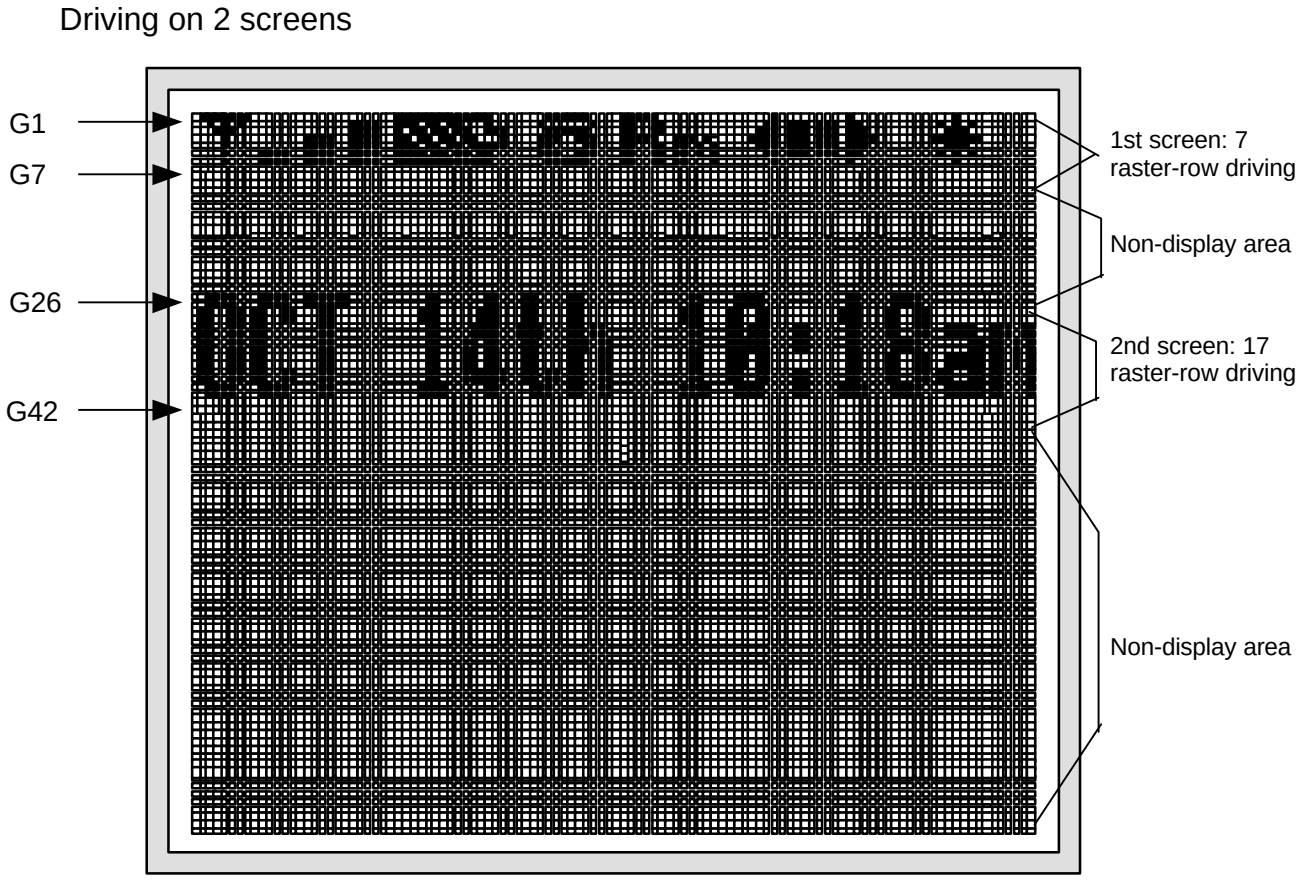
fosc = 60Hz x (0+16) clock x 1 division x (176+8) lines = 177 [kHz]

In this case, the CR oscillation frequency becomes 177 kHz. The external resistance value of the R-C oscillator must be adjusted to be 177 kHz.

Screen-division Driving Function

The HD66773 can select and drive two screens at any position with the screen-driving position registers (R14 and R15). Any two screens required for display are selectively driven and reducing LCD-driving voltage and power consumption.

For the 1st division screen, start lines (SS17 to 10) and end lines (SE17 to 10) are specified by the 1st screen-driving position register (R14). For the 2nd division screen, start line (SS27 to 20) and end lines (SE27 to 20) are specified by the 2nd screen-driving position register (R15). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must be the number of LCD drive raster-rows or less.



Driving raster-row: NL4-0 = "10101" (176 lines)
1st screen setting: SS17-10 = "00"H, SE17-10 = "06"H
2nd screen setting: SS27-20 = "19"H, SE27-20 = "29"H, SPT = "1"

Figure 102: Display Example in 2-screen Division Driving

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS17 to 10) and end line (SE17 to 10) of the 1st screen driving position register (R14) and the start line (SS27 to 20) and end line (SE27 to 20) of the 2nd screen driving position register (R15) for the HD66773.
Note that incorrect display may occur if the restrictions are not satisfied.

Table 54: Restrictions on the 1st/2nd Screen Driving Position Register Settings

1st Screen Driving (SPT = 0)

Register setting	Display operation
(SE17 to 10) – (SS17 to 10) = NL	Full screen display Normally displays (SE17 to 10) to (SS17 to 10)
(SE17 to 10) – (SS17 to 10) < NL	Partial display Normally displays (SE17 to 10) to (SS17 to 10) In all other display area refers to the output level based on the PT setting. (non-display)
(SE17 to 1) – (SS17 to 10) > NL	**Setting disabled**

Note 1: SS17 to 10 <= SE17 to 10 <= AFH
Note 2: Setting SE27 to 20 and SS27 to 20 are invalid.

Table 55

2nd Screen Driving (SPT = 1)

Register setting	Display operation
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27-20)) = NL	Full screen display Normally displays (SE27 to 20) to (SE17 to 10)
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27 to 20)) < NL	Partial display Normally displays (SE27 to 20) to (SS17 to 10) In all other display area refers to the output level based on the PT setting. (non-display)
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27 to 20)) > NL	Setting disabled

Note 1: SS17 to 10 <= SE17 to 10 < SS27 to 20 <= SE27 to 20 <= AFH
Note 2: (SE27 to 20) – (SS17 to 10) <= NL

The driver output can not be set for non-display area during the partial display. Determine based on characteristic of the display panels.

PT1	PT0	Source output in non-display area		Gate output in non-display area
		Positive polarity	Negative polarity	
0	0	V31	V0	Normal operation
0	1	V31	V0	Vgoff
1	0	GND	GND	Vgoff
1	1	Hi-z	Hi-z	Vgoff

Table 56

Refer to the following flow to set up the partial display.

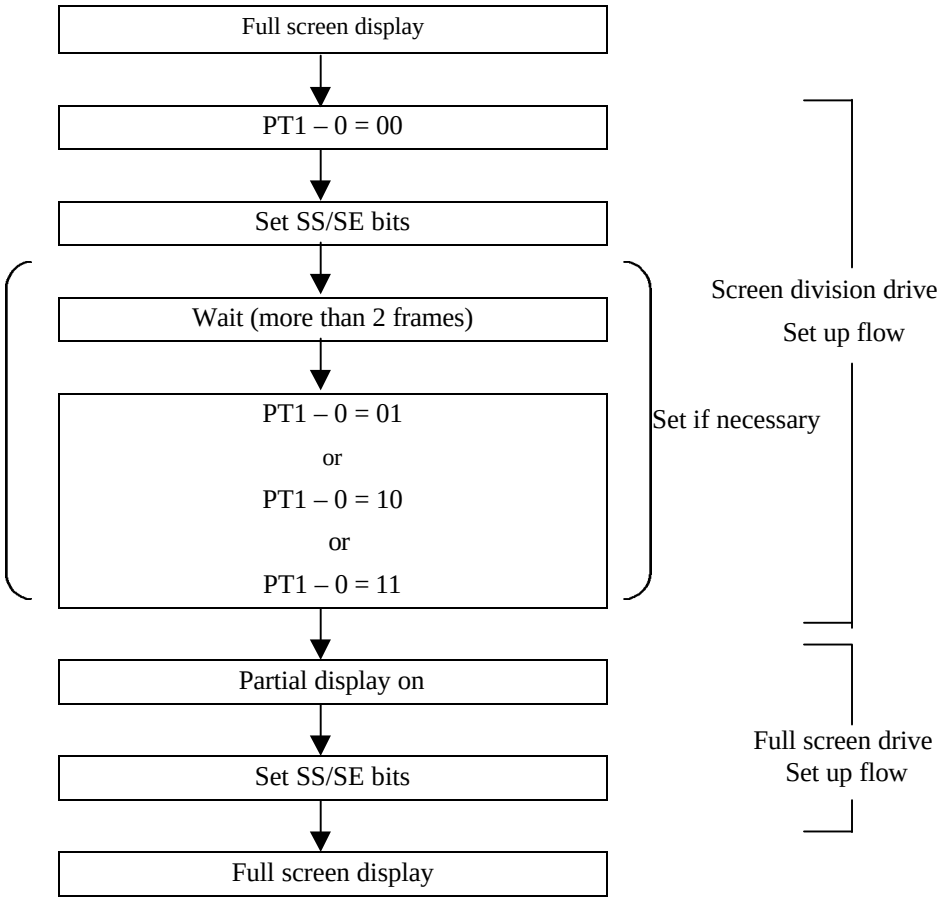
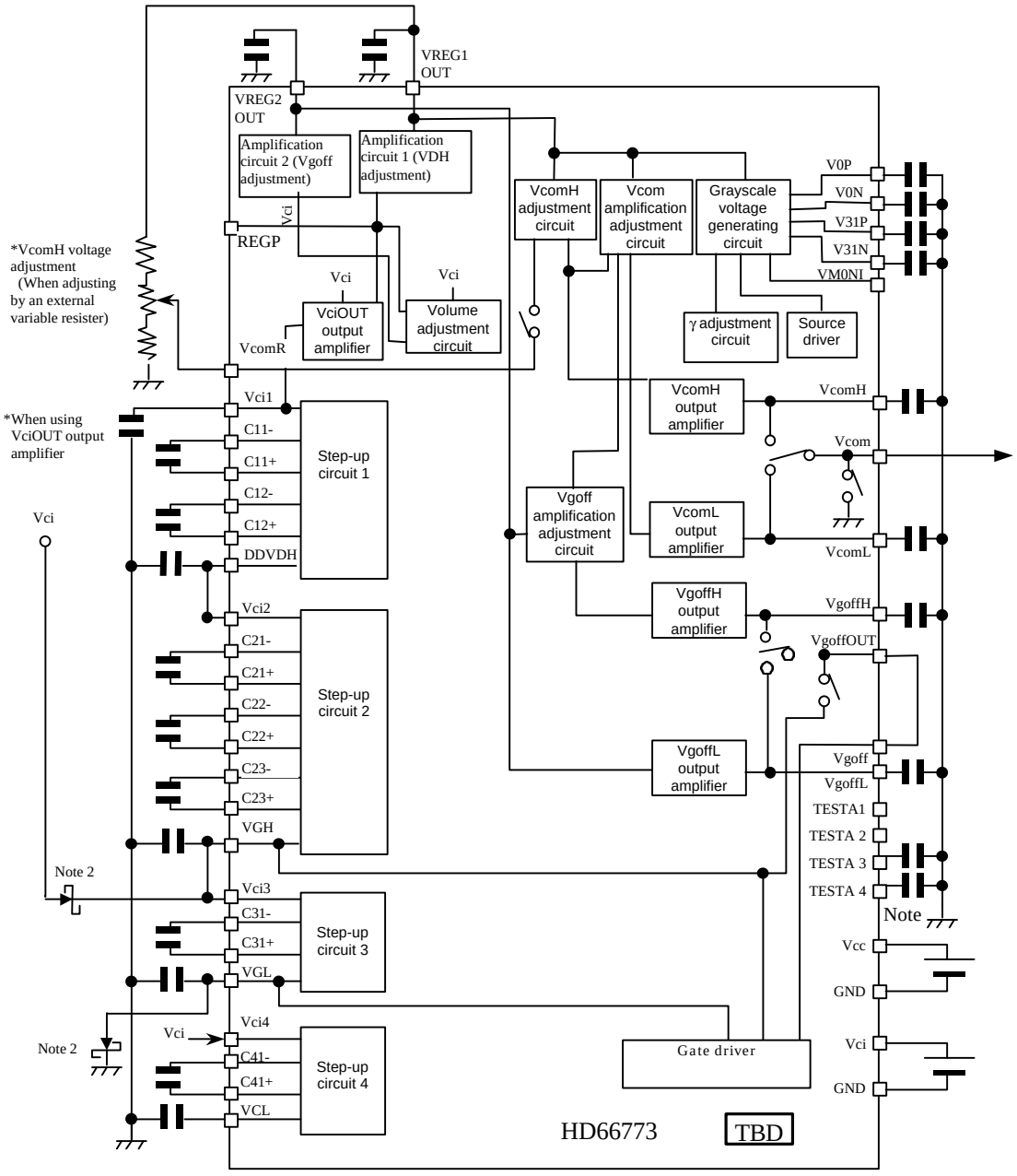


Figure 103

Configuration of Internal Power-Supply Generation Circuit

Figure 90 shows a configuration of the voltage generation circuit for HD66773. The step-up circuits consist of step-up circuits 1 to 4. Step-up circuit 1 doubled or triples the voltage supplied to Vci1, and that voltage is doubled, tripled, or quadrupled in step-up circuit2. Step-up circuit 3 reverses the VGH level with reference to GND and generates the VGL level. Step-up circuit 4 reverses the Vci level with reference to GND and generates the VCL level. These step-up circuits generate power supplies required for TFT liquid crystal display operation. Reference voltages VDH, Vcom, and Vgoff for the HD66773 grayscale voltage are amplified in amplification circuits 1 and 2 from the internal-voltage adjustment circuit, or REGP, REGN, and generate each level depending on that voltage. The Vcom and Vgoff voltages can be alternated with any voltages. Connect Vcom to the panel.



Note 1) The capcitor is 0.1uF (B characteristics).
Use the 1 uF (B charactersitics) capacitor for other positions. Connect the capacitor for stabilization to TESTA1 through TESTA4 according to the display quality and power consumption.
Note 2) Insert a shot-key barrier diode. (VF =0.4V/20mA, VR≥ 30V / Hitachi product:HRC0203B, HSC226)

Figure 104 Configuration of the Internal Power-Supply Circuit

Specification of capacitor connected to HD66773

Table 57

The following table indicates the specification of capacitor connected to HD66773.

Capacity of capacitor	Recommendation resist pressure for capacitor	Connect pins
1F (B character)	6V	VREG1OUT, Vci1, Note1 C41-/+, Note1 VCL, V_{COM}H, Note1 V_{COM}L
	10V	DDVDH, C11-/+, C12-/+, C21-/+, C22-/+, C23-/+
	25V	VREG2OUT, VGH, VGL, DC31-/+, VgoffH, VgoffL
0.1F (B character)	25V	NOTE2 (TESTA3), NOTE2 (TESTA4)
0.1F (B character)	6V	V0P, V0N, V31P, V31N

Note1: According to the mode set HD66773, there is one cases in which capacitor is unnecessary.

2: Connect a capacitor for stabilization according to the picture quality and power consumption.

Pattern Diagrams for Voltage Setting

Figure 105 shows a pattern diagram for the HD66773 voltage setting and an example of waveforms.

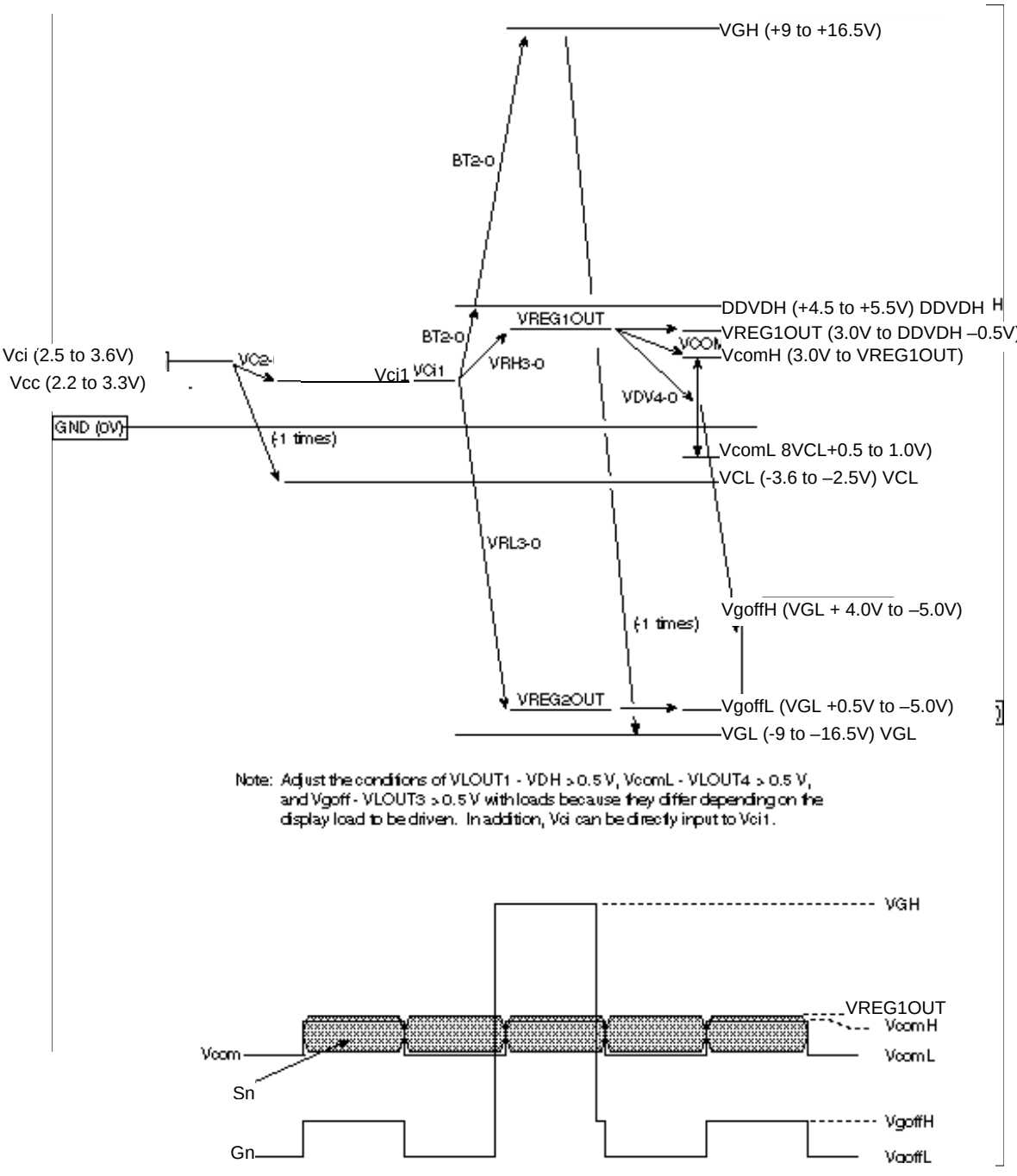


Figure 105 Pattern Diagram and an Example of Waveforms

Absolute Maximum Ratings

Table 58

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	Vcc	V	-0.3 to + 4.6	1, 2
Power supply voltage (2)	Vci-GND	V	-0.3 to + 4.6	1, 2
Power supply voltage (3)	DDVDH-GND	V	-0.3 to + 6.0	1, 2
Power supply voltage (4)	GND-VCL	V	-0.3 to + 4.6	1, 2
Power supply voltage (5)	DDVDH-VCL	V	-0.3 to + 9.0	1
Power supply voltage (6)	VGH- GND	V	-0.3 to + 18.5	1, 2
Power supply voltage (7)	GND- VGL	V	-0.3 to + 18.5	1, 2
Input voltage	Vt	V	-0.3 to Vcc + 0.3	1
Operating temperature	Topr	°C	-40 to + 85	1, 3
Storage temperature	Tstg	°C	-55 to + 110	1

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limit is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2. Indicate the voltage form GND

3. DC characteristics and AC characteristics of shipping chips and shipping wafer are guaranteed at 85 °C.

DC Characteristics (V_{CC} = 2.2 to 3.3 V, Ta = –40 to +85°C*[1])

Table 59

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	V_{IH}	V	V_{CC} = 2.2 to 3.3 V	0.7 V_{CC}	—	V_{CC}	2, 3
Input low voltage (1) (OSC1 pin)	V_{IL1}	V	V_{CC} = 2.2 to 3.3 V	–0.3	—	0.15V_{CC}	2, 3
Input low voltage (2) (OSC1 pin)	V_{IL2}	V	V_{CC} = 2.2 to 3.3 V	–0.3	—	0.15V_{CC}	2, 3
(Except OSC1 pin)			Vcc = 2.4 to 3.3V	–0.3	—	0.2 V_{CC}	2, 3
Output high voltage (1) (DB0-17 pins)	V_{OH1}	V	I0H = -0.1mA	-0.75Vcc	—	—	2
Output low voltage (1) (DB0-17 pins)	V_{OL1}	V	Vcc = 2.2V to 2.4V, I_{OL} =0.1mA	—	—	0.2Vcc	2
			Vcc = 2.4V to 3.3V, I_{OL} =0.1mA	—	—	0.15Vcc	2
I/O leakage current	I_{Li}	µA	Vin = 0 to Vcc	- 1	—	1	4
Current consumption during normal operation (Vcc – GND)	I_{OP}	µA	Ta = 25°C, 260,000 colors display, Vcc = 3V, CR oscillation; fosc = 176kHz (176 line drive), RAM data: 0000h, AP=001, CAD=1, VCOMG=1 VCI1 = 0.92 x VCI (VC2-0 = 001), DDVDH = 2 x VCI1, VGH = 3 x VCI2 (BT2-0 = 000), Step up circuit 1 = 60 divided cycle, Step up circuit 2, 3, and 4 = 240 divided cycle (DC2-0 = 000), VREG1OUT = REGP x 1.65 = 4.55V, (VRH = 0011) VCOMH = VREG1OUT x 0.76 = 3.46V, (VCM = 10011), VCOML = 3.46 – (VREG1OUT x 1.23) = -2.13V, (VDV = 10110), VREG2OUT = VCI x –5.5 = -16.5V, (VRL = 1001), VgoffL = -16.5V, VgoffH = -16.5V + 5.59V = -10.9V	—	90	200	5
Current consumption during standby mode (Vcc – GND)	I_{VGL}	µA	V_{CC} = 3V, VGL = -5.5V, Ta = 25°C	—	—	40	5
Current consumption during standby mode (VGL – GND)	I_{ST}	µA	Vcc = 3V, Ta <=50°C	—	0.1	5	5
			Vcc = 3V, Ta >50°C	—	—	20	
Output voltage deviation	Vo	$_m$V	—	—	5	—	7
Dispersion of the average output voltage	V	$_m$V	—	—	—	35	8

AC Characteristics (V_{CC} = 2.2 to 3.3 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 2.2 to 3.3 V)

Table 60

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
External clock frequency	Fcp	kHz	V_{CC} = 2.2 to 3.3 V	100	176	600	8
External clock duty ratio	Duty	%	V_{CC} = 2.2 to 3.3 V	45	50	55	8
External clock rise time	Trcp	µs	V_{CC} = 2.2 to 3.3 V	—	—	0.2	8
External clock fall time	Tfcp	µs	V_{CC} = 2.2 to 3.3 V	—	—	0.2	8
R-C oscillation clock	f_{OSC}	kHz	Rf = 240kΩ, V_{CC} = 3 V	184	229	274	9

80-system Bus Interface Timing Characteristics

Normal Write Mode (HWM=0) (Vcc = 2.2 to 2.4 V)

Table 61

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	600	—	—
	Read	t_{CYCR}	ns	Figure 1	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	300	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Setup time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure1	10	—	—
Address hold time		t_{AH}	ns	Figure 1	5	—	—
Write data set up time		t_{DSW}	ns	Figure 1	60	—	—
Write data hold time		t_{H}	ns	Figure 1	15	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

High-Speed Write Mode (HWM=1) (Vcc = 2.2 to 2.4 V)

Table 62

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	200	—	—
	Read	t_{CYCR}	ns	Figure 1	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	90	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 1	10	—	—
Address hold time		t_{AH}	ns	Figure 1	5	—	—
Write data set up time		t_{DSW}	ns	Figure 1	60	—	—
Write data hold time		t_{H}	ns	Figure 1	15	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

Normal Write Mode (HWM=0)
(Vcc = 2.2 to 2.4 V)
Table 63

Item		Symbol	Unit	Test Condition	Min	Typ	Max	Note
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	200	—	—	
	Read	t_{CYCR}	ns	Figure 2	300	—	—	
Write low-level pulse width		PW_{LW}	ns	Figure 2	40	—	—	
Read low-level pulse width		PW_{LR}	ns	Figure 2	150	—	—	
Write high-level pulse width		PW_{HW}	ns	Figure 2	100	—	—	
Read high-level pulse width		PW_{HR}	ns	Figure 2	100	—	—	
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25	
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—	When using status read
					0	—	—	When not using status read
Address hold time		t_{AH}	ns	Figure 2	2	—	—	
Write data setup time		t_{DSW}	ns	Figure 2	60	—	—	
Write data hold time		t_{H}	ns	Figure 2	2	—	—	
Read data delay time		t_{DDR}	ns	Figure 2	—	—	100	
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—	

High-Speed Write Mode (HWM=1)

(Vcc = 2.4 to 3.3 V)

Table 64

Item		Symbol	Unit	Test Condition	Min	Typ	Max	Note
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	100	—	—	
	Read	t_{CYCR}	ns	Figure 2	300	—	—	
Write low-level pulse width		PW_{Lw}	ns	Figure 2	40	—	—	
Read low-level pulse width		PW_{LR}	ns	Figure 2	150	—	—	
Write high -level pulse width		PW_{HW}	ns	Figure 2	40	—	—	
Read high -level pulse width		PW_{HR}	ns	Figure 2	100	—	—	
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25	
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—	When using status read
					0			When not using status read
Address hold time		t_{AH}	ns	Figure 2	2	—	—	
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—	
Write data hold time		t_{H}	ns	Figure 2	2	—	—	
Read data delay time		t_{DDR}	ns	Figure 2	—	—	100	
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—	

Reset Timing Characteristics

(V_{CC} = 2.2 to 3.3 V)

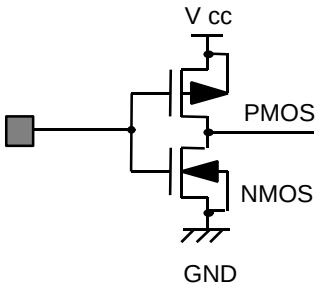
Table 65

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Reset low-level width	t_{RES}	ms	Figure 2	1	—	—
Reset rise time	t_{rRES}	µs	Figure 2	—	—	10

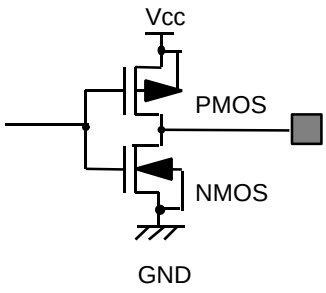
Electrical Characteristics Notes

1. For bare die and wafer products, specified up to 85°C.
2. The following three circuits are I pin, I/O pin, O pin configurations.

Pins: RESET*, CS*, E/WR/SCL, RW/RD, RS, OSC1, IM3-1, IM0/ID, TEST1, TEST2, TESTV1, DCTEST



Pins: OSC2



Pins: DB17 -DB2, DB1／SD0, DB0/SDI

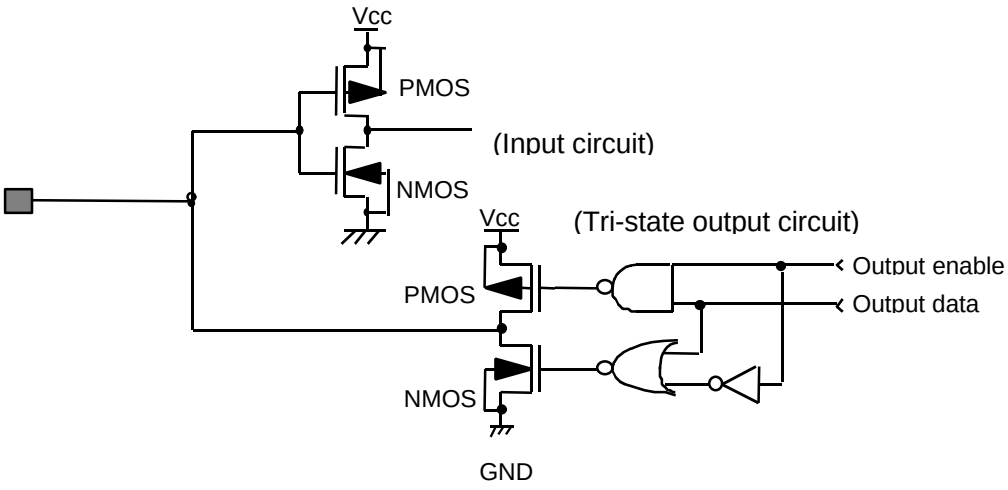


Figure 106 I/O Pin Configuration

3.The TEST1, TEST2/TESTV1, DCTEST pin must be grounded and the IM3/IM2/IM1 and IM0/ID pins must be grounded or connected to Vcc.

4.This exclude the current flowing through output drive MOSs.

5.This exclude the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin is low or high when an access with the interface pin is not performed, current consumption does not change.

6.The following show the relationship between the operation frequency (fosc) and current consumption (Icc) (figure).

7.Dispersion of the average output voltage is the difference of the average of output voltage between chips next to each other.

8.Applies to the external clock input (figure).

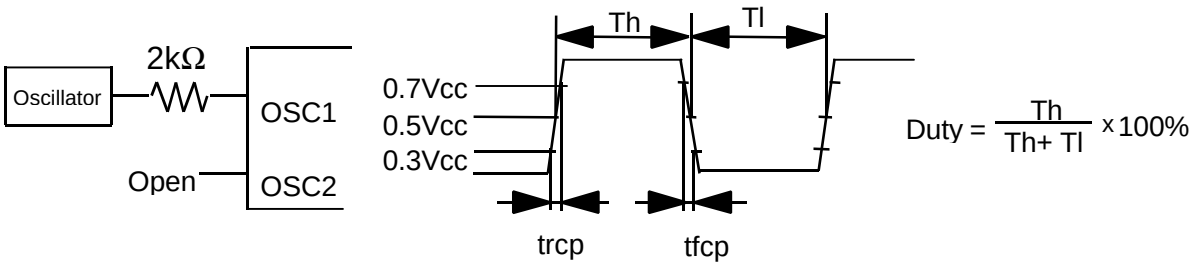
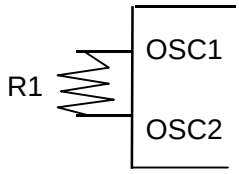


Figure 107 External Clock Supply

9. Applies to the internal oscillator operations using external oscillation resistor Rf (figure and table).



Shorten these pin's wiring as much as possible, because the number of oscillation wave changes according to the capacity of OSC1, OSC2 pins.

Figure 108 Internal Oscillation

(Referential Data)

Table 66

R-C Oscillation Frequency: fosc (kHz)

Oscillation Resistance (kW)	Vcc = 2.0 V	Vcc = 2.4 V	Vcc = 3.0V	Vcc = 3.3V
110kΩ	362.6	399.4	438.5	447.6
150kΩ	285.4	313.3	337.4	343.4
180kΩ	252.2	274.0	294.9	302.1
200 kΩ	230.4	251.5	268.7	274.8
240 kΩ	201.3	216.8	229.4	234.8
270 kΩ	181.3	195.1	206.9	210.2
300 kΩ	166.1	178.2	187.5	191.1
390 kΩ	133.7	142.3	148.9	151.6
430 kΩ	121.6	129.0	135.2	137.3

AC Characteristics Test Load Circuits
Data bus: DB17 to DB0

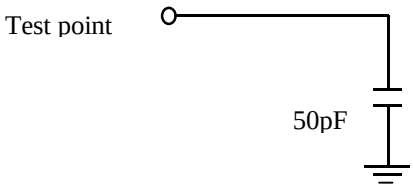


Figure 109 Load Circuit

80-system Bus Operation

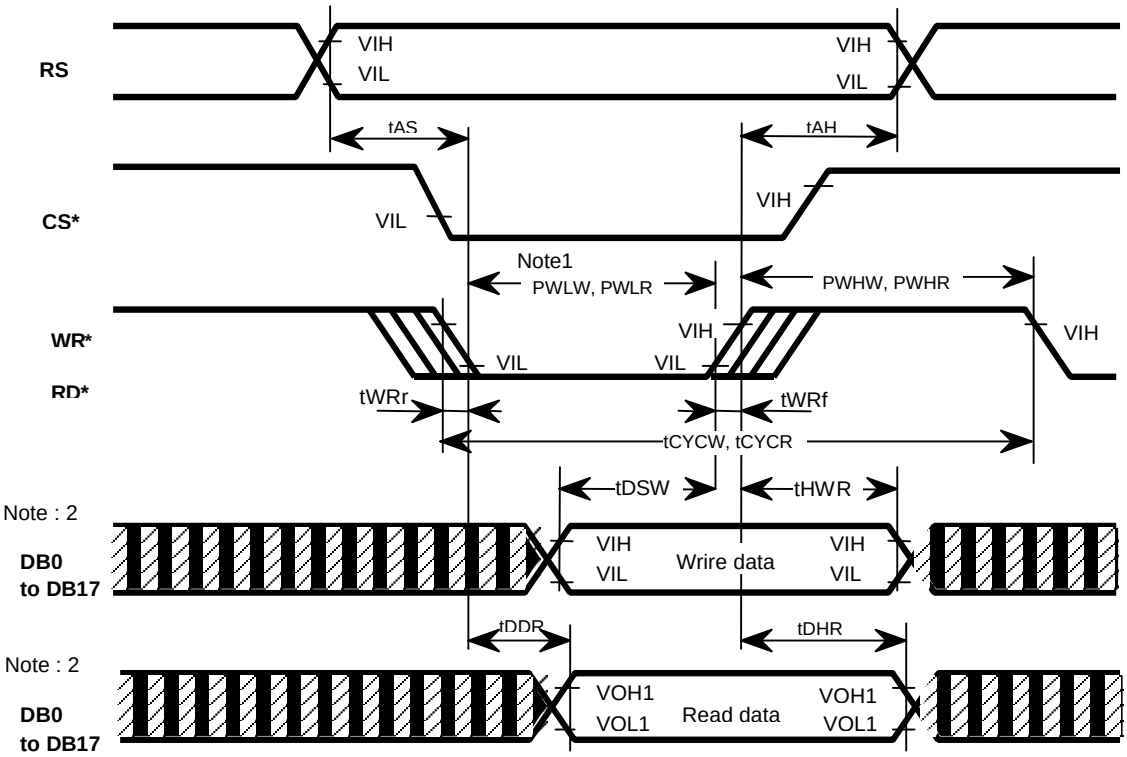


Figure 110 80-system Bus Timing

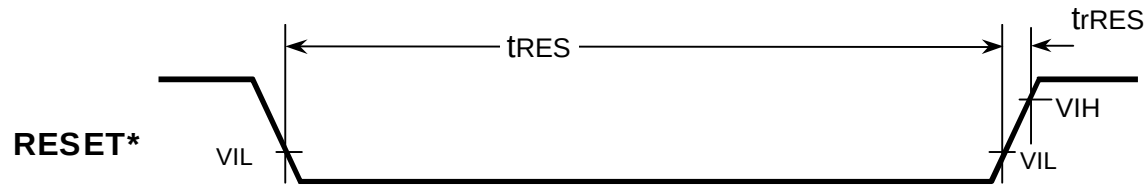
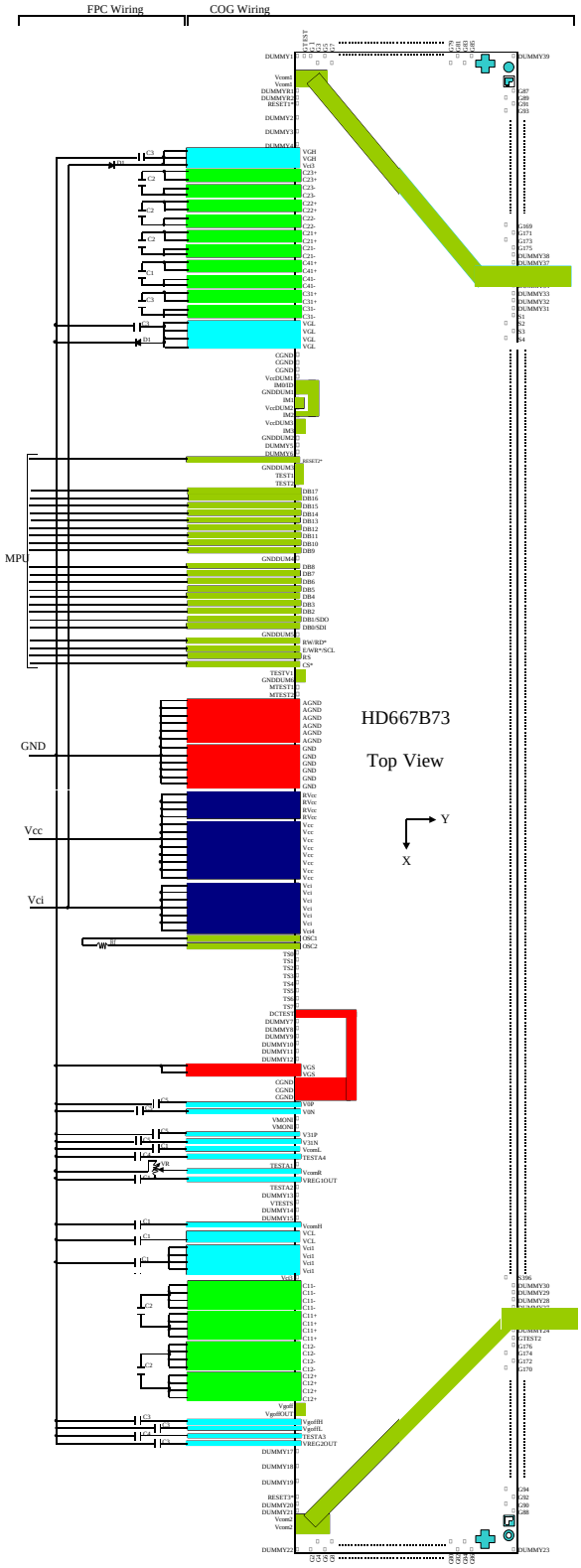


Figure 111 Reset Timing

■ Writing Example of HD66773 (260,000 color mode)

Writing example shile using 80i/F 18bit (VGS = GND)



Rev. 0.0	2002.04.16
Rev. 0.1	2002.04.22

External parts
D1: Shot key barrier diode
VF=0.4/20mA (approximately), VR>=30V

C1: Capacitor 1uF Pressure resistance 6V

C2: Capacitor 1uF Pressure resistance 10V

C3: Capacitor 1uF Pressure resistance 25V

C4: Capacitor 0.1uF Pressure resistance 25V

C5: Capacitor 0.1uF Pressure resistance 6V

Rf: Oscillation resistance TBD

VR: Variable resister

Figure 112 Reset Timing

Maintenance history report
P = page, L = line, - = blank

Rev	Date	Page	Maintenance history
0.1	2002.5.24		First edition
1.0	2002.10.17	1	Description: line 4/ Change “1.8V” to “2.2V”.
		2	Low-power operation supports: Change “Vcc = 1.8 to 3.3V” to “2.2 to 3.3V”
			Output power supply voltage: Change “VcomH-GND = VDH max” to “VREG1OUT (max).
		8	Connect pin of RESET 1, 2, and 3: Change “MUP or Reset generating Circuit” to “MPU or RESET generating circuit”.
			Functions of Vcc, GND: Change “1.8V” to “2.2V”.
			Connect pin of DDVDH: Change “Capacitor for stabilization or power supply” to “Capacitor for stabilization or open”.
			Functions of DDVDH: Change “ connect an external power supply lower than 5.5V” to “leave it open”.
		13	Power supply circuit for LCD opeartion: Change “VDH, VGH, VGL, VgoffOUT, Vcom” to “V0P, V0N, V31P, V31N, VGH, VGL, VgoffOUT, Vcom”.
		22	Index (IR): line 1/ Change “(R00h to R4h)” to “(R00h to R3B)”.
		26	Table 10: Step-up Cycle in Step-up Circuit 1/ Change “DCCLK divided by 15” to “DCCLK divided by 60”, change “DCCLK divided by 60” to “DCCLK divided 15”.
			Table 10: Step-up Cycle in Step-up Circuit 2/ Change “DCCLK divided by 240” to “DCCLK divdied by 60”, change “DCCLK divided by 60” to “DCCLK divided by 240”.
		27	VC2-0: Change “VC2-0= “1111”” to “VC2-0 = “111””.
			VRL3-0: Change “(voltate for the reference voltage, VREG2 while generating Vgoff.)” to “(voltage for the reference while generating Vgoff.)”.
			VRH3-0: Change “VREGOUT1” to “VREG1OUT”.
			Change “(REGP from 1.33 to 2.85 times)” to “(REGP from 1.33 to 2.775 times)”.
			VCOMG: “When VCOMG = 0 and when Vcom is driven in A/C, setting of the VDV4-0 is invalid.”: Delete “when Vcom is driven in A/C” from the sentence.
			VDV4-0: “When Vcom is not driven in A/C, the set up is invalid.” Delete “When Vcom is not driven in A/C” from the sentence.
		29	Table 13: VREG1OUT Voltage/ Change as follows. REGP x 2.325 times → REGP x 2.175 REGP x 2.475 times → REGP x 2.325 REGP x 2.625 times → REGP x 2.475 REGP x 2.700 times → REGP x 2.625 REGP x 2.775 times → REGP x 2.700 REGP x 2.850 times → REGP x 2.775
		34	Delete Table 19, and 20 in rev. 0.1.
			Table 19 Bits and Operation: Add GON and DTE to the table.
		35	Table 22 Add “Note” under the table.

Rev	Date	Page	Maintenance history
1.0	2002.10.17	37	Figure 33: Right figure: Change “SCN4-0 = 00111” to “SCN4-0 = 01110”.
		59	Table 36: AM setting for High-speed RAM write: Change “AM = 1/0” to “AM = 0””.
		73	Figure 84: the bottom figure: Change the length of right and left arrows. (Refer to the figure.)
		76	Figure 87: Change “VRP0 2 ~ 30-R” to “VRP0 0 ~ 30R”. Change “VRN0 2 ~ 30R” to “VRN0 0 ~ 30R”.
		79	Table 41: Change register value “VRP (N)0 [4:0]” to “VRP(0)[3:0].
		81	Table 45: Change Formula for V1 from “V4+V3D+(VINP1-V4)*(8/24)” to “V3D+(VINP1-V3D)*(8/24)”.
		83	Table 47: Change Formulq for V1 form “V4+(V3D+(VINP1-V4)*(8/24)” to “V3D+(VINP1-V3D)*(8/24)”.
		90	Add a new figure.
		99	Figure 104: Delete shotkey diode between Vci and Vci2
		101	Figure 105: Change “Vcc (1.8 ~ 3.3V)” to “(2.2 ~ 3.3V)” in upper figure. Change “Vcom (3.0 ~ VDH)” to “Vcom (3.0 ~ VREG1OUT) in upper figure. Change “VDH” to “VREG1OUT” in lower figure.
		103	Change “Vcc = 1.8V ~ 3.7V” to “Vcc = 2.2V ~ 3.3V” for DC characteristics
			Add a row of “Current consumpition during standby mode (VGL-GND)
		104	Delete 68 Bus interface timing characteristics Table 57,58,59, and 60 in rev.0.1.
			Table 61 and 62: Change “Vcc = 1.8” to “Vcc = 2.4”.
			Table 61 and 62: Change Test Condition “Figure2” to “Figure 1”.
		105	Table 63 and 64: Change Test Condition “Figure2” to “Figure1”.
			Table 65: Change “Vcc = 1.8 to 3.3V” to “Vcc = 2.2 to 3.3V”.
			Table 65: Change Test Condition from “Figure 4” to “Figure 2”.
			Table 65: Change Unit for Reset rise time from “ns” to “ s”
			Table 65: Change Max for Reset rise time from “100” to “10”.
		107	Delete Figure 107 “R-C oscillation frequencies” and note 7 in Rev. 0.1.
		108	Fill in contents of Table 66 “R-C Oscillation Frequency: fosc (kHz).
			Delete Figure 110 <Reference data> and note 11 in Rev. 0.1.
			Delete Figure 112 “Load Circuit” in Rev. 0.1.
		109	Delete Figure 113 “68-system Bus Operation” in Rev. 0.1.
			Dlete Figure 115 “Clock Synchronized Serial Interface Timing” in Rev. 0.1.
		110	Add a new page “Writing Example of HD66773 (260,000 color mode).
1.0-1	2002.10.28	3	Correct pin name “YM0N1” to “VM0NI”
		4	Correct Figure 2.
		5	Correct Table 1. (No.55 to No.62)
		99	Correct Figue 104.