LPC2300 Series
I2S Audio Interface
USB Audio Demo

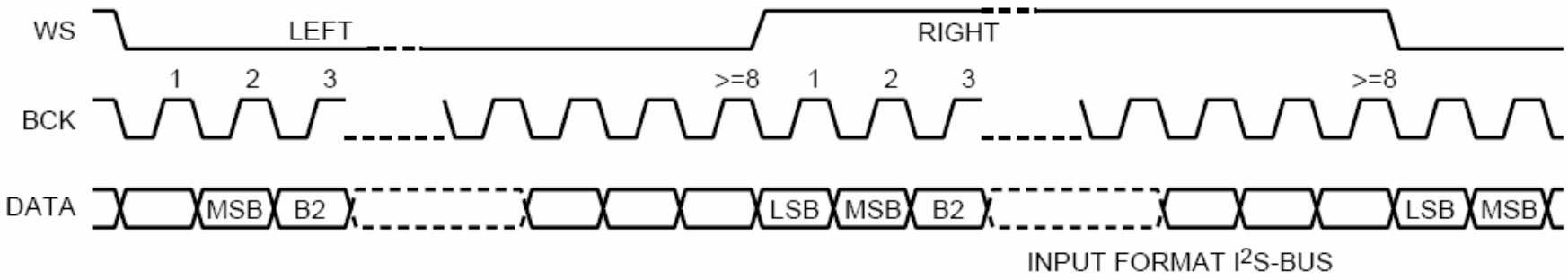
ARM Devcon
October 2007

I2S Interface

A standard communication interface for digital audio applications.

- The I2S bus specification defines a 3-wire serial bus, having 1 data, 1 clock, and one word select signal.
- The basic I2S connection has one master, which is always the master, and one slave.
- The I2S interface on the LPC2300 provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

I2S Format



INPUT FORMAT I²S-BUS

LPC2300 I2S Interface

- The I2S input can operate in both master and slave mode.
- The I2S output can operate in both master and slave mode,
- I2S Input and output are independent.
- Capable of handling 8, 16, and 32 bit word sizes.
- Supports Mono and stereo audio data
- The sampling frequency can range (in practice) from 16 - 48 kHz. (16, 22.05, 32, 44.1,48 kHz).
- Word Select period in master mode is configurable output
- Two 8 byte FIFO data buffers are provided, one for transmit and one for receive.
- Generates buffer level interrupt requests
- Two DMA requests, connected to the General Purpose DMA controller.
- Controls include reset, stop and mute options separately for I2S input and I2S output.

I2S Interface

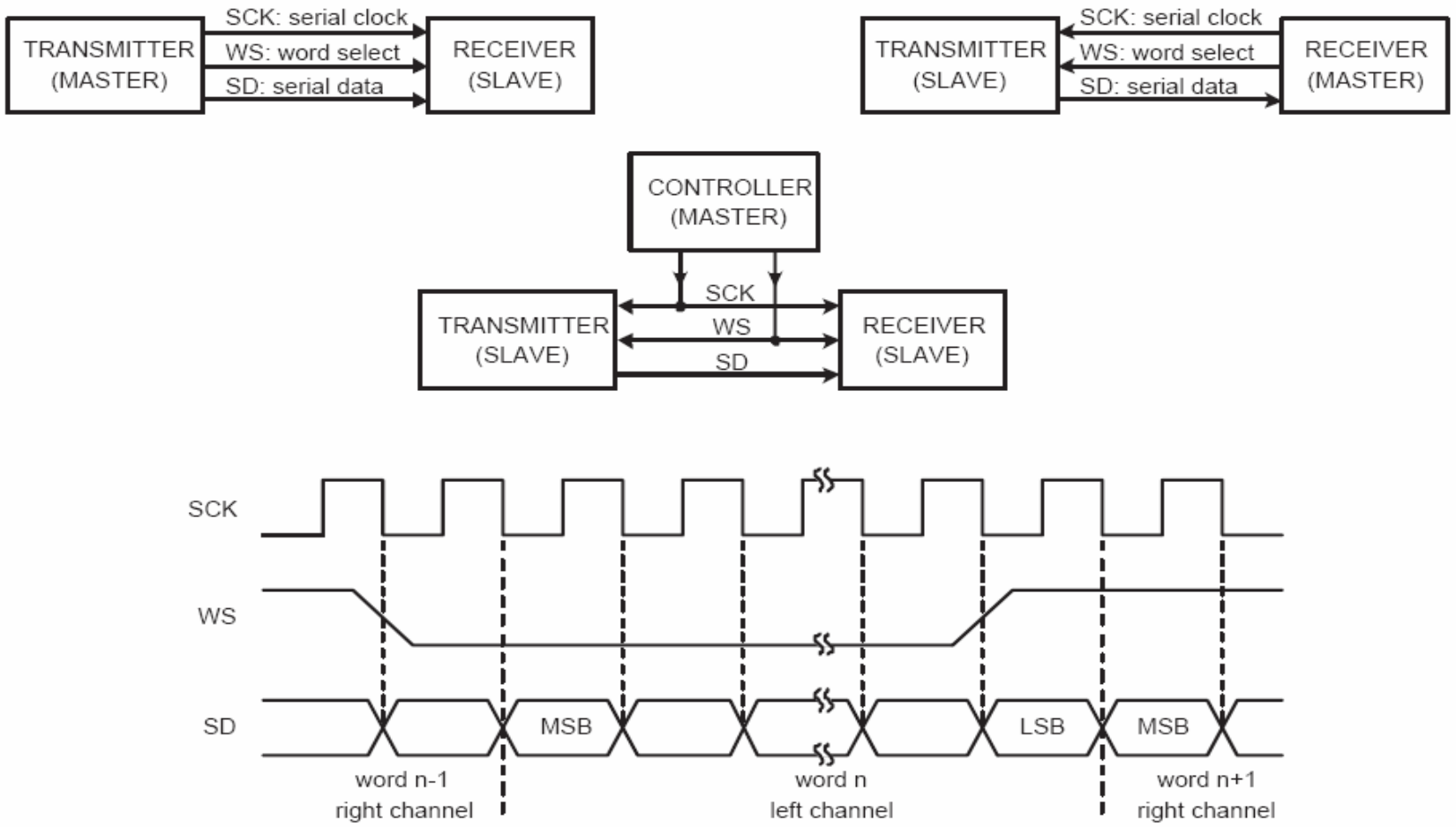
a standard communication interface for digital

Application	Sample Rate	Word Width	Format	Uncompressed bit rate
Telephone Audio	8 kHz	8-bit	Mono	64 kbps
FM Radio	22.050 kHz	16-bit	Stereo	705.6 kbps
CD Audio	44.1 kHz	16-bit	Stereo	1411.2 kbps
DAT Tape	48 kHz	16-bit	Stereo	1536 kbps
High End Audio	96 kHz	24-bit	Stereo	4608 kbps

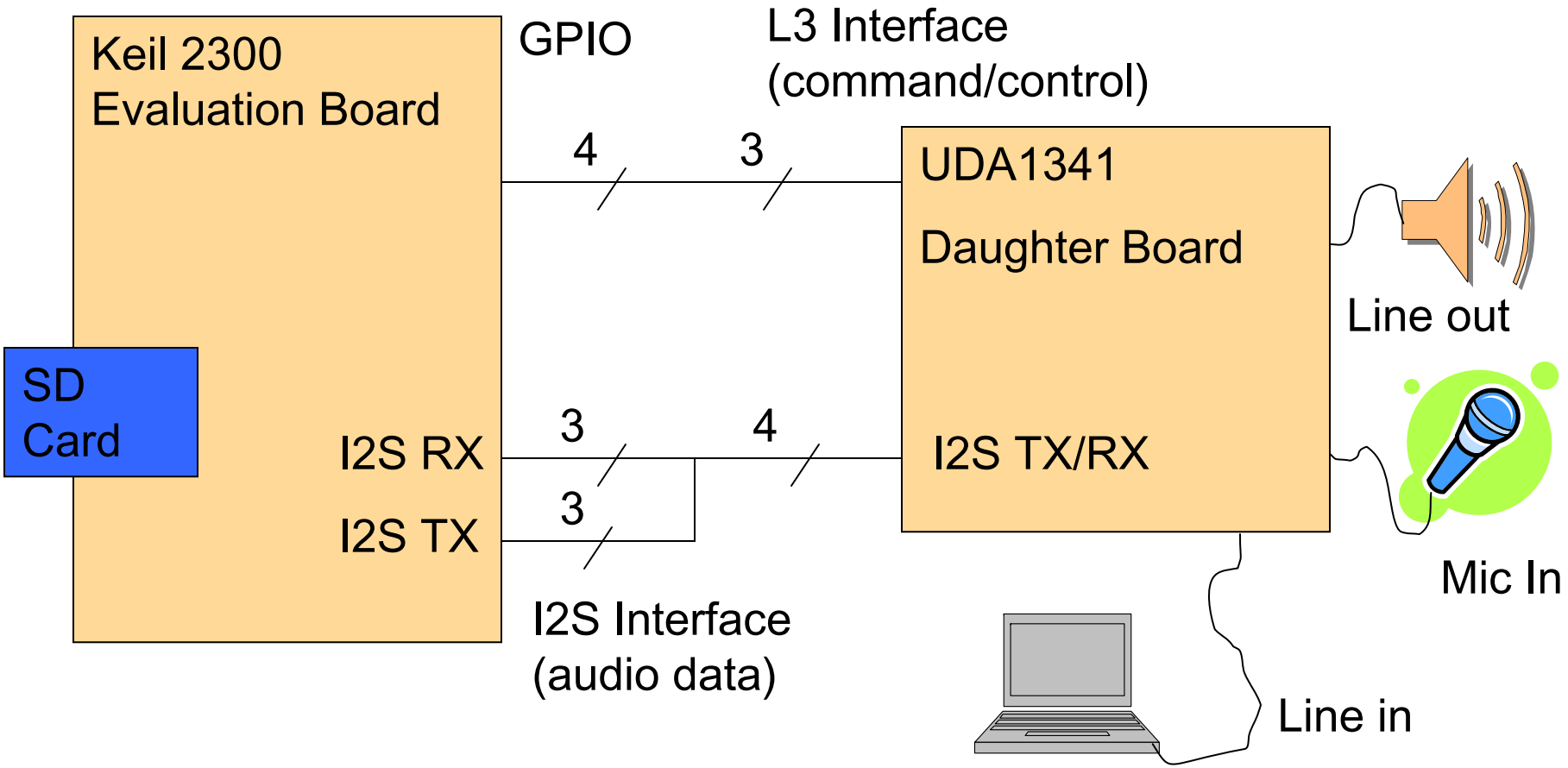
Source Wikipedia

Compression reference	Bit rate
MP3	128 kbps

I2S Interface

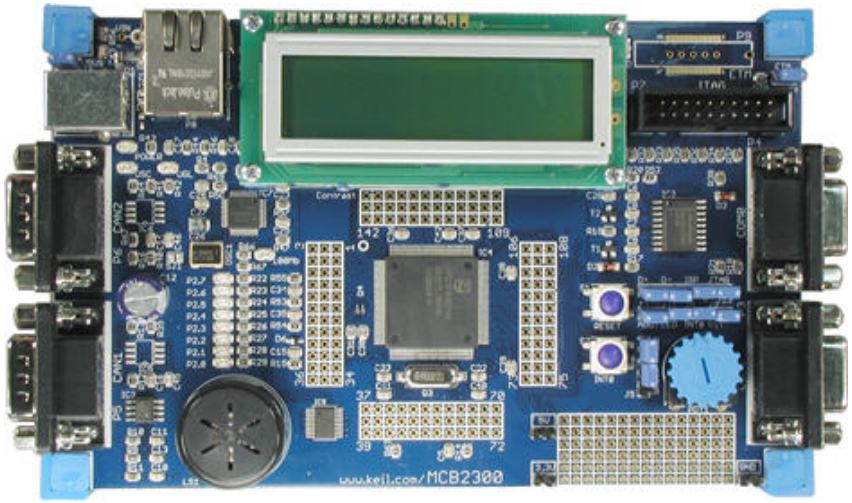


System Diagram



MCB2300 Evaluation Board from Keil

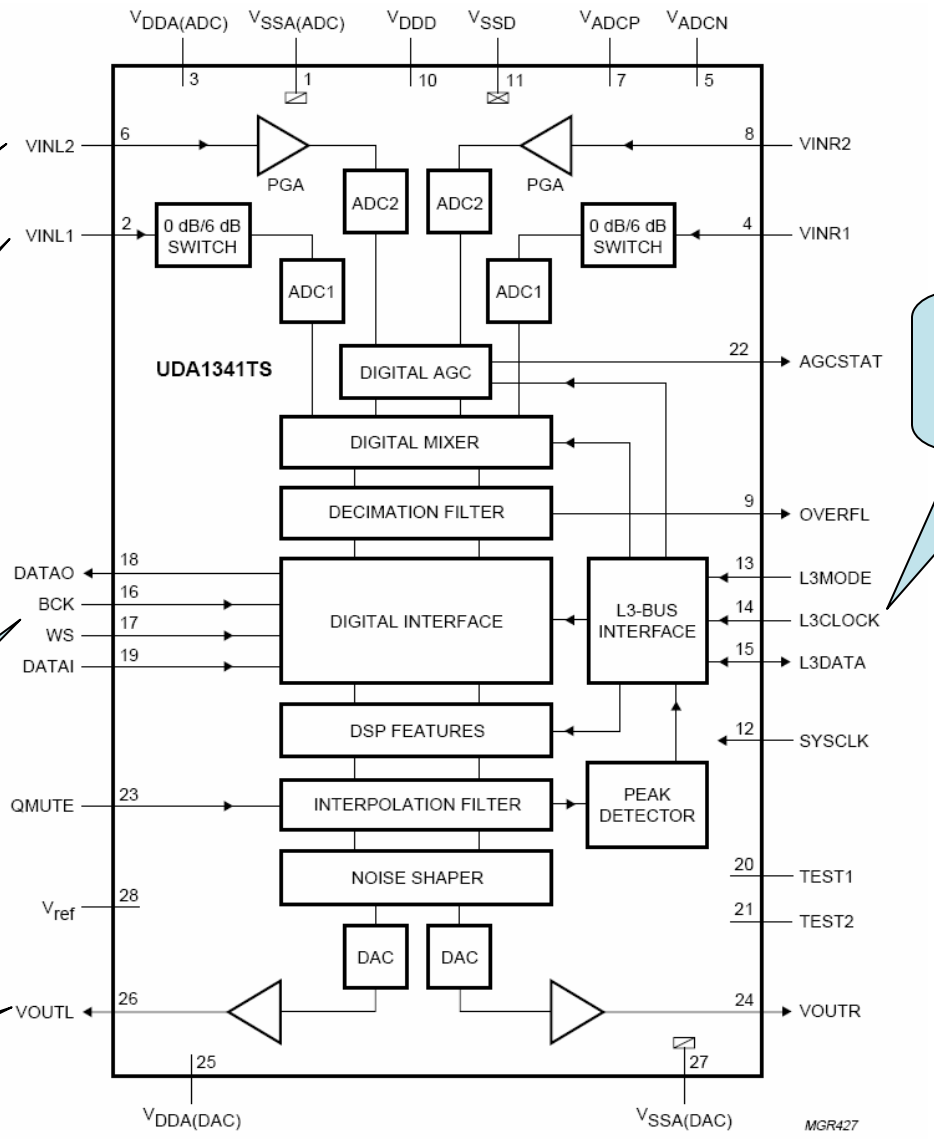
- Connects to your PC using:
  - Serial port for Flash download using FlashMagic
  - JTAG interface for program debug using the Keil ULINK and µVision IDE and Debugger
- Two board options:
  - MCB236x with 100 pin LPC2368
  - MCB237x with 144 pin LPC2378
- Board features:
  - On-chip Ethernet interface
  - USB device interface
  - Two serial interfaces
  - Two CAN interfaces
  - Speaker
  - Analog input (via potentiometer)
  - Eight LEDs



- Available directly from Keil or from NXP's Distributors starting $199

UDA1341TS

Economy audio CODEC for MiniDisc (MD) home stereo and portable applications



MIC In

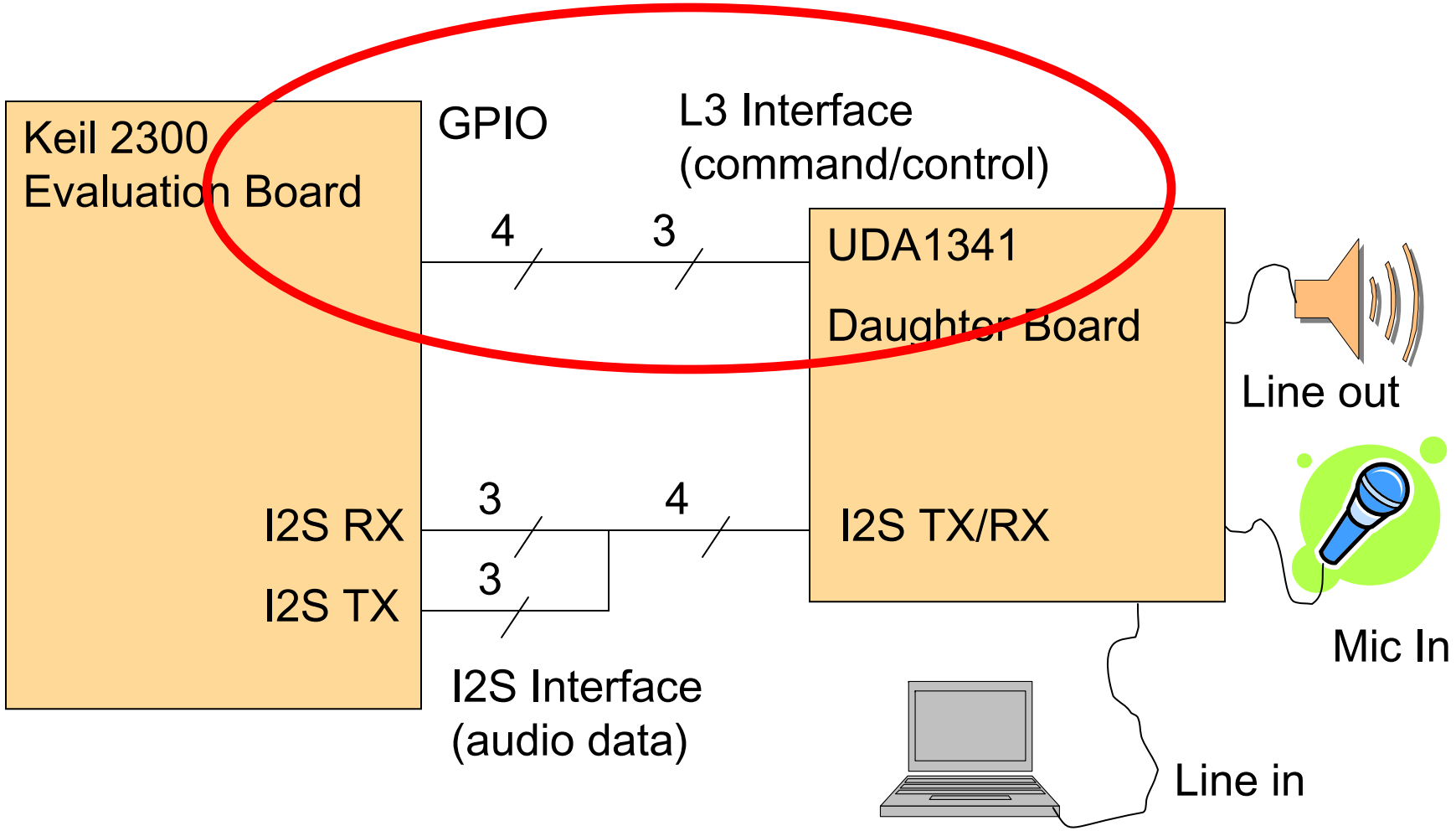
Line In

I2S Interface

Audio OUT

L3 Interface

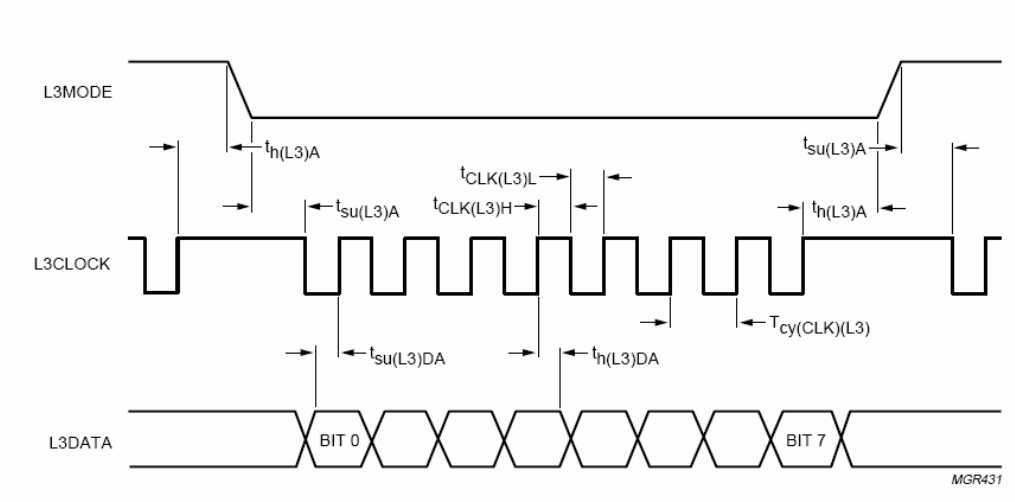
System Diagram



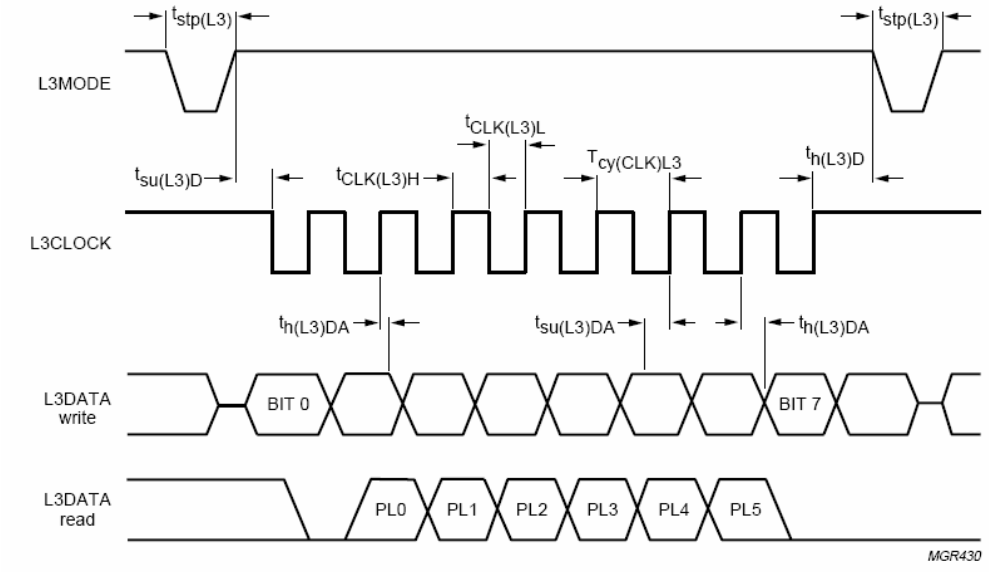
L3 Interface

- For command and control of UDA1341
- Controls the UDA1342 filters (volume, mute, bass, treble, etc…)
- Software driven from GPIO interface on LPC2378

L3 V1 interface timing on the UDA1341



Address mode



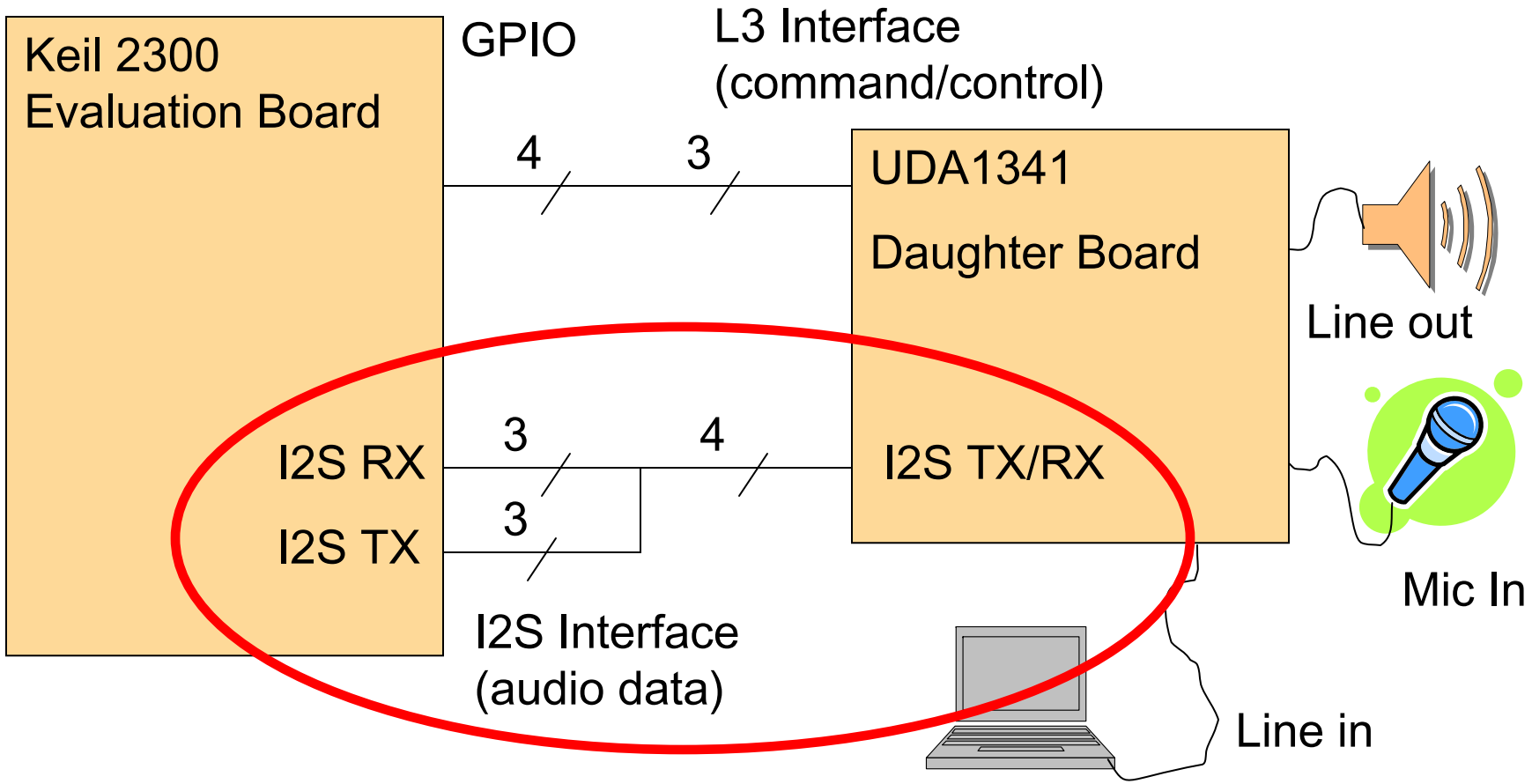
Data mode

Table 17 Data transfer of type 'DATA0'

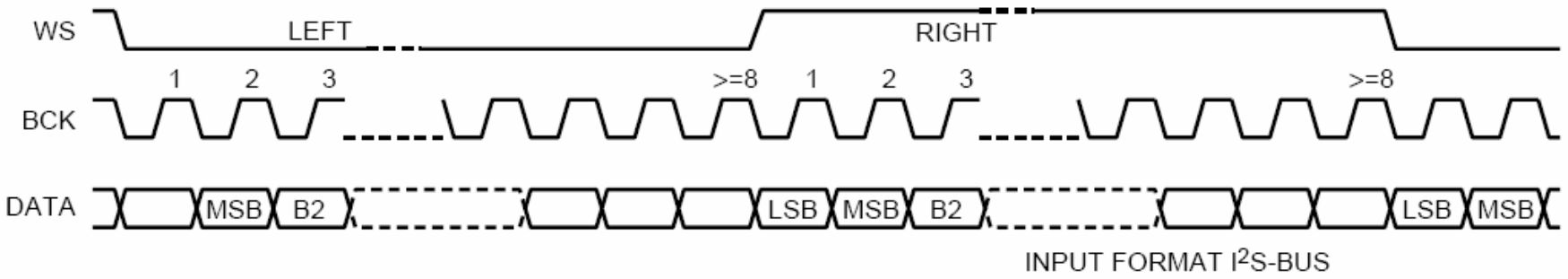
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	VC5	VC4	VC3	VC2	VC1	VC0	VC = volume control (6 bits)
0	1	BB3	BB2	BB1	BB0	TR1	TR0	BB = bass boost (4 bits)
								TR = treble (2 bits)
1	0	PP	DE1	DE0	MT	M1	M0	PP = peak detection position
								DE = de-emphasis (2 bits)
								MT = mute
								M = mode switch (2 bits)
1	1	0	0	0	EA2	EA1	EA0	EA = extended address (3 bits)
1	1	1	ED4	ED3	ED2	ED1	ED0	ED = extended data (5 bits)

Sample Data Commands on the UDA1341

System Diagram



I2S Format

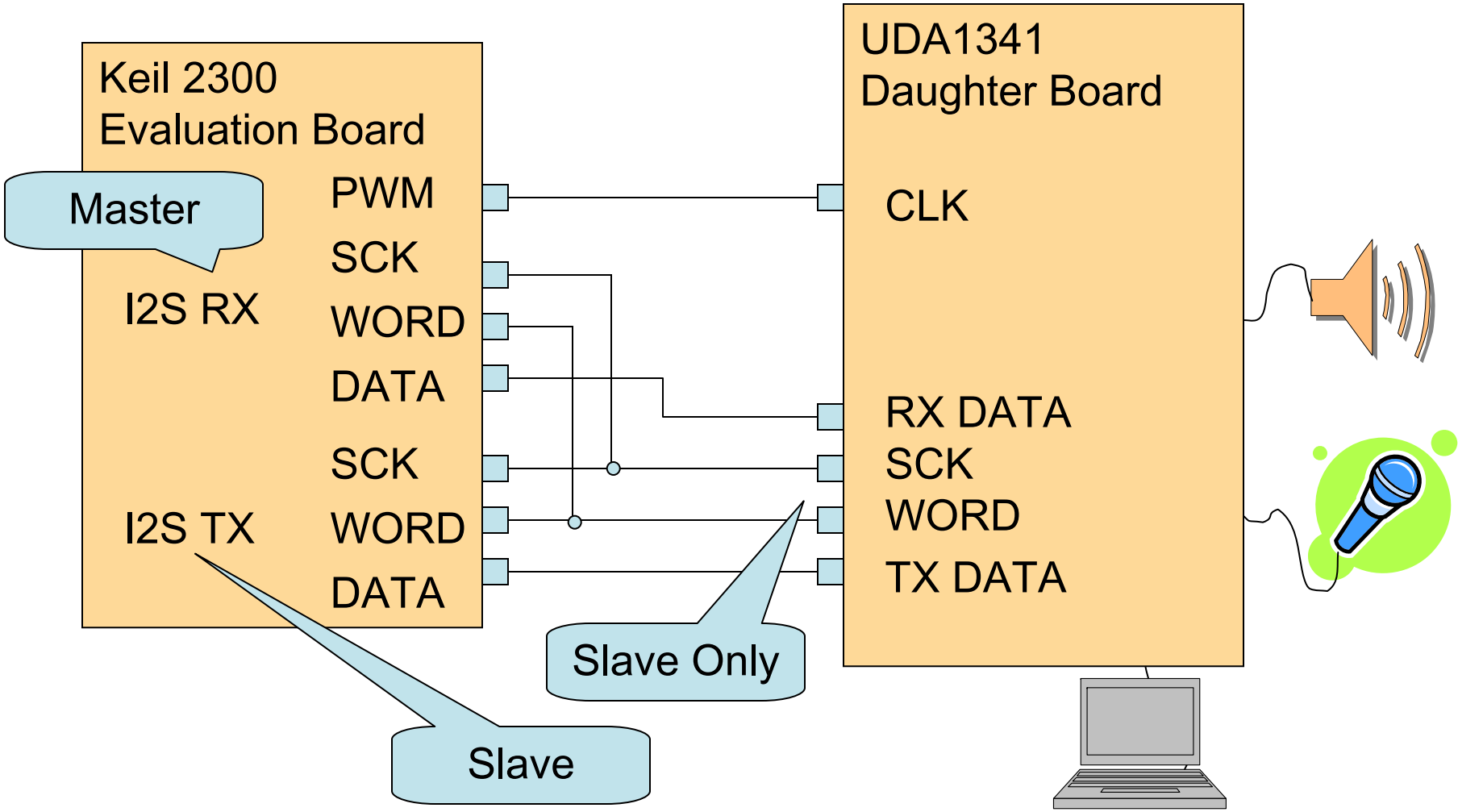


INPUT FORMAT I^2S-BUS

I2S interface

- Transmits and/or receives audio data stream
- LPC2378 has two separate I2S channels; one for TX, one for RX
- UDA1341 uses single clock for both TX and RX I2S lines
- Solution is to set LPC2378 I2S RX as master and I2S TX as slave
  - RX clock output feeds TX clock input

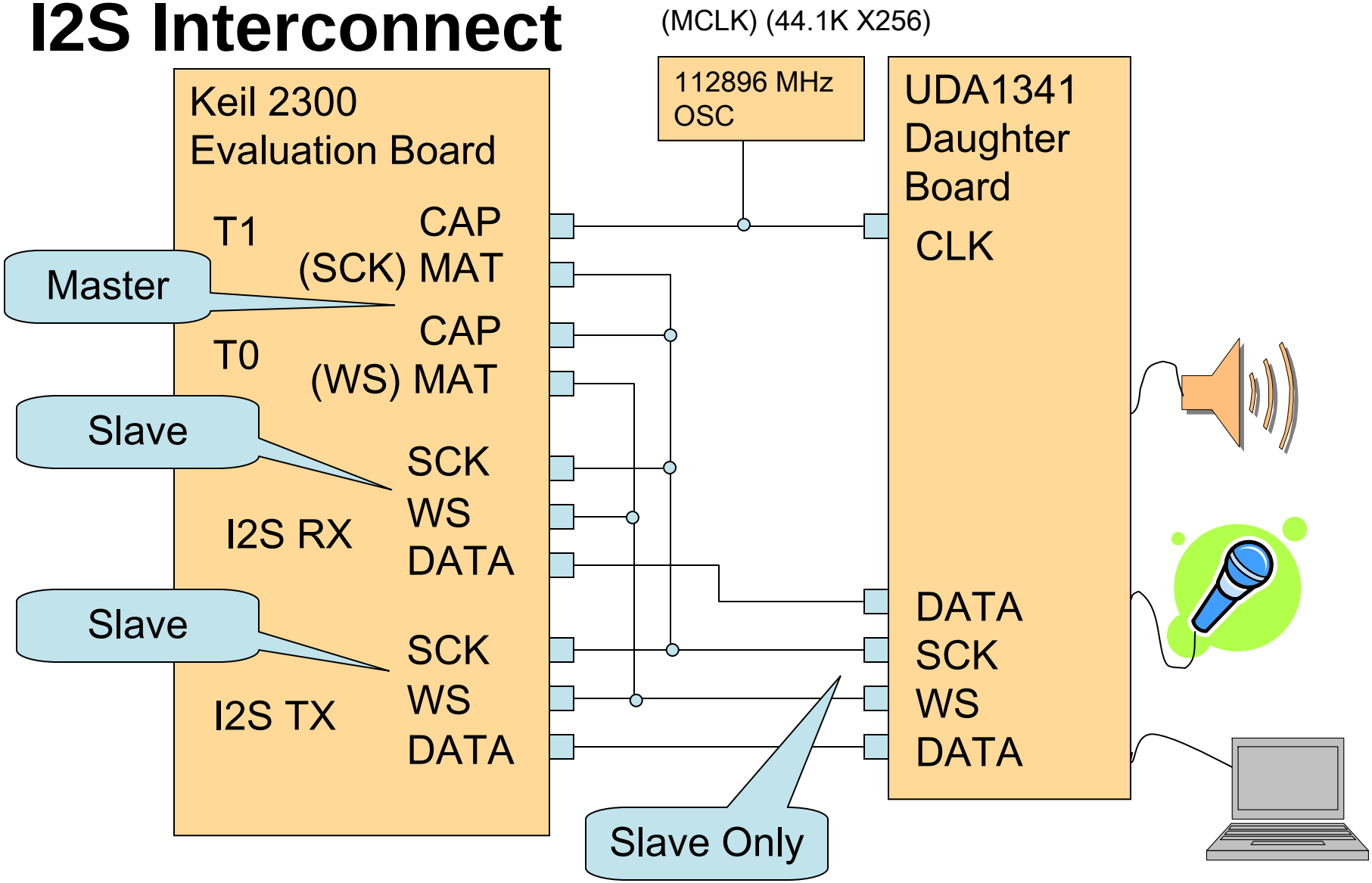
I2S Interconnect



I2S interface and USB clocking

- Transmits and/or receives audio data stream
- LPC2378 has two separate I2S channels; one for TX, one for RX
- UDA1341 uses single clock for both TX and RX I2S lines
- LPC2300 requires a 48 MHz USB clock
- The UDA1341 Demands in-Phase OSC clock and I2S Clock
- Problem: the timing requirements needed by the UDA1341 and the USB conflict
- Solution is an external oscillator to clock the UDA1341 and input into the capture pin of a timer. The timer is simply a divider to generate the I2S Bit clock (SCK) timing. The external match output of the timer is then feed to second capture input of another timer for division to generate I2S Word Clock (WS) on that timers Match output.
- The TWO timers together act as an I2S master clocking system supplying the WS and SCK inputs. Tx and RX FIFO's supplied by the LPC23xx I2S Slaves
- All other I2S interfaces are configured as slaves

I2S Interconnect



Timings

- OSC always 11.2896 MHz (256X44.1Khz)
- Timers configured to use rising edge capture; means 1/2 frequency then use count register for additional divide
- 8-Bit data word on I2S

  SCK = t1 = 11.2896 MHz /8 = 1.4112 MHz/2 = 705.60 KHz

  WS = t0 = (t1)/8 = 705.60 KHz / 8 = 88.2 KHz/2 = 44.1KHz
- 16-Bit data word on I2S

  SCK = t1 = 11.2896 MHz /4 = 2.8224 MHz/2 = 1.4112 MHz

  WS = t0 = (t1)/16 = 1.4112 MHz / 16 = 88.2 KHz/2 = 44.1KHz
- 32-Bit data word on I2S

  SCK = t1 = 11.2896 MHz /2 = 5.6448 MHz/2 = 2.8224 MHz

  WS = t0 = (t1)/32 = 2.8224 MHz / 32 = 88.2 KHz/2 = 44.1KHz

DEMO