SE6100

ASK Transceiver IC

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Description

The SE6100 is a single chip ASK (Amplitude Shift Key) transceiver IC.
It is designed to operate in low power µC-controlled and stand alone applications with half duplex data transmission.
The unsymmetrical antenna input and output are separated for applications with apart transmission and receiving antenna.
The SE6100 is suitable for European or North American ISM band applications.
Integrated functions as stand by mode, low bat control, RSSI output, level detector, locked loop detection, and clock output for µC offer features for universal applications.

Features

- ❑ Single chip ASK Transceiver
- ❑ Wide frequency range (200 .. 500 MHz)
- ❑ Low voltage operation (2.3 .. 3.6 V)
- ❑ Low power consumption
- ❑ PLL with 25 kHz channel space
- ❑ Adjustable output power
- ❑ High sensitivity
- ❑ Data rates up to 9600 bps
- ❑ Stand alone application available
- ❑ Automotive temperature range
- ❑ TQFP32 Package and Die

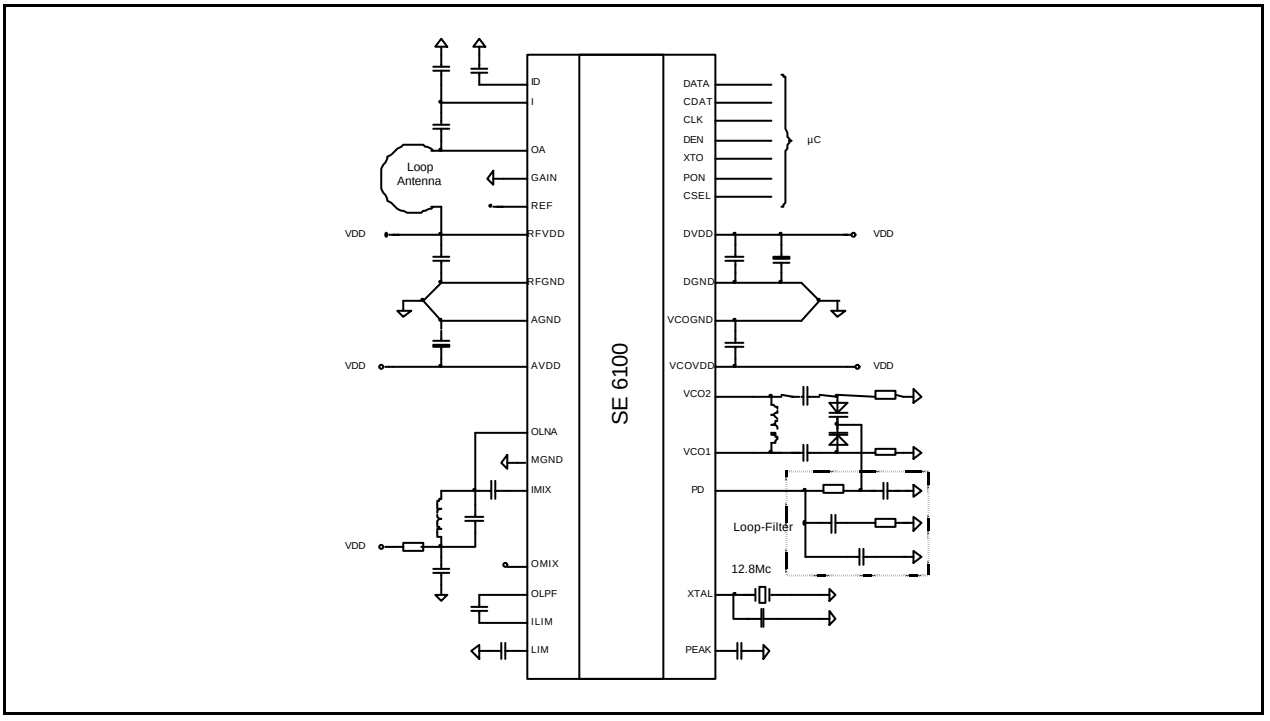
Applications

- ❑ Intelligent keyless entry
- ❑ Security systems
- ❑ Remote control systems
- ❑ Communication systems

Medical applications

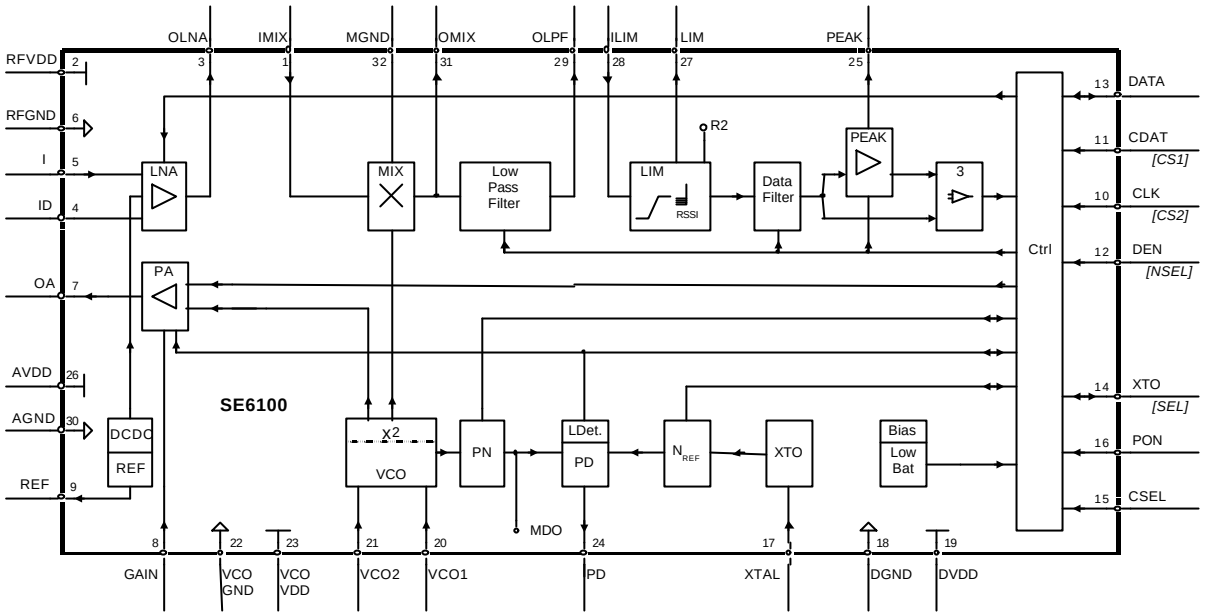
Typical Application

Low power data transceiver using SE6100



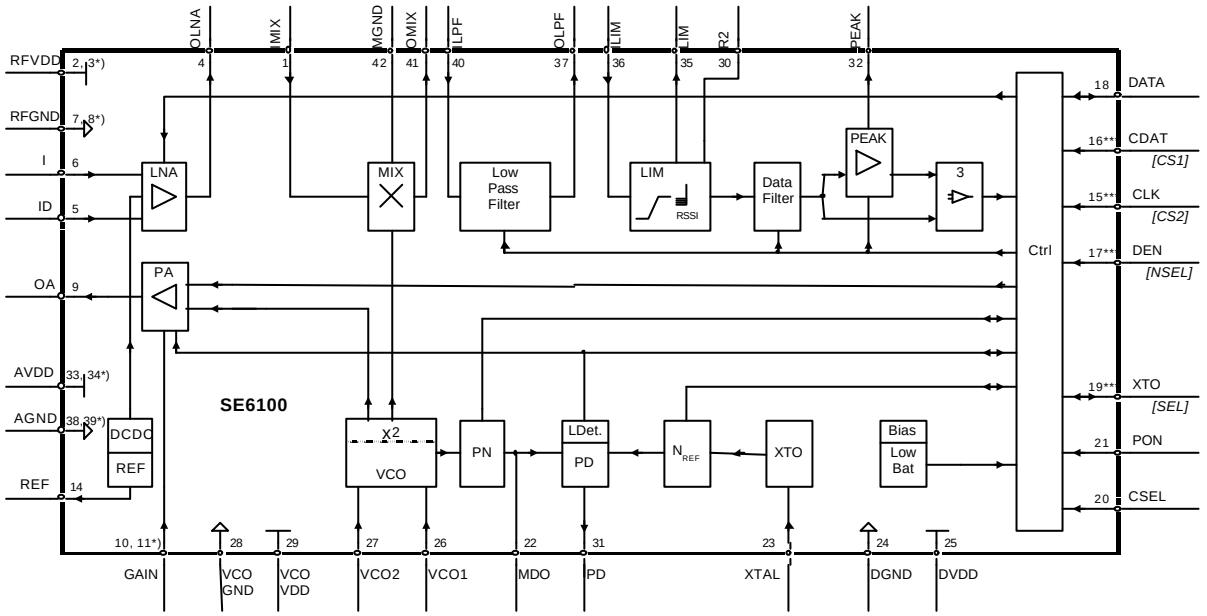
Device Block Diagram

TQFP32



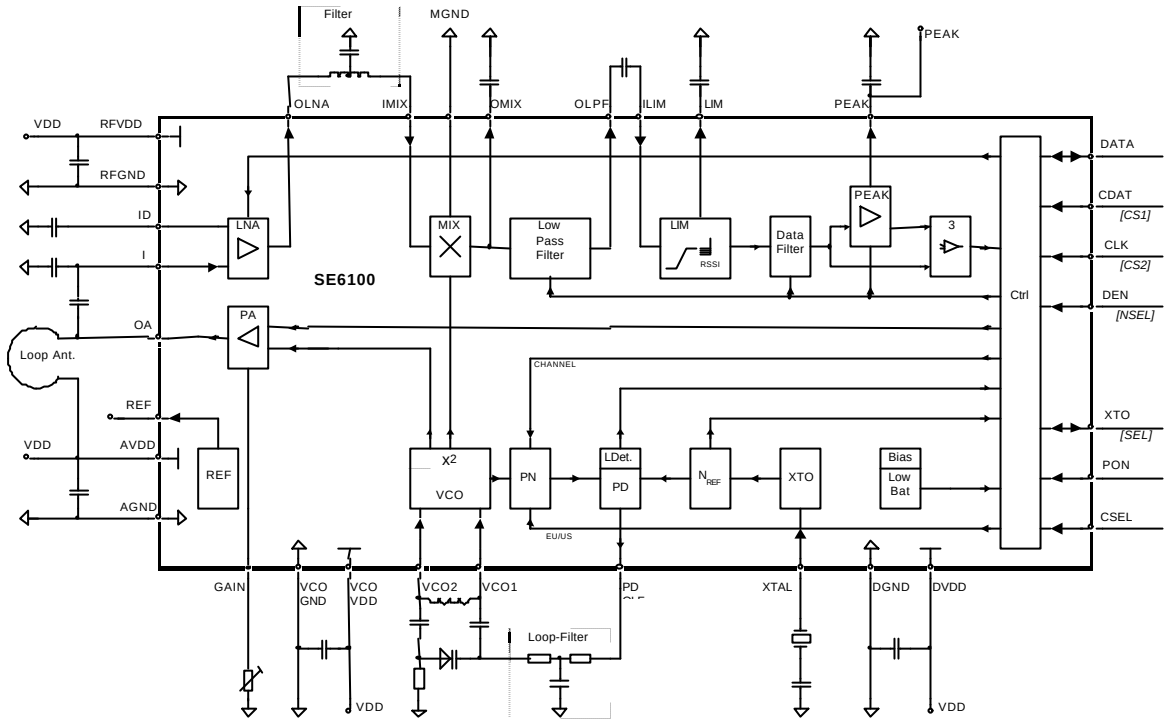
[***] different Pin functions in case of stand alone application

DIE



[***] different Pin functions in case of stand alone application
[*] double bonding required

Functional Block Diagram



[***] different Pin functions for stand alone application

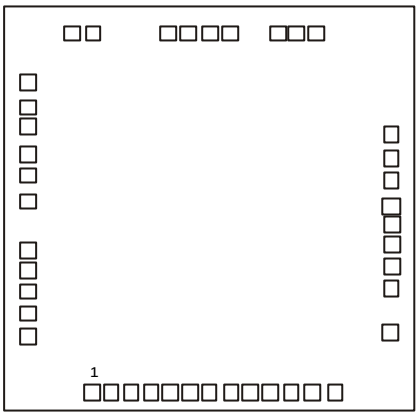
Device PinOut (package: TQFP32, Die)

Pin	Pad	Symbol	Description
1	1	IMIX	Mixer Input
2	2,3 [1)]	RFVDD	RF Supply
3	4	OLNA	Low Noise Amplifier Output
4	5	ID	LNA Input decoupling (emitter)
5	6	I	LNA Input (base)
6	7,8 [1)]	RFGND	RF Supply Ground
7	9	OA	Power Amplifier Output
8	10,11 [1)]	GAIN	Gain Adjust (Power Amplifier)
	12		Not used
	13		Not used
9	14	REF	Reference voltage output(for external LNA/Power Amp)
10	15	CLK / CS2 [2)]	Shift Register Clock / Channel Selector Bit 2 [2)]
11	16	CDAT / CS1 [2)]	Serial Input for Control Data Shift Register / Channel Selector Bit 1 [2)]
12	17	DEN / NSEL [2)]	Control Data Enable / Divider Switch [2)]
13	18	DATA	Data-Input/Output
14	19	XTO / SEL [2)]	Clock Output for µC / RX/TX Selection [2)]
15	20	CSEL	Control Switch
16	21	PON	Power up/down
	22	MDO	Test Pad, do not connect
17	23	XTAL	Crystal-Oscillator Input
18	24	DGND	Digital Supply Ground
19	25	DVDD	Digtal Supply Voltage
20	26	VCO1	Voltage Controlled Oscillator
21	27	VCO2	Voltage Controlled Oscillator
22	28	VCOGND	VCO Supply Ground
23	29	VCOVDD	VCO Supply
	30	R2	Test Pad, do not connect
24	31	PD	Charge Pump Output
25	32	PEAK	Peak Detector Output, RSS / Output
26	33,34 [1)]	AVDD	Analog Supply Voltage
27	35	LIM	Limiter Decoupling
28	36	ILIM	Limiter Input
29	37	OLPF	Low Pass Filter Output
30	38,39 [1)]	AGND	Analog Supply Ground
	40 [1)]	ILPF	Low Pass Filter Input
31	41 [1)]	OMIX	Mixer Output
32	42	MGND	Mixer Ground

[1)] double bonding required [2)] different pin function in case of stand alone mode

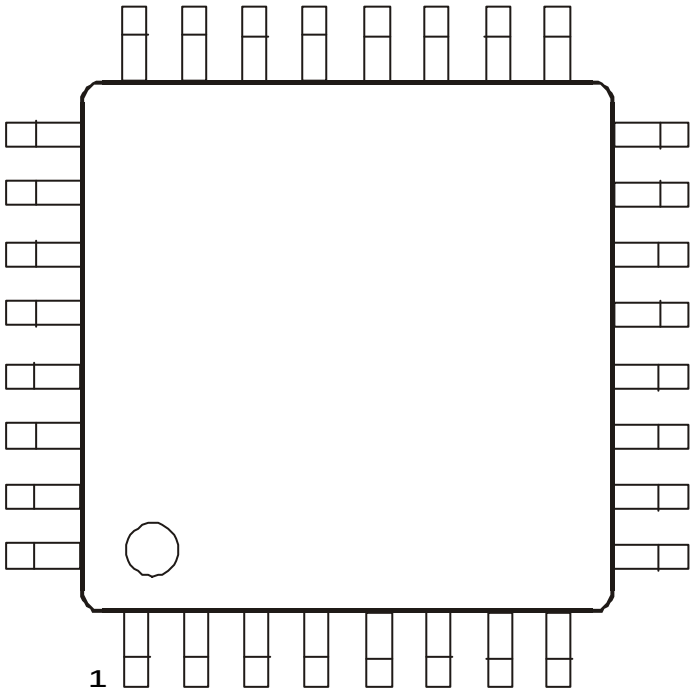
ESD protection according to MIL-STD. 883c (minimum 2kV)
except pins IMIX, OLNA, I1, OA, VCO1, VCO2 (minimum 1kV)

PAD-LAYOUT



Chip size: 2,53 mm x 2,59 mm
Chip thickness: 340 µm

PIN-LAYOUT



Housing type: TQFP 32

Block by Block Description

- LNA
  Single input and output
  Especially designed for small loop antennas
  Disable feature (for using external LNA)
  Suitable to use the same antenna for receiving and transmitting mode (half duplex)
  full gain: 17dB (depending on external circuitry)
  gain reducing: about 17dB (using the -20dB switch)
  IP3 = +1.3dBm (full gain)
  IP3 = +4dBm (reduced gain)
  NF ≈ 3dB (R_G=1.5kΩ)

- Mixer
  Single input and single current output
  Maximum output frequency 100kHz
  Mixer gain: 27dB

- LPF
  Single current input
  Bessel filter (n=10)
  Selectable Bandwidth 40kHz / 80kHz
  Gain ≈ -2dB
  3dB Bandwidth: 38kHz / 75kHz
  maximum attenuation: 77dB (BW=80kHz); >80dB (BW=40kHz)
  70dB attenuation @ 270kHz (BW=40kHz); @450kHz (BW=80kHz)

- Mixer/LPF
  IP3 = 4.5dBm (at limiter input)
  V_{ONOISE} = 150µV (BW=40kHz)
  V_{INOISE} = 8µV (R_G = 50Ω)

- Limiter / RSSI Detector
  Limiter amplifier with 7 stages
  internal speed load circuit for input coupling capacitors
  t_{ON} about 5ms
  RSSI Detector with 7 stages and current output
  IF Bandwidth about 150kHz
  Dynamic Range about 70dB
  minimum input sensitivity: 200µV_{RMS}

- Data Demodulator / Signal Detector
  Data Filter: Sallen-Key-Low Pass Filter
  Selectable Bandwidth: 5k / 10k bps
  1 Comparator for pulse generation
  3 comparators to detect input voltage level

- Whole Receiver
  minimum input sensitivity: 4µV (R_G = 50Ω)
  minimum input sensitivity with transformation circuit: -102dBm
  maximum input voltage (full LNA gain): 2mV
  maximum input voltage (reduced LNA gain): 11mV
  maximum input voltage (LNA disabled): 100mV
  IP3: -14dBm (full LNA gain)
  IP3: 1.8dBm (reduced LNA gain)
  power on settling time: 18ms
  60 channel change settling time(µC-mode): 4ms
  TX RX mode settling time (µC-mode): 3ms
  RX TX mode settling time (µC-mode): 2ms

- Power Amplifier (ASK)
  Single output (open collector)
  Output current control (external resistor)

- Whole Transmitter
  TX-Peak Current consumption (DATA=high, R_{GAIN}=0): about 5.6 mA
  TX-Quiescent Current consumption (DATA=low, R_{GAIN}=0): about 3.1mA
  RF output voltage @ 50Ω: about 190mV_{RMS}
  RF_ON / RF_OFF blanking : about 75dB
  power on settling time: 18ms
  RX TX mode settling time: 2ms

- Voltage Controlled Oscillator
  Cross coupled oscillator
  Oscillator frequency f_{Center} = 216.95 MHz / 157.5 MHz (EU / US)
  Fixed Frequency-Doubler (multiplies by 2)
  Frequency control by external Varicap and other external components
  Tuning range ± 5 MHz (depends on external components)
  $V_{VCO1/2}$ = 320mV_{PP} (L_{OSC} = 120nH)

- Reference Oscillator (XTO)
  Crystal oscillator
  Frequency 12.8 MHz
  V_{XTAL} = 1.9V_{PP}
  Power on settling time (measured at XTO –output): 15ms

- Reference Divider
  Divides by 1024 → 12.5kHz channel space for PLL (with multiplier: 25 kHz)
  XTO output: 25 kHz, 50 kHz, 100kHz, 200kHz, 400kHz, 800kHz, 1.6MHz, no signal (recommended if not used)

- Main Divider
  Programmable divider with swallow counter
  64 channels (channel width 25 kHz)
  2 selectable frequency bands:
    EU: f_{Center} = 433.9MHz, Divider Ratio: 17324 ..64.. 17387
    US: f_{Center} = 315.0MHz, Divider Ratio: 12568 ..64.. 12631
  Maximum divider input frequency: 270MHz

- Frequency / Phase Detector (PD)
  Frequency and Phase Detector with charge pump
  Selectable charge pump current (40 / 80 µA)
  Lock In Detector
  Lock Detect History Flag
  Lock-In-Time: about 4ms (for a 60 channel change)

- Control Block
  Controls the functionality of the circuit for both µC and stand alone applications
  Selection of control mode by Pin CSEL (µC/stA)
  Stand alone mode: reduced functionality
  µC mode: controlled by 16 Bit words

- REF/LBAT
  Reference voltage for optional external LNA and Booster
  V_{REF} (ext.) = 1.13V [200µA load current]
  V_{TRH} (LBAT) = 2.3V typical
  V_{TRH} (LBAT) + 2.45V
  V_{TRH} (LBAT) ++ 2.6V typical

Selected Pin Functions

Control Pins

- PON

PON → GND : active
PON → VDD : power down

- CSEL

CSEL → GND : µC application (all functions controlled by a serial data word)
CSEL → VDD : stand alone application (different Pin functions: CDAT→CS1, CLK→CS2, DEN→NSEL, XTO →SEL)

Stand Alone Pin Functions

- CS1 / CS2

CS1 and CS2 are connected directly to the channel decoder to select one of 2^2 available channels.

CS2	CS1	Channel	f_{EU}	f_{US}
low	low	10	433,350MHz	314,450MHz
low	high	14	433,450MHz	314,550MHz
high	low	46	434,250MHz	315,350MHz
high	high	51	434,375MHz	315,475MHz

- SEL

Selects receive or transmit mode:
SEL → GND : receive mode
SEL → VDD : transmit mode
DATA will be wired to RxData or TxData respectively. It is not possible to read out other information like CMPx, LDET, LBAT.

- NSEL

Selects between the European and North American ISM band; connected to the N1 divider to adapt its divider ratio to the frequency range:
NSEL → GND : EU mode
NSEL → VDD : US mode

µC-Application Pin Functions

- CDAT

Serial data input for 16-Bit data words. (LSB first)

- CLK

Clock input for shift register.

- DEN

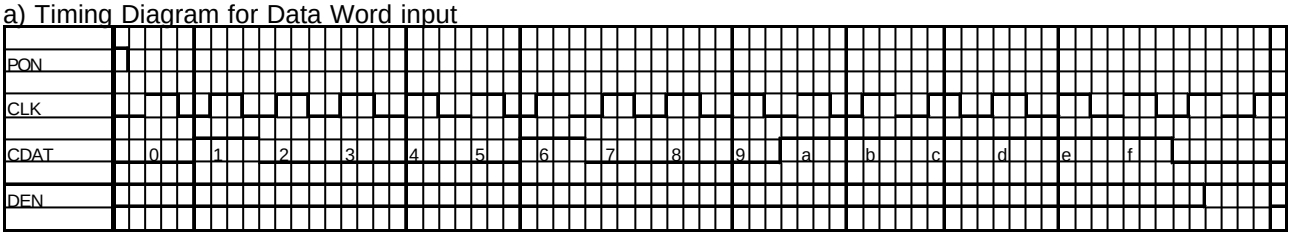
Enables to copy the data word from the input shift register into a 16-Bit parallel output storage register.

- XTO

XTO provides clock signals for external use. The frequency is programmable by the configuration control word. The default frequency is 25kHz. 50kHz, 100kHz, 200kHz, 400kHz, 800kHz, 1.6MHz and 0Hz are also available.
The settling time is about 40us.

Data word description

a) Timing Diagram for Data Word input



The figure shows how to input the data words using the pins CLK, CDAT, DEN. in this special case the data word 010000 1000 111111 (TX mode, TxData connected, Channel63) would be put in. The maximum clock frequency should not exceed 1MHz.

Remark:
The data words have to be sent in the form 'First LSB - Last MSB'. That means for the example (see above):
0100 0010 0011 1111 (LSB in front)
&423f (hexCode)

b) control data word (after PowerOn reset all bits low)

Bit	internal Name	Status	Description
0		low high	marks the data word as control word marks the data word as configuration word
1	RXTX	low high	enables RX mode enables TX mode
2	LNAGAIN	low high	enables maximum LNA gain enables decreased LNA gain (-20dB)
3	DR	low high	enables 9600 bps data rate for data filter enables 4800 bps data rate for data filter
4	BW	low high	enables 80 kHz bandwidth for LPF enables 40 kHz bandwidth for LPF
5	CHPC	low high	enables 40uA charge pump current enables 80uA charge pump current
6-9			I/O buffer activation of RxData / TxData / LBAT / LDET /LDET_HIST / CMP1 / CMP2 / CMP3 / NREF / PN
a-f			2^6 = maximum 64 channel decoder (a 25kHz)

c) configuration data word (optional, after PowerOn reset all bits low)

Bit	internal Name	Status	Description
0			see description of control data word
1	LNADIS	low high	enables internal LNA disables internal LNA
2	LDBP	low high	Loop Detect Bypass off (Default !) Loop Detect Bypass on (Test mode only, Do not use !)
3	EUUS	low high	enables EU frequency range enables US frequency range
4-6			select the output frequency at CLK, default 25 kHz
7	COMP *)	high	enables alternative DataCompTreshold level ($0.7*V_{PEAK}$)
8	LBP *)	high	enables increased LBAT treshold level (approx. +100mV)
9	LBPP *)	high	enables increased LBAT treshold level (approx. +100mV)
a	LDTC *)	high	enables increased current in loopDetectTimer
b-f			Not used

*) not guaranteed function, default low

Logic table of data words (short description)

Control Data Word Description	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f	Remarks
Select Control Word	0																
Select Configuration Word	1																
RX - Mode	0	0															
TX - Mode	0	1															
LNA Gain normal	0		0														
LNA Gain -20dB	0		1														
DataRate=9600bps	0			0													
DataRate=4800bps	0			1													
BandWidth=50kHz	0				0												
BandWidth=25kHz	0				1												
ChargePumpCurrent=40uA	0					0											
ChargePumpCurrent=80uA	0					1											
RX-Data connected to DATA	0						0	0	0	0							
TX-Data connected to DATA	0						1	0	0	0							
LDET connected to DATA	0						0	1	0	0							
LDET_HIST connected to DATA	0						1	1	0	0							
CMP1 connected to DATA	0						0	0	1	0							high input level
CMP2 connected to DATA	0						1	0	1	0							medium input level
CMP3 connected to DATA	0						0	1	1	0							low input level
not used	0						1	1	1	0							
LBAT connected to DATA	0						0	0	0	1							
NREF connected to DATA	0						1	0	0	1							
PN connected to DATA	0						0	1	0	1							
Channel 0-63	0										l	x	x	x	x	m	first LSB, last MSB
Configuration Data Word Description																	
Internal LNA enabled	1	0															
Internal LNA disabled	1	1															
Lock detect bypass off	1		0														
Lock detect bypass on	1		1														test mode only!
EU frequency range	1			0													
US frequency range	1			1													
CLK 25 kHz	1				0	0	0										
CLK 50 kHz	1				1	0	0										
CLK 100 kHz	1				0	1	0										
CLK 200 kHz	1				1	1	0										
CLK 400 kHz	1				0	0	1										
CLK 800 kHz	1				1	0	1										
CLK 1.6 MHz	1				0	1	1										
no signal	1				1	1	1										
COMP Threshold=0.8*Vpeak	1							0									
COMP Threshold=0.7*Vpeak	1							1									
LBAT Threshold 2.3V	1								0	0							
LBAT Threshold 2.45V	1								1	0							
LBAT Threshold 2.6V	1								1	1							

Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances.

Symbol	Parameter	Min	Max	Unit
Tj	Junction Temperature	-55	150	°C
Tstg	Storage Temperature Range	-55	150	°C
V_{DD}	Supply Voltage	-0.5	5.5	V
	Voltage at any Pin (except IMIX, OLNA, I1, OA, VCO1 VCO2)	-0.5	VDD+0.5	V
	Voltage at Pins IMIX, OLNA, I1, OA, VCO1 VCO2	-0.5	5.5	V

Electrical Characteristics

Operational Range

Within the operational range the IC operates as described in the circuit description. The DC and AC limits are not guaranteed.

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	2.3	3.6	V
$f_{EU\ mode}$	frequency (Europe)	433.1	434.675	MHz
$f_{US\ mode}$	frequency (USA)	314.2	315.775	MHz
$N_{CHANNEL}$	Number of channels available	32	64	-
T_A	Ambient Temperature	-40	85	°C

DC Characteristics

Supply voltage: V_{DD} = 3.0 V; Ambient temperature: T_A = 27°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD} TX	Supply Current (TX Mode)			4.8 [1)]	5.6	mA
I_{DD} RX	Supply Current (RX Mode)			4.6	5.4	mA
I_{DD} 0	Supply Current (Sleep Mode)			0.6	1	µA
V_{IH}	Data Input Voltage - logic high	[3)]	$0.7*V_{DD}$	V_{DD}	V_{DD}+0.5	V
V_{IL}	Data Input Voltage - logic low	[3)]	-0.5	0	0.3* VDD	V
I_{IH}	Data Input Current - logic high	[3)]		0	1	µA
$-I_{IL}$	Data Input Current - logic low	[3)]		0	1	µA
V_{OH}	Output Voltage - logic high	[4)]	$0.7*V_{DD}$	V_{DD}	V_{DD}	V
V_{OL}	Output Voltage - logic low	[4)]	0	0	$0.3* V_{DD}$	V
I_{OH}	Output Current - logic high	[4)]	50	>1000		µA
$-I_{OL}$	Output Current - logic low	[4)]	50	>1000		µA

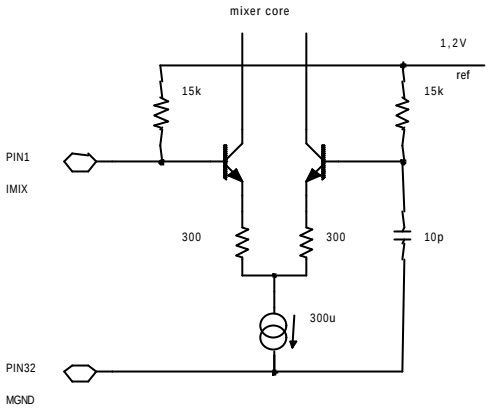
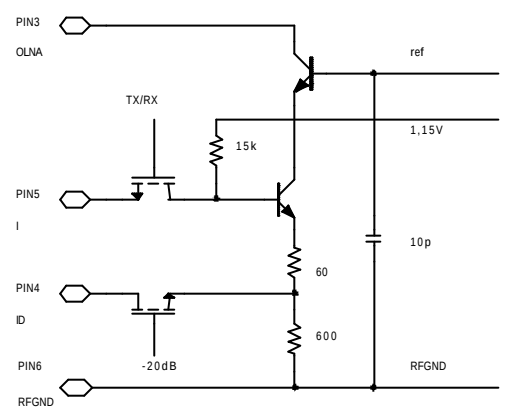
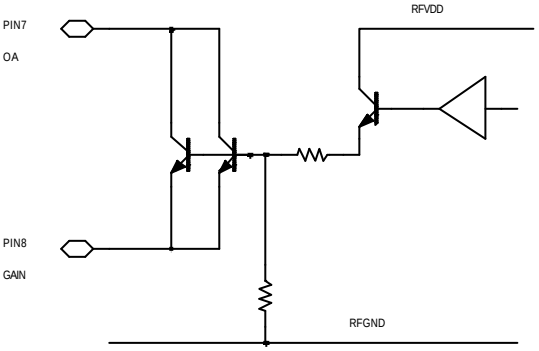
[1)] R_{GAIN} = 0Ω, DataRate = 5kBit, DutyCycle = 50%
[2)] R_{GAIN} = 50Ω||100p, DataRate =5kBit, DutyCycle=50%
[3)] Pins CSEL, PON, DATA, CDAT, CLK, DEN, XTO
[4)] Pins DATA, XTO

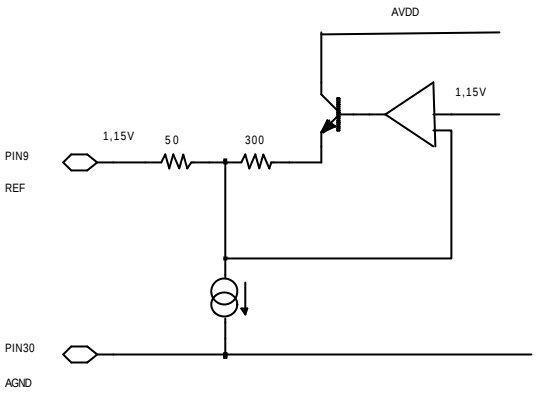
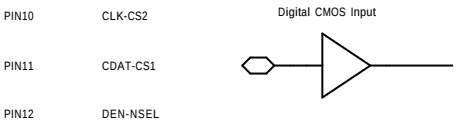
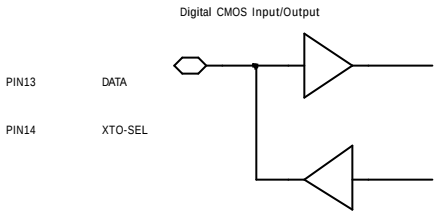
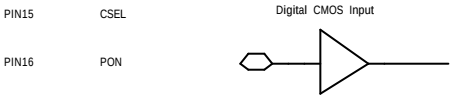
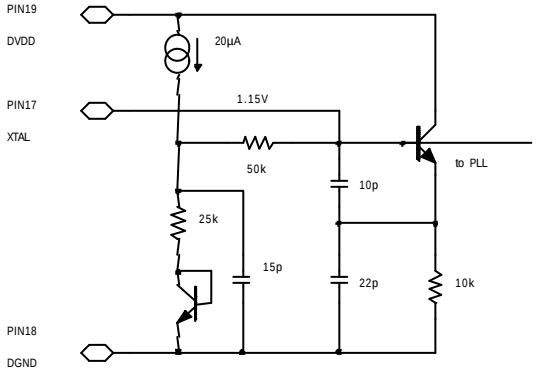
AC Characteristics

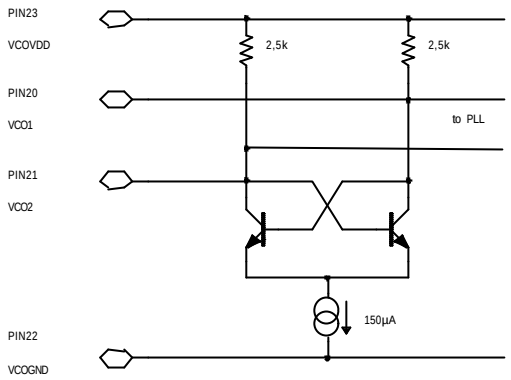
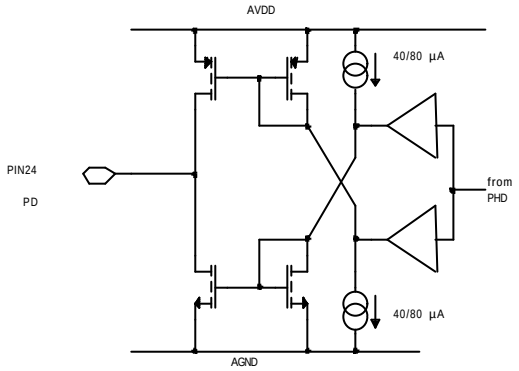
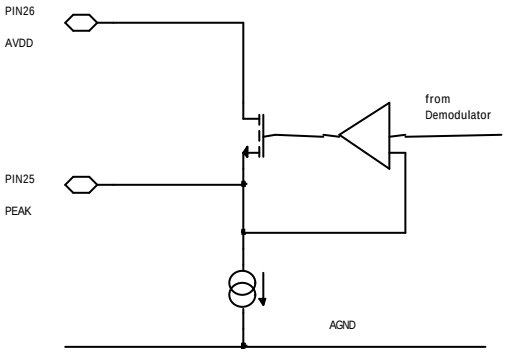
Supply voltage: V_{DD} = 3.0 V; Ambient temperature: T_A = 27°C

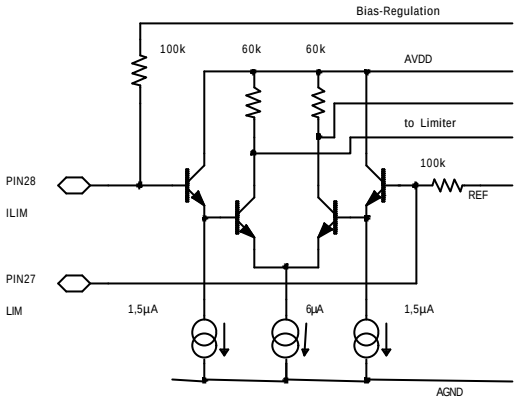
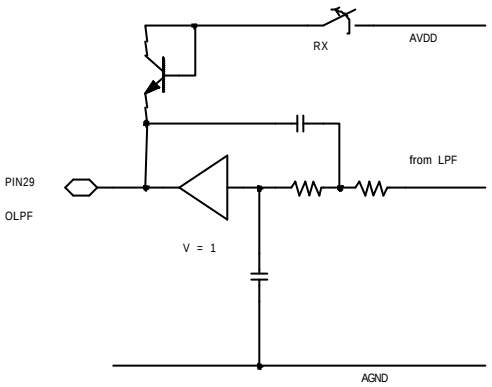
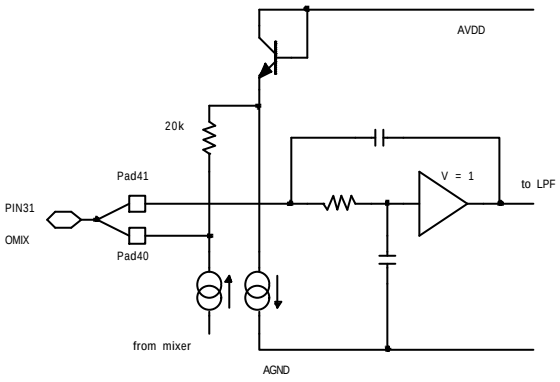
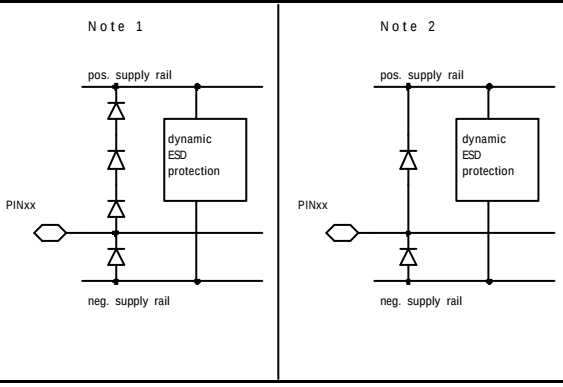
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTAL}	Oscillator Frequency		8	12.8	14	MHz
	Osc. Temperature Stability		-5	-	5	ppm
$t_{ON\ PLL}$	PLL Settling Time			4		ms
I_{PD}	Phase Detector Output Current			38/77		µA
$t_{ON\ RX}$	Receiver settling time			18		ms
BW1	Bandwidth LPF	BW=low		75		kHz
BW2	Bandwidth LPF	BW=high		38		kHz
DR1	Data Rate	DR=low			9600	bps
DR2	Data Rate	DR=high			4800	bps
	Sensitivity	BW=25kHz		-102 [2)] -95 [4)]		dBm
$t_{ON\ TX}$	Transmitter settling time			17		ms
P_A	Output Power (Transmit Mode)			1 [3)]		mW

[1)] depends on external tank circuit
[2)] transformer circuit (Test circuit)
[3)] R_{GAIN} = 0Ω, (Test circuit)
[4)] V_{imin} at the IC (R_{SOURCE}=50Ω)

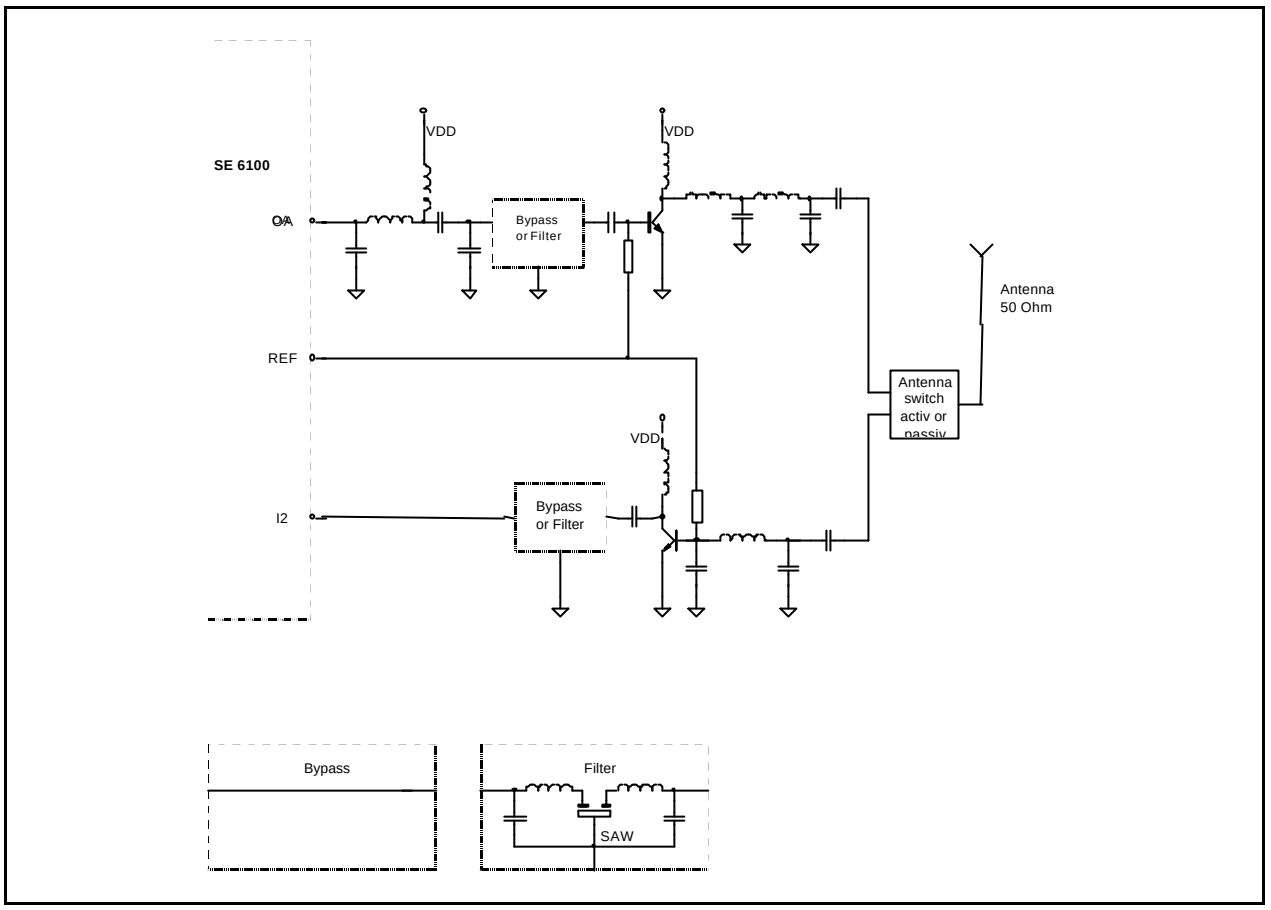
TQFP Pin	Symbol	Internal Equivalent Circuit	Function
1	**IMIX**		**Mixer Input** Single input differential amplifier stage with emitter degradation to improve the large signal behaviour Input impedance 5kΩ || 1.5pF Lower limit frequency will be determined by the internal decoupling capacitor Mixer gain about 27dB ESD Protection according note 1
2	**RFVDD**		**RF Supply** Positive supply voltage for LNA, Mixer, PAMP
3 **5** **4**	**OLNA** **I** **ID**		**LNA Output, LNA Input 2, LNA Input 1** Cascode Configuration with emitter degradation to improve the large signal behaviour Especially designed for loop antennas OLNA: open collector output ESD Protection according note 1 I: RF input with internal antenna switch to disconnect the LNA during TX mode Input Impedance 3.5kΩ || 1.5pF ESD Protection according note 1 ID: disconnectable emitter decoupling (-20dB switch) ESD Protection according note 2
6	**RFGND**		**RF Supply Ground** Negative supply voltage for LNA, PAMP
7 **8**	**OA** **GAIN**		**Power Amplifier Output, Gain Adjust** OA: open collector output ESD Protection according note 1 GAIN: output power adjustment by external components (e.g. R || C) to ground Maximum output power: direct connection to ground ESD Protection according note 2

TQFP Pin	Symbol	Internal Equivalent Circuit	Function
9	**REF**		**Reference Voltage Output** Suitable to bias external LNA or PAMP Typical output voltage 1.15V Maximum load current 200µA ESD Protection according note 2
10 **11** **12**	**CLK-CS2** **CDAT-CS1** **DEN-NSEL**		**CLK-CS2, CDAT-CS1, DEN-NSEL** Digital CMOS Input Function depends on chose mode (µC-StandAlone) ESD Protection according note 2
13 **14**	**DATA** **XTO-SEL**		**DATA, XTO-SEL** Digital CMOS Input / Output Function depends on chose mode (µC-StandAlone) ESD Protection according note 2
15 **16**	**CSEL** **PON**		**CSEL, PON** Digital CMOS Input CSEL low: µC Mode high: StandAlone Mode PON low: Power ON high: Power OFF ESD Protection according note 2
17	**XTAL**		**Crystal Oscillator Input** Single pin Colpitts oscillator Frequency range 8 .. 14 MHz ESD Protection according note 2
18	**DGND**		**Digital Supply Ground** Negative supply voltage for XTAL, Digital Blocks

TQFP Pin	Symbol	Internal Equivalent Circuit	Function
19	**DVDD**		**Digital Supply Voltage** Positive supply voltage for XTAL, Digital Blocks
20 **21**	**VCO1** **VCO2**		**Voltage Controlled Oscillator** Current controlled oscillator External LC tank circuit needed VCO operates at half of working frequency (internal frequency doubler) ESD Protection according note 1
22	**VCOGND**		**VCO Supply Ground** Negative supply voltage for VCO
23	**VCOVDD**		**VCO Supply Voltage** Positive supply voltage for VCO
24	**PD**		**Charge Pump Output** Selectable output current (40 / 80 µA) ESD Protection according note 2
25	**PEAK**		**Peak Detector Output** Needs to be connected to an external capacitor Peak voltage depends on input field strength Used internally as reference voltage for signal detector and signal strength comparators ESD Protection according note 2
26	**AVDD**		**Analog Supply Voltage** Positive supply voltage for IF Blocks, LPF, others

TQFP Pin	Symbol	Internal Equivalent Circuit	Function
27 **28**	**LIM** **ILIM**		**Limiter Decoupling, Limiter Input** LIM: reference voltage for limiter needs to be connected to ground ESD Protection according note 2 ILIM: signal input for limiter needs to be connected to LPF output by a capacitor (47 .. 150 nF) Input voltage range 200µV ... 500mV ESD Protection according note 2
29	**OLPF**		**Low Pass Filter Output** Butherworth filter 10th order LPF gain: about 1dB During PowerOFF / TX mode the output will be clamped to near VDD ESD Protection according note 2
30	**AGND**		**Analog Supply Ground** Negative supply voltage for IF Blocks, LPF, others
31	**OMIX**		**Mixer Output (LPF input)** An external RC circuit can be used to adjust the mixer gain. Pad 40 / 41 are connected in TQFP32 version. They need to be connected externally in case of using dice. ESD Protection according note 2
32	**MGND**		**Mixer Ground** Negative supply voltage for Mixer
-	**-**		**ESD Protection Notes**

Further Applications (external LNA and Booster)



Package

TQFP32

Note

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