16-Channel Constant Current LED Driver

HALOGEN FREE LEAD FREE™ RoHS Compliance

FEATURES

- **16 Constant current-sink channels**
- **Serial interface up to 25MHz clock frequency**
- **3V to 5.5V logic supply**
- **LED current range from 2mA to 100mA**
- **LED current set by external RSET resistor**
- **300mV LED dropout at 30mA**
- **Thermal shutdown protection**
- **Available in RoHS-compliant 24-lead SOIC, TSSOP, QSOP, and 4 x 4mm TQFN packages**

APPLICATION

- **Billboard Display**
- **Marquee Display**
- **Instrument Display**
- **General Purpose Display**

For Ordering Information details, see page 14.

DESCRIPTION

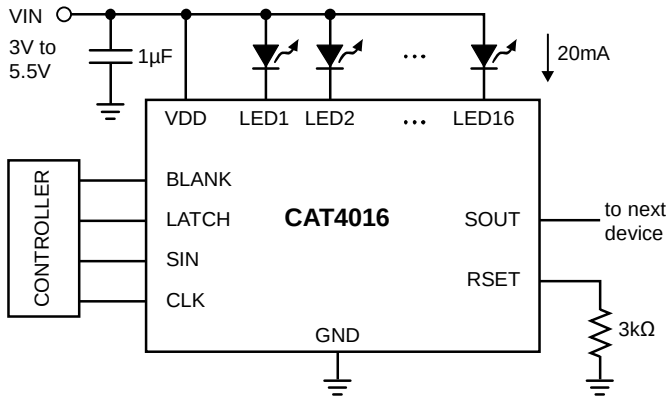
The CAT4016 is a 16 channel constant current driver for LED billboard and other general display applications. LED channel currents are programmed together via an external RSET resistor. Low output voltage operation on the LED channels as low as 0.4V (for 2 to 100mA LED current) allows for more power efficient designs.

A high-speed 4-wire serial interface of up to 25MHz clock frequency controls each individual channel using a shift register and latch configuration. A serial output data pin (SOUT) allows multiple devices to be cascaded and programmed via one serial interface. The device also includes a blanking control pin (BLANK) that can be used to disable all channels independently of the interface.

Thermal shutdown protection is incorporated in the device to disable the LED outputs if the die temperature exceeds a set limit.

The device is available in the 24-lead SOIC, TSSOP, QSOP and the compact TQFN 4 x 4mm packages.

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

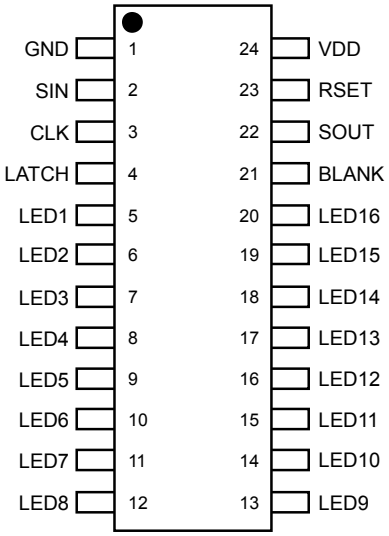
Part Number	Package	Quantity per Reel	Package Marking
CAT4016W-T1	SOIC24(1)	1,000	CAT4016W
CAT4016Y-T2	TSSOP24(1)	2,000	CAT4016Y
CAT4016VS-T2	QSOP24(1)	2,000	4016VS
CAT4016VSR-T2	QSOP24(1)	2,000	4016VSR
CAT4016HV6-T2	TQFN24(1)	2,000	LAAA
CAT4016HV6-GT2	TQFN24(2)	2,000	LAAD

Notes:

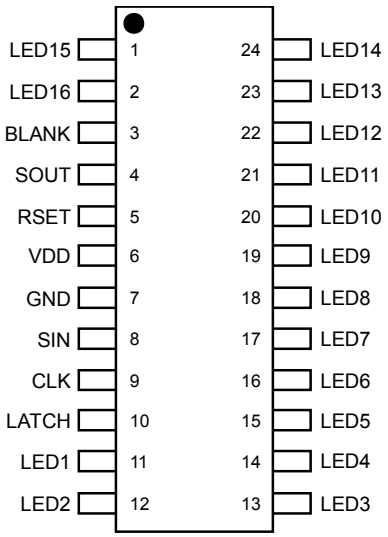
(1) Matte-Tin Plated Finish (RoHS-compliant)
(2) NiPdAu Plated Finish (RoHS-compliant)

PIN CONFIGURATION

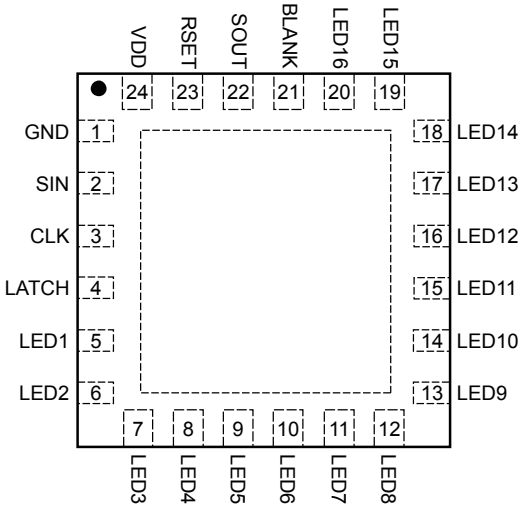
24-Lead SOIC (W), TSSOP (Y), QSOP (VS)



24-Lead QSOP (VSR)



24-Lead TQFN (HV6)



ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
V_{DD} Supply Voltage	6	V
Logic input/output voltage (SIN, SOUT, CLK, BLANK, LATCH)	-0.3V to V_{DD}+0.3V	V
LEDn voltage	6	V
DC output current on LED1 to LED16	150	mA
Storage Temperature Range	-55 to +160	°C
Junction Temperature Range	-40 to +150	°C
Lead Soldering Temperature (10sec.)	300	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Range	Units
V_{DD}	3.0 to 5.5	V
Voltage applied to LED1 to LED16	0.4 to 5.5	V
LED current RSET control range	up to 100	mA
Ambient Temperature Range	-40 to +85	°C

ELECTRICAL OPERATING CHARACTERISTICS

DC Characteristics

V_{DD} = 5.0V, T_{AMB} = 25 ºC, over recommended operating conditions unless specified otherwise.

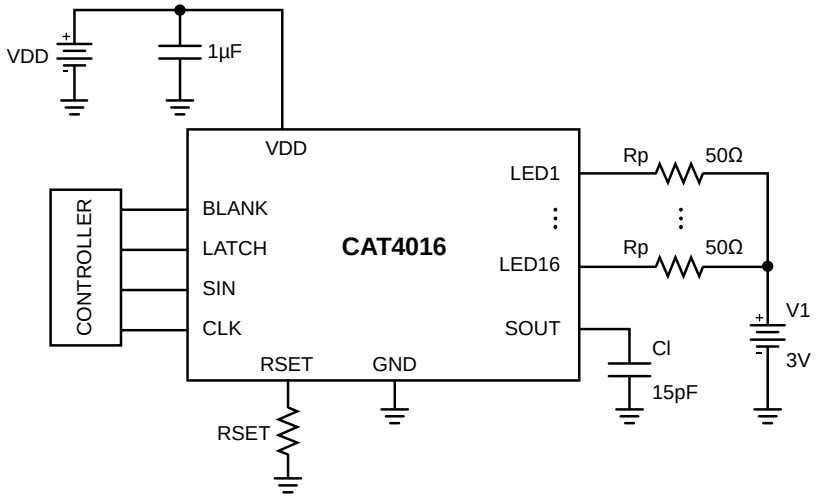
Symbol	Name	Conditions	Min	Typ	Max	Units
$I_{LED-ACC}$	LED Current (any channel)	V_{LED} = 1V, R_{SET} = 3kΩ	18	20	22	mA
		V_{LED} = 1V, R_{SET} = 1.5kΩ	36	40	44	
		V_{LED} = 1V, R_{SET} = 750Ω		80		
$I_{LED-MAT}$	LED Current Matching (I_{LED} - I_{LEDAVR}) / I_{LEDAVR}	V_{LED} = 1V, R_{SET} = 3kΩ		±1.5		%
		V_{LED} = 1V, R_{SET} = 1.5kΩ	-6.0	±1.5	+6.0	
		V_{LED} = 1V, R_{SET} = 750Ω		±2.0		
ΔI_{VDD}	LED current regulation vs. V_{DD}	V_{DD} within 4.5V and 5.5V LED current 30mA		±0.1		% / V
ΔI_{VLED}	LED current regulation vs. V_{LED}	V_{LED} within 1V and 3V LED current 30mA		±0.05		% / V
I_{DDOFF}	Supply Current (all outputs off)	R_{SET} = 3kΩ		3	8	mA
		R_{SET} = 750Ω		8.5		mA
I_{DDON}	Supply Current (all outputs on)	R_{SET} = 3kΩ		4	9	mA
		R_{SET} = 750Ω		10		mA
I_{LKG}	LEDn output Leakage	V_{LED} = 5V, outputs off	-1		1	µA
R_{LATCH}	LATCH Pull-down Resistance		100	180	300	kΩ
R_{BLANK}	BLANK Pull-up Resistance		100	180	300	kΩ
V_{IH} V_{IL}	Logic high input voltage Logic low input voltage		0.7xV_{DD}		 0.3xV_{DD}	V V
V_{HYS}	Logic input hysteresis voltage			0.1xV_{DD}		V
I_{IL}	Logic Input leakage current (CLK, SIN)	V_I = V_{DD} or GND	-5	0	5	µA
V_{OH} V_{OL}	SOUT logic high output voltage SOUT logic low output voltage	I_{OH} = -1mA I_{OL} = 1mA	V_{CC}-0.3V		 0.3	V
V_{RSET}	RSET Regulated Voltage		1.17	1.20	1.23	V
T_{SD}	Thermal Shutdown			160		ºC
T_{HYST}	Thermal Hysteresis			20		ºC

Timing Characteristics

For 3.0V ≤ V_{DD} ≤ 5.5V, T_{AMB} = 25 ºC, unless specified otherwise.

Symbol	Name	Conditions	Min(1)	Typ(2)	Max(1)	Units
CLK						
f_{clk}	CLK Clock Frequency				25	MHz
t_{cwh}	CLK Pulse Width High		20			ns
t_{cwl}	CLK Pulse Width Low		20			ns
SIN						
t_{ssu}	Setup time SIN to CLK		4			ns
t_{sh}	Hold time SIN to CLK		4			ns
LATCH						
t_{lwh}	LATCH Pulse width		20			ns
T_{lh}	Hold time LATCH to CLK		4			ns
T_{lsu}	Setup time LATCH to CLK	Channel Stagger Delay	800			ns
LEDn						
t_{ld}	LED1 Propagation delay	LATCH to LED1 off/on		40	300	ns
t_{ls}	LED Propagation delay stagger	LED(n) to LED(n+1)		17	40	ns
t_{lst}	LED Propagation delay stagger total	LED1 to LED16		250		ns
t_{bd}	BLANK Propagation delay	BLANK to LED(n) off/on		60	300	ns
t_{lr}	LED rise time (10% to 90%)	Pull-up resistor = 50Ω to 3.0V		40	200	ns
t_{lf}	LED fall time (90% to 10%)	Pull-up resistor = 50Ω to 3.0V		30	250	ns
SOUT						
t_{or}	SOUT rise time (10% to 90%)	C_L = 15pF		5		ns
t_{of}	SOUT fall time (90% to 10%)	C_L = 15pF		5		ns
t_{od}	Propagation delay time SOUT	CLK to SOUT	8	15	25	ns

Test Circuit for AC Characteristics



Notes:
(1) All min and max values are guaranteed by design.
(2) V_{DD} = 5V, LED current 30mA.

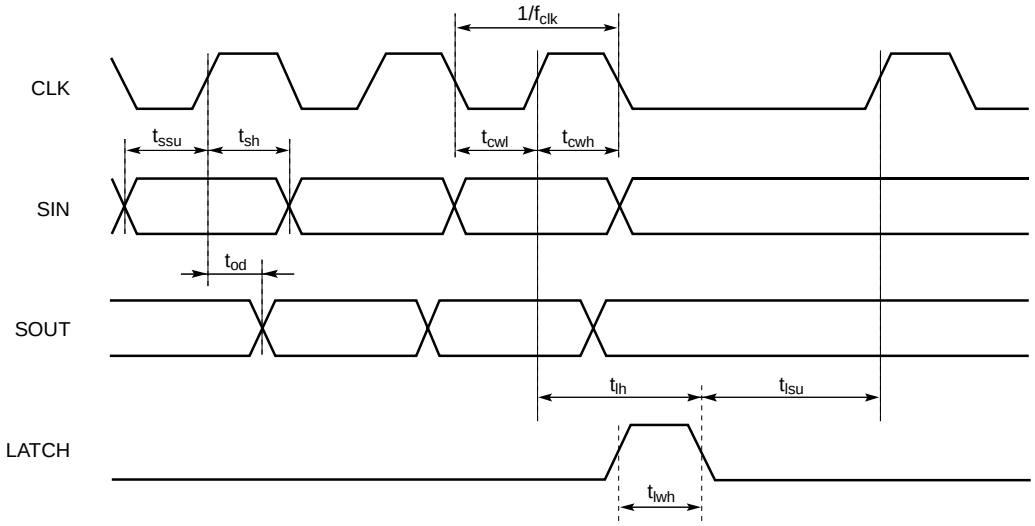


Figure 1. Serial Input Timing Diagram

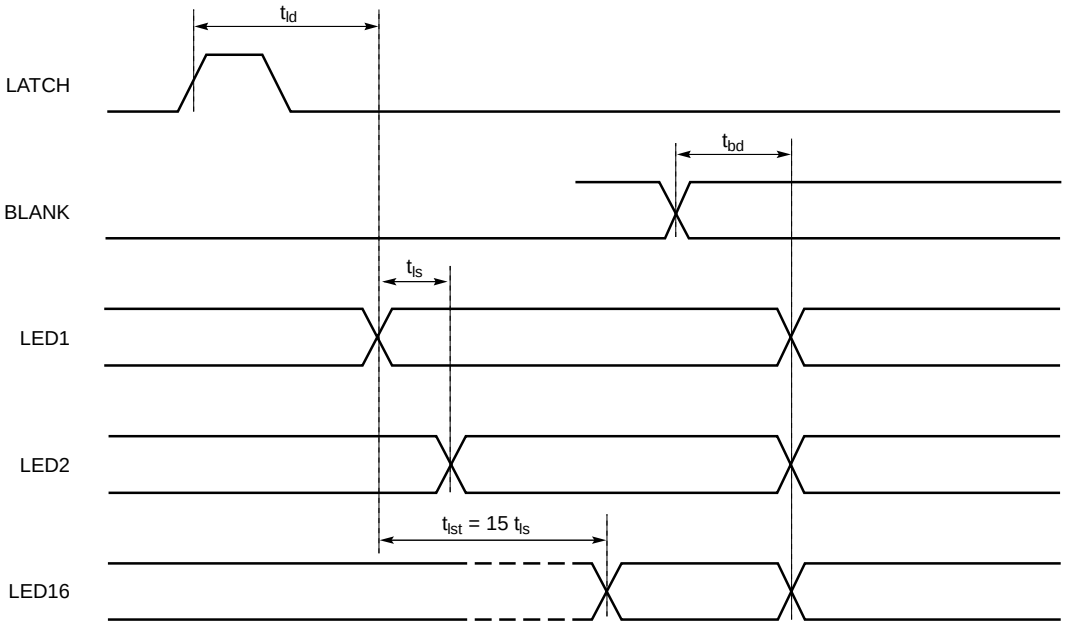
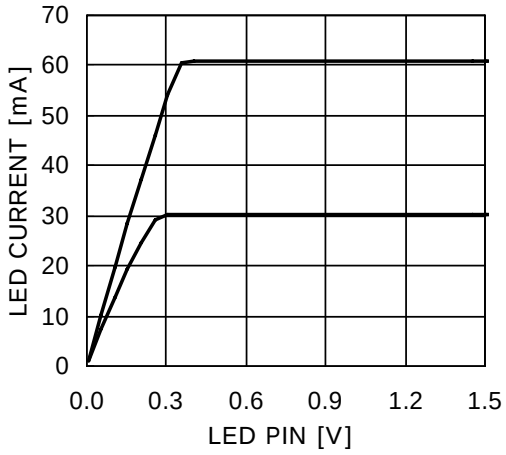


Figure 2. LED Output Timing Diagram

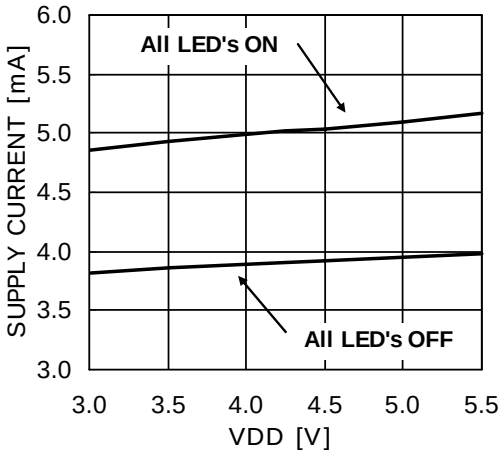
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5.0V, LED current 30mA, all LEDs On, T_{AMB} = 25°C unless otherwise specified.

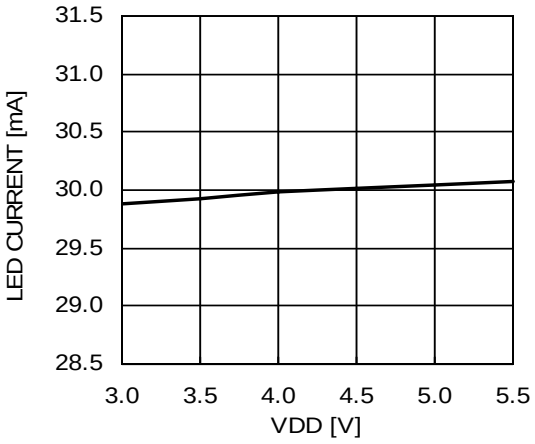
LED Current vs. LED Pin Voltage



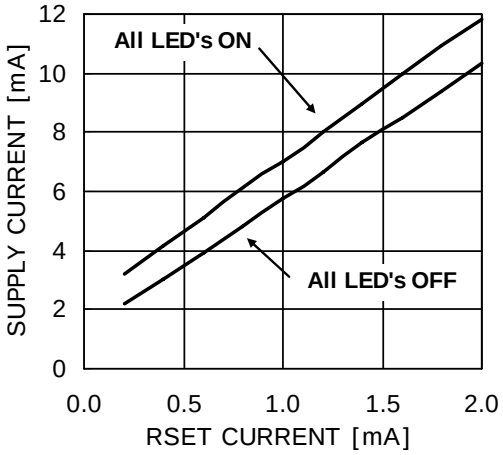
Supply Current vs. VDD Pin Voltage



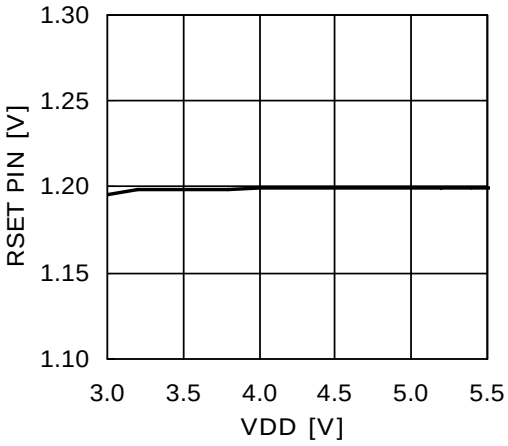
LED Current vs. VDD Pin Voltage



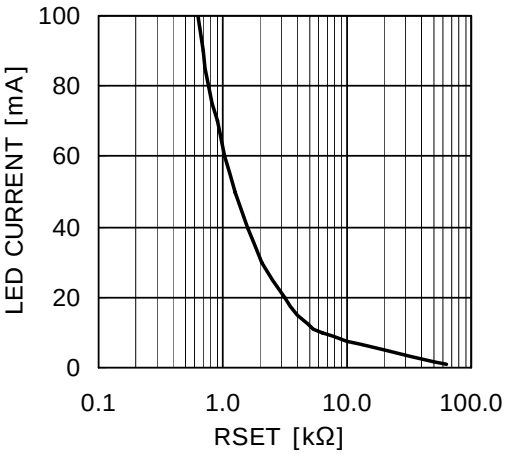
Supply Current vs. RSET Current



RSET Voltage vs. VDD Pin Voltage



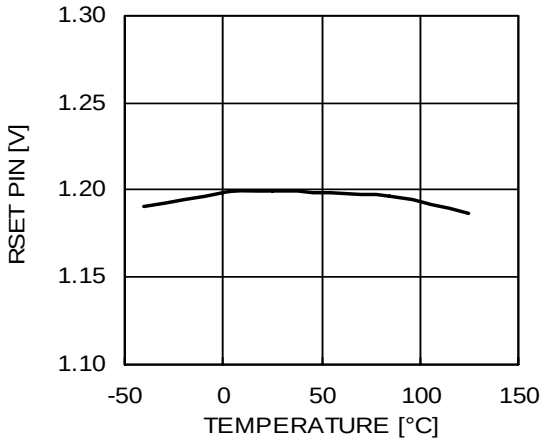
LED Current vs. RSET Resistor



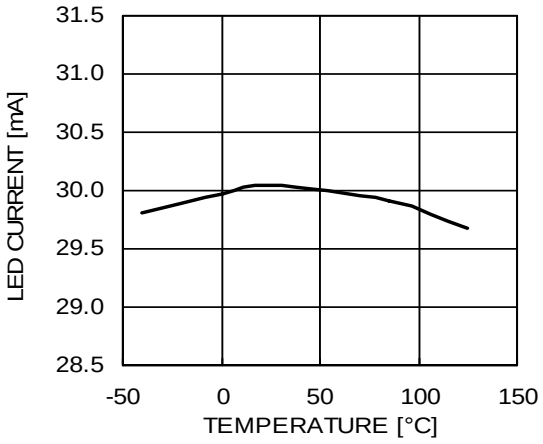
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5.0V, LED current 30mA, all LEDs On, T_{AMB} = 25°C unless otherwise specified.

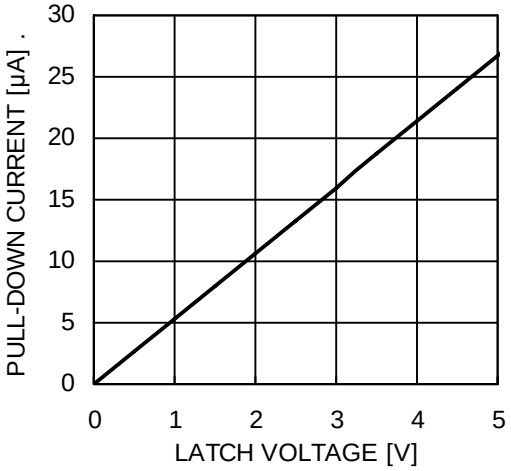
RSET Voltage vs. Temperature



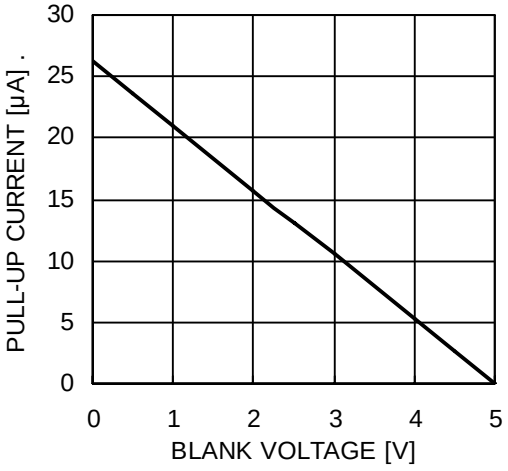
LED Current vs. Temperature



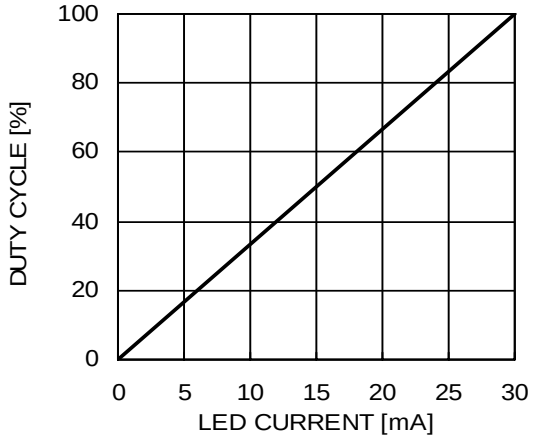
Internal Pull-Down Current (LATCH pin)



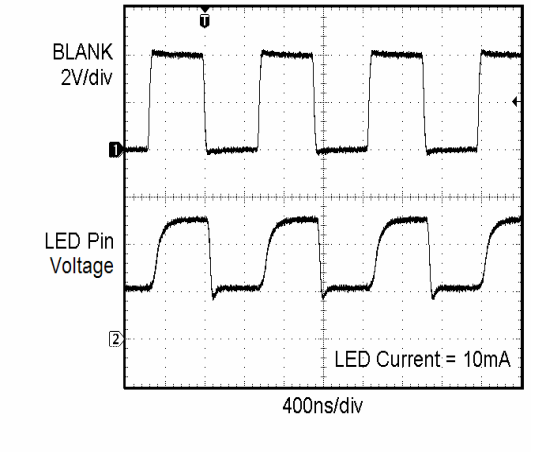
Internal Pull-Up Current (BLANK pin)



PWM Dimming on BLANK pin (f = 10kHz)



BLANK Transient Response



PIN DESCRIPTION

Name	Function
GND	Ground
SIN	Serial data input pin
CLK	Serial clock input pin
LATCH	Latch serial data to output registers
LED1-LED16	LED channel 1 to 16 cathode terminals
BLANK	Enable / disable all channels
SOUT	Serial data output pin.
RSET	LED current set pin
VDD	Positive supply Voltage
TAB (TQFN package only)	Connect to GND on the PCB

PIN FUNCTION

GND is the ground reference pin for the device. This pin must be connected to the ground plane on the PCB.

SIN is the serial data input. Data is loaded into the internal register on each rising edge of CLK.

CLK is the serial clock input. On each rising CLK edge, data is transferred from SIN to the internal 16-bit serial shift register.

LATCH is the latch data input. On the rising edge of LATCH, data is loaded from the 16-bit serial shift register into the output register latch. On the falling edge, this data is latched in the output register and isolated from the state of the serial shift register.

LED1 - LED16 are the LED current sink channels. These pins are connected to the LED cathodes. The current sinks drive the LEDs with a current equal to 50 times RSET pin current. For the LED sink to operate correctly, the voltage on the LED pin must be above 0.4V.

BLANK is the LED channel enable and disable input pin. When low, LEDs are enabled according to the output latch register content. When high, all LEDs are off, while preserving the data in the output latch register.

SOUT is the serial data output of the 16-bit serial shift register. This pin is used to cascade several devices on the serial bus. The SOUT pin is then connected to the SIN input of the next device on the serial bus to cascade.

RSET is the LED current setting pin. A resistor is connected between this pin and ground. Each LED channel current is set to 50 times the current pulled out of the pin. The RSET pin voltage is regulated to 1.2V.

VDD is the positive supply pin voltage for the entire device. A small 1µF ceramic is recommended close to pin.

BLOCK DIAGRAM

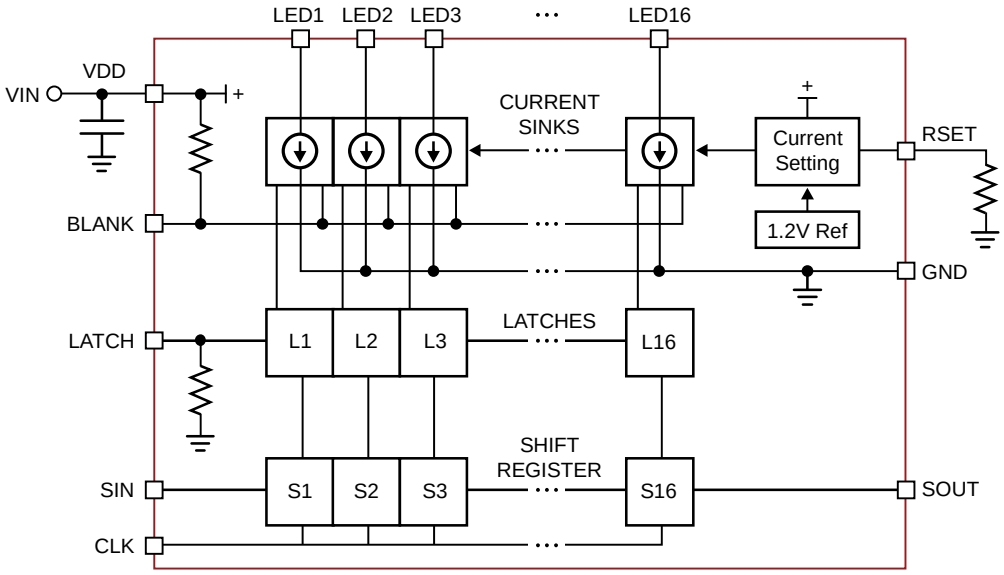


Figure 2. CAT4016 Functional Block Diagram

BASIC OPERATION

The CAT4016 uses 16 tightly matched current sinks to accurately regulate the LED current in each channel. The external resistor, R_{SET}, is used to set the LED channel current to 50 times the current in R_{SET}.

$$\text{LED current} = 50 \times \frac{1.2}{R_{SET}}$$

Tight current regulation for all channels is possible over a wide range of input and LED voltages due to independent current sensing circuitry on each channel. The LED channels have a maximum dropout of 0.4V for most current and supply voltage conditions. This helps improve the heat dissipation and efficiency of the LED driver.

Upon power-up, an under-voltage lockout circuit clears all latches and shift registers and sets all outputs to off. Once the under-voltage lockout threshold has been reached the device can be programmed.

The driver delays the activation of each consecutive LED output channel by 17ns (typical). Relative to LED1, LED2 is delayed by 17ns, LED3 by 34ns and LED16 by 250ns typical. The delay is introduced when LATCH is activated. The delay minimizes the inrush current on the LED supply by staggering the turn on and off current spikes over a period of time and therefore allowing usage of smaller bypass capacitors.

Pull-up and pull-down resistors are internally provided to set the state of the BLANK and LATCH pins to the off-state when not externally driven.

SERIAL INTERFACE

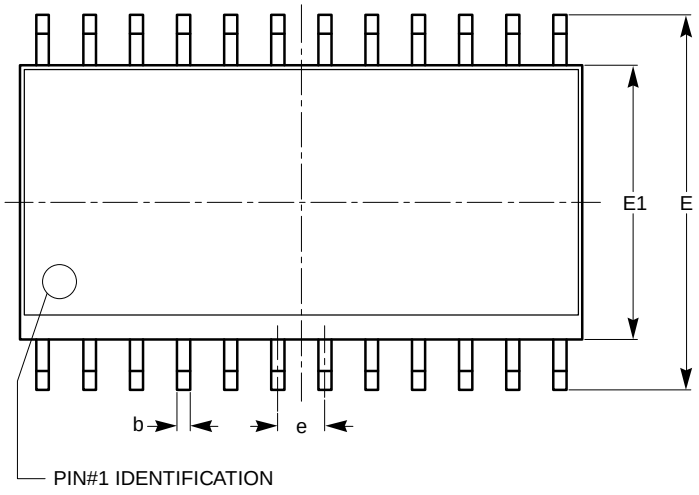
A high-speed serial 4-wire interface is provided to program the state of each LED on or off. The interface contains a 16-bit serial to parallel shift register (S1-S16) and a 16-bit latch (L1-L16). Programming the serial to parallel register is accomplished via SIN and CLK input pins. On each rising edge of the CLK signal, the data from SIN is moved through the shift register serially. Data is also moved out of SOUT which can be connected to a next device if programming more then one device on the same interface.

On the rising edge of LATCH, the data contents of the serial to parallel shift register is reflected in the latches. On the falling edge of LATCH, the state of the serial to parallel register at that particular time is saved in the latches and does not change irrespective of the contents of the serial to parallel register.

BLANK is used to disable all LEDs (turn off) simultaneously while maintaining the same data in the latch register. When low, the LED outputs reflect the data in the latches. When high, all outputs are high impedance (zero current).

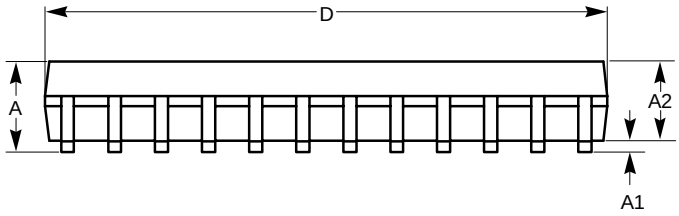
PACKAGE OUTLINE DRAWINGS

SOIC 24-Lead 300mils (W)

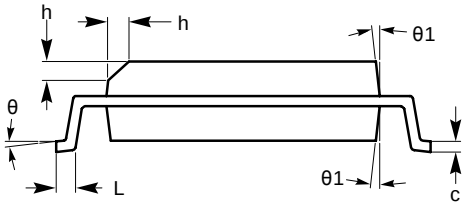


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	15.20		15.40
E	10.11		10.51
E1	7.34		7.60
e	1.27 BSC		
h	0.25		0.75
L	0.40		1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW

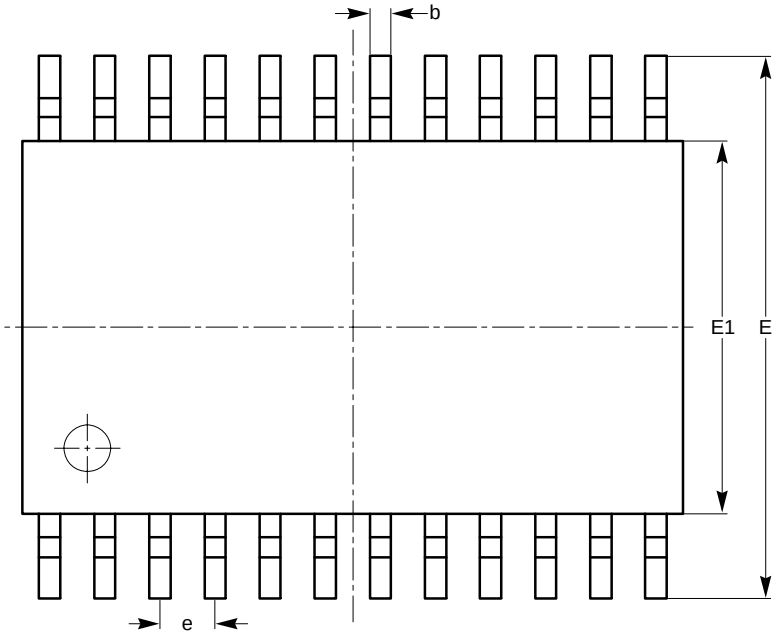


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

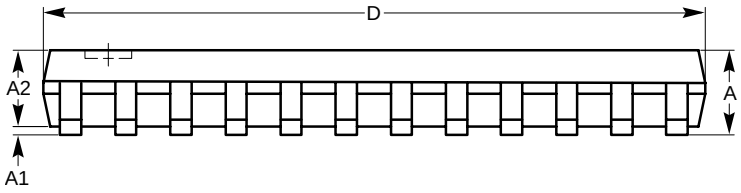
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

TSSOP 24-Lead 4.4mm (Y)

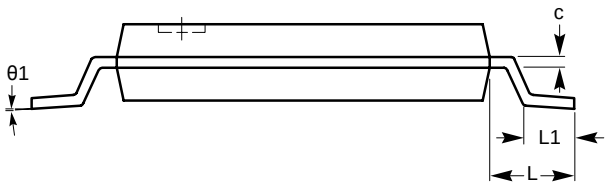


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.50	0.60	0.70
θ1	0°		8°



SIDE VIEW

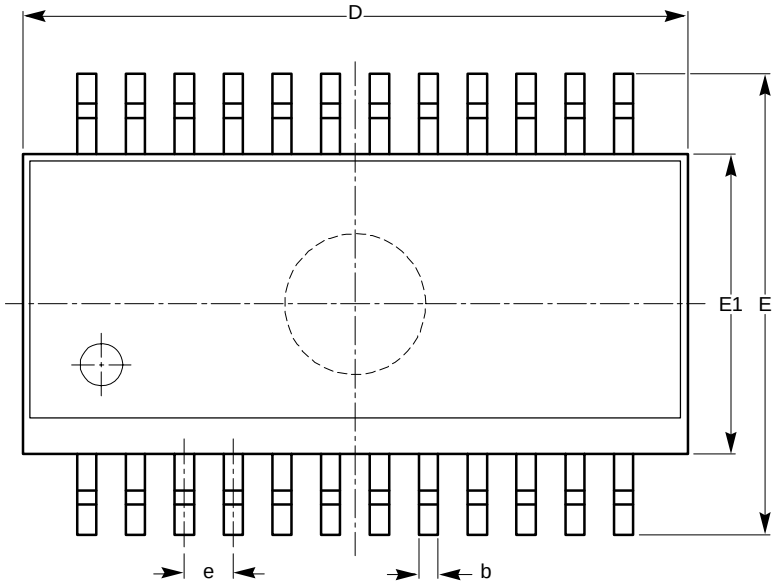


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

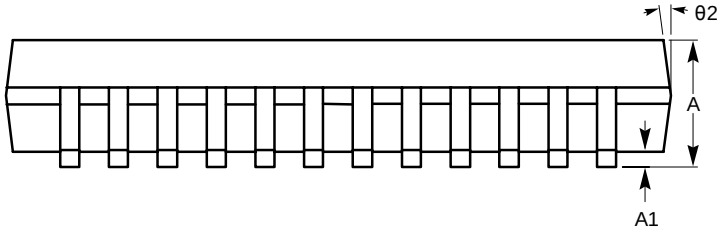
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

QSOP 24-Lead (VS, VSR)

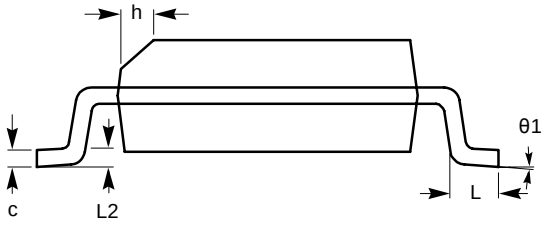


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.37		1.73
A1	0.10		0.25
b	0.20		0.31
c	0.19		0.25
D	8.56		8.74
E	5.82		6.19
E1	3.81		3.98
e		0.635 BSC	
h	0.28		0.48
L	0.41		0.86
L2		0.254 BSC	
θ1	0°		8°
θ2		7° BSC	



SIDE VIEW

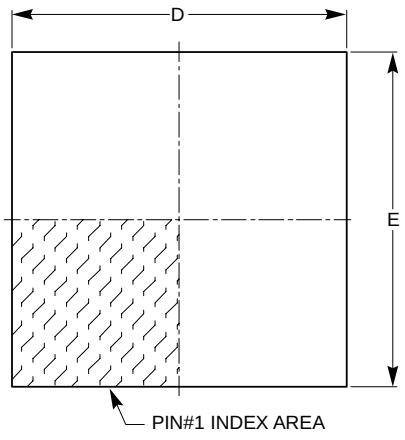


END VIEW

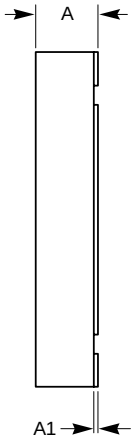
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-137.

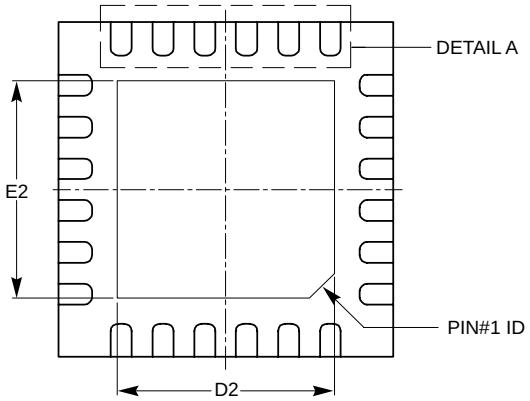
TQFN 24-Pad 4 x 4mm (HV6)



TOP VIEW

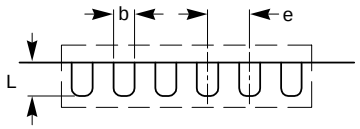


SIDE VIEW

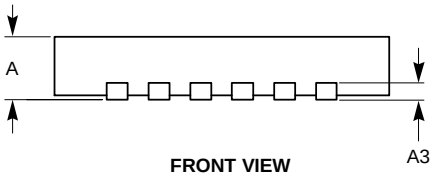


BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.40	–	2.90
E	3.90	4.00	4.10
E2	2.40	–	2.90
e		0.50 BSC	
L	0.30	0.40	0.50



DETAIL A

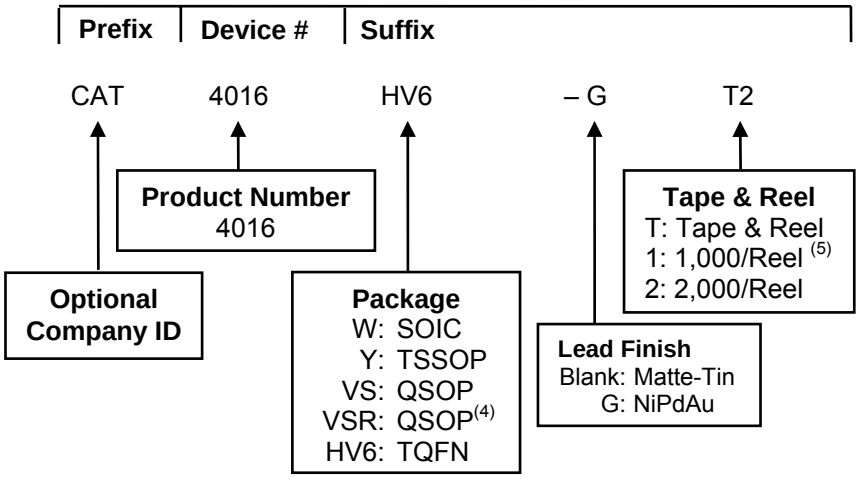


FRONT VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-220.

EXAMPLE OF ORDERING INFORMATION



For Product Top Mark Codes, click here:
http://www.catsemi.com/techsupport/producttopmark.asp

Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The device used in the above example is a CAT4016HV6–GT2 (TQFN, NiPdAu, Tape & Reel, 2,000/Reel).
(3) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.
(4) Different pin outs, see page 2.
(5) SOIC package availability in 1,000/Reel. All other packages are 2,000/Reel.

REVISION HISTORY

Date	Rev.	Reason
09/26/2007	A	Initial Issue
10/17/2007	B	Update Absolute Maximum Ratings
04/09/2008	C	Update Ordering Information table, added TQFN in NiPdAu plated finish. Update Package Outline Drawings Update Example of Ordering Information Add Top Mark Codes link

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Issue date: 04/09/08