APPLICATION NOTE

A wideband 30 W push-pull amplifier with two MOS transistors BLF244 (V_{DS} = 28 V); range 25 – 110 MHz

NCO8701

Philips
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CONTENTS

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1 INTRODUCTION

A wideband push-pull power amplifier has been developed for the frequency range 25-110 MHz. The design is based on the BLF244, a silicon N-channel enhancement mode vertical D-MOS transistor designed for large-signal amplifier applications in the VHF range. This device can deliver 15 W output power at 175 MHz when operated from a 28 V supply. The transistor has a 4-lead flange envelope with a ceramic cap (SOT123).
The objective was to design and construct a 30 W wideband amplifier with high gain and efficiency and low input VSWR and second order distortion. With respect to gain and efficiency a reasonable flatness was desired. The push-pull design is employed because of its low second order distortion.
The design and practical realization of this amplifier are described in the following chapters.

2 AMPLIFIER DESIGN

2.1 General

The schematic set up of the amplifier is depicted in Fig.1.

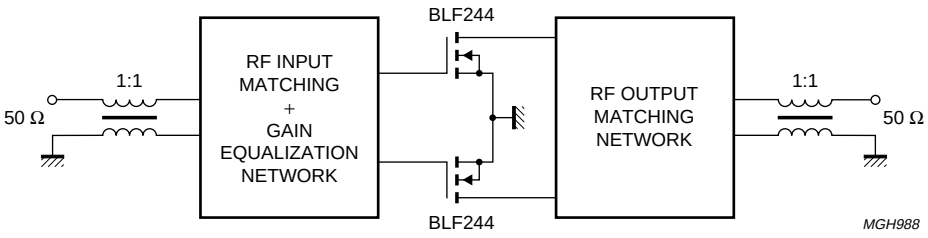

Fig.1

Two 1 : 1 balance to unbalance transformers are applied; one for splitting the single-ended input source into two out of phase sources driving the transistor-inputs, the other for adding the outputs from the transistors.
Transmission line transformers are employed because of there excellent broadband response. These transformers consist of a twisted-wire-pair transmission line wound on a ferrite toroid.
At the input side a special matching network is applied to obtain a low VSWR and compensation for variation in gain with frequency.
The matching network at the output side provides the transistors with the optimum load for an output power of 30 W at V_{DS} = 28 V.

2.2 Powergain, input- and output impedance

The design has been started by determining powergain, input impedance and output impedance of the transistor for the frequency range 25-110 MHz.

First the output impedance was determined.
For HF and VHF the optimum load resistance RL can be calculated with reasonable accuracy with the formula:

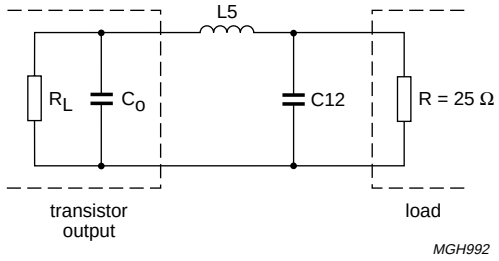

Fig.2

$$R_L = \frac{V^2_{DS}}{2 \cdot P_O} \quad (1)$$

For V_{DS} = 28 V and P_O = 15 W we get: R_L = 26.1 Ω.
The output impedance is the parallel combination of the output capacitance C_O of the transistor and the optimum load resistance.
Because of the large drain voltage swing the effective output capacitance C_O is approx. 15% higher than the value of C_{oss}. For BLF244 C_{OSS} is typical 38 pF, so C_O is equal to 43.7 pF. So the output impedance of this transistor can be represented by 26.1 Ω//43.7 pF for the whole frequency range.
Second the large-signal input impedance and powergain versus frequency were determined by measurement. For this purpose a single-ended test amplifier was constructed. This amplifier was matched at the output side to a load of 25 Ω by a broadband matching network: Dimensioning of this network was based on a practical dummy transistor of 24 Ω//43 pF. The maximum VSWR measured within the band was 1.16.
At the input side tunable narrowband matching networks were applied at several frequencies. By tuning this amplifier for minimum return loss at P_O = 15 W the powergain was measured directly.

For measurement of the input impedance the DC power, signal source and transistor were disconnected from the amplifier and the signal source circuit connection was terminated with 50 Ω. After that the impedance was measured at the gate connection of the transistor. The input impedance of the transistor is the conjugate of the measured impedance if the circuit doesn't contain resistive components.
This procedure was repeated at several frequencies in the band to get sufficient data for the design.
Figures 14, 15 and 16 present the data in graphical form.

2.3 Output matching section

Because of the symmetrical set-up of this amplifier its matching sections can be divided into two equal parts. Each part belonging to one transistor. In the next discussion one half of the output matching section will be considered.

As mentioned in the previous section the optimum load resistance for P_O = 15 W and V_{DS} = 28 V is 26.1 Ω according to equation (1).
When two of these transistors are used in a push-pull configuration the optimum load resistance adds up to 52.2 Ω. This value is very close to 50 Ω to which these transistors have to be matched. So, if we choose the optimum load resistance to be 50 Ω we can suffice with a 1 : 1 balance to unbalance transformer.
The output capacitance C_O of the transistor can be compensated over a certain bandwidth by absorbing it in a low-pass Chebyshev π-section, see Fig.2.

R_L represents the optimum load resistance for the transistor. The components L5 and C12 can be determined with the following formulae if $R_L = R$ and $C_O = C12 = C$:
The normalized value of C is:

$$A = \omega_m \cdot C \cdot R \tag{2}$$

in which $\omega_m = 2 \times \pi \times f_{max}$

The normalized value of L5 can be calculated as follows:

$$B = \frac{\omega_m \times L_5}{R} \tag{3}$$

$$B = \frac{8 \times A}{3 \cdot A^2 + 4} \tag{4}$$

The maximum VSWR of this network follows from:

$$VSWR_{max} = \left\{\frac{x^3 + 1}{x^3 - 1}\right\}^2 \tag{5}$$

in which $x = \gamma + (\gamma^2 + 1)^{1/2}$

and $\gamma = 1/A$

For this section R = 25 Ω and C = 43 pF. This results in: A = 0.7430 → B = 1.0509 → L5 = 38 nH and $VSWR_{max}$ = 1.156.

In practice this circuit comprises some additional components, see Fig.3.

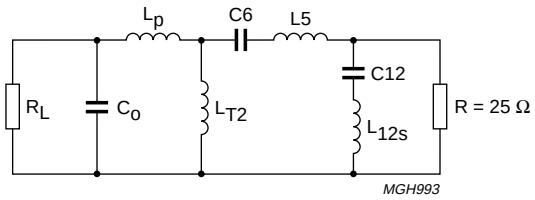

Fig.3

These are:

L_p – the parasitic drain and source inductance which has been accounted for by this way. Its value is approx. 1.4 nH

L_{T2} – the drain choke inductance which equals approx. 0.8 μH. Determination of this inductance will be treated in a later chapter.

L_{12S} – the parasitic series inductance of C12, which is approx. 1 nH

C_6 – the DC-blocking capacitor which is also employed for low frequency compensation of L_{T2}.

The value of C_6 is calculated with the aid of the information given in ref.(1). The drain load circuit for low frequency is shown in Fig.4.

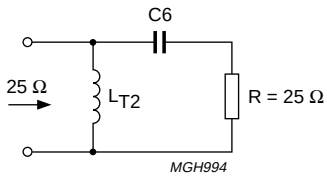

Fig.4

Compensation according to ref.(1) gives at f = 25 MHz:

C_6 = 1.28 nF with $VSWR_{max}$ = 1.04

The circuit in Fig.3 was optimized for the frequency range 25-110 MHz. For this purpose a computer optimization program was used. The criterion used was for overall minimum VSWR with respect to 25 Ω.

The results before and after optimization are shown in Table 1.

Table 1

BEFORE OPTIMIZATION		AFTER OPTIMIZATION	
C_6	1.28 nF	C_6	7.9 nF
L_5	38 nH	L_5	34.6 nH
C_{12}	43 pF	C_{12}	37.9 pF
$VSWR_{max}$	1.169	$VSWR_{max}$	1.098

2.4 Input matching section

The purpose of the input matching section is two-fold. First to match the transistor input impedance to the source impedance of 50 Ω with a sufficiently low VSWR across the frequency band.
Second to compensate the variation in gain with frequency.

The input matching section chosen is depicted in Fig.5 for one transistor.

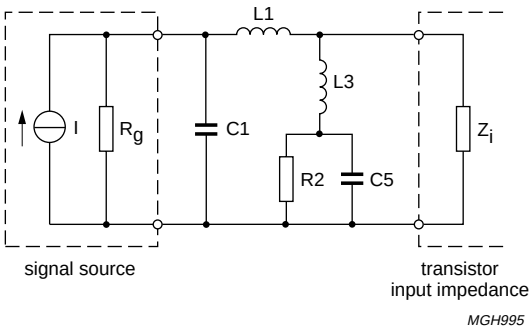

Fig.5

Since the input impedance of the transistor is strongly capacitive, Zi can be approximated by an ideal capacitor. This network can then be treated as a symmetrical double pi-section, see Fig.6.

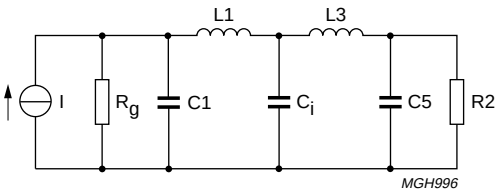

Fig.6

In order to get sufficient gain flatness a constant voltage has to be developed across capacitor Ci. For optimum dimensioning of this network the following formulae are valid:

$$Rg = R2 = \frac{1.6}{\omega_m \cdot ci} \quad (6)$$

$$C1 = C5 = 0.386 \times Ci \quad (7)$$

$$L1 = L3 = 0.997 \times \frac{Rg}{\omega_m} \quad (8)$$

in which ωm is the maximum angular frequency. These formulae have been obtained by a computer optimization program which also indicates that the maximum voltage variation across Ci is ±0.36 dB and the maximum VSWR seen by the generator 1.36. When the input capacitance at the lowest frequency is chosen, which is approx. 117 pF, we find that:

Rg = R2 = 19.8 Ω

C1 = C5 = 45.2 pF

L1 = L3 = 28.6 nH.

In practice Rg is equal to 25 Ω and Zi varies with frequency. This required a re-optimization of this network with the actual values of Zi and Rg. The values calculated above were used as the initial values and parasitics of C1 and C5 were included. The target gain was set to 17.5 dB.
The results of this optimization are shown in Table 2.

Table 2

BEFORE OPTIMIZATION		AFTER OPTIMIZATION	
C1	45.2 pF	C1	60.1 pF
C5	45.2 pF	C5	47.5 pF
L1	28.6 nH	L1	36 nH
L3	28.6 nH	L3	43.8 nH
R2	19.8 Ω	R2	20.8 Ω
Rg	25 Ω	Rg	25 Ω
$VSWR_{max}$	1.812	$VSWR_{max}$	1.376
G_{pmin}	15.8 dB	G_{pmin}	17.1 dB
G_{pmax}	16.9 dB	G_{pmax}	17.9 dB

3 TRANSFORMER DESIGN

3.1 General

As mentioned before transformers employed at the input and output side utilize twisted-wire-pair transmission lines wound on a toroidal core.
The windings are uniformly distributed around the toroid. The required characteristic impedance of the transmission lines is 50 Ω. In practice Zo will differ from this required value and compensation measures will be necessary (2). This can be achieved with:

- Parallel capacitances across input and output terminals of the transformers if Zo > 50 Ω
- Inductances in series with the input and output terminals of the transformer if Zo < 50 Ω.

The result of this compensation is an exact match at the maximum frequency. There will be however, a slight mismatch at low frequency which is many times smaller then that at the maximum frequency without compensation. Because the amount of HF compensation will depend on the circuit layout and the exact transformer construction no calculations will be made on this aspect of the transformers. The amount of compensation will be determined in the circuit by employing adjustable capacitors.

3.2 Design of the output transformer

The characteristic impedance of 50 Ω for the transmission line of the output transformer has been obtained with enamelled copper wire of 0.6 mm diameter. Its diameter with isolation included is 0.66 mm.
The number of twists applied are 2 per centimeter.

A suitable core material for this frequency range is Philips 4C6 grade available in several sizes of toroid. The size of the toroid is determined by the maximum allowable dissipation which is limited to 350 mW/cm^3 to prevent excessive rise in temperature. Designing for a maximum of 1% power loss in the core (300 mW) the minimum effective volume required is:

$$Ve_{min} = \frac{P_{loss}}{350\ mW/cm^3} = \frac{300}{350} = 0.85\ cm^3$$

The smallest toroid that is suitable is a core with dimensions D × d × h = 23 × 14 × 7 mm corresponding with a effective core volume of 1.79 cm^3. As a result the core loss reduces to 170 mW/cm^3.
According to reference (3) this corresponds to a maximum flux density (B) of 0.2 mT at 110 MHz. The required number of turns is determined by the ratio Rp/L in which R_p is the loss resistance that represents the core loss and L the inductance in parallel with the output terminals, see reference (4).
This ratio is equal to:

$$R_p/L = \frac{\omega^2 \times B^2 \times Ve}{2 \times \mu_o \times \mu_r \times P_{loss}} \quad (9)$$

which amounts to: $R_p/L = \frac{\left(2 \times \pi \times 110 \times 10^6\right)^2 \times \left(0.2 \times 10^{-3}\right)^2 \times 1.79 \times 10^{-6}}{2 \times 4 \times \pi \times 10^{-7} \times 120 \times 0.3} = 472\Omega/\mu H$

To keep the core loss below 1% we must keep the parallel loss resistance above 5000 Ω with reference to 50 Ω. This means an inductance of: L = Rp/472 = 10.6 μH

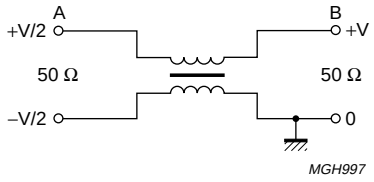

Fig.7

Between point A and B in Fig.7 the voltage is one half of the output voltage. Therefore the inductance between these points must be a quarter of that across the 50 Ω terminals, so:

L_{AB} = L/4 = 10.6/4 = 2.65 μH

The number of turns required can be calculated with the following formula (3):

$$L = A_L \times N^2 \quad (10)$$

$$A_L = \frac{0.4 \times \pi \times \mu r}{\Sigma l/A} \quad (11)$$

in which:

A_L is the inductance in (nH)

$\Sigma l/A$ is the core constant in (mm^{-1}) given in (3)

N is the number of turns

μr is the relative permeability (120 for grade 4C6).

For a toroid of 23 mm the core constant is 1.81 mm^{-1}. So, the inductance factor amounts to:

$A_L = \frac{0.4 \times \pi \times 120}{1.81} = 83.3$ nH

and the required number of turns:

$$N = \sqrt{\frac{2.65 \times 10^3}{83.3}} = 5.6 \text{ turns}$$

In practice the number of turns will be 6, so the inductance in parallel with the output terminals rises to:

$(6/5.6)^2 \times 10.6 = 12\ \mu H$

This corresponds to a reactance of 1885 Ω at 25 MHz which is high enough to be neglected.
The core loss reduces to:

$(5.6/6)^2 \times 1\% = 0.87\%$

The measured value of L_{AB} was approx. 3.5 μH.

3.3 Design of the input transformer

The input transformer is of the same type as the output transformer and is also designed in the same way.

To obtain a characteristic impedance of 50 Ω for the windings enamelled Cu-wire with a bare diameter of 0.50 mm is used. The diameter with isolation included is 0.55 mm. The number of twists applied is 2¾ per centimeter.

Allowing an input power level of 1.5 W the minimum effective volume for 1% power loss in the core is:

$Ve_{min} = 15/350 = 0.043\ cm^3$

The smallest toroid that suits our need is a type with dimensions D × d × h = 9 × 6 × 3 mm. The effective core volume is 0.105 cm^3, so the core loss reduces to 143 mW/cm^3. This corresponds to a maximum flux density B of approx. 0.18 mT at f = 110 MHz according to ref.(3). The ratio Rp/L amounts to:

$$Rp/L = \frac{\left(2 \times \pi \times 110 \times 10^6\right)^2 \times \left(0.18 \times 10^{-3}\right)^2 \times 0.105 \times 10^{-6}}{2 \times 4 \times \pi \times 10^{-7} \times 120 \times 0.015} = 360 \Omega/\mu H$$

For 1% loss L amount to:

L = Rp/360 = 5000/360 = 13.9 μH

L_{AB} = 13.9/4 = 3.48 μH

The required number of turns for a 9 mm toroid with a core constant of 5.17 mm^{-1} is:

$$A_L = \frac{0.4 \times \pi \times 120}{5.17} = 29.2 \text{ nH}$$

$$N = \sqrt{\frac{3.48 \times 10^3}{29.2}} = 11 \text{ turns}$$

An inductance of L = 13.9 μH corresponds to a reactance of 2183 Ω at 25 MHz which is high enough to be neglected.

According to measurements 10 turns were sufficient to obtain $L_{AB} \approx 3.5\ \mu H$.

3.4 The tapped choke (T2)

The chokes in the drain circuits are wound on a common ferrite rod. The windings are twisted together. Constructional details are shown in Fig.8. With this arrangement the dc flux components in the core cancel out and a much smaller component results. Because a rod has a open magnetic circuit saturation effects will hardly occur.
In Fig.9 the output part of the amplifier is given in a different way.

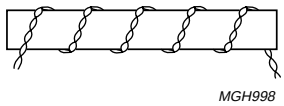

Fig.8

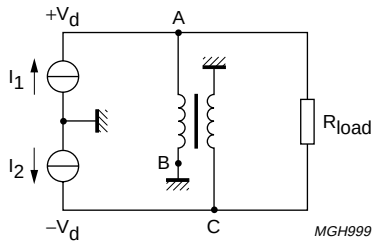

Fig.9

The current sources have a frequency spectrum in which the even order components are in phase and the odd order ones in anti-phase.
For the even harmonics the impedance between point A and C will depend on the coupling factor K between the windings with:

$$\omega L_{AB}(1-K) \tag{12}$$

If the coupling factor amounts to 1 points A and C will be short circuited. If the current components are in anti-phase the total inductance between these points shunts the load resistance. Because the voltage between point A and B is equal to ½ V_{AC} the total inductance L_{AC} is equal to 4 L_{AB} if the coupling factor is 1.
The reactance of this shunting inductance is allowed to be at least 4 times the load resistance or 200 Ω at 25 MHz. So, L_{AC} amounts to 1.27 μH and L_{AB} to 0.318 μH.

To obtain the inductance L_{AB} a ferrite rod grade 4B1 has been used with a length of 30 mm and a diameter of 5 mm. According to ref.(3) its relative permeability is equal to 20. The number of turns can be determined with:

$$N = \sqrt{\frac{L \times l}{\mu o \times \mu r \times A}} \tag{13}$$

For L_{AB} this amount to:

$$N = \sqrt{\frac{0.318 \times 10^{-6} \times 30 \times 10^{-3}}{4 \times \pi \times 10^{-7} \times 1/4 \times \pi \times \left(5 \times 10^{-3}\right)^2}} = 4.4 \text{ turns}$$

In practice 5 turns will be used so L_{AC} will be equal to 1.6 μH. The measured value for L_{AB} was 0.48 μH at 25 MHz. The windings are constructed of enamelled copper wire of 0.8 mm diameter.

4 AMPLIFIER CONSTRUCTION

4.1 Printed circuit board and component layout

The printer circuit board of this amplifier is made of two-sided copper clad epoxy fibre glass (εr = 4.5) laminate of 1/16" thickness.
Circuit components are situated on one side of this board, the other side serves as ground plane. A full sized pattern of the printed circuit board and component layout is given in Fig.13. The parasitic inductance of the printed tracks are absorbed in the inductances of the matching networks. Connections to the ground plane are made by means of tubular rivets, straps under the source leads and at the N-connectors and the mounting screws.

4.2 Heatsink

The printed circuit board is attached to a solid copper plate, with dimensions 120 × 100 × 10 mm, which functions as a heatsink. It is provided with a tube in order to control its temperature by means of a water cooling system. Good thermal contacts between transistors and heatsink is obtained by use of a heat-sinking compound.

5 AMPLIFIER ALIGNMENT

The amplifier was constructed according to the theoretical design procedures. Figure 12 shows the total circuit diagram of this amplifier. Parallel matching components as C1, C5 and C12 are connected directly from one side of the circuit to the other. Therefore their values are exactly one half of those calculated. The component list is given in Table 4.

Alignment of this amplifier was first done on a small signal basis. First the output circuit was aligned by replacing the BLF244 transistors with dummy loads, representing the conjugate of the optimum load impedance. The dummy's consisted of a 25 Ω resistance and a 43 pF capacitance. Several components in parallel were used to obtain symmetry and to reduce parasitic inductances. These components were soldered in an empty SOT123 header. The return loss was measured versus frequency at the load connection of the amplifier and minimized by applying compensation capacitors between the terminals of the output transformer. At the load site of the transformer 3.6 pF (C13) was needed and at the transistor side C12 was increased from 20 to 22 pF. The maximum VSWR obtained was 1.22.

Alignment of the input circuit has been done with the transistors in the circuit and supply and load connected. The quiescent drain current was set to approx. 200 mA per transistor and return loss was measured versus frequency. Experiments with capacitors in parallel with the input transformer terminals showed that no compensation was needed. The maximum VSWR obtained was 1.30.

After the small signal alignment the transistors were set to class-B operation by decreasing the quiescent drain current to 25 mA.
The first results obtained at P_{out} = 30 W were:
Gp = 15.6 ±1.2 dB; Eff. = 61.3 ±10%; VSWR ≤ 1.40 and second harmonic level ≤ –33 dB.

In order to improve the total performance of this amplifier especially with respect to gain flatness, variation in efficiency and second harmonic level some minor changes were introduced in the amplifier.

1. At the input side the circuit configuration shown in Fig.10a was changed into that of Fig.10b. No appreciable improvement was achieved with respect to gain performance but variations in efficiency reduced to ±6%. However, at the lower side of the band the second harmonic level increased to –28 dB.

2. Raising the quiescent drain current to 50 mA improved the gain with approx. 0.3 dB. However, the efficiency decreased with approx. 0.8%.
3. A resistance of approx. 12 Ω from the mid tap of the drain choke T2 to ground instead of direct grounding increased the average efficiency with approx. 1% and its variations decreased to ±2.8%. The second harmonic level improved with 2 dB.
4. The input balun was originally connected as shown in Fig.11a. For a perfect symmetrical push-pull amplifier it does not matter which terminal is grounded. In this case exchange of the terminals strongly affected the second harmonic level. For the case of Fig.11b this level improved to < –40 dB.
5. Finally the value of the resistors shown in Fig.10 was increased to 23.7 Ω. This improved the gain flatness to approx. ±0.6 dB. The input VSWR increased to 1.5.

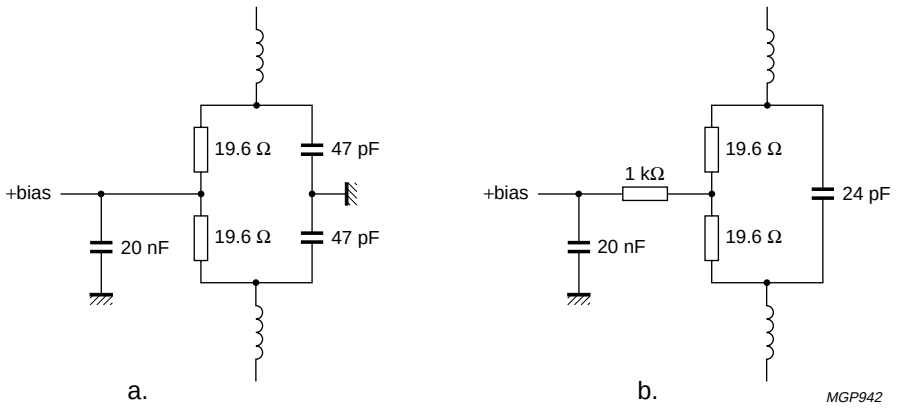

Fig.10

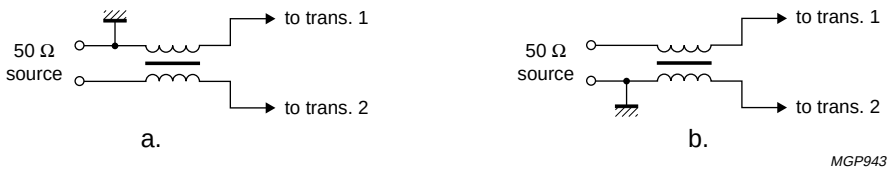

Fig.11

6 AMPLIFIER PERFORMANCE

6.1 General

Measurement of the amplifier performance was carried out under nominal conditions unless stated otherwise. These conditions are:

Supply voltage V_{dd} = 28 V

Quiescent drain current I_{dq} = 50 mA

Heatsink temperature T_{hs} = 25 °C.

Measurements were done at 10 frequencies within the band and 2 frequencies outside the band.

The BLF244 samples used, are matched on their threshold voltage V. The measured parameters of these transistors which can be relevant for balanced operation are given in Table 3.

Table 3

PARAMETER	CONDITIONS	UNIT	T1	T2
V_T	V_{ds} = 10 V; I_d = 5 mA	V	3.14	3.14
G_{FS}	V_{ds} = 10 V; I_d = 750 mA	mS	794	838
C_{rss}	V_{ds} = 28 V; V_{gs} = 0 V; f = 1 MHz	pF	4.46	4.21

The largest asymmetry observed in the drain current was ±3% at f = 25 MHz and P_o = 30 W.

6.2 Performance at constant output power

Measurements of the performance at a constant output power of 30 W were carried out at two heatsink temperatures, viz. T_h = 25 and 70 °C.

The results obtained are:

Powergain = 15.7 ±0.7 dB, see Fig.17

Drain eff. = 60.6 ±3.3%, see Fig.18

Input return loss <–14 dB (VSWR <1.50), see Fig.19

Second harmonic level <–40 dB, see Fig.20

Third harmonic level <–14 dB, see Fig.21.

At T_h = 70 °C the powergain decreased with approx. 1.2 dB see Fig.17.
The other parameters showed no appreciable change.

6.3 Performance at constant input power

Performance of this amplifier was also measured at a constant input power of 700 mW. The result obtained are:

Output power = 27.9 ±2.3 W, see Fig.22

Power gain = 16.0 ±0.3 dB, see Fig.23

Drain eff. = 59.0 ±4.5%, see Fig.24.

6.4 Performance at constant frequency

Figures 25, 26 and 27 show the following curves measured at 5 different frequencies:

$P_o = f(P_i)$

$G_p = f(P_o)$

Eff. = $f(P_o)$.

7 CONCLUSIONS

Using two BLF244 MOS transistors (matched on threshold voltage) in a push-pull configuration approx. 16 dB power gain and 60% drain efficiency have been obtained for an output power of 30 W, when operated with a quiescent drain current of 50 mA per transistor at V_{ds} = 28 V. The largest asymmetry observed in the drain current was ±3% at P_{out} = 30 W and f = 25 MHz. The input VSWR was below 1.5.

Throughout the band the second harmonic level was lower than –40 dB with reference to the fundamental. At a heatsink temperature of 70 °C the powergain decreased with approximately 1 dB while the other parameters showed no appreciable change.

8 REFERENCES

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3. Philips Data Handbook: 'MA01 on Magnetic Products: Soft Ferrites. For power handling of 4C6 material. See also earlier version of this handbook.
4. A.H. Hilbers; 'Power transformers for the frequency range of 30 – 80 MHz'; Laboratory report ECO7703, 1977.

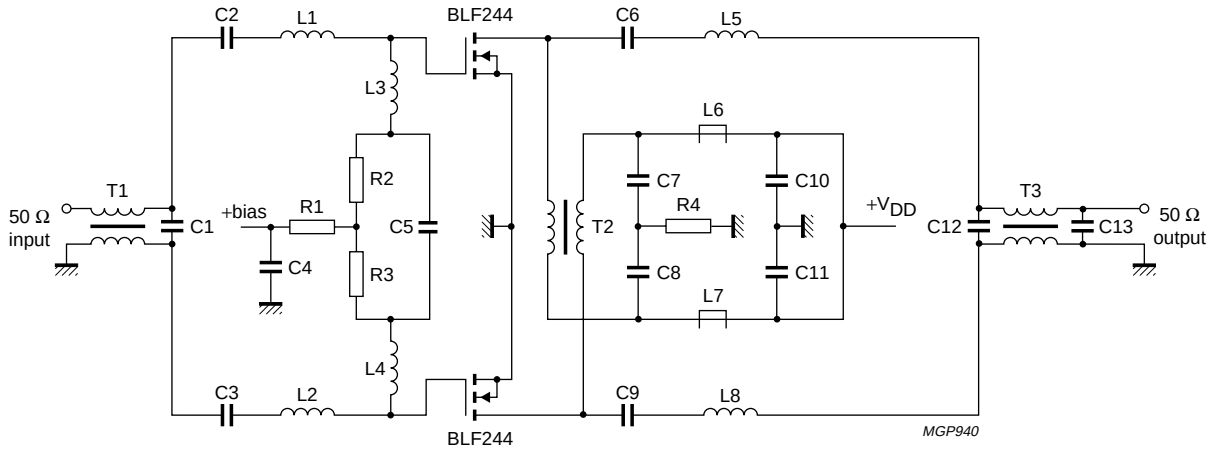

Fig.12 Circuit diagram of the wideband push-pull amplifier.

Table 4 List of components

Capacitors	
C1 = 30 pF	multilayer ceramic chip capacitor; note 1
C2 = C3 = C6 = C7 = C8 = C9 = 10 nF	multilayer ceramic capacitor (cat.nr. 2222 852 47103)
C4 = 2 × 10 nF	multilayer ceramic chip capacitor (cat.nr. 2222 852 47103)
C5 = 24 pF	multilayer ceramic chip capacitor; note 1
C10 = C11 = 100 nF	multilayer ceramic chip capacitor (cat.nr. 2222 852 47104)
C12 = 22 pF	multilayer ceramic chip capacitor; note 1
C13 = 3.6 pF	multilayer ceramic chip capacitor; note 1
Inductors	
L1 = L2 = 27 nH	3 turns enamelled Cu-wire (0.8 mm); int.dia. = 4.0 mm; length = 6.1 mm; leads 2 × 3 mm
L3 = L4 = 48 nH	4 turns enamelled Cu-wire (0.8 mm); int.dia = 4.0 mm; length 6.2 mm; leads 2 × 1 mm
L5 = L8 = 30 nH	3 turns enamelled Cu-wire (0.8 mm); int.dia. = 4.0 mm; length = 4.8 mm; leads 2 × 2 mm
L6 = L7 = Ferroxcube RF choke	grade 3B (cat.nr. 4312 020 36640)
Resistors	
R1 = 1 kΩ	metal film resistor; 0.4 W
R2 = R3 = 23.7 Ω	metal film resistor; 0.4 W
R4 = 12.1 Ω	metal film resistor; 0.4 W
Transformers	
T1– $\frac{1}{1}$ Balun	10 turns of twisted pair of 0.5 mm enamelled Cu-wire (2¾ twists per cm) wound on a toroidal core grade 4C6, dimensions (9 × 6 × 3) mm (cat.nr. 4322 020 97191)
T2– Drain choke	5 turns of twisted pair of enamelled Cu-wire (4.5 twists per cm) wound on a ferroxcube rod grade 4B1, dimensions (5 × 30) mm
T3– $\frac{1}{1}$ Balun	6 turns of twisted pair of 0.6 mm enamelled Cu-wire (2 twists per cm) wound on a toroidal core grade 4C6, dimensions (23 × 14 × 7) mm (cat.nr. 4322 020 97171)
Printed circuit board	double sided Cu-clad epoxy fibreglass laminate (εr = 4.5), thickness 1/16”

Note

1. American Technical Ceramics capacitor type 100B.

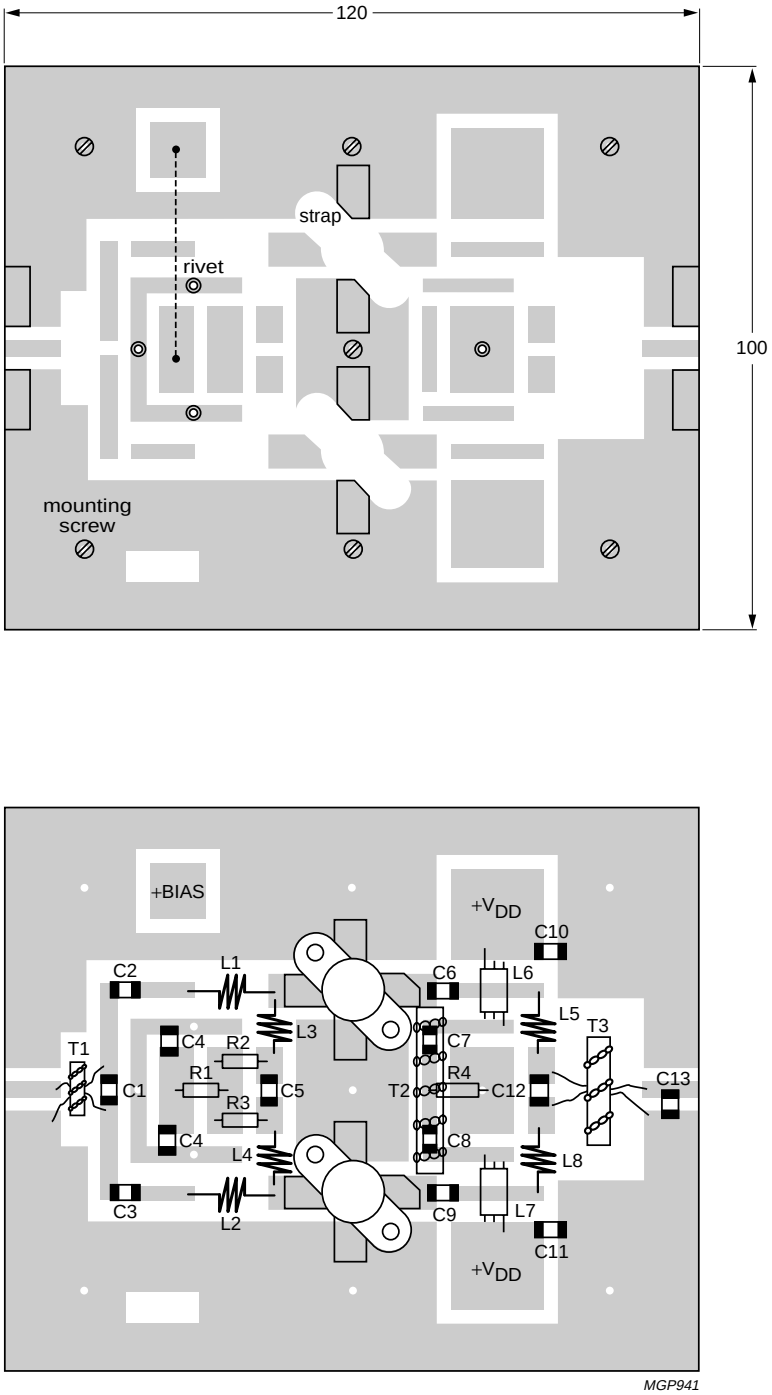

Fig.13 Printed circuit board and component lay-out.

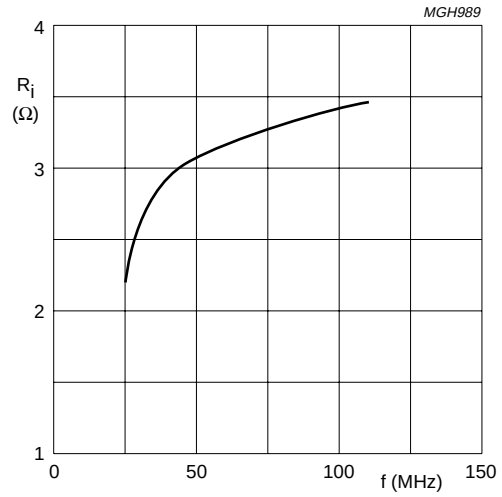

Fig.14 Real part of input impedance.

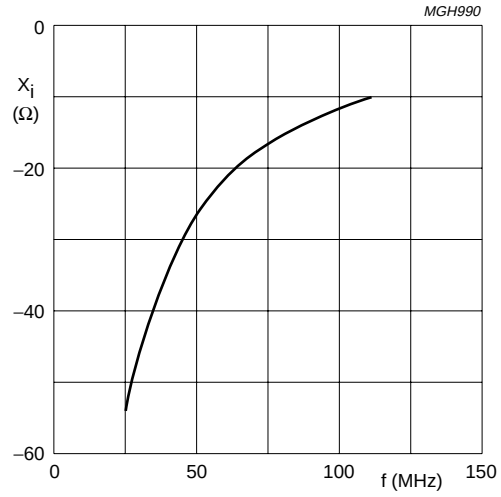

Fig.15 Imaginary part of input impedance.

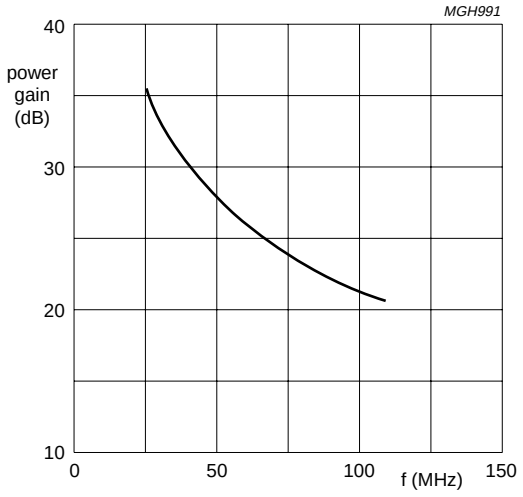

Fig.16 Powergain of transistor.

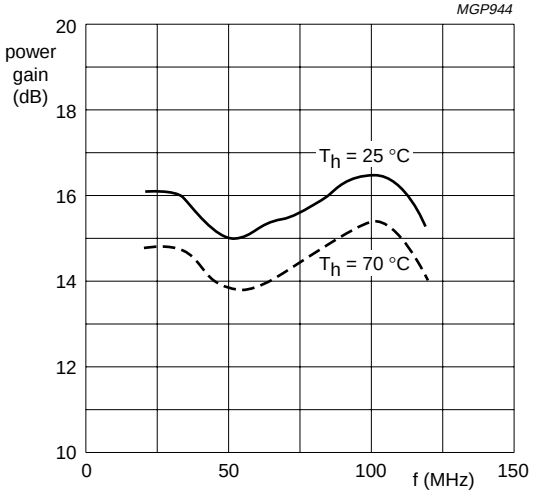

Fig.17 Powergain versus frequency.

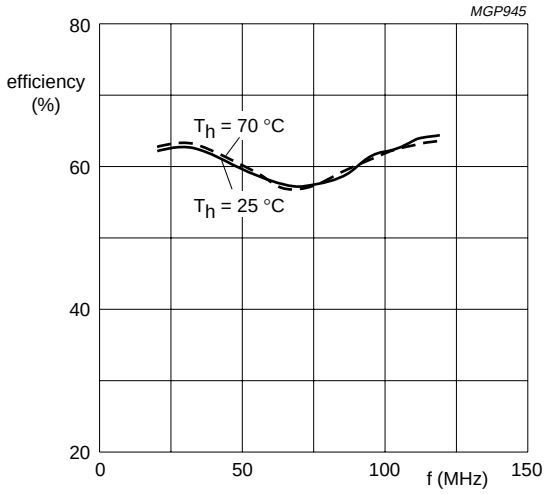

Fig.18 Drain efficiency versus frequency.

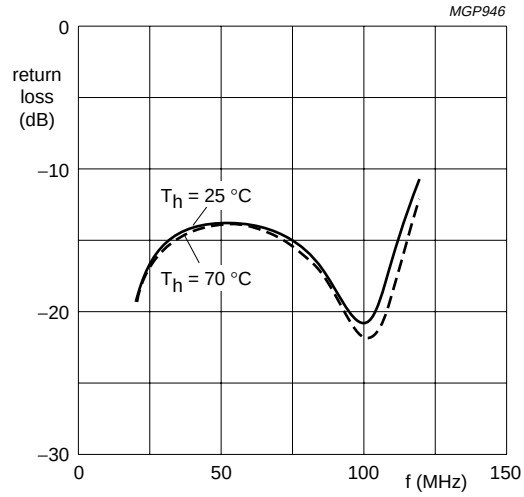

Fig.19 Return loss versus frequency.

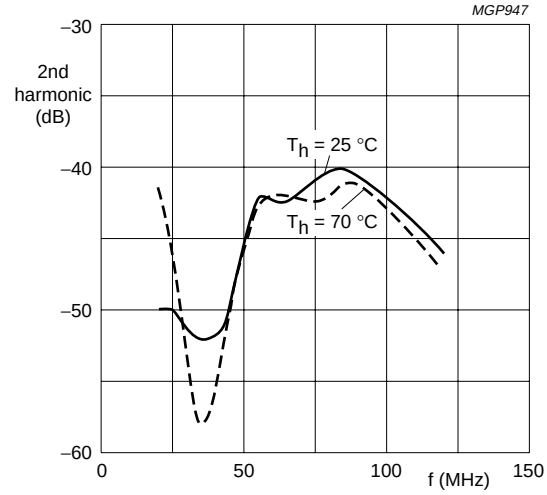

Fig.20 2nd harmonic level versus frequency.

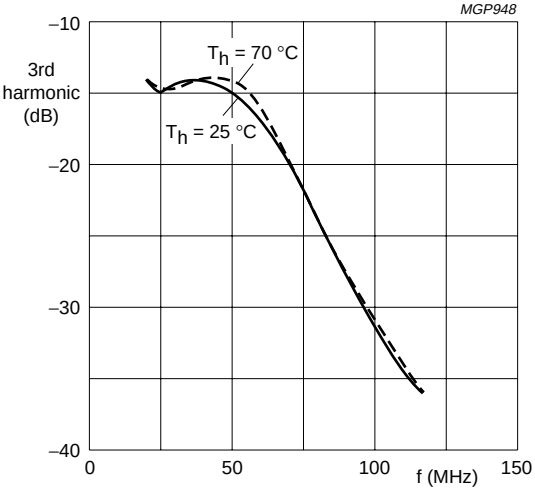

Fig.21 3rd harmonic level versus frequency.

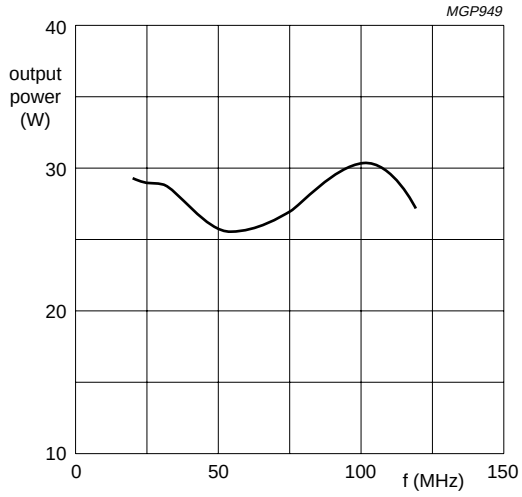

Fig.22 Output power versus frequency.

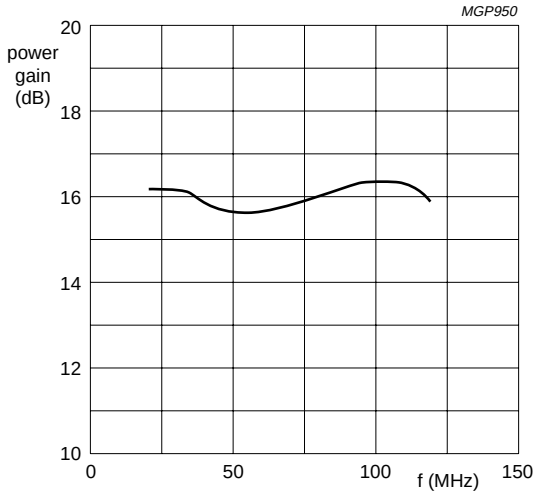

Fig.23 Powergain versus frequency.

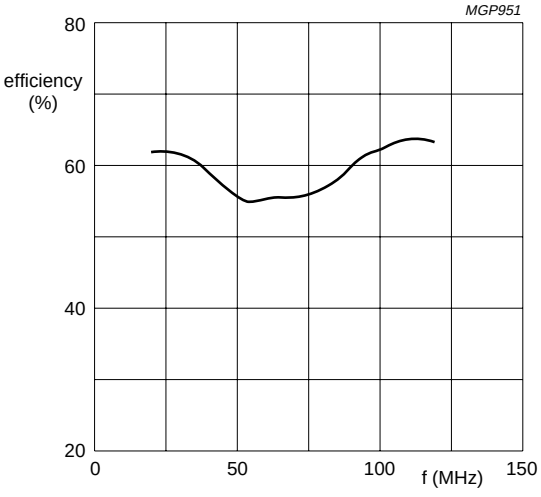

Fig.24 Drain efficiency versus frequency.

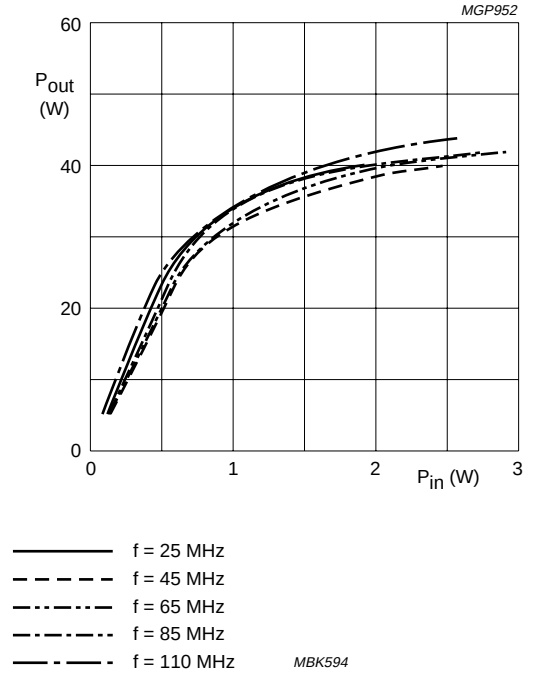

Fig.25 Output power versus input power.

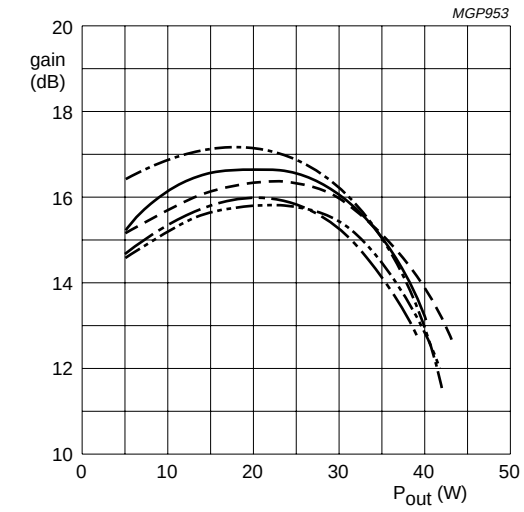

Fig.26 Powergain versus output power.

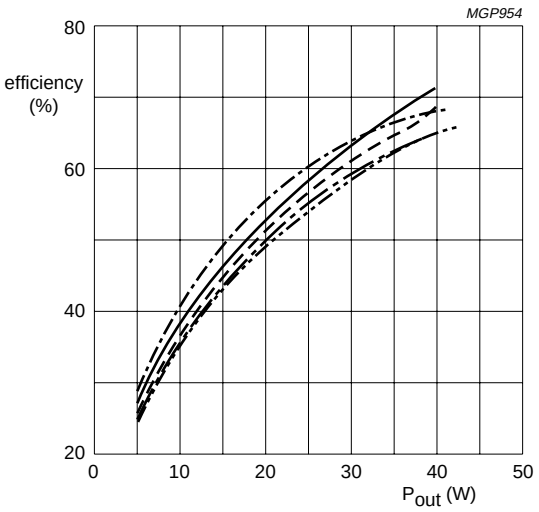

Fig.27 Drain efficiency versus output power.

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