XPLA PC-ISP Download Software

The XPLA™ PC-ISP Download software provides the capability for performing ISP (In System Programming) of CoolRunner™ parts. This software allows for the programming of single or multiple parts in any standard JTAG chain and includes the ability to bypass non-CoolRunner CPLDs in the same chain. Other features include SVF generation, batch mode processing, UES (User Electronic Signature) programming, and Master device copying.

This manual is comprised of four main sections:

- Installation
- Quick Start
- Hardware
- ISP GUI: Interface and Commands
- Generating MCS Files for XPLA2
- Trouble Shooting ISP Issues
  - Hardware
  - Software
- Revision History

INSTALLATION

System Requirements:

Minimum requirements are:
IBM PC 386
Windows 3.1, 3.11, 95,98 (for 3.1, 3.11, Win32S is required)
5 Meg disk space
16 Meg RAM

It is recommended that a monitor and video card capable of supporting 800X600 in 16 bit True Color be used.

Setup

XPLA PC-ISP software is available on any of the XPLA software CD's, or may be downloaded from our technical support web site (www.xilinx.com/products/coolrunner/programming). If downloaded, the setup files are compressed into a self extracting executable file. Running this executable will yield a 'setup.exe' file which will initiate installation. This setup file is found within the \ISP directory of the XPLA CD.

Launching the 'Setup' file will invoke a dialog box requesting a drive letter and directory path for the installation of the software program. Completion of the path (or selection of the default path) and confirmation of this information by clicking 'OK' will allow the setup program to complete installation.

Software updates for the XPLA PC-ISP software are always available free of charge on the CoolRunner website.

QUICK START

This Quick Start overview will use the ISP Proto board for example purposes. After installation, attach the ISP cable to one of the parallel ports on the computer and attach the other end to the ISP header on the target PCB. Apply power to the board and launch the ISP software. After initialization, the opening GUI should resemble figure 1: Initial GUI. Note that the message window indicates that there is one device in the JTAG chain. If the software does not locate any JTAG parts in the chain, check the integrity of the cable connections, confirm that adequate board power is supplied, then click on the 'Hypercable' and 'Check Connection' menu option to query the system for JTAG parts. If this still does not find any devices in the chain, refer to 'Trouble Shooting ISP Issues' in this document.

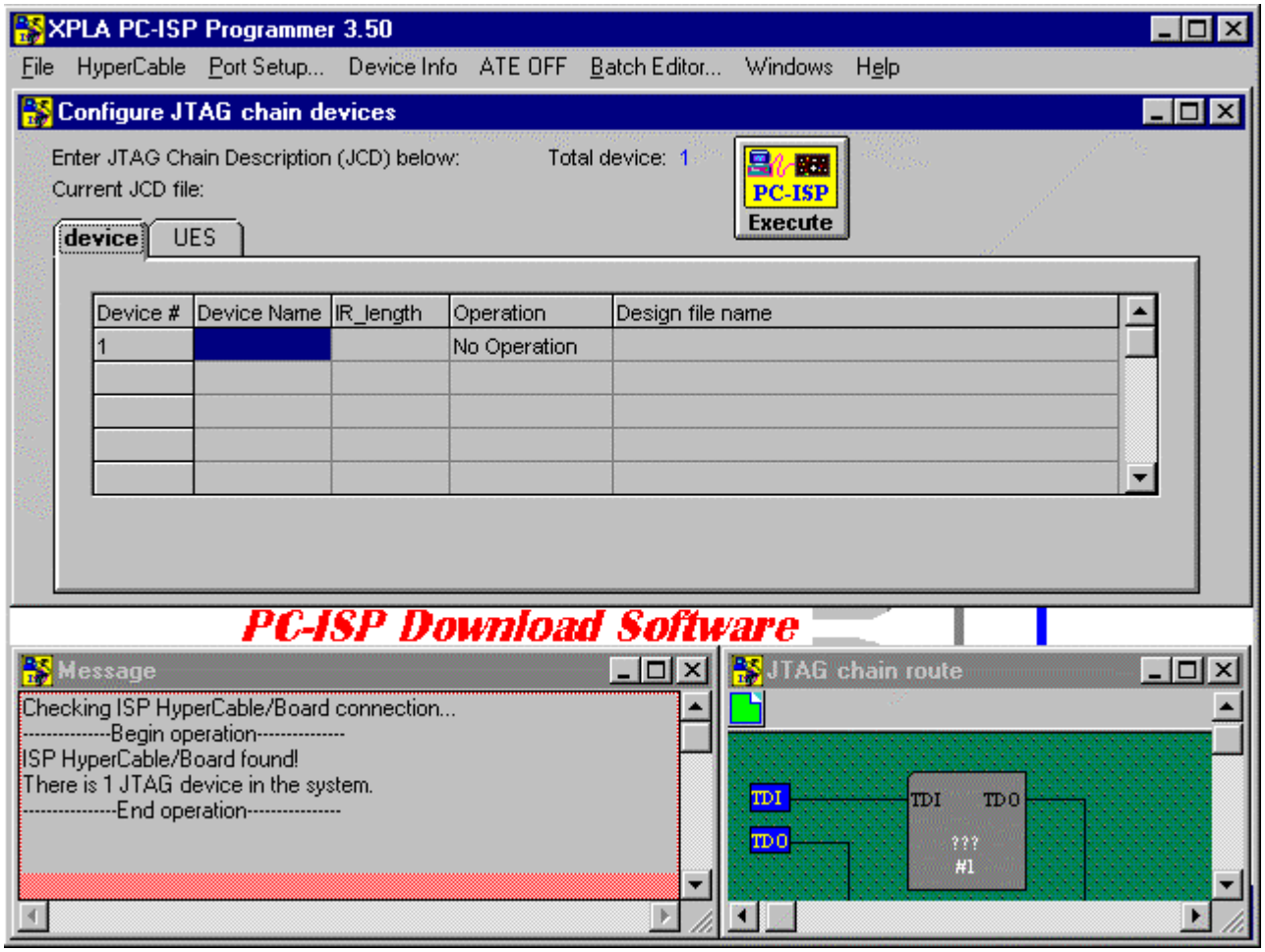

Figure 1: Initial GUI

This initial GUI can be expanded to fit the entire display, and the windows resized for optimal use. Note that the 'Configure JTAG Device' window has a single device in the chain, and that the JTAG Chain Route window displays this device graphically.

The next step in performing ISP operations is to define the components in the JTAG chain. This is done by double clicking on the cell in the device name column of the 'Configure' window. Select the appropriate part (in this instance it is a PZx128 device. The IR (Instruction Register) Length is automatically set to four bits whenever you select a CoolRunner JTAG CPLD. Next, double click on the 'Operation' cell associated with the device, and select an

option. For basic programming use, the 'Program and Verify' selection will most commonly be used. Finally, double click on the cell below 'Design File Name' and use the browser to select either a valid *.jed or *.bin file to use with the 'Operation' assignment. When finished, the 'Configure' window should look similar to figure 2: Configured GUI

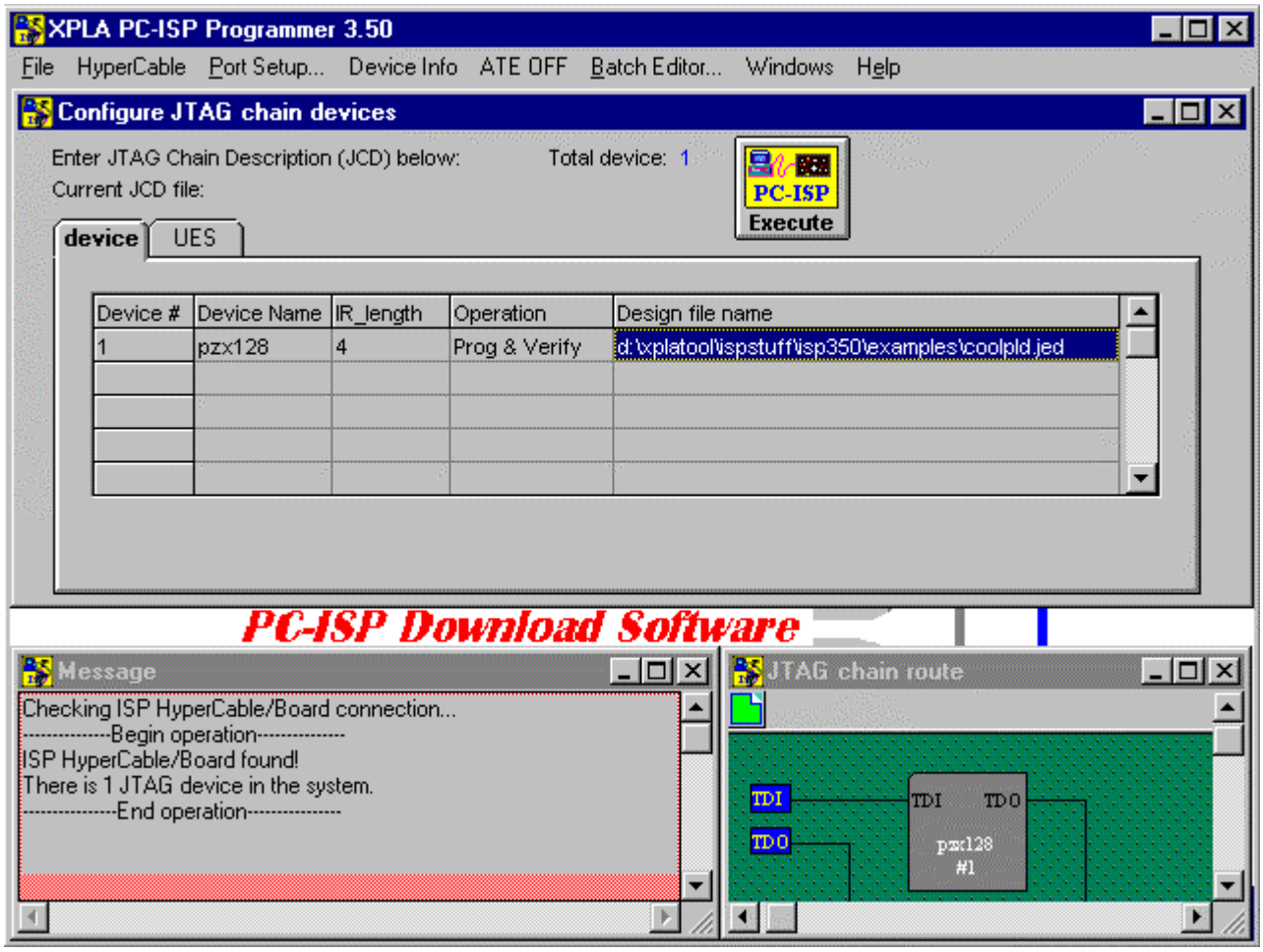

Figure 2: Configured GUI

To perform the operation selected in the 'Operation' cell, click on the 'Execute' button. This will perform the operation and record the status and results of the operation in the Message window. Refer to the appropriate section of this manual for additional information on menus, options, and features.

HARDWARE

Download Cable

It is recommended that the end user use a Xilinx download cable, however, a passive cable may be made that will support CoolRunner CPLD's. This passive cable is comprised of a 10 conductor ribbon cable of no more than approximately six feet in length, terminated on one end by a 2X5 pin (Berg Strip type) female ribbon connector, and on the other end by a parallel port compatible (typically DB25 Male) connector. See Figure3: ISP Cable.

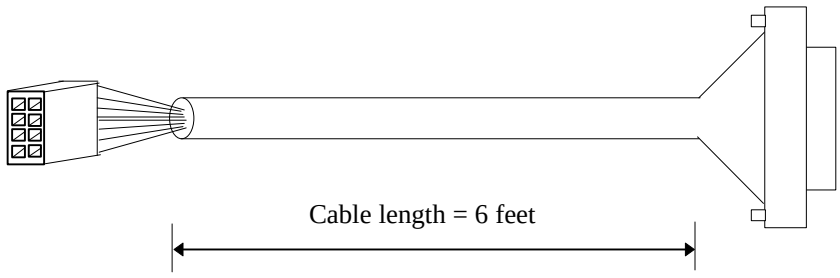

Figure 3: ISP Cable

Each of the signal lines (TMS,TCK,TDI,TDO) should be series terminated at the source (DB25 end) with 100 Ohm resistors. The signal lines should be interleaved with ground for noise rejection and general shielding. See Figure 4: Cable Wiring Diagram for additional details.

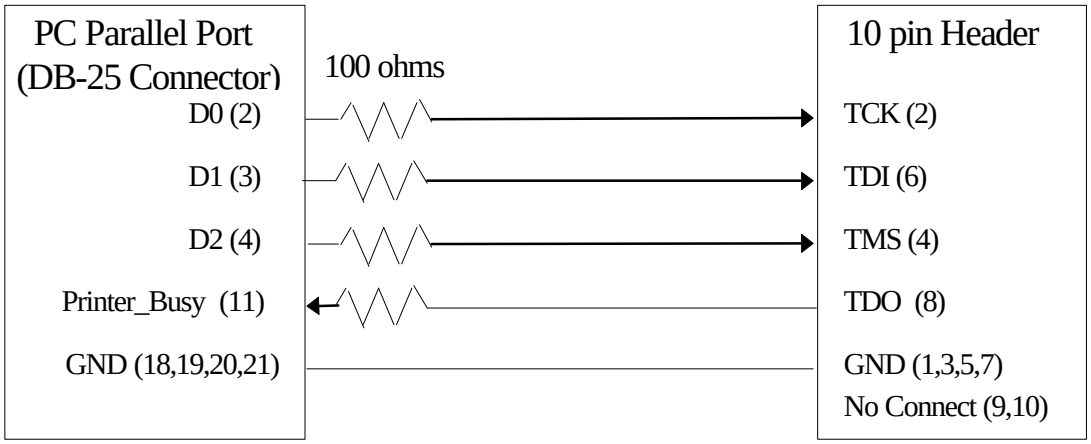

Figure 4: Cable Wiring Diagram

To interface the cable to the Original XPLA ISP Demo Board, the header connector should be wired as in Figure 5: ISP Cable Header Bottom View. If a Xilinx cable is used, the customer will have to provide for an interface cable.

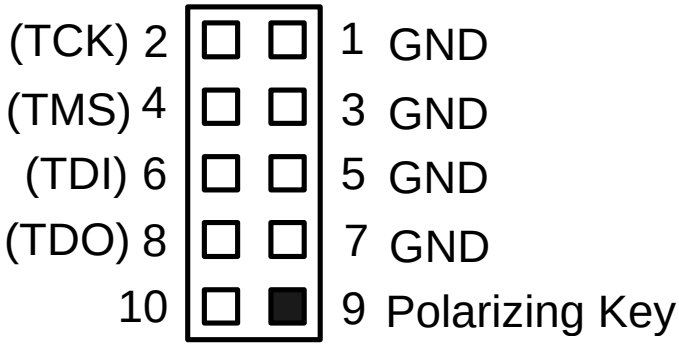

Figure 5: ISP Cable Header Bottom View

! Note: The actual silk-screen numbering on the ISP Proto Board is incorrect. Refer to figure 5 and use the mirror image of this for correct PCB layout numbering.

For more information on cable construction (for the XPLA CPLD ISP Demo Board) refer to: 'isp_cable.pdf' which may be found on the CoolRunner website under the software page.

PC Board Connection

For programming of multiple devices in a JTAG chain, it is required that each device be tied in series with regards to the data lines (TDO of device 1 tied to TDI of device 2 and so forth), and that the control lines (TMS and TCK) be tied in parallel. Do not allow any of the JTAG inputs (TDI,TMS,TCK) to float. Noise on these lines may be interpreted as signals and could cause erratic operation. It is best to pull these inputs high when not being used for JTAG purposes (a typical pull-up value is 10k Ohms to VCC). It is considered good practice to buffer all signals that enter or exit a PC Board, and this is especially true when multiple devices are connected in parallel to a single line. Keep in mind that a PC Parallel port has a typical output impedance of approximately 10k Ohms which is not low enough to drive multiple loads and support higher bandwidths.

An excellent additional reference is: 'ISP Design Considerations for the CoolRunner PZx128 CPLD' which can be found on the www.coolpld.com website.

Note: a common mistake is to overlook the requirement for a ground connection at the JTAG header on the PC Board.

ISP GUI

Launching the ISP software results in the display of the front panel of the GUI (See Figure 1: Initial GUI). Upon invocation, the software performs a test that interrogates the parallel port / cable to determine the number of JTAG devices in the JTAG chain. The results are displayed in the Message window. Notice that there are three windows displayed and several pull down menu options. This section will cover the following:

- Pull Down Menus
  - File
  - Hypercable
  - Port Setup
  - Device Info
  - ATE Options
  - Batch Editor
  - Windows
  - Help

- GUI Description and Use
  - Configure JTAG Device Window
  - Message Window
  - JTAG Chain Display Window

Pull Down Menus

The pull down menus allow for the configuration and test of the operating software and system, and provide access to batch mode processing, and creation of output files.

File

This Menu allows the user to save or to recall a .jcd (JEDEC Chain Description) file. A JCD file may be created by the user to preserve chain information. The JCD file also preserves commands for each individual device; multiple JCD files may be combined using the batch editor to streamline production programming of ISP systems.

An ASCII editor may also be started from this menu. The editor can be used to modify the JCD or batch files by hand. Or to examine or modify JEDEC files. The '**File**' menu option is not used to load JEDEC files for downloading. The designation of a JEDEC file for use is performed by double clicking in the 'Design File Name' cell in the 'Configure JTAG Chain Devices' window.

Hypercable

When selected, this menu option will examine the JTAG chain to determine if the chain is correctly connected, and that the cable and parallel port are functioning properly. This is the same function that occurs when the PC-ISP software is first launched. This is convenient if the program was started without the cable/board attached, or any time the integrity of the JTAG chain needs to be evaluated.

Port Setup

The PC-ISP software has the ability to examine each of the parallel ports whenever the **Hypercable** command is run to determine which port the cable and board are attached to. There are four choices in the selection window for the port, three of which will force the software to a specific port. The forth choice is the Auto Port Selection, which will automatically determine the correct port. See Figure 6: Port Setup.

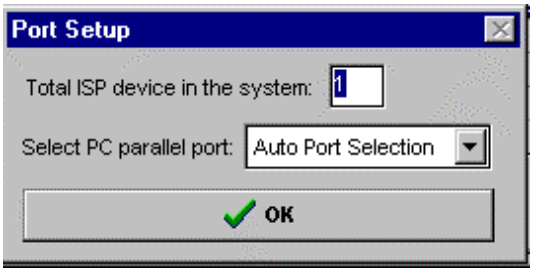

Figure 6: Port Setup

If a user does not have a cable or board in place, but still wants to run the software for evaluation or creation of JCD or batch files, they may do so by forcing the software to create phantom devices. This is done by entering a number of devices in this Port Setup Window. Clicking on OK will allow the software to run as if those devices were actually in place.

Do not modify the number of devices in the port setup window unless it is required for the software to run in trial mode. Any modification of this value will result in the software going into trial mode.

Device Info

This menu item will provide a Device ID button. When pushed, the Device ID and Security Status window will appear. The user must have configured the JTAG chain and read the Device ID for each of the devices in the chain for this Status window to display valid information. Once the Device ID's have been read, security status as well as factory programmed identification may be examined for each of the CoolRunner CPLDs in the JTAG chain. See **Configuration Window** commands for more information.

ATE

ATE (Automated Test Equipment) vector files may be created from the ISP Download software. This function will create the Erase / Program / Verify files necessary for programming on a Teradyne or other SVF compatible test equipment. When ATE is turned on, the parallel port connection must be turned off (under 'Help' then 'Ouput Options').

Batch

The Batch menu allows for the creation, save, load, and execution of batch files. A batch ISP file is comprised of one or more JCD files that are performed in succession. This enables the user to create complex ISP procedures and execute these procedures with a minimal amount of intervention. A total of 20 JCD files may be included in a single batch file. See Figure 7: Example of Batch file for an illustration of the creation of a batch file.

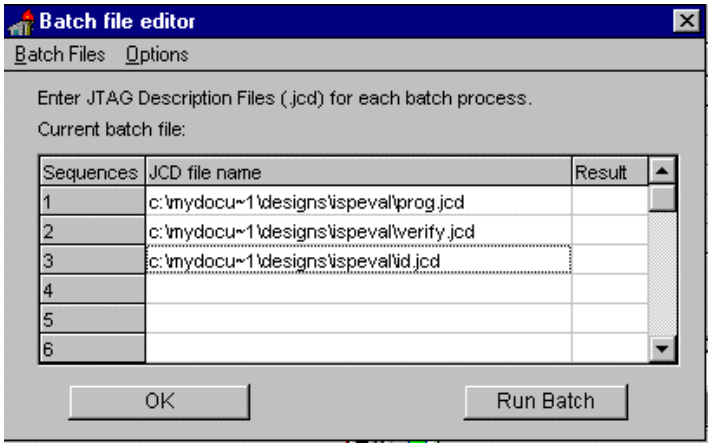

Figure 7: Example of Batch file

During the processing of a Batch file, the result of each individual operation will be displayed in the 'Result' cell. The user is encouraged to examine this result to verify that all steps were processed correctly.

Windows

The windows menu enables the user to reconfigure the display to show only the pertinent windows required for any function. The windows may be tiled, cascaded, restored, or minimized.

Help

The help menu allows access to help information regarding PC-ISP as well as general information such as version number. The ISP Debug Operation Panel includes a checkbox for outputting a text file with a record of events and results of ISP operations. The Debug panel includes:

- Verify Operation Result
- Off Line Programming
- Use Standard Data Frame
- Reserved

Verify Operation Result

When this option is checked, a text file will be created during verify for XPLA1 components. This file will contain the discrepancy data between the device file and the master file.

Use Standard Data Frame

This option forces the ISP tool to output a MCS file that is not compressed. The default format of the MCS output (for XPLA2 devices) is compressed. See 'Generating MCS Files' for more information on MCS generation.

Off Line Programming

When this option is selected, it will force the programmer to go into the off line programming mode. This will disable the parallel port and is used to create .jcd files, batch files, and MCS files. It may also be used to run the software in an evaluation mode.

Reserved

This button is reserved for future features.

GUI Description and Use

Configuration Window

The configuration window is primarily a spread sheet type display that organizes the parts in the JTAG chain and associates these parts with instructions or commands for ISP activity. This window also includes a large 'Execute' button for starting the list of commands on the device sheet. There are two sheets in this window that will be covered in this section:

- Device Sheet
- UES Sheet

Device Sheet

Upon entering the PC-ISP Program, the software determines if a JTAG chain of devices is present, and if so, how many devices are in the chain. It does this by assuming that there are 256 devices with four bit Instruction Registers (IR). The universal instruction for bypass is an IR full of '1's. The software fills all of the devices (overflow is of no concern) with '1's which places a single register between TDI and TDO. Then a single '0' is placed onto TDI and the number of clocks are counted until this bit arrives back at the parallel port on TDO. The number of clocks between the sending and receive of this zero is equal to the number of JTAG devices in the chain.

Device Name Column

Once the software knows how many devices are in the chain, it fills the first column of the Device Sheet with a number that corresponds to the JTAG device's position in the chain. It is up to the user to fill in the device name for each of the JTAG components. This is done by double clicking within the corresponding cell and selecting the type of part for each device.

IR Length Column

If the device is a CoolRunner CPLD, then the Instruction Register Length is automatically filled in for you with the number '4'. For non-CoolRunner CPLD parts, the user must enter the correct instruction register length for each of the other parts. Contact the vendors of your other parts (or consult a data sheet) to obtain this critical information. Other CPLD vendor's Instruction Registers are shown in Figure 8: IR Length for Other CPLD's

Vendor	Instruction Register Length
Altera	10
Lattice (Most ISPLSI)	5

Vantis	6
Xilinx 9500	8

Figure 8: IR Length for Other CPLD's

Operation Column

The Operation column contains the actual operation that is required to be performed on that particular device once the 'Execute' button is pressed. Double clicking on each cell in this column will call up a menu of operations which include:

- Bulk Erase
- Program
- Prog_&_Verify
- Secure Device
- Read User Signature
- No Operation (Bypass)
- Blank Check
- Verify
- Read Device ID
- Program User Signature
- Upload Device

Bulk Erase

! This will erase the entire EE array within the device and will return it to a fully blank device. Note that this will also erase the User Electronic Signature portion of the EE and all UES information will be lost. This also resets the secure device bit.

Blank Check

Verifies that the EE array is in a completely blank state. All EE cell locations should verify as a '1'.

Program

'Program' will use the .jed file or the .bin file specified in the corresponding 'Design File Name' cell and program the appropriate device with this file.

Verify

'Verify' will compare the contents of the ISP device with that of the file specified in the corresponding 'Design File Name' and indicate as to whether or not the two files match.

Program and Verify

This command combines the functions of 'Program' and 'Verify' into a single command. The operations of 'Program' and those of 'Verify' are performed in an interleaved fashion.

Read Device ID

'Read Device ID' will upload the manufacturing data for each of the CoolRunner CPLD parts in the JTAG chain this information consists of the data shown in Figure 9: Device ID Information Window

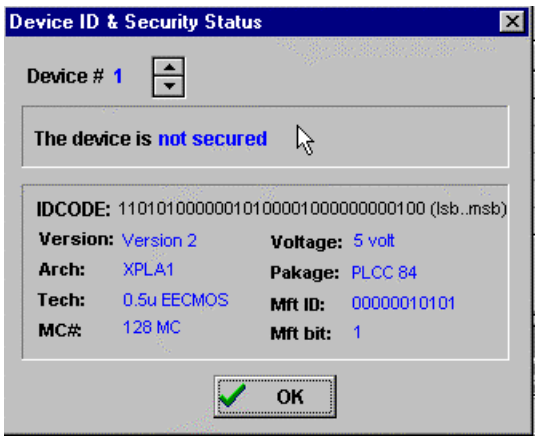

Figure 9: Device ID Information Window

Once the Device ID has been read, positioning of the cursor over any device in the 'JTAG Chain Route' window in the top GUI will result in an information box displayed with the corresponding information annotated for that device. See 'Figure 10: JTAG Chain ID Display' for an example.

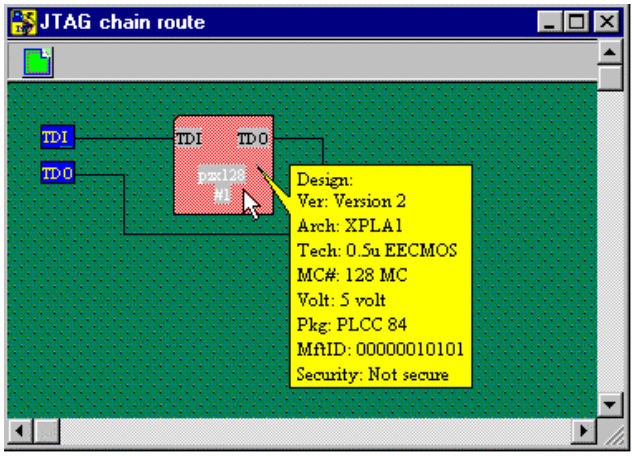

Figure 10: JTAG Chain ID Display

Secure Device

This command will set the security bit within the corresponding device. It will not be possible to upload the design, nor will it be possible to successfully verify after this command has been performed. The user is encouraged to secure the device as the last step in the ISP process.

Program User Signature

'Program User Signature' will take the ASCII information from the dialogue box on the UES page (See **UES Sheet** section) and will program the appropriate part with that information.

Read User Signature

This operation will upload the UES section of a device and then display the UES sheet with the recorded UES displayed within the cells.

Upload Device

'Upload Device' allows for the capture and recording of a master device to be used for duplication. This command requires that a unique filename (terminated with the extension .bin) be entered in the 'Design File Name' cell. This file will then be saved to the path indicated in that same cell. Note: Secured devices will result in a file that has non-useable data. These files should not be used to attempt to program a device; improper binary files could result in problematic or self destructive characteristics.

No Operation / Bypass

When this operation is selected, the instruction register is filled with '1's and the device is placed in bypass. A single register will be placed between TDI and TDO while this operation is selected. This is the only operation allowed for non-CoolRunner CPLD devices.

Design File Name Column

The final column is the 'Design File Name Column'. This cell contains the path and name of the JEDEC file that will be used for both the program and verify operations. A binary file may also be used in this cell. A Binary file is used whenever a previous device has been 'Uploaded' and it is desired to make a copy of that master device. Double clicking on this cell will launch a dialogue box for entering information; the user may also browse and point to the desired file. The information in this cell will be ignored for operations other than program or verify.

UES Sheet

The UES Sheet provides the user with access to a text cell for each of the devices in the JTAG chain. When a 'Program UES' command is executed from the Device window, the UES information for this command is read from this cell. This information is also saved whenever a JCD file is created. See Figure 11: UES Sheet Example

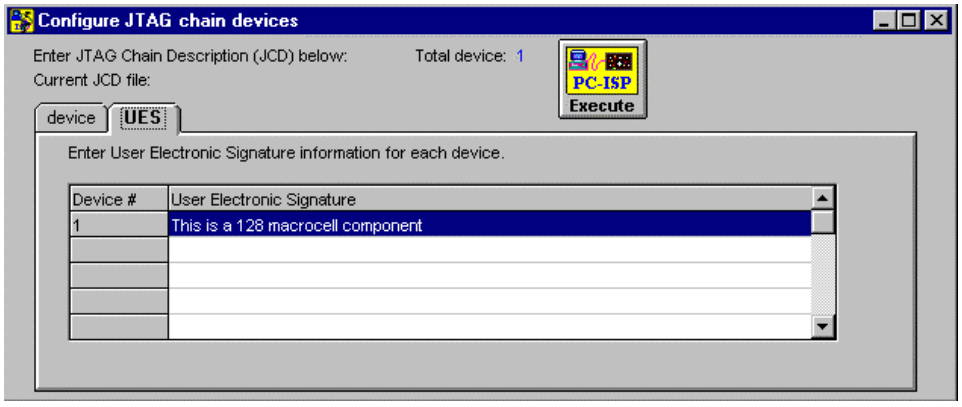

Figure 11: UES Sheet Example

It is important to note that the UES portion of each CoolRunner CPLD may be written to only one time after each Bulk Erase. In order to clear the UES memory of a device, the entire EE array must be erased which will completely remove the logic configuration of the CPLD.

The user volume in terms of ASCII characters in the UES section of each CoolRunner CPLD is shown in Figure 11: Useable UES Space.

Device Part Type	UES characters
X032	30
X064	60
X128	120

Figure 12: Useable UES Space

Message Window

The message window displays the status and results of operation of the PC-ISP software. This information may also be captured and archived in a text file. Under **Help** there is a debug menu option. Selecting this option will display a checkbox for enabling the operation text file.

JTAG Device Chain Window

This window is a graphical representation of the devices in the JTAG chain. Note that an information box appears whenever the mouse pointer is positioned on top of any device in this window. This information box is empty until a 'Read Device ID' operation has been performed. After the successful reading of device ID's, that information is annotated into the device information in the JTAG Device Chain Window (Figure 10: JTAG Chain ID Display).

GENERATING MCS FILES

To generate MCS files for the XPLA2 family of devices, a valid JEDEC file must be present for the device, then follow these steps:

1) Select the appropriate device (PZx960 or PZx320) in the Device Name Column
2) Select the appropriate operation (Program or Verify only) in the Operation Column.
3) Select the correct JEDEC file in the 'Design File Name' cell.
4) Under '**Help'** then '**Output Debug Options**' select the 'Off-line Programming Mode'.
5) Select 'Standard Data Frame' if required. A compressed data frame is the default mode. If the user wants the full data frame, this option must be selected.
6) Click on the Execute button to generate the MCS file.

TROUBLE SHOOTING ISP IMPLEMENTATION

Several common errors may happen in the implementation of ISP designs. Primary causes are typically hardware related, but in some instances the JEDEC file or download software may be to blame.

Hardware Issues

The most common hardware problem is incorrect wiring of the ISP cable or headers. However, there may be other problems to check for as well. If the software cannot locate any ISP devices, the following steps should be performed:

1) Verify that the appropriate power has been applied to the device. XPLA devices have extremely low operating currents, however, the power required to perform ISP operation (because of internal charge pump issues) is higher. It is not uncommon for a PZ5128 device to require 100mA of current at 5V for a few seconds. If this power is not available then the EE array may not program correctly.

2) Verify that the correct Parallel port is selected

3) Verify that the cable is connected to the PC and to the header on the PCB. Refer to figure 4 and figure 5 to confirm wiring. To verify that continuity is correct to the actual ISP part in the application, use an Ohmmeter to measure from the DB25 pins to the JTAG pins on the device (see Figure 13: DB25 JTAG Pin Description). There should be approximately 100 Ohms from DB pin to device pin.

DB25 Pin Number	JTAG Signal Name
2	TCK
3	TDI
4	TMS
11	TDO

Figure 13: DB25 JTAG Pin Description

4) It is good technique to decouple each power pin to ground. The decoupling capacitor should be placed as physically close to each power pin as possible; using surface mount capacitors will also help to decrease overall inductance. Remember to bulk decouple boards, and to have good power and ground planes. These items are not critical for the success of low bandwidth designs, but higher bandwidth designs or designers seeking good design and signal integrity may want to explore these suggestions.

5) The ISP Proto Board is equipped with a footprint and mounting holes for a BNC connector. Whenever this is used to input a high frequency clock, this clock is terminated on the board with an R/C combination (R2 and C7). If the user is satisfied using the onboard oscillator (which is a 555 timer), it is recommended that R7 be removed to decrease the rise time of the clock signal to ensure adequate clock slew. If this resistor is not removed, the ISP board may not function correctly.

Software Issues

The most common type of software error encountered when using XPLA PC-ISP is to have an incorrect JEDEC file specified for the 'Design File Name'. The error that occurs is 'Specified JEDEC file does not match device'. This occurs when the user selects the wrong part during 'fitting' in the design cycle. The user should verify that the correct device is called out in the JEDEC file by opening the JEDEC file with a text editor and examining line three of the file for device type (For XPLA generated JEDEC files only). Note that for the 32 and 64 macrocell parts, there must be a designation code of 'S' in the part name to qualify as an ISP part.

REVISION HISTORY

Version 3.50 provides the following features above 3.40:

- Supports up to 40 devices in JTAG Chain
- Supports 3960 and 3320 in JTAG programming and MCS Creation
- Binary File Upload/Download
- Enhanced Batch Editor with status report
- Enhanced Error checking

Version 3.40 provides the following features above 3.30:

- Batch mode processing of ISP manufacturing tasks
- SVF file generation
- Enhanced GUI for ease of use.
- Generate MCS file for 960
- ISP programming support for 960 device
- Decode Device ID for 32 and 64 macrocell packages

Version 3.30 provides the following features above 3.20:

- Multiple window operation
- Multiple device operation
  - 32 macrocell support (enhanced clock parts)
  - 64 macrocell support (enhanced clock parts)
- Allow non-CoolRunner device in JTAG chain. Devices other that XPLA CPLD's may be placed in bypass mode.
- Device / UES pages in Operation Window

Version 3.20 was an upgrade patch for 3.14 It provided the following enhancements:

- Enhanced ISP algorithms which improve
  - functionality
  - programming times
- Added the enhanced clocking 128 Macrocell devices
  - i.e. PZ5128c Enhanced Clocking -Commercial
  - i.e. PZ5128n Enhanced Clocking -Industrial

Version 3.14 was the first official release of the PC-ISP software. It supported a single PZX128 device.