1 Preface

This document does describe the open source oscilloscope specific peripherals implemented in the FPGA of the Welec W2000A series oscilloscopes. This FPGA design is called the LEON3 design by the Welec W2000A open source community and does support only 2 channels at the moment. For a CPU, the FPGA design does use the open source LEON3 SparcV8 processor from www.gaisler.com. All parts from www.gaisler.com are not documented here. If you need information of these parts read the grip.pdf and the Sparcv8.pdf reference manuals on www.gaisler.com.

1.1 GPL

2 Design concept

2.1 Portability

2.1.1 FPGA types and Vendors

This FPGA design can run on each FPGA with enough resources (LUTs, multipliers, sram blocks). The powerful LEON3 should be portable to almost all FPGA vendors. The oscilloscope part is now limited to Altera FPGAs, only because of the instantiated plls and sram blocks (and nothing else!). With a little work, it should run on every target.

2.1.2 Oscilloscope types

The LEON3 core does come with a lot of periphials an a debug support unit. Especially the debug support unit makes this design more flexible, because it can be used as a stupid address data interface with read and write access. Also the debug support unit is divided into a special function register and a debug communication link. The debug communication link is on the Welec W2000A series oscilloscopes the AHBUART and for example on the SandboxX the GRETH 100 Mbit Ethernet Controller with EDCL. So this FPGA design could also be ported to a ethernet connected oscilloscope without any processor or a display.

2.2 Features

2.2.1 Signal Capture Part

The design does use 4 interleaved 8 bit ADCs @ 250 MHz generating a sampling rate of 1 GS/s.
The downsampling stages do provide flexible builtin lowpass filters to improve the signal quality on

the fly from noisy 8 bits up to theoretical 16 bits before the signal capture buffer.
The available ranges are 1 GS/s, 500 MS/s, 250 MS/s (non interleaved), 125 MS/s (non interleaved), 100 MS/s, etc. downto 10 kS/s.

2.2.2 Trigger

The analog trigger is implemented as a Schmitt trigger working with one sample precision also @ 1 GS/s. It can be used as a flexible pretrigger, setting the trigger point anywere in the buffer. As a special feature this trigger does have a glitch detection mode. The trigger does handle the signal capture buffer and does provide the roll mode capability.

2.2.3 Capture Buffer

The signal capture buffer is limited to 32 kB by the FPGA. It could be used for 32 kS for 1 channel with 8 bit downto to 8 kS for 2 channels with 16 bit. The maximum roll mode sampling speed is limited to the processor access side performance.

2.3 VGA interface

Here the standard GRIP framebuffer SVGACTRL is used as 16 bit with a resolution from 640x480 pixels. For each color the 3 most significant bits are used. The least significant bit is pulsed to get the 9 bit colors linear on the Welec W2000A series oscilloscopes.

2.3.1 Frontpanel

All keys and knobs are scanned automatically in the hardware with interrupt notification posibility. All leds or analog setting are made with GPOs by the software for portability reasons.

2.3.2 Other IP Blocks

All other blocks are taken from the GRIP, the LEON3 periphial library from Gaisler Research. The SRAM controller has been modified to read 3 times faster and write 32 bit words 1/3 faster than the original ESA SRAM/FLASH controller.

3 Input capture part

3.1 Clock domain solution

First thing in the input capture part is lowering the data clock frequency for 1 sample @ 250 MHz to 2 samples @ 125 MHz. After this the data from the ADCs 0-2 are transferred to the clock domain the of the ADC 3. All samples are delayed to get in the right order to the filter stages.

4 Memory Mapping

library	device	memory start	size (HEX)	size (bytes)
W2000L	ROM	0x00000000	0x80000	8 MB
W2000L	unchached RAM mirror	0x20000000	0x20000	2 MB mirror
W2000L	cached RAM	0x40000000	0x20000	2 MB
GRIP	APBCTRL AHB/APB bridge	0x80000000	0x10000	APB address range
GRIP	memory control register dummy	0x80000000		
GRIP	APBUART generic UART	0x80000100		
GRIP	IRQMP Interrupt control	0x80000200		one processor
GRIP	GPTIMER	0x80000300		2 timers
W2000L	Oscilloscope core	0x80000500	0x20	128 Byte
GRIP	SVGACTRL SVGA core	0x80000600		
GRIP	AHBUART debug UART	0x80000700		
GRIP	DSU3 Debug Support Unit	0x90000000	0x10000000	DSU address range
W2000L	Signal Caption Buffer	0xA0000000	0x8000	32 kB

5 Oscillocope core registers (DSO/W2000L regs)

5.1 Overview

device indentification reg	0x00	read only	only device identification
interrupt ACK reg	0x04	read, write	for the interrupt routine selection
interrupt mask reg	0x08	read, write	interrupt masking
analog settings reg	0x0C	read, write	analog settings, front panel
sampling frequence reg	0x10	read, write	sampling frequence settings
sampling filter reg	0x14	read, write	downsampling filter configuration
external trigger source reg	0x18	read, write	external and auto trigger settings
reserved, obsolete	0x1C	read only	
signal source byte(0)	0x20	read, write	channel + upper and lower byte selection
signal source byte(1)	0x24	read, write	channel + upper and lower byte selection
signal source byte(2)	0x28	read, write	channel + upper and lower byte selection
signal source byte(3)	0x2C	read, write	channel + upper and lower byte selection
trigger source reg	0x30	read, write	trigger does watch on selected byte(n)
trigger once reg	0x34	read, write	start trigger and stop trigger or capture
trigger prefetch reg	0x38	read, write	trigger prefetch samples
trigger storage mode reg	0x3C	read, write	capture buffer storage mode
trigger read offset reg	0x40	read, write	capture buffer offset, roll mode reg
trigger type reg	0x44	read, write	trigger type selection
trigger low level reg	0x48	read, write	trigger low level detection
trigger low glitch reg	0x4C	read, write	glitch detection time register
trigger high level reg	0x50	read, write	trigger high level detection
trigger high glitch reg	0x54	read, write	glitch detection time register
trigger status reg	0x58	read only	trigger status register
trigger current addr reg	0x5C	read only	write address of the signal capture, roll mode reg
target specific reg	0x60	read, write	W2000L: generic or debug UART select register
lED register	0x64	read, write	led output register, rotary knobs
key reg(0)	0x68	read, write	rotary knob counter register
key reg(1)	0x6C	read, write	key register

5.2 Detailed register description

5.2.1 device indentification reg @ 0x00

It is read only and returns the device identification. Writing on it has no effect.

5.2.2 interrupt ACK reg @ 0x04

The interrupt ACK register is nessesary to know which interrupts of the DSO interrupts had requested the main DSO interrupt routine. Read the interrupt flags, reset the most important active flag and call the coresponding ISR routine for resetted flag.

bit n	description
0	capture data finished: ACK this bit to low in the ISR.
1	capture data triggered: Comes one time for the roll mode. ACK this bit to low in the ISR.
2	reserved, obsolete
3	keychange interrupt: ACK this bit to low in the ISR.

5.2.3 interrupt mask reg @ 0x08

Interrupt enable flag register, writing the corresponding flag to one will enable this interrupt. *Note that you have to enable the device interrupt number 5 on the GRIP Interrupt controller to use these interrupts.*

bit n	description
0	capture data finished: This interrupt is fired once when the signal capturing is done and the data is ready for reading the signal capture buffer.
1	capture data triggered: Comes one time for the beginnig. It's the roll mode interrupt.
2	reserved, obsolete
3	keychange interrupt.

5.2.4 analog settings reg @ 0x0C

bits n	description
0	data bit
1	serial clock bit
2	chip select, strobe and enable bit
3	reserved
4	enable key clock and automatic key value capturing
7-5	reserved, obsolete
10-8	chip select mux address

5.2.5 sampling frequence reg @ 0x10

This register does set the sampling frequence of the input capture part. The downsampling is done by sampling stages with switchable filters. The possible decimation factors can be set directly to the corresponding bits.

There are 4 types of stages:

Adder Tree Decimator Stage (A)	This stage is for sampling down from 1 GS/s to 100 MS/s.
possible decimation settings	M = {1, 2, 4, 8, 10}
interleaved mode	M = {1, 2, 10}
non interleved mode	M = {4, 8}
Fast Polyphase Decimator Stage (F)	This stage is for sampling down from 125 or 100 MS/s to 12.5 or 10 MS/s.
possible decimation settings	M = {1, 2, 4, 10}
Normal Polyphase Decimator Stage (N)	This stages do provide each an additional decimation filter.
possible decimation settings	M = {1, 2, 4, 10}
unfilterd decimator stage (U)	Decimation filters do not make a real benefit any more, so they do not exist here.
possible decimation settings	M = {1, 2, 4, 10}

This unit is configured by writing the decimation factor in the corresponding bit field.

bits n	type	description
3:0	A stage(0)	1 GS/s -> 100MS/s. It must be set to 8 or 10 when stage(1) is not set to 1.
7:4	F stage(1)	125 MS/s -> 10 MS/s. It must be set to 10 when stages(2–n) are not set to 1.
11:8	N stage(2)	12.5 MS/s -> 1 MS/s.
15:12	N stage(3)	1.25 MS/s -> 100 kS/s.
19:16	U stage(4)	125 kS/s -> 10 kS/s.

5.2.6 sampling filter reg @ 0x14

bits n	type	description
0	reserved, obsolete	
1	enable = 1	disable = 0
	stage(1) decimation 1	no filtering
	stage(1) decimation 2	lowpass FIR filter with 16 coefficients Kaiser beta 4 window 1/4 output sampling frequency stopband (15.12 or 12.5 MHz)
	stage(1) decimation 4	lowpass FIR filter with 32 coefficients Kaiser beta 4 window 1/4 output sampling frequency stopband (7.56 or 6.25 MHz)
	stage(1) decimation 10	lowpass FIR filter with 40 coefficients Kaiser beta 4 window 1/4 output sampling frequency stopband (3.24 or 2.5 MHz)
2	enable = 1	disable = 0
	stage(2) decimation 1	no filtering
	stage(2) decimation 2	lowpass FIR filter with 16 coefficients Kaiser beta 4 window 1/4 output sampling frequency stopband (1.512 or 1.25 MHz)
	stage(2) decimation 4	lowpass FIR filter with 32 coefficients Kaiser beta 4 window 1/4 output sampling frequency stopband (756 or 625 kHz)
	stage(2) decimation 10	lowpass FIR filter with 40 coefficients Kaiser beta 4 window 1/4 output sampling frequency stopband (324 or 25 kHz)
3	enable = 1	disable = 0
	stage(3) decimation 1	no filtering
	stage(3) decimation 2	lowpass FIR filter with 16 coefficients Kaiser beta 4 window 1/4 output sampling frequency stopband (151.2 or 125 kHz)
	stage(3) decimation 4	lowpass FIR filter with 32 coefficients Kaiser beta 4 window 1/4 output sampling frequency stopband (75.6 or 62.5 kHz)
	stage(3) decimation 10	lowpass FIR filter with 40 coefficients Kaiser beta 4 window 1/4 output sampling frequency stopband (32.4 or 2.5 kHz)
29:4	reserved	
31:30	stage(0) "00"	no bartlett window filter
	stage(0) "01"	Bartlett window with 3 coefficients
	stage(0) "10"	Bartlett window with 7 coefficients
	stage(0) "11"	Bartlett window with 15 coefficients

5.2.7 external trigger source reg @ 0x18

Writing 0 to this register will select the auto trigger! Writing 1 to this register will select first external trigger input! Writing 2 to this register will select second external trigger input! Writing 3 to this register will select third ... .
Note that the external triggers have to exist and they are untestet at the moment.

5.2.8 signal source regs byte(0) @ 0x20, byte(1) @ 0x24, byte(2) @ 0x28, byte(3) @ 0x2C

The output of the decimation stage does provide 2 channels with each 8 values at once of 16 bits. The signal source selection is built to handle 4 channels with each 16 bits at the input and 4 individual output channels with each 8 bit going into the trigger with the builtin signal capture buffer. These registers control indirect the the trigger source and the 32 bit wide circular signal capture buffer content at start address 0xA0000000. The storage mode is described in the storage mode register. Following table does show some useful examples how these registers could be set.

storage mode	channels	channel bitwidth	byte(0) 31...24	byte(1) 23...16	byte(2) 15..8	byte(3) 7..0
00	1	32	$CH0_{MSB}$ #0	CH0 #0	CH0 #0	$CH0_{LSB}$ #0
00	2	8	CH0 #0	CH1 #0	—	—
00	2	16	$CH0_{MSB}$ #0	$CH0_{LSB}$ #0	$CH1_{MSB}$ #0	$CH1_{LSB}$ #0
00	4	8	CH0 #0	CH1 #0	CH2 #0	CH3 #0
01	2	8	CH0 #0	CH1 #0	CH0 #0x2000	CH1 #0x2000
01	1	16	$CH0_{MSB}$ #0	$CH0_{LSB}$ #0	$CH0_{MSB}$ #0x2000	$CH0_{LSB}$ #0x2000
11	1	8	CH0 #0	CH0 #0x2000	CH0 #0x4000	CH0 #0x6000

5.2.9 trigger source reg @ 0x30

The trigger can only handle 8 bits and one channel at the moment. Here you select one of the 4 input sources defined by the signal source registers for triggering.

5.2.10 trigger once reg @ 0x34

Start triggered capture for one time writing 1 to this register. Stop triggering or capture writing 0 to this register. Use the auto trigger to start capturing without triggering on something.

5.2.11 trigger prefetch reg @ 0x38

This trigger does provide the possibility to prefetch data before the trigger event. The maximum prefetch bytes are limited by the capture buffer size. Note that the specific trigger does need some samples to generate the trigger event and the trigger does always handle 8 Samples per channel at once. It is a good practise to compensate this delay with some extra prefetch samples fitting to the selected trigger type. The lower 3 bits are discarded.

5.2.12 trigger storage mode reg @ 0x3C

The capture buffer storage mode is designed to be able to use the whole buffer size when the input size is smaller then 32 bit. In roll mode the signal capture buffer does act as a cache so it is recommand to use mode "00". It is the only mode where this capture device does store the input value in one turn. For more information see the signal source registers description.

bits n	setting	description
1:0	"00"	one turn 32 bit write mode or roll mode
	"01"	two turns 16 bit write mode
	"10"	illegal mode
	"11"	four turns 8 bit write mode

5.2.13 trigger read offset reg @ 0x40

When a trigger event has fired and the main trigger capture state machine is going to the record state, this offset does show the start pointer offset to the base address of the signal capture buffer. The capturing does stop when the write address of the trigger state machine gets to this point once, twice

or four times depending on the trigger storage mode (register).
In roll mode it is nessesary to overwrite this register with to the last address which was read on the processor side, to prevent the trigger to stop to early.
Note that the trigger read offset does show the offset with one sample precision, but the trigger engine does write 8 entries of the signal capture buffer at once.
More information about the roll mode is written in the strorage mode register and the trigger current address register.

5.2.14 trigger type reg @ 0x44

This trigger capturing device is built to handle various trigger types and it could be extended later.

bits n	setting	description
2:0	0	external trigger rising edge, auto trigger see external trigger source register
	1	external trigger falling edge, auto trigger see external trigger source register
	2	normal trigger rising edge
	3	normal trigger falling edge
	4	glitch trigger rising edge
	5	glitch trigger falling edge
	6	digital trigger arrive (untestet)
	7	digital trigger leave (untestet)

5.2.15 trigger low level reg @ 0x48

The trigger low level detection can be configured straightforward with this signed 8 bit register. A rising edge is detected when the signal was below the low level register and it is going higher than the high level of the Trigger high level register. A falling edge is detected when the signal was higher than the high level register and it is going under the the low level register.

5.2.16 trigger low glitch reg @ 0x4C

This is the low level glitch detection time register. The glitch time is defined with minimum from 1 to 7 samples added with (8 samples * register entry). Note that the normal trigger does not trigger on glitches, this is only done by the glitch trigger.

5.2.17 trigger high level reg @ 0x50

The trigger low level detection can be configured straightforward with this signed 8 bit register. For more information look at the trigger low level register.

5.2.18 trigger high glitch reg @ 0x54

This is the high level glitch detection time register. For more information look at the trigger low glitch register.

5.2.19 trigger status reg @ 0x58

Interrupts of this flags are handled in the interrupt registers of this device.

bits n	settings	description
0	busy flag = 1	The trigger capture device is waiting for a trigger event or is in record mode.
	busy flag = 0	The device is inactive.
1	record flag = 1	The capture device has got its trigger event and does record at the moment.
0	record flag = 0	The capture device is inactive or waiting for the trigger event.

5.2.20 trigger current addr reg @ 0x5C

This register is needed only for the roll mode and it is read only. It does show the write address of the capture device at the moment. In roll mode you have to make sure to not overtake this address with the read address. For more information look at the trigger offset address register.

5.2.21 target specific reg @ 0x60

W2000L devices: This is the generic or debug UART select register. This is nessesary for the Welec W2000A series oscilloscopes with slog2's ALTERA JTAG port of the USB to serial chip from CYPRESS. The debug UART and the generic uart do share one hardwired serial connection over the standard RS232 plug. The debug UART is nessesary to upload the firmware and for debugging purposes. But sometimes for text debugging or data storage is is necessary to have a generic UART on board.
Set this register to 0 to get the generic UART, for this gdb debugging or a firmware update is disabled. Set this register to 1 to get the debug UART. As a second alternative when the software has been crashed press the 2 buttons next to the power switch on the oscilloscope to switch back to the debug UART. *Note that the hardware state machine of the debug UART is not at all failsafe against wrong data inputs. If you brought this engine down you have to upload the FPGA image again to be able to use the debug UART again for firmware upload and so on!*

5.2.22 LED reg @ 0x64

The LED register does contain the whole set of LEDs for the W2000L oscilloscope. Correspondig bit = 1 means LED is on.
It also does contain some read only rotary knobs described in the key reg(0).

bits n	description
0	Channel 0 button led
1	Channel 1 button led
2	Channel 2 button led
3	Channel 3 button led
4	Math button led
5	Quickmeasure button led
6	Cursors button led
7	Cursors weel led
8	Pulsewidth button led
9	Edge button led
10	Run button red led
11	Run button green led
12	Single button red led
13	Single button green led
15:14	reserved
19:16	Timebase rotary knob
23:20	Trigger vertical position offset rotary knob
27:24	Trigger level rotary knob
31:28	Cursors rotary knob

5.2.23 key reg(0) @ 0x68

Rotary knob counter register. All rotary knobs do have builtin 3 bit wide rotation counters for both directions. This should reduce the interrupt or polling timing troubles. The counters are all read only and do not provide a specific initial value! More information about interrupts for this part are written in the interrupt registers descriptions.

bits n	description
3:0	Channel 0 dc offset
7:4	Channel 1 dc offset
11:8	Channel 2 dc offset
15:12	Channel 3 dc offset
19:16	Channel 0 range
23:20	Channel 1 range
27:24	Channel 2 range
31:28	Channel 3 range

5.2.24 key reg(1) @ 0x6C

This key reg(1) is read only and it does contain all buttons. If the corresponding bit to a button is 1 then this button is pressed. More information about interrupts for this part are written in the interrupt registers descriptions.

bits n	description
0	Display button 0
1	Display button 1
2	Display button 2
3	Display button 3
4	Display button 4
5	Display button 5
6	Math button
7	Channel 0 button
8	Channel 1 button
9	Channel 2 button
10	Channel 3 button
11	Main/delayed button
12	Run/Stop button
13	Single button
14	Cursors button
15	Quickmeasure button
16	Acquire button
17	Display button
18	Edge button
19	Mode Coupling button
20	Autoscale button
21	Save/Recall button
22	Quickprint button
23	Utility button
24	Pulsewidth button
25	internal X1 button
26	internal X2 button