Implementing standard-compliant Power over Ethernet devices

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DESIGNING 802.3AF COMPLIANT DEVICES REQUIRES UNDERSTANDING THE IEEE STANDARD, INTEROPERABILITY ISSUES, AND COMPONENT BEHAVIOR.

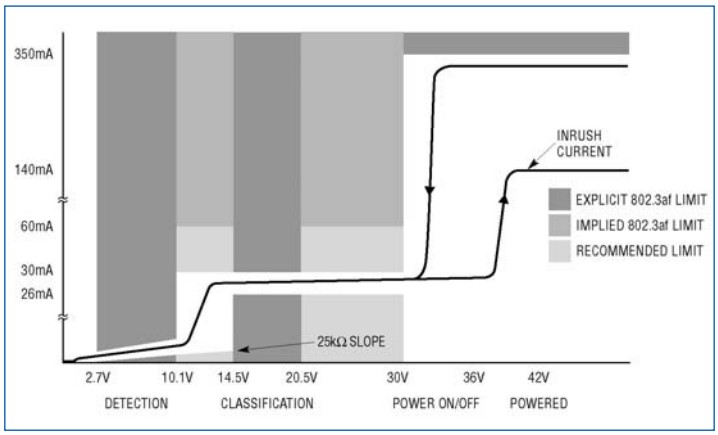

Figure 1. I–V Curve of the example PD shown in figure 3. Shaded areas show IEEE limits for detection, classification and turn-on and the author's recommended limits.

The IEEE 802.3af standard for Power over Ethernet (PoE) describes how to distribute up to 12.95W over Ethernet's CAT-5 cable so network devices can operate without an AC power cord. The goal of 802.3af is to enable a new class of Ethernet device, the Powered Devices (PDs), which does not need a connection to AC line power in order to operate. Most of the IEEE 802.3af standard for PDs is a description of the PD's I-V curve as shown in figure 1.

The curve is broken up into three voltage ranges of interest: detection from 2.7V to 10.1V, classification from 14.5V to 20.5V, power on/off and powered from 30V to 57V. The behavior of the PD within these ranges is mandated by the IEEE standard but the transitions between ranges are equally important for interoperability. The PSE probes the detection region to distinguish the PD with a 25kΩ resistance from non-powered devices with 150Ω common mode termination. In the classification range the PD's current corresponds to the amount of power it needs to operate. When its input or port voltage exceeds 30V, the PD begins drawing power from the cable to operate the rest of its circuitry. In most PDs the 48V input from the Ethernet port is DC/DC converted to voltages like 3.3V or 2.5V which are appropriate for the PD's circuitry. The schematics of figures 2 and 3 show a circuit that handles the PD's entire PoE interface including DC/DC conversion. With this grouping, the PoE interface becomes a self-contained power supply allowing PD designers to concentrate on the circuitry and software that makes their PD different from others.

Both the PD's PoE interface and Ethernet data interface or PHY must connect to the RJ-45 Ethernet jack. Figure 2 shows the ideal way to make these connections. The 75Ω common mode termination resistors are AC coupled so they do not interfere with PoE. The termination is connected on the cable side of the common mode choke so the choke's inductance and hence high AC impedance does not affect the impedance of the termination. Thicker wires in figures 2 and 3 show where PoE's up to 400mA of DC current flows. Wiring and circuit board traces in these paths need special attention to keep their resistance down. On the circuit board, use wide traces and place components close together to reduce trace length. In the magnetics (T1–T6), controlling wire resistance is particularly important to ensure DC current does not saturate T5 or T6 and block data transfer. Autotransformers T1 and T2 must be wound so the center tap sees the same resistance to both wires of the pair. Even when T1 and T2 are wound perfectly, cable resistance may still cause some DC differential voltage. The magnetic can encourage the resulting DC current to flow through T1 or T2 by making them lower resistance than chokes T3, T4 and the data transformers T5, T6. This is illustrated in figure 2 with wider lines representing low resistance wires. Connecting the PD to the spare pairs is much simpler because these wires do not transfer data, as shown in figure 2; there is no need for magnetics. (For Gigabit Ethernet, which does put data on the spare pairs, connect them with the same magnetics as the data pairs in figure 2.)

Once the power and data are extracted from the cable by the magnetics, the PD looks the same whether viewed from the spare or the data pairs. In fact the requirements on the PD's I-V curve are the same for both voltage polarities and both pairs. The pair of diode bridges, D1–D8 in figure 3, combine signals from both pairs into a unipolar output, allowing one 802.3af-compliant PD interface (controlled by the LTC4267 in figure 3) to service both inputs pairs and both polarities.

Beyond the diode bridges, figure 2 has a transient voltage suppressor (TVS) to protect the PD's input because ringing, overshoot transients, static electricity, ground differences, and so on can put hundreds or thousands of volts on the cable. Because the cable has up to 0.05µF with low series inductance and resistance, the energy behind these voltages can be quite large. Transient voltage suppressors can absorb much of this energy but the rest of the

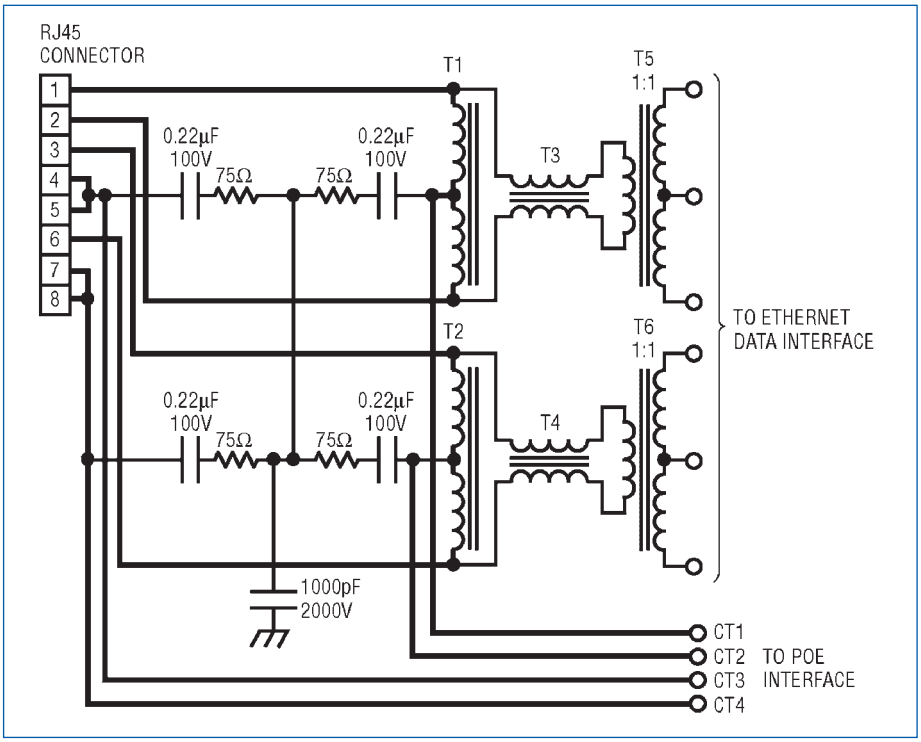

Figure 2. Example Ethernet magnetics for receiving PoE power and 10/100 data from the Ethernet cable. Connections CT1–CT4 connect to the inputs of Figure 3.

PoE interface must be designed to survive an additional 20V to 30V above the operating range until the TVS limits the voltage.

Detection is the first and most important step in establishing a PoE connection. A PD has 25kΩ of common mode resistance while most non-powered devices have 150Ω common mode termination. Between 2.7V and 10.1V, the PD must have a detection signature resistance of 25±1.25kΩ. Besides the resistor itself, which is included with the LTC4267 in figure 3, the nature which the standard requires to be less than 1.9V (sufficient for silicon diodes at -40°C). Non-linear series resistance of the diodes affects the signature as shown in figure 4. Reverse biased bridge diodes add leakage so 2 diodes in parallel must leak less than the IEEE's 10µA limit with 10.1V of reverse bias. The LTC4267 solves many of these problems by integrating and optimizing the signature resistance, shown in figure 4, to compensate for the diode bridges and its own supply current, removing this burden from the designer.

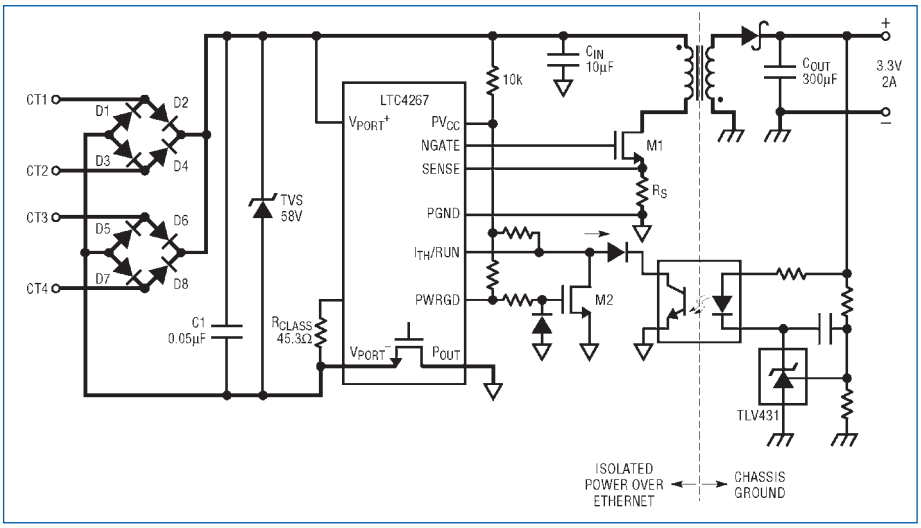

Figure 3. Schematic of an example 802.3af compliant PoE interface and DC/DC converter

diode bridges are the most important element of the PD's 25kΩ detection signature. The forward voltage of the diodes adds offset to the sig-

Following a successful detection, most PSEs will classify the PD to determine how much power it will consume. Classification improves a PSE's power management allowing it to power more PDs from the same wattage power supply. For example, 9 PDs that consume 5W but advertise themselves as class 0 maximize the capabilities of a 150W supply since the PSE must allocate 15.4W to each class 0 PD. If the same PDs used class 2, the PSE allocates 7W to them and its 150W can supply 21 PDs. Use the table to select the appropriate class for your PD by choosing the lowest class number (1, 2, or 3) whose maximum continuous power and peak current is less than that of the PD.

Classification is accomplished by the PSE forcing the port voltage into the classification range and then measuring the PD's current. Throughout the classification region, the PD's current must be within one of the 3 ranges listed in the table. Although the 802.af standard puts more than 5V between detection and classification, most of this range is consumed by the variation of diode forward voltage (V_F) with temperature. At high temperatures the diode's V_F will be about 0.5V while at low temperatures the diodes V_F is about a 0.9V so the LTC4267 must switch from detection to classification within just over 3V. Over this range the LTC4267 does its best to maximize interoperability by slowly turning on the classification current; note the slope of the typical I-V curve in figure 1. A change from 0mA to up to 30mA may cause the port voltage to fall below the classification range so the PD turns off its classification current thus oscillations can occur. Even with a stable voltage from the PSE, rapid changes in the PD's current combined with inductance of 100m of cable can cause ringing. Negative resistance from turning off classification current above 20.5V can cause more severe oscillations and interoperability problems. For maximum interoperability, PDs should attempt to have smooth monotonic I-V curves like that shown in figure 1.

When the PD turns on and begins drawing its power from the cable, the PD design becomes more complicated because the PoE interface, DC/DC converters and the rest of the PD's circuitry must work together to maintain 802.3af compliance. The LTC4267 includes the two most important members of this cooperative, the PoE interface and the DC/DC converter and thus is a good example with which to illustrate these principles. The LTC4267 waits until its input reaches 36V before it begins drawing power and limits inrush current to 140mA (see figure 1). By waiting until 36V, the LTC4267 puts 6V of hysteresis between its turn-on (36V) and turn-off (30V) voltages. This hysteresis prevents the LTC4267 from oscillating on and off if the port voltage drops (2.8V=20Ω*140mA) due to the LTC4267's increased current of 140mA through up to 20Ω of cable resistance. Once the LTC4267-

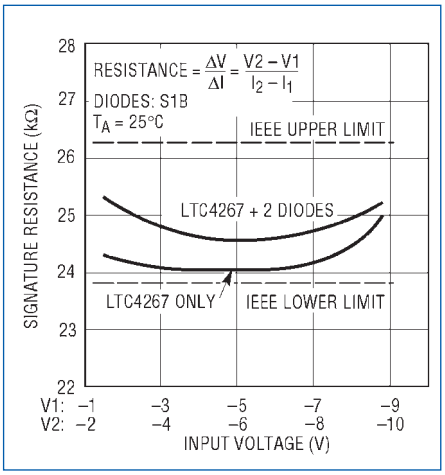

Figure 4. Detection I–V curves showing the effect of diode resistance on the PD's detection signature

equipped PD is powered up, the LTC4267 switches to a 375mA current limit, allowing the PD to get the full 12.95W of class 3 power from the cable. PDs with a higher inrush current limit will need a larger hysteresis, 802.3af allows up to 12V, to prevent oscillations.

PDs are not required to implement a current limit of their own provided they can power up within 50ms with the 400mA to 450mA current limit of the PSE. PDs that do not limit current themselves or power up in 50ms will have their power turned off. PD controller ICs like the LTC4267 use current limit and another feature, called "power good" to ensure the PD powers up properly. The controller's power good output keeps the rest of the PD's circuitry turned off until CIN charges to the port voltage. This is shown in figure 3 where the LTC4267's PWRGD pin prevents its DC/DC converter from operating until there's less than 1.5V between VPORTN and POUT. Using power good is very important with DC/DC converters as a converter providing constant output power will draw more current as its input voltage drops. If the converter turns on at a low voltage its high current draw can slow or even prevent CIN charging. Consequently, power good or some other method of delaying DC/DC converter turn on is critical to the PD's successful power-up sequence.

Once the 50ms start-up time has expired, the PD's CIN should be charged to VPORT (less the 2*VF of the diode bridge) and the PD's power consumption must be less than the maximum allotted to its class (see table). The PD must also signal its continued presence with a maintain power signature (MPS). If the MPS is absent, the PSE will turn off the power, preventing a powered cable being plugged into Ethernet equipment that is not designed to accept power. The MPS is a DC current of 10mA or more and an impedance of less than 26.35kΩ in parallel with more than 0.05µF. Very few PDs will need special circuitry to provide the MPS. In most cases CIN, the impedance of the DC/DC converter and current used for the PDs normal operation will meet the 802.3af MPS requirements. Very low power PDs like thermostats where power dissipation can cause problems in the application are allowed to pulse their MPS current above 10mA for 75ms with up to 250ms between pulses, reducing power to about 100mW.

802.3af Class	Classification Current	Maximum PD Power	Peak PD Current	Class Description
1	9 – 12 mA	3.84 W	120 mA	Low Power PD
2	17 – 20 mA	6.49 W	210 mA	Medium Power PD
3	26 – 30 mA	12.95 W	400 mA	High or Full Power PD

IEEE 802.3af PD classes

Like the MPS, in most cases staying within the class limits is handled by the PD's DC/DC converter and the circuitry drawing power from it. The designer must ensure the PD's circuitry always uses less than the class power in figure 3. The load circuitry cannot consume 12.95W because power is lost to the PoE interface (mostly in the diode bridges) and to the DC/DC converter. Using low leakage Schottky diodes can reduce the 0.5W=2*0.7V*350mA losses in the diode bridges. In figure 3, the LTC4267's PoE interface uses less than 180mW, and 200mW is lost across the 1.6Ω RON MOSFET between VPORTN and POUT, leaving 12.07W=12.95W–0.50W–0.18W–0.20W. How much of this 12W is available to the PD's circuitry depends on the DC/DC converter's efficiency. The operation of DC/DC converters and circuit techniques for improving their efficiency is beyond the scope of this article. The reader is directed to text books and applications notes of converter manufacturers.

The most important aspect of the DC/DC converter in figure 3 is isolation between the input and output. Most PDs will need isolated DC/DC converters because the 802.3af standard requires that the pins in the Ethernet jack be isolated from any other conductive elements on the outside of the PD. An isolated DC/DC converter meets this isolation challenge and the rest of the PD's circuitry can be designed without additional isolation.

The circuit in figure 3 provides an example of a PD's PoE interface and isolated DC/DC converter to meet the requirements of 802.3af. Figure 3 is not the only way to meet these requirements. Implementations for simpler PDs can avoid integrated circuits and use discrete components while other implementations may add complexity to figure 3 and deliver more power to the PD's circuitry. Regardless of the circuitry a designer chooses to meet the 802.3af requirements, the challenges of PD design discussed here should be considered carefully. How the circuitry in figure 3 meets these challenges provides one example PD designers can look to when solving these problems themselves. ■