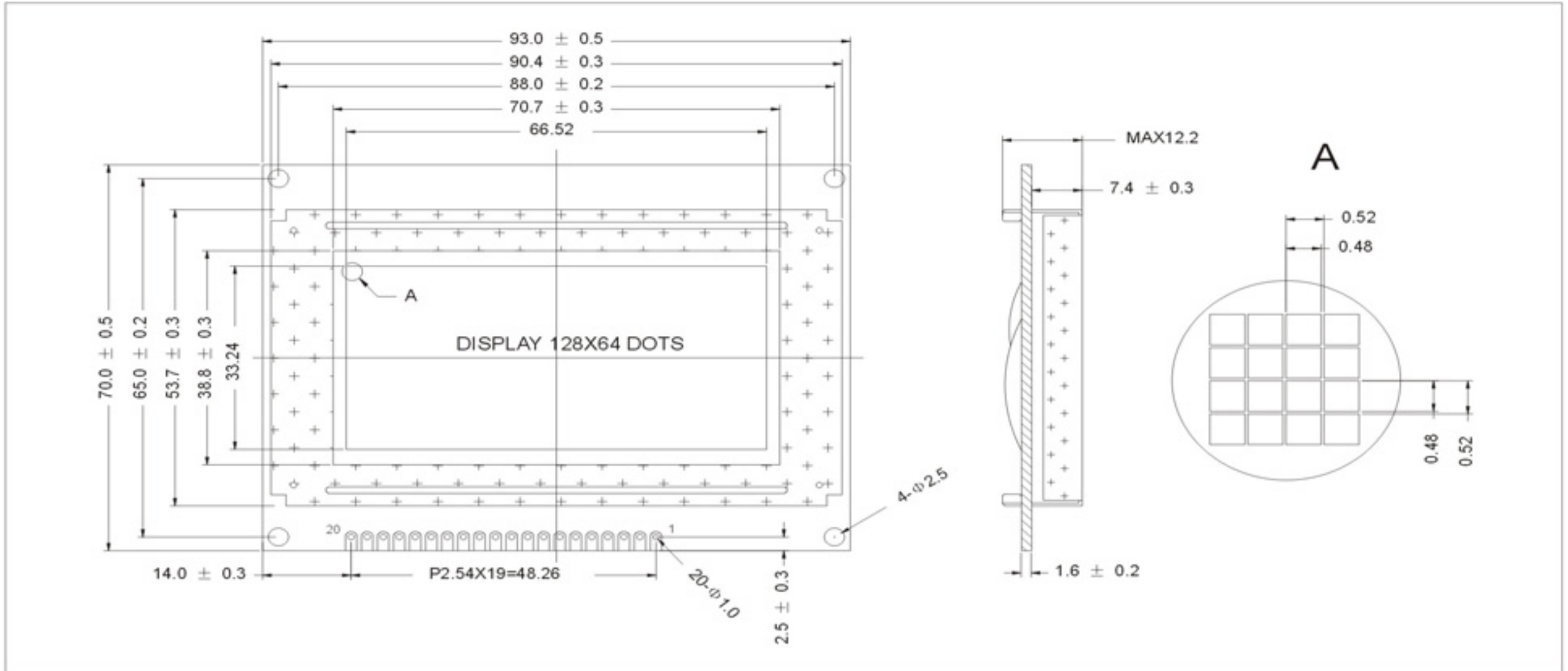


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128 x 64DOTS
1/64DUTY, 1/9BIAS

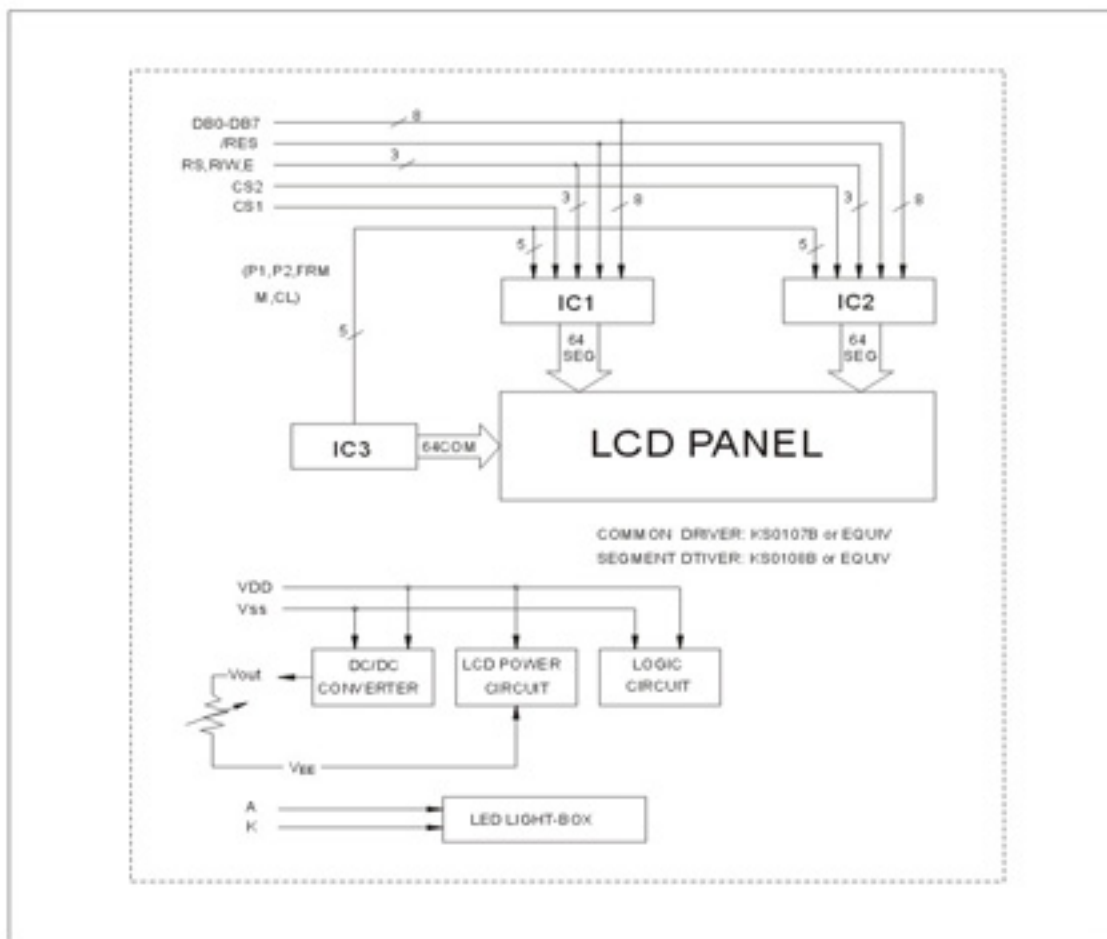
1 EXTERNAL DIMENSION AND DISPLAY PATTERN



2 MECHANICAL DATA

ITEM	SPECIFICATION	UNIT
Module Size(WXHXH)	93.0 x 70.0 x 12.2	mm
Viewing Area(WXH)	70.7 x 38.8	mm
Number of Dots(WXH)	128 x 64	dots
Dot Pitch(WXH)	0.52 x 0.52	mm
Dot Size(WXH)	0.48 x 0.48	mm

3 BLOCK DIAGRAM



4 PIN CONFIGURATION

PIN	SYMBOL	LEVEL	SIGNAL DESCRIPTION
1	V _{SS}	0V	Ground
2	V _{DD}	+5V	Supply Voltage for Logic And LCD
3	V _{EE}	-	Operating Voltage for LCD (Variable)
4	RS	H/L	H:Data,L:Instruction Code
5	R/W	H/L	H:Read(Module-MPU),L:Write(MPU-Module)
6	E	H,H-L	Chip Enable Signal
7	DB0	H/L	Data Bit 0
8	DB1	H/L	Data Bit 1
9	DB2	H/L	Data Bit 2
10	DB3	H/L	Data Bit 3
11	DB4	H/L	Data Bit 4
12	DB5	H/L	Data Bit 5
13	DB6	H/L	Data Bit 6
14	DB7	H/L	Data Bit 7
15	CS1	H/L	Chip Select Signal for IC 1
16	CS2	H/L	Chip Select Signal for IC 2
17	/RES	H,H-L	Reset Signal
18	V _{out}	-	Power Supply Voltage for LCD
19	A		Anode of LED Unit
20	K		Cathode of LED Unit

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PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage Logic	V _{DD} (V _{DD} -V _{SS})	-0.3	7.0	V
Supply Voltage Driver	V _{DD} -V _{EE}	-0.3	18.0	V
Input Voltage	V _{IN}	-0.3	V _{DD} +0.3	V

Operating Temp.	See page 9
Storage Temp.	

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128 x 64DOTS
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ITEM	SYMBOL	CONDITION	SPEC. VALUE			UNIT
			MIN.	TYP.	MAX.	
Supply Voltage (Logic)	$V_{DD}-V_{SS}$		4.5	5.0	5.5	V
Supply Current (Logic)	I_{DD}	$V_{DD}=5V$	-	3.0	4.5	mA
Input Voltage	"HIGH"	V_{IH}	$0.7 V_{DD}$	-	V_{DD}	V
	"LOW"	V_{IL}	0	-	$0.3 V_{DD}$	V
Output Voltage	"HIGH"	V_{OH}	$I_{OH}=-0.205mA$	2.4	-	V
	"LOW"	V_{OL}	$I_{OL}=1.6mA$	-	0.4	V
LCD Operating Voltage	$V_{DD}-V_{EE}$	$V_{DD}=5V$	-	13.5	-	V
Supply Current LCD Drive	I_{EE}		-	3.0	4.5	mA

Note(1): () Value is high Reliability type.
Note(2): Electro-Optical Characteristics: See page 6.

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LED

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{LE}	-	3.90	4.15	4.30	V
Power Consumption	P_{LE}	$IF=180mA$	-	738	-	mW
Luminous	I_v	$IF=180mA$	51	69	-	cd/m ²

8 INTERFACE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
E Cycle Time	t_{CYC}	1000	-	ns
E High Level Width	t_{WEH}	450	-	ns
E Low Level Width	t_{WEL}	450	-	ns
E Rise Time	t_R	-	25	ns
E Fall Time	t_F	-	25	ns
Address Setup Time	t_{AS}	140	-	ns
Address Hold Time	t_{AH}	10	-	ns
Data Setup Time	t_{DSW}	200	-	ns
Data Delay Time	t_{DDR}	-	320	ns
Data Delay Time(Write)	t_{DHW}	10	-	ns
Data Hold Time(Read)	t_{DHR}	20	-	ns

