U 6050 B · U 6051 B
U 6052 B

LOCAL MULTIPLEX SYSTEM

Technology: Bipolar

Application:

Transmitter (U 6050 B) and receiver (U 6051 B, U 6052 B) for permanent scanning of 8 switch-positions, serial data transmission via a single data line and driving up to 8 relays.

Features:

- Only a single line is necessary
- Quadruple comparison of the data signal for high transmission safety
- All outputs switched off if data line is disturbed
- Short circuit detection of the integrated relay driver
- Transmitter and receiver prepared for master/slave operation (16 switches, 16 relays)
- Reduced power dissipation by pulsed driver outputs
- Transmitter data output short circuit protected
- Transmitter can be powered via data line
- Wide supply voltage range
- U 6050 B: 8 relay drivers,
  U 6051 B: 4 relay drivers and 4 logic outputs
- Meet the demands of VDE regulation 0839
- Load dump protected

Cases:

18 pin dual inline plastic (U 6050 B, U 6051 B, U 6052 B)
20 pin SO plastic (U 6050 B-FP)
24 pin SO plastic (U 6051 B-FP, U 6052 B-FP)

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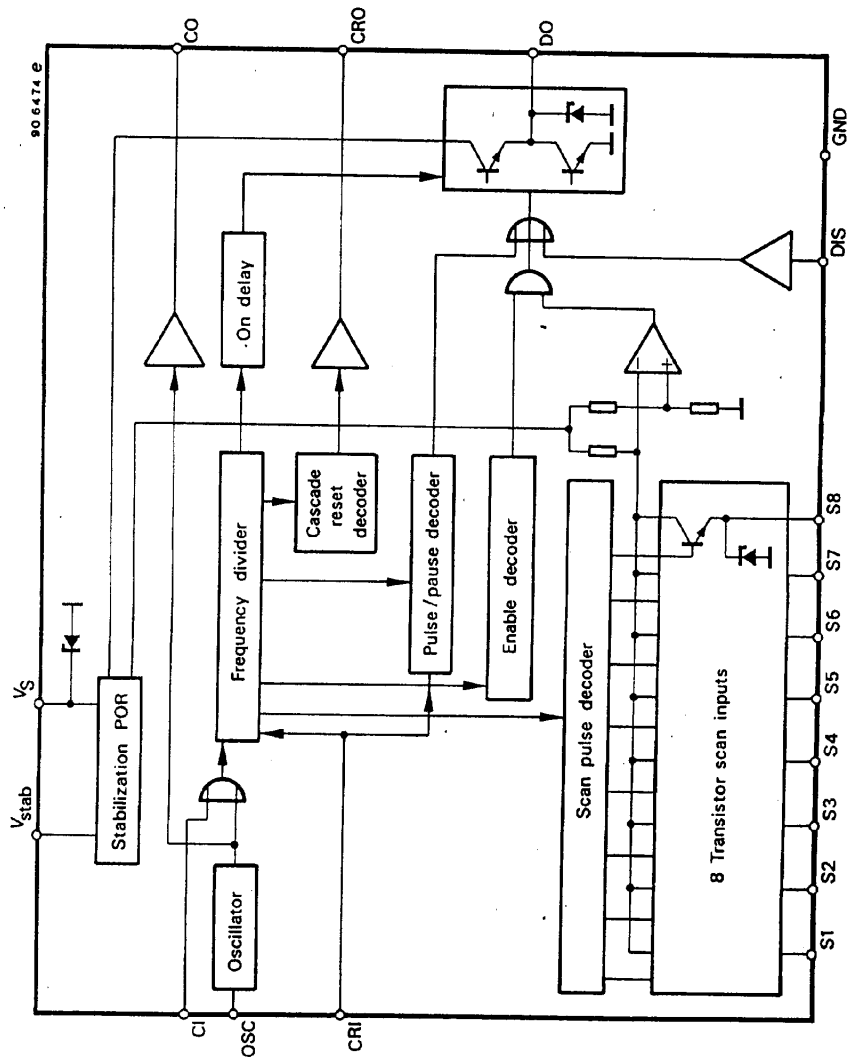
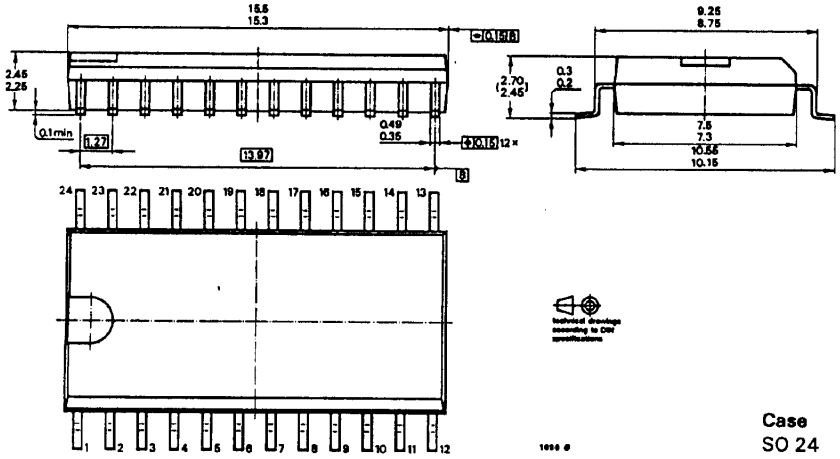


Fig. 1 Block diagram U 6050 B

Dimensions in mm



Case
SO 24

		Min.	Typ.	Max.	
Load dump detection LD					
Recommended voltage divider 270/20 kΩ					
Load dump threshold	V_{LD}		2.1/1.4		V
Load dump threshold	V_{Batt}		30/21		V
Internal clamping	V_Z		7		V
Input current ($V_{LD} = 0$ V)	$-I_{LD}$			1	µA
Program pin Pulsed Output PO					
Recommended voltage divider 150/39 kΩ					
Threshold pulsed output off	V_{PO}		2.0/2.27		V
Threshold pulsed output off	V_{Batt}		10/11		V
Internal clamping	V_Z		7		V
Input current ($V_{PO} = 0$ V)	$-I_{PO}$			1	µA
Input current ($V_{PO} = V_S$)	I_{PO}			1	µA
$V_{PP} = 0$ V : static output $V_{PP} = V_S$: pulsed output					
IC power consumption					
($V_{Batt} = 16$ V, $V_{sat} = 0.5$ V, eight 80 Ω relays activated, $R_{DC} = 200$ Ω)					
U 6052 B static	P_{tot}		1130		mW
U 6052 B pulsed	P_{tot}		500		mW
U 6051 B static	P_{tot}		750		mW
U 6051 B pulsed	P_{tot}		475		mW

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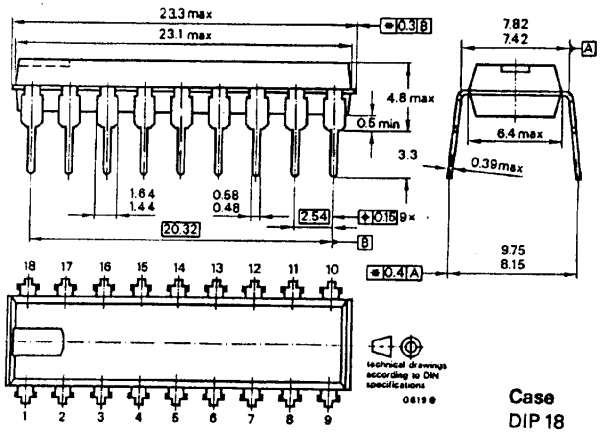
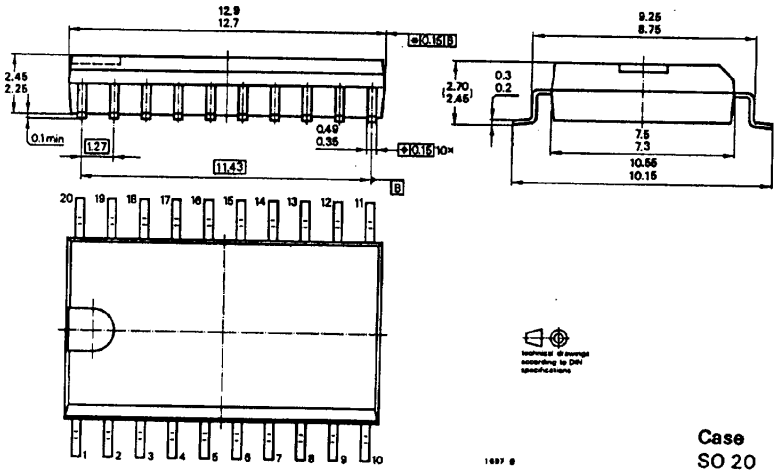
Dimensions in mm



Case
DIP 18



Case
SO 20

U 6051 B, U 6052 B Receiver (with recommended circuitry)

Absolute maximum ratings

Supply voltage (static) no operation 60 s	V_S	25	V
Ambient temperature range	T_{amb}	−40...+ 85	°C
Storage temperature range	T_{stg}	−55...+125	°C
Junction temperature	T_j	125	°C
Power dissipation (T_{amb} = 85 °C)	P_{tot}	860	mW

Maximum thermal resistance

Junction ambient	R_{thJA}	75	K/W

Electrical characteristics

		Min.	Typ.	Max.	
V_{Batt} = 13.5 V, T_{amb} = 25 °C, reference GND Receiver operated with recommended circuitry					
Supply voltage	V_{Batt}	6		16	V
5 V supply (without R_V, C_V)	V_S, V_{Stab}	4.3		6	V
Stabilized voltage	V_{Stab}		5.2		V
Protection resistor	R_V	510			Ω
Filter capacitor	C_V		100		µF
POR threshold	V_S	3.0		4.2	V
Current consumption (all outputs off)	I_S		2.0		mA
Internal clamping	V_Z		14.3		V
Relay output 01...08 (U 6052 B); R01...R04 (U6051B)					
Saturation voltage (I_O = 150 mA)	V_O			0.5	V
Relay coil resistance	R_O	80			Ω
Collector current (normal operation)	I_O			200	mA
Collector pulse current (load dump)	I_{OP}			1.5	A
Threshold short circuit detection (output activated)	V_{OS}		2		V

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		Min.	Typ.	Max.	
Logic outputs D01...D04 (U 6051B)					
Saturation voltage (I_O = 20 mA)	V_O			1.0	V
Collector current	I_O			30	mA
Internal clamping	V_Z		22		V
Threshold short circuit detection	V_{OS}		2		V
Oscillator input OSC					
Internal discharge resistor	R_{DIS}	1.6	2.0	2.4	kΩ
Lower threshold	V_{OSC}		1.1		V
Upper threshold	V_{OSC}		3.3		V
Input current (V_{OSC} = 0 V)	$-I_{OSC}$			1	µA
Frequency	f_{OSC}	1.0	25.6	50.0	kHz
Data input DI					
Threshold	V_{DI}		0.5 · V_S		V
Internal pull down resistor	R_{DI}		100		kΩ
Internal clamping	V_Z		14		V
Input current (V_{DI} = 0 V)	$-I_{DI}$			1	µA
External protection resistor	R	100			Ω
Programm pin PP					
Lower threshold	V_{PP}		0.13 · V_S		V
Upper threshold	V_{PP}		0.50 · V_S		V
Pin PP open	V_{PP}		0.27 · V_S		V
Input current (V_{PP} = 0 V)	$-I_{PP}$		30		µA
(V_{PP} = V_S)	I_{PP}		50		µA

Pin PP:	operation mode
open	single
GND	slave
V_S	master

Clock output CO (activated only in master mode)					
Output current "high" (V_{CO} = 0 V)	$-I_{IO}$			150	µA
Saturation voltage "low"	V_{IO}			1	V
Separate driver control DC					
External protection resistor	R_{DC}	200			Ω
Control current	I_{DC}			40	mA
Load dump reduction voltage	V_{DC}			2	V

U 6050 B Transmitter (with recommended circuitry)

Absolute maximum ratings

Supply voltage (static) no operation 60 s		V_S	25	V
Ambient temperature range		T_{amb}	−40...+85	°C
Storage temperature range		T_{stg}	−55...+125	°C
Junction temperature		T_j	150	°C
Power dissipation T_{amb} = 85 °C		P_{tot}	810	mW
Maximum thermal resistance				
Junction ambient	DIP 18	R_{thJA}	80	K/W
	SO 20	R_{thJA}	100	K/W

Electrical characteristics

V_{Batt} = 13.5 V, T_{amb} = 25 °C, reference: GND
Transmitter operated with recommended circuitry (Fig. 8)

		Min.	Typ.	Max.	
Supply voltage	V_{Batt}	6		16	V
5 V supply (without R_V, C_V)	V_S, V_{Stab}	4.3		6	V
Stabilized voltage	V_{Stab}		5.2		V
Protection resistor	R_V	510			Ω
Filter capacitor	C_V		100		µF
POR threshold	V_S	3.0		4.2	V
Current consumption	I_S		1.5		mA
Internal clamping	V_Z		14.3		V
Switch input S1...S8					
Scan current ($V_{S1...S8}$ = 0 V)	$-I_{S1...S8}$		2		mA
Leakage resistance	$R_{S1...S8}$	1.8		3	kΩ
Internal reference	V_{Ref}		2.5		V
Recommended protection resistor	$R_{S1...S8}$		100		Ω
Internal clamping	$V_{Z1...Z8}$		14.3		V
Oscillator input OSC					
Internal discharge resistor	R_{Dis}	1.6	2.0	2.4	kΩ
Lower threshold	V_{osc}		1.1		V
Upper threshold	V_{osc}		3.3		V
Input current (V_{osc} = 0 V)	$-I_{osc}$			1	µA
Oscillator frequency	f_{osc}	1.0	6.4	20.0	kHz

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		Min.	Typ.	Max.	
Clock input CI					
Internal serial resistor	R_{CI1}		2		kΩ
Internal pull down resistor	R_{CI2}		20		kΩ
Threshold	V_{CI}		0.6		V
Clock output CO					
Output current "high" (V_{CO} = 0 V)	$-I_{CO}$			150	µA
Saturation voltage "low"	V_{CO}			1	V
Cascade reset input CRI					
Internal serial resistor	R_{CRI1}		2		kΩ
Internal pull down resistor	R_{CRI2}		20		kΩ
Threshold V_{CRI} = 0 V: normal operation V_{CRI} = V_S : reset	V_{CRI}		0.6		V
Cascade reset output CRO					
Output current "high" (V_{CRO} = 0 V)	$-I_{CRO}$			150	µA
Saturation voltage "low"	V_{CRO}			1	V
Data output DO					
Saturation voltage "low" (20 mA)	V_{DO}			1.5	V
Saturation voltage "high" (20 mA)	V_{DO}/V_S			2.4	V
Current limitation (V_{DO} = 0 V)	$-I_{DO}$		30		mA
(V_{DO} = V_{Batt})	I_{DO}		30		mA
Internal clamping	V_Z		14.3		V
External protection resistor	R_{DO}	100			Ω
Data input – slave DIS					
Internal pull-up resistor	R_{DIS}		100		kΩ
Detection threshold	V_{DIS}		0.66·V_S		V

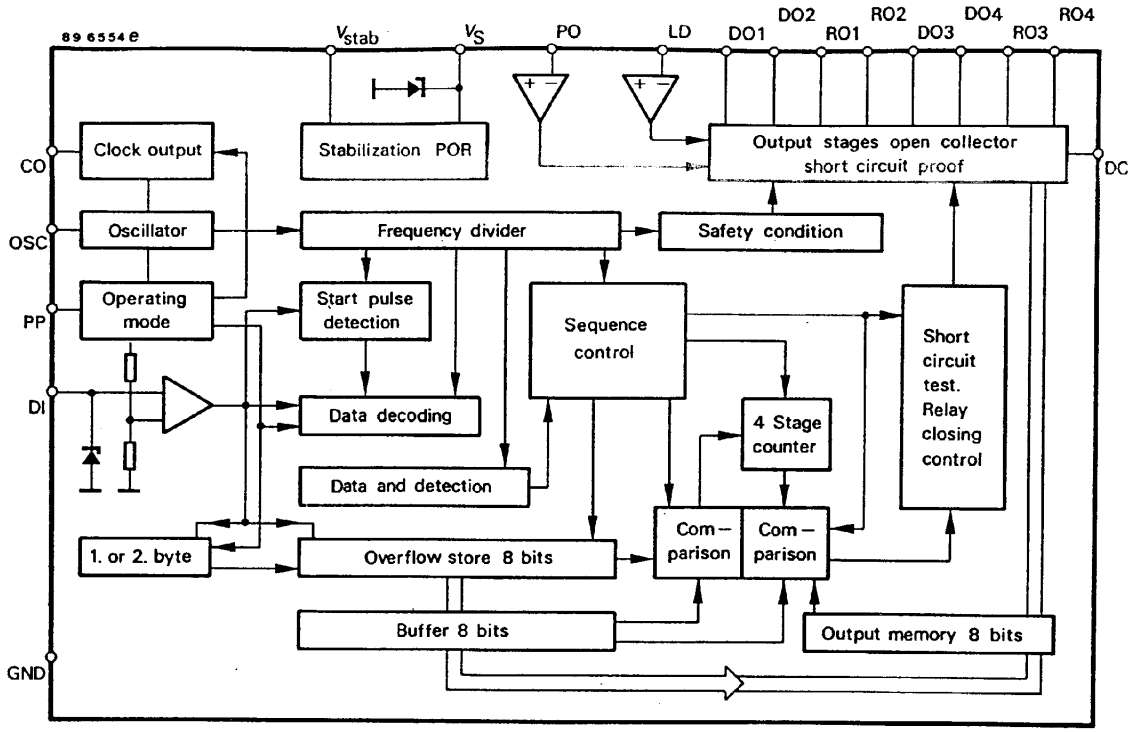

Fig. 2 Block diagram U 6051 B

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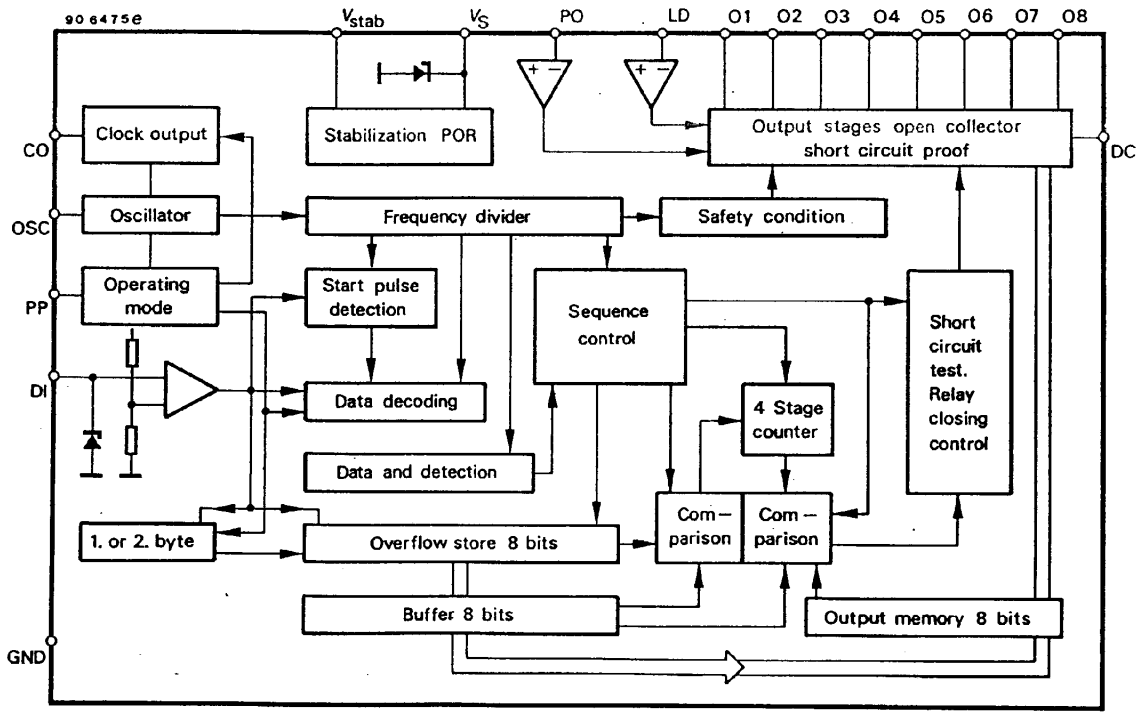


Fig. 3 Block diagram U 6052 B

1. Functional description of transmitter and receiver

1.1 Power supply

For reasons of protection against interference and surges must all circuits be equipped with an RC circuit for current limitation in the event overvoltages and for buffering in the event of voltage dips at V_S.
Suggested dimensions: $R_V = 510\ \Omega$, $C_V = 100\ \mu F$.
An integrated 14 V Z-diode is located between V_S and GND in each case.

1.2 Oscillator

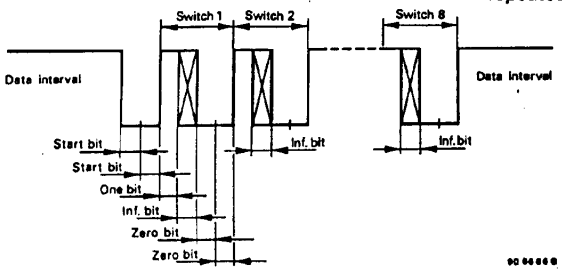
All timing in the circuits is derived from an RC-oscillator in each case; the oscillator's charging time t_1 is determined by an external resistor R_{osc} and its discharge time t_2 by an integrated 2 kΩ resistor. Since the tolerance and temperature sensitivity of the integrated resistor are considerably greater than those of the external resistor, $t_1/t_2 \geqq 20$ must be selected for stability reasons. The minimum value of R_{osc} should not be less than 68 kΩ.

Recommended frequencies and dimensioning:

$f_{transmitter}$ = 6.4 kHz; C_{osc} = 1 nF; R_{osc} = 200 kΩ
$f_{receiver}$ = 25.6 kHz; C_{osc} = 220 pF; R_{osc} = 200 kΩ

Times derived from the transmitter frequency (6.4 kHz):

Start pulse	: 312 µs
One bit	: 156 µs
Information bit	: 156 µs
Zero bit	: 156 µs
Information unit	: 625 µs
Data word	: 5 ms + 312 µs start bit
Data pause	: 9.688 ms
Transmission cycle	: 15 ms
Minimum reaction time	: 60 ms
Data word master-slave	: 10 ms + 312 µs start bit
Data pause master-slave	: 4.688 ms
Scanning pulse	: 312 µs
ON delay	: 75 ms



2. Transmitter supply via the data line

The supply line is not required if the transmitter is supplied via the data line. Refer to Fig. 16 for the wiring. It must be noted that there is greater susceptibility to faults with this wiring arrangement, but this can be eliminated by a suitable external circuit, e.g. a capacitor to ground after the reverse voltage protection diode.
Both transmitter and receiver possess an integrated 14 V Z-diode at the data output DO and data input DI for limitation of positive voltage peaks.

3. 5 V supply

Both the transmitters and receivers can be supplied from one stabilized, noise-free 5 V voltage source. In this case, the series resistor and the filter capacitor are not required. Pin V_{stab} is also supplied by the 5 V supply.
Refer to Figs. 15, 17, 18 and 20.

4. Functional description of the transmitter U 6050 B

Eight switch or pushbutton inputs are scanned cyclically every 15 ms and the result is permanently transmitted to the receiver as a serial data word via the data line.

4.1 Structure of the data word

A switch information unit consists of 4 parts:
1. One bit for receiver synchronization
2. Information bit with "High" = switch open
   "Low" = switch closed
3. Zero bit
4. Zero bit

The data word consists of 2 start bits and 8 information units. For a transmitter frequency of 6.4 kHz, the data word length is 5 ms plus the start pulse, followed by a 10 ms long data interval. The data interval has high potential. When the supply voltage is applied, data transmission is constantly repeated in accordance with this pattern (Fig. 4).

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4.2 ON delay and POR

After the supply voltage V_{batt} is applied to the transmitter, a POWER-ON-RESET pulse (POR) is generated internally which sets the logic of the U 6050 B to a basic condition. This also applies to the other circuits. The data output is blocked for approx. 75 ms so that the supply capacitor can be charged up when V_{batt} is switched on in the case of transmitter supply via the data line (Fig. 5).

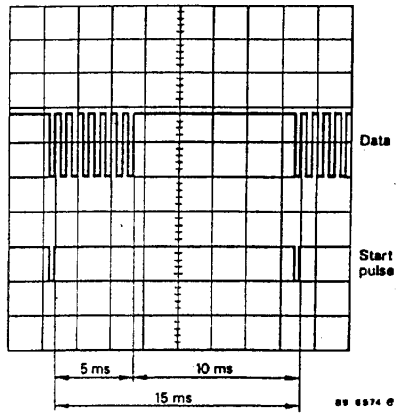

Fig. 4

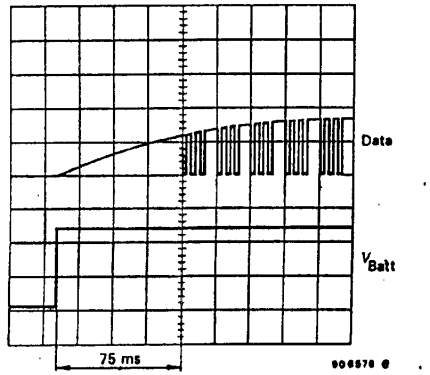

Fig. 5

4.3 Switch input scanning

For reliable detection of the switch condition, a certain minimum current must flow through the switch contact so that soiling and moisture cannot lead to misinterpretations.
A value of 2 mA was planned for the contact current. To reduce the overall current consumption of the transmitter, the switches are supplied cyclically with the contact current, so that the power consumption is rediced from the maximum of 16 mA to 0.33 mA owing to the duty factor of 2.5/15.

The voltage drop across the inputs caused by the current is compared with a reference voltage of 2.5 V: if the potential is less than 2.5 V during the scan pulse, the switch is closed, while the switch is open if the potential is greater than 2.5 V. The leakage resistance of the switching contact can thus be approx. 2.5 kΩ if a protective resistor of 100 Ω is provided. Protective resistors for limitation of interference voltage peaks at the inputs are required mainly where the lines to the switches are long. In a noise-free environment, the protective resistors at the switch inputs can be omitted. The input posses an integrated 14 V Z-diode.

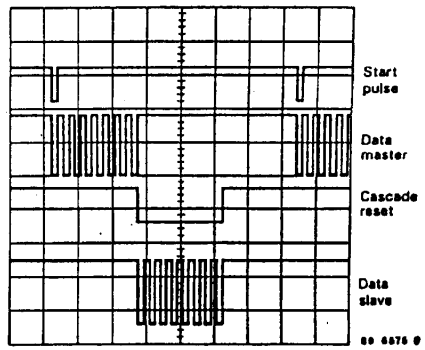

Fig. 6

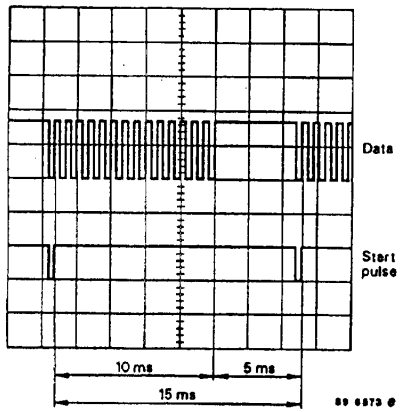

Fig. 7

4.4 Cascading (master-slave operation)

Scanning of up to 16 switches or pushbuttons is possible by connecting together two transmitters. The connection between master and slave is shown in Fig. 19. The data output DO of the slave is connected with the data input DIS of the master; the two data signals are combined with each other there and are available at the data output DO of the master (Fig. 6 and 7).
The master transmits the start bit and the first eight information units; in this time, the frequency divider of the slave is disabled by the master's cascade reset. After the last master information unit, the slave frequency divider is enabled so that the slave scanning cycle and slave data transmission can be performed. In master-slave operation, the data word consists of the start bit and 16 information units (10 ms); the data interval is 5 ms. The clock output CO of the master is connected with the clock input of the slave CI so that the time sequences of both circuits are synchronous. The voltage supply can be realized with a common series resistor and a common filter capacitor.
Operation with 5 V is possible, refer to Fig. 20.

4.5 Data output DO

The data output is a push-pull output which is short-circuit proof both with respect to ground and V_{batt}. The current limiter is set to approx. 30 mA in both cases. A 14 V Z-diode is located between DO and GND to clip interference voltages. For this reason, an external series resistor of 100 Ω is also required to limit the current in the Z-diode (Fig. 8).

5. Functional description: receiver U 6050 B/U 6051 B

Reception of the information arriving from the transmitter, decoding of the data word, i.e. recognition of the switch conditions and activation of the corresponding relay drivers after a data check.

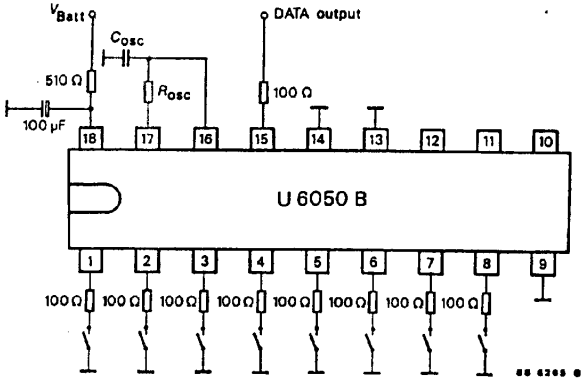

Fig. 8

5.1 Data decoding

If a negative edge appears at the data input, the receiver checks wether a start pulse or a fault is present by measuring the duration of the pulse. (A minimum time must be observed). If there is a fault, the receiver waits for the next negative edge.
If it recognises a start pulse, it checks wether an information unit with 8 bits is following and stores this in an 8-bit overflow store. The arriving data are ignored if there is no 8-bit string owing to a fault or a synchronism. The receiver is synchronized by each one bit; scanning of the information takes place in the middle of the information bit. In order to make scanning sufficiently precise, the oscillator frequency of the receiver was selected to be four times as large as that of the transmitter. The deviation of the receiver frequency to the four-fold transmitter frequency may be up to ± 15% while still guaranteeing reliable data recognition.

5.2 Data check

The data read into the 8-bit overflow store are compared with the contents of the buffer. If they are identical, a 4-stage counter is incremented by one stage: if they are not identical, the counter is reset. The new data combination is transferred to the buffer after each comparison, irrespective of the result.
After coincidence has been established four times, the contents of the buffer are compared with the contents of the output memory. If both are identical, the 4-stage counter is reset. However, since nothing has changed with respect to the switch position, the information from the buffer is not transferred to the output memory. This is important if the relay drivers are in clocked condition. However, if the contents of the two memories differ, the switch position must have changed in the meantime, and the following process occurs:

a. Relays are operated statically.
The information is transferred from the buffer to the output memory and the corresponding relay outputs are activated. An individual short-circuit test takes place for 10 ms after approx. 35 ms. If a short-circuit is detected, the respective output is disabled until a new POR occurs.

b. Relays are clocked.
After transfer to the output memory, the corresponding relay outputs are activated statically for approx. 120 ms; in this time, the short-circuit test described in a) is performed. The relay outputs are then clocked with the oscillator frequency.

Since the period of a data transmission is 15 ms, this results in a minimum delay time or debouncing time of 4 · 15 ms = 60 ms for detection of a change in switch position. Faults on the data line and switch bouncing may lead to an extension of the delay time.

5.3 Safety position of the relay drivers

If no data reach the receiver any longer owing to a break in the data line or a short-circuit to ground or V_S, then all relay drivers are disabled after approx. 50 ms. It is possible to visually indicate the malfunction by permanently wiring a transmitter input to ground and connecting the corresponding relay output in accordance with Fig. 9. This applies only to static operation or when using a digital output of U 6051 B.

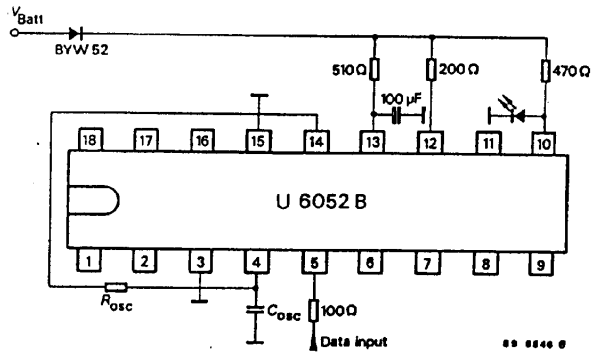

Fig. 9

5.4 Short circuit detection of the outputs

Approx. 35 ms after a new data transfer operation to the output memory, a comparator measures the collector voltage of every active output transistor for 10 ms. If the saturation voltage exceeds the value of 2 V, this is interpreted as a short-circuit. The delay of 35 ms also permits connection of a 1.2 W lamp: the high initial current after switching on has died away by then and cannot lead to erroneous tripping of the short-circuit detection circuit. Measurement is not performed statically so that faults cannot simulate a short-circuit; in practice, this means that each active output is measured four times in the period of 10 ms (Fig. 10). Experience shows that fault pulses in a motor vehicle are shorter than 2 ms. The corresponding transistor is rendered reverse-biased only if the collector voltage is greater than 2 V for longer than 10 ms owing to a short circuit; this condition is then stored and can be cancelled again only by a POR. A short-circuit which occurs at a later time can be detected only when a new switch combination is set and a new short-circuit test takes place. However, an active transistor will be destroyed by a subsequent short-circuit to V_{batt}. If a transistor is reverse-biased owing to a short-circuit, the remaining functions of the receiver are not impaired by this.

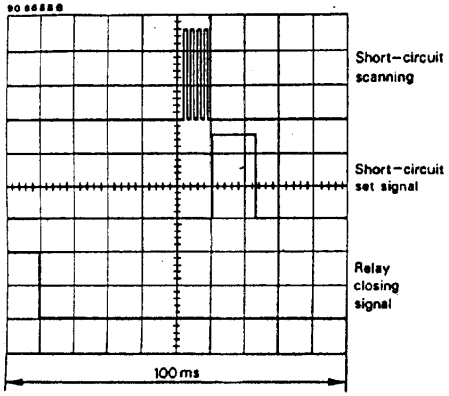

Fig. 10

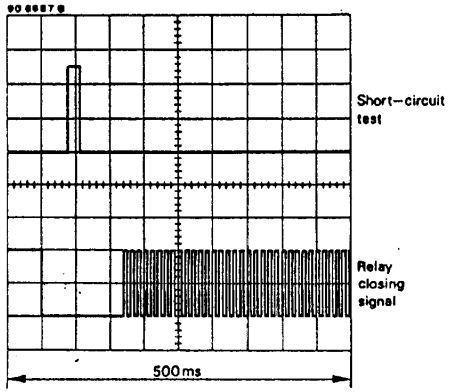

Fig. 11

5.5 Output clocking

Clocking of the relay outputs leads to a reduction in the power dissipation of the circuit and the overall equipment. The operating modes "output clocking", PO = V_S or "static activation", PO = GND, can be selected by the input PO.
After a new information transfer operation to the output memory, the relay outputs to be activated are statically activated for a period of approx. 120 ms. The above-described short-circuit test also takes place in this time and the outputs are then clocked with a frequency of 25.6 kHz, i.e. with the oscillator's fundamental frequency. Refer to Fig. 11.
Clocking of the outputs is switched off in the event of a supply voltage of $V_{Batt} \leq 10$ V: clocking is then switched back on again for $V_{Batt} \geq 11$ V. Detection of these voltage thresholds is also performed by the input PO if this is provided with a voltage divider. The reference voltage for "clocking off" is around 2 V/2.27 V. With an external voltage divider of 150 kΩ/39 kΩ, this corresponds to a response threshold of V_{Batt} = 10 V/11 V, refer to Fig. 12. Clocking of the relays over the whole supply voltage range requires a separate free-wheeling diode for each relay which can also block the required interference voltages, e.g. BAV 21. Since negative interference voltages can reach the collectors of the output transistors with low resistance via these free-wheeling diodes, a high-blocking capability reverse voltage protection diode, e.g. a BYW 52, must be connected in the supply line, because these interference voltages would otherwise lead to destruction of the transistors.

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5.6 Driver control DC

A relatively high current is required for activation of all eight output transistors. This would lead to a large voltage drop across R_v if this current were taken from the internal supply voltage. For this reason, the activation current of the relay drivers is routed via a separate terminal DC.
It was not possible to use Darlington transistors with low base currents because the aim was a maximum saturation voltage of $V_{CEsat} \leq 0.5$ for $I_C = 150$ mA. In the event of a fault, the potential of DC is connected to ground via a Darlington transistor. Recommended series resistance for DC: $R_{DC} = 200\ \Omega$.

5.7 Surge immunity, input LD

The IC supply is protected by an external RC circuit and an integrated 14 V Z-diode.
Since the output transistors cannot withstand long positive voltage peaks and the load dump pulse in reverse-biased condition without damage, they are switched to forward-biased condition in the event of a fault. The output transistors are dimensioned so that they can cope with the current produced through an 80 Ω winding as a result of the load dump pulse.
At the same time, the potential at DC is also connected to ground via a Darlington transistor. The outputs are gated via output transistors reconnected to form Darlington transistors.
If a lamp is connected, the current may become so high in the event of a load dump in conjunction with the initial resistance of the lamp that the output transistor and lamp may be destroyed.
The response threshold is defined with an external voltage divider at the input LD. The reference voltage for overvoltages is around 2 V/1.5 V, this corresponding to a V_{batt} response voltage of approx. 30 V and a hysteresis of approx. 9 V.
In the event of positive overvoltages, every short-circuit scan is also suppressed.

5.8 Cascading (master-slave operation)

Determination of master or slave is performed by wiring the programming input PP at the U 6052 B:

Master : PP to V_S
Alone : PP open
Slave : PP to GND

In "master" mode, the oscillator is connected with R_{osc} and C_{osc} and the clock output CO is active.
If the receiver is operated alone, CO is disabled. In "slave" mode, the oscillator is blocked internally and must be activated by the clock output of the master; the slave's clock output is disabled.
The master recognises the start bit and decodes the first eight information bits. The slave also recognises the start bit, but decodes the second eight information bits.
Except for the synchronous clock control, the functions for master and slave are executed independently. The wiring and configuration in master-slave mode is shown in Figs. 21 and 22.

5.9 Activation of 8 logic outputs with U 6052 B

Instead of being used for activation of relays, the 8 outputs can also be used for activation of a downstream digital circuit. The outputs must then not be clocked: PO = GND.
The outputs must also not be gated by overvoltages, i.e. LD = GND. Refer to Fig. 13.
The outputs are npn open collector transistors and are capable of switching 200 mA and blocking up to 25 V. However, it must be ensured that no overvoltages and no load dump can reach the output transistors in this circuit configuration.

6. Modified receiver U 6051 B

The U 6051 B is a mask version of U 6052 B possessing 4 relay outputs and 4 logic outputs, refer to Figs. 14 and 22.
The relay outputs correspond to those of U 6052 B. The logic outputs are connected by means of an aluminium mask to form an npn Darlington open collector with integrated 22 V Z-diode. Clocking and gating by overvoltages are not possible. The saturation voltage is less than 1 V for $I_C = 20$ mA. Overvoltages may reach the logic outputs only with a series resistance of 1 kΩ.

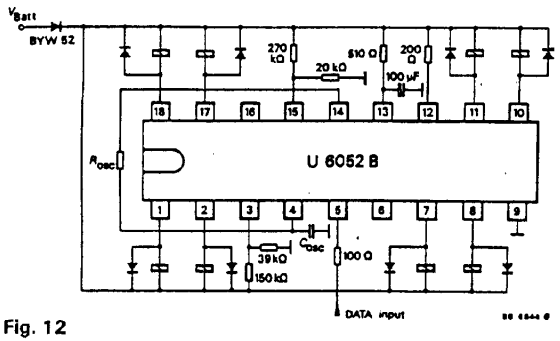

Fig. 12

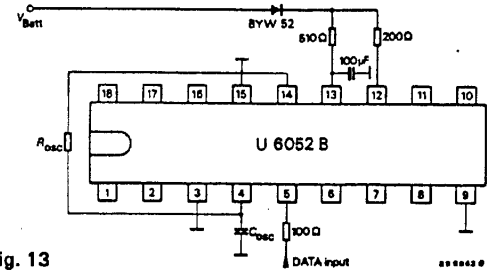

Fig. 13

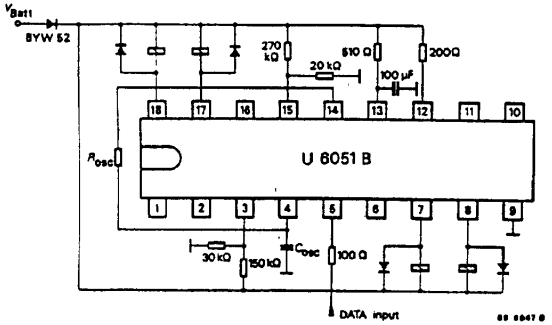

Fig. 14

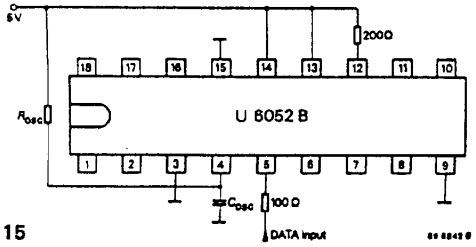

Fig. 15

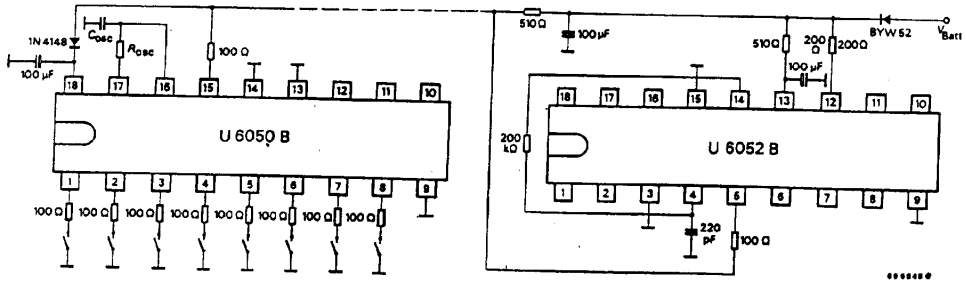

Fig. 16

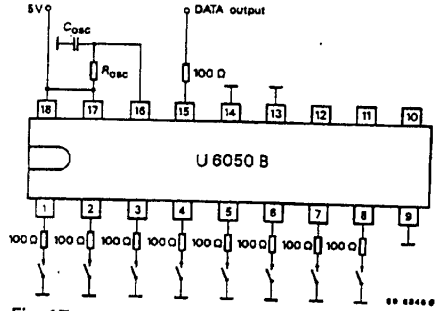

Fig. 17

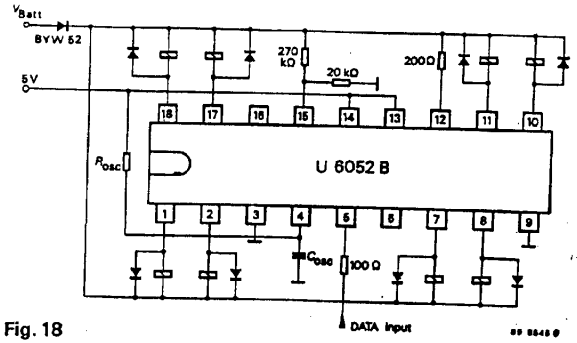

Fig. 18

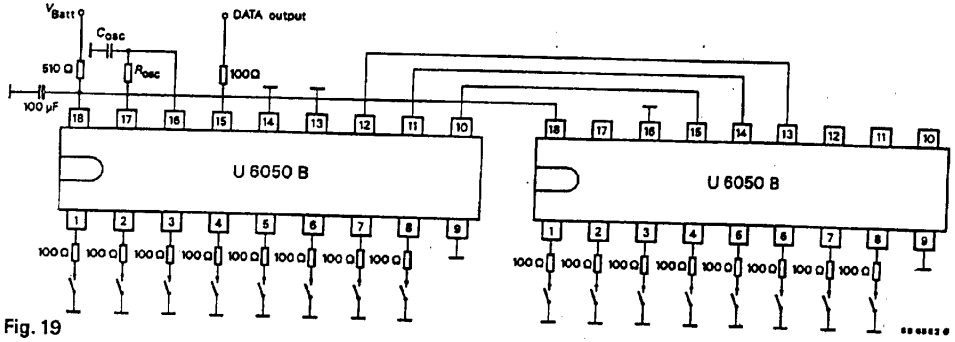

Fig. 19

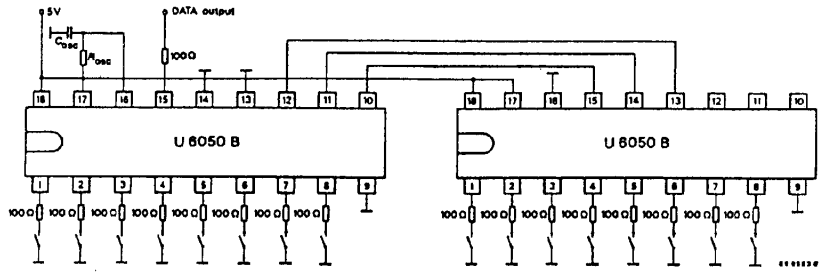

Fig. 20

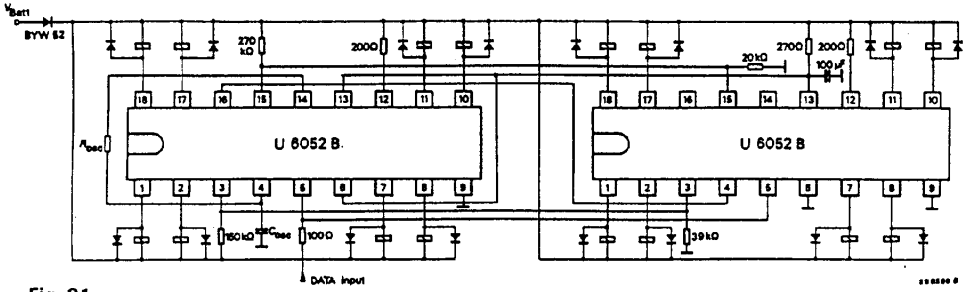

Fig. 21

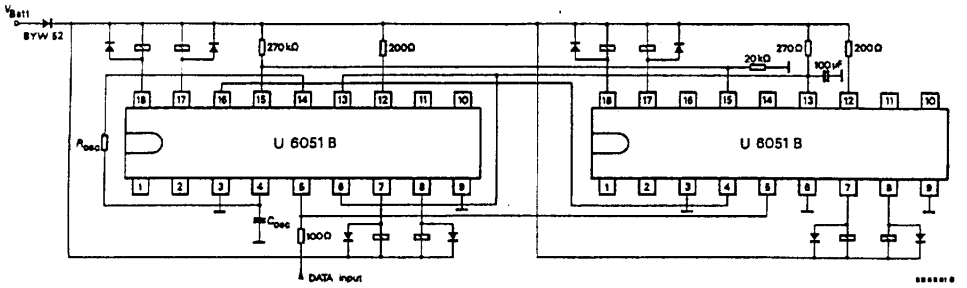

Fig. 22

U 6050 B · U 6051 B
U 6052 B

Pin configuration (U 6050 B)

Pin	Function
1...8 (2...9)	Switch inputs S1...S8
9 (10)	Ground GND
10 (11)	Data input slave DIS
11 (13)	Cascading reset output CRO
12 (14)	Clock output for cascading CO
13 (15)	Clock input for cascading CI
14 (16)	Cascading reset input CRI
15 (17)	Data output DO
16 (18)	RC-oscillator input OSC
17 (19)	Stabilized voltage V_{stab}
18 (20)	Supply voltage V_S
(1, 12)	N. C.

Pin configuration (U 6051 B)

Pin	Function
(1)	Ground GND
1 (2)	Logic output DO1
2 (3)	Logic output DO2
3 (5)	Program pin pulsed output PO
4 (6)	RC-oscillator input OSC
5 (7)	Data input DI
6 (8)	Program pin (tristate) PP
7 (10)	Relay output RO1
8 (11)	Relay output RO2
9 (12)	Ground GND
(13)	Ground GND
10 (14)	Logic output DO3
11 (15)	Logic output DO4
12 (17)	Driver control DC
13 (18)	Supply voltage V_S
14 (19)	Stabilized voltage V_{stab}
15 (20)	Load dump detection LD
16 (21)	Clock output for cascading CO
17 (22)	Relay output RO3
18 (23)	Relay output 04
(24)	Ground GND
(4, 9, 16)	N. C.

Pin configuration (U 6052 B)

Pin	Function
(1)	Ground GND
1 (2)	Relay output 01
2 (3)	Relay output 02
3 (5)	Program pin pulsed output PO
4 (6)	RC-oscillator input OSC
5 (7)	Data input DI
6 (8)	Program pin (tristate) PP
7 (10)	Relay output 03
8 (11)	Relay output 04
9 (12)	Ground GND
(13)	Ground GND
10 (14)	Relay output 05
11 (15)	Relay output 06
12 (17)	Driver control DC
13 (18)	Supply voltage V_S
14 (19)	Stabilized voltage V_{stab}
15 (20)	Load dump detection LD
16 (21)	Clock output for cascading CO
17 (22)	Relay output 07
18 (23)	Relay output 08
(24)	Ground GND
(4, 9, 16)	N. C.

Numbers in brackets apply to SO package