Recommended PCB Design Rules

Recommended PCB Design Rules for QFP Packages

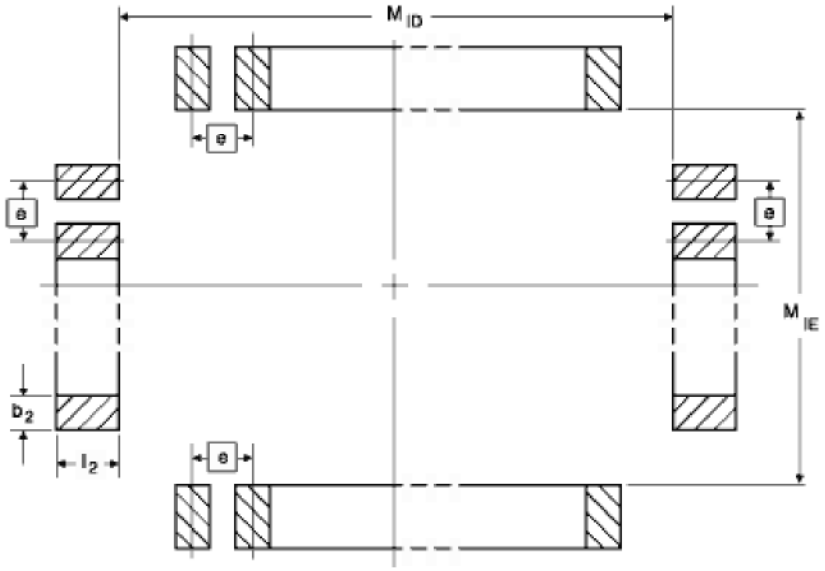

Figure 1-12: **EIA Standard Board Layout of Soldered Pads for QFP Packages**

Table 1-9: **PCB Land Pad Dimensions for Xilinx Quad Flat Packs(1)**

Dim.	VQ44, VQG44	VQ64, VQG64	PQ100, PQG100	HQ160, HQG160, PQ160, PQG160	HQ208, HQG208, PQ208, PQG208	VQ100, VQG100, TQ100, TQG100	TQ144, TQG144	TQ176, TQG176	HQ240, HQG240, PQ240, PQG240	HQ304, HQG304
M_{ID}	9.80	9.80	20.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
M_{IE}	9.80	9.80	14.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
e	0.80	0.50	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50
b_2	0.4-0.6	0.3-0.4	0.3-0.5	0.3-0.5	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4
l_2	1.60	1.60	1.80(2)	1.80	1.60	1.60	1.60	1.60	1.60	1.60

Notes:

1. Dimensions in millimeters.
2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

Recommended PCB Design Rules for TSOP/TSSOP Packages

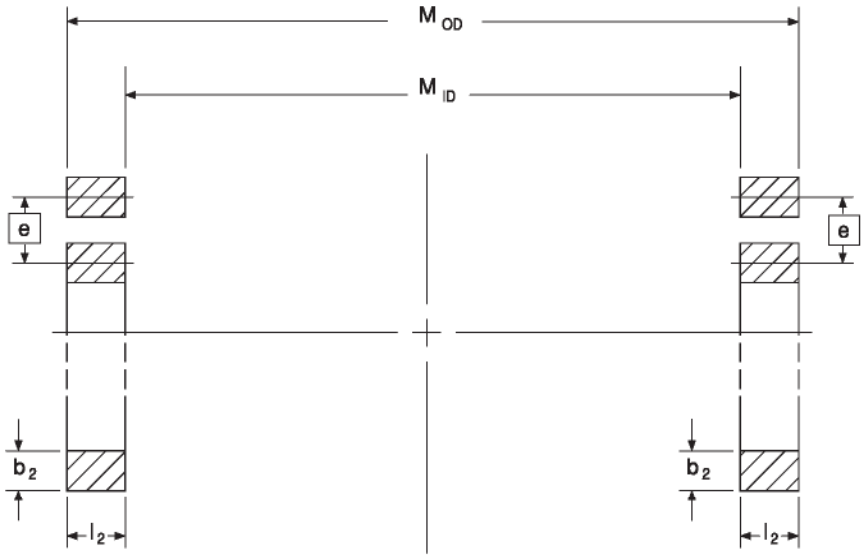

Figure 1-13: **IPC Standard Board Layout of Soldered Pads for TSOP/TSSOP Packages**

Table 1-10: **Dimensions for Xilinx TSOP/TSSOP Packages (mm)**

Dimension	VO20, VOG20	VO48, VOG48
M_{ID}	4.20 - 4.40	17.80 - 18.00
M_{OD}	7.20 - 7.40	20.80 - 21.00
e	0.65	0.50
b_2	0.40 - 0.50	0.30 - 0.40
I_2	1.50	1.50