El Camino
Training - Engineering - Consultancy

DIGILAB 1Kx208 MANUAL

Programmable Logic Prototyping and Demo Board

DECEMBER 2000 ENGLISH - VERSION 1.2

Chapter
1

Digilab – What and Where

With your Digilab you have received the following items:

- DIGILAB 1Kx208 board
- Parallel Port Cable
  used to connect your board to a PCs parallel port and download your configuration file into the Altera ACEX device or program the optional serial Flash EPROM EPC2.
- Altera Digital Library CD containing:
  - Altera MAX+plus II BASELINE programmable logic development system
  - Current Altera data sheets and application notes
  - Acrobat Reader for viewing and printing this and other documents
- Documentation Floppy Disc containing:
  - Readme file on installing the Acrobat Reader and viewing this document
  - This Digilab manual
  - System On a Programmable Chip (SOPC) demo design featuring a pre-parameterized, pre-synthesized16-bit NIOS RISC CPU core.

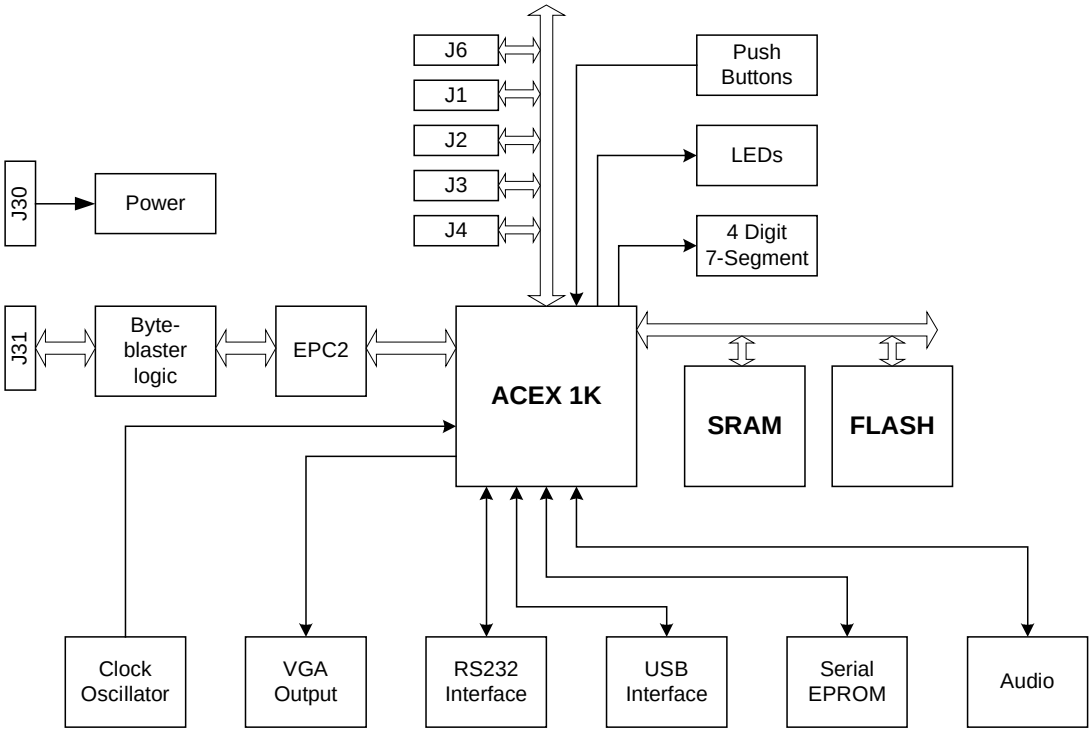
Warning:
This is a class A device. This device may cause radio interference in the living area.
The user may be required to carry out and be responsible for appropriate measures.

Chapter
2

Digilab – Block Diagram

DIGILAB 1Kx208 General Description

- Altera's development system MAX+plus II Baseline on CD ROM included
- 100k Gate ACEX 1K device (EP1K100QC208-1)
- Convenient access to all ACEX 1K pins
- Supports Excalibur™/Nios™ embedded processors
- On-board, fast SRAM 256k x 16
- On-board FLASH 512k x 16
- 6-Layer PCB in Europe-Standard format
- Configuration Flash EPROM EPC2 socket
- Bi-colour status LED for nSTATUS, CONF_DONE
- Debounced reboot-/reset-push buttons
- On-board configuration hardware (no Byteblaster required)
- Insertion slots for various sub-modules
- IDE, VGA interfaces/connector
- Three individual operating voltages
  (VCC-INT, VCC-IO, VCC-AUX) @ 2.5V, 3.3V and 5V
- RS232, USB physical interfaces
- Quarz oscillator
- Full PLL support
- 4-digit 7-segment display
- LEDs and push buttons
- 1k serial EEPROM
- On-board 18-bit stereo AC97 DSPCodec (2 ADCs and 4 DACs)



Chapter

3

Obtaining Your License File

The MAX+plus II BASELINE software is a free, entry-level version of the Altera MAX+plus II programmable logic development system. In order to use MAX+plus II BASELINE you need to request a license and register with Altera. The license is valid for six month and free of charge. You may renew your licenses whenever necessary or use multiple systems or licenses. Refer to the Altera license agreement for further details. In order to request your license file you will need to fill out the form at the following WWW address.

http://www.altera.com/authcode/index.html

If the address should have changed check http://www.altera.com for Tools/Baseline

You will need to provide your hard disk volume serial number.

Your hard disk volume serial number is an 8-digit Hexadecimal number (with an optional hyphen) of the format *nnnn-nnnn*, where *n* is any Hexadecimal character (e.g., 62E4-5A74). You can obtain your hard drive volume serial number by typing `dir /p` at a DOS or command prompt on your PC.

Your license file information will be sent to the e-mail address you specify. If you don't have e-mail or access to the WWW you may also use the fax form below. Follow the instructions you receive with your license file information and save it as "license.dat" on your hard disk.

If you don't have WWW access fill out the form below with block letters and fax it to:

El Camino GmbH, Fax +49-(0)8751-842876

Hard Disk ID: _____

E-mail: _____

_____

First Name: _____

Last Name: _____

Company: _____

Address: _____

City: _____

State/Province: _____ Zip/Postal Code: _____

Country: _____

Phone: _____

Fax: _____

Chapter

4

Installing MAX+plus II BASELINE

System Requirements

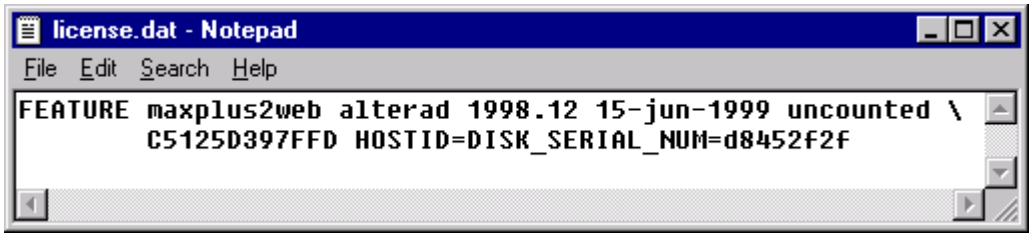
- Pentium class or higher- (recommended) or 486-based PC
- Microsoft Windows NT version 3.51 or 4.0, Microsoft Windows 95 or 98
- Microsoft Windows-compatible graphics card and monitor
- CD-ROM drive
- Microsoft Windows-compatible 2- or 3-button mouse
- Parallel Port
- 100 MByte free hard disk space
- 16 MByte RAM

MAX+plus II BASELINE Installation

To install the MAX+plus II BASELINE software, perform the following steps:

1) Create a directory on your hard disk to store the installed MAX+plus II BASELINE files and your license file. For example, create the directory c:\baseline

2) Create a license.dat file as instructed in your MAX+plus II BASELINE license file e-mail and save it into the installation directory you created. A sample license file is shown below:



Important: If you are using Notepad be sure the file is saved as "license.dat" and not as "license.dat.txt". Registered extensions might not be shown. Use the DIR command in a DOS box to verify the name is correct.

3) Begin installation by executing the **baseline.exe** file from the Altera Digital Library CD **\baseline** directory.

4) The MAX+plus II installation wizard is launched. In the Welcome page click **Next**

5) After reading the license agreement, click **YES.** You need to scroll all the way to the bottom before you can click YES.

6) Click **OK** in the Warning message box.

7) Enter your name and company in the User Information page and click **Next**.

8) Select **Full Installation** in the Setup Type page and click **Next**.

9) Specify a destination directory for the MAX+plus II BASELINE software installation (e.g., **c:\baseline**). This directory should be the same one you created in step 1, and it should contain the license.dat file.

10) Specify a destination folder for the work directory (e.g., **c:\baseline\max2work**). Click **Next**.

11) Select a program folder in which the installation program will add a program icon. Click **Next**.

12) Your installation choices are displayed in the Start Copying Files page. Click **Next** to begin installation.

13) If you are installing on a PC with Windows NT operating system, you will receive a message that the Sentinel driver was installed successfully. This is a driver for an external software guard that only comes with some purchased versions of MAX+plus II. On Windows NT machines the installation of the driver will only work if you have administrator privileges. Click **OK**.

14) To view the read.me file, click **YES** when prompted.

Installing the Byteblaster Driver for Windows NT

On a PC with Windows NT you need to install a driver for the Altera download cable Byteblaster, which is also part of your Digilab board. The Byteblaster is used for downloading the configuration information through the parallel port of your PC to the JTAG port of the ACEX device. You don't need to install a driver on PCs with Windows 95 or 98.

1) Go to **Start/Settings/Control Panel** and double-click on **Multimedia** icon.

2) Click on **Devices** tab and choose the **Add** button

3) Select **Unlisted or Updated Driver** from the List of Drivers list box and choose **OK**. The Install Driver dialog box opens.

4) Type or select **\<MAX+plus II system directory>\drivers** in the text box, and choose **OK**. The Add Unlisted or Updated Driver dialog box opens.

5) Select **Altera ByteBlaster** from the list box and choose **OK**.

6) To install the driver at the current address, choose **OK**. The System Setting Change dialog box is displayed.

7) Choose the **Restart Now** button in the System Settings Change dialog box to reboot your computer.

Setting Up MAX+plus II BASELINE Licensing

1) Start the software by double-clicking the MAX+plus II icon.

2) After reading the license agreement, click **YES.** You might need to scroll all the way to the bottom before you can click YES.

3) Click **OK** in the MAX+plus II Copy Protection message box. You will enter your license file later.

4) Choose **License Setup** (**Options** menu).

5) Specify the license file by clicking Browse. In the Directories box, go to the directory, where your **license.dat** file is located. (e.g. c:\baseline), select the license.dat file in the Files box, and click **OK**.
The following features should be listed in the **Licensed Features** box:
Hierarchy Display, Message Processor, Text Editor, Graphic Editor, Symbol Editor, Floorplan Editor, Compiler, Timing Analyzer, Programmer, Classic Family, MAX 5000 Family, MAX 7000 Family, EDIF I/O, SVF/JAM Output

6) Click **OK** to save your changes.

Setting Up the ByteBlaster in MAX+plus II

1) If not running, start the software. For example, double-click the MAX+plus II icon.

2) Choose **MAX+plus II/Programmer**

3) While no hardware has been selected the Hardware Setup box automatically shows up. Later it can be accessed through **Options/Hardware Setup**.

4) Select **ByteBlaster** in the Hardware Type box.

5) Select the appropriate parallel port. On PCs with Windows NT this box is only accessible after the ByteBlaster driver has been installed.

6) Choose **OK** and close the Programmer window

Congratulations! You have successfully installed and licensed the MAX+plus II BASELINE development system.

Chapter

5

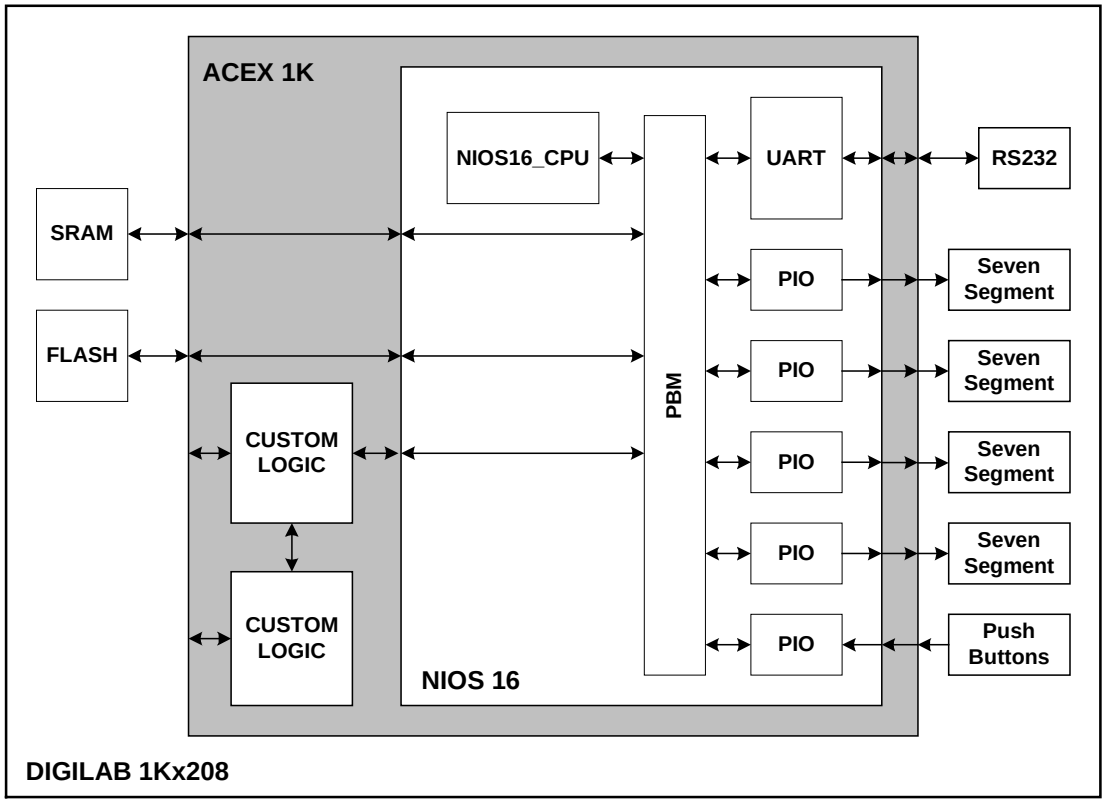
Design Example

System On A Programmable Chip (SOPC) Demo Design

The DIGILAB 1Kx208 comes with a SOPC demo design. It contains a 16-bit NIOS RISC processor core with some basic peripherals, as well as a 16-bit interface, that allows to connect custom on-chip logic to the NIOS CPU core.

Included is also the “nios16_custom_sdk” directory that has all the include and library files you need to develop and compile your own C/C++ or low level assembly language code.

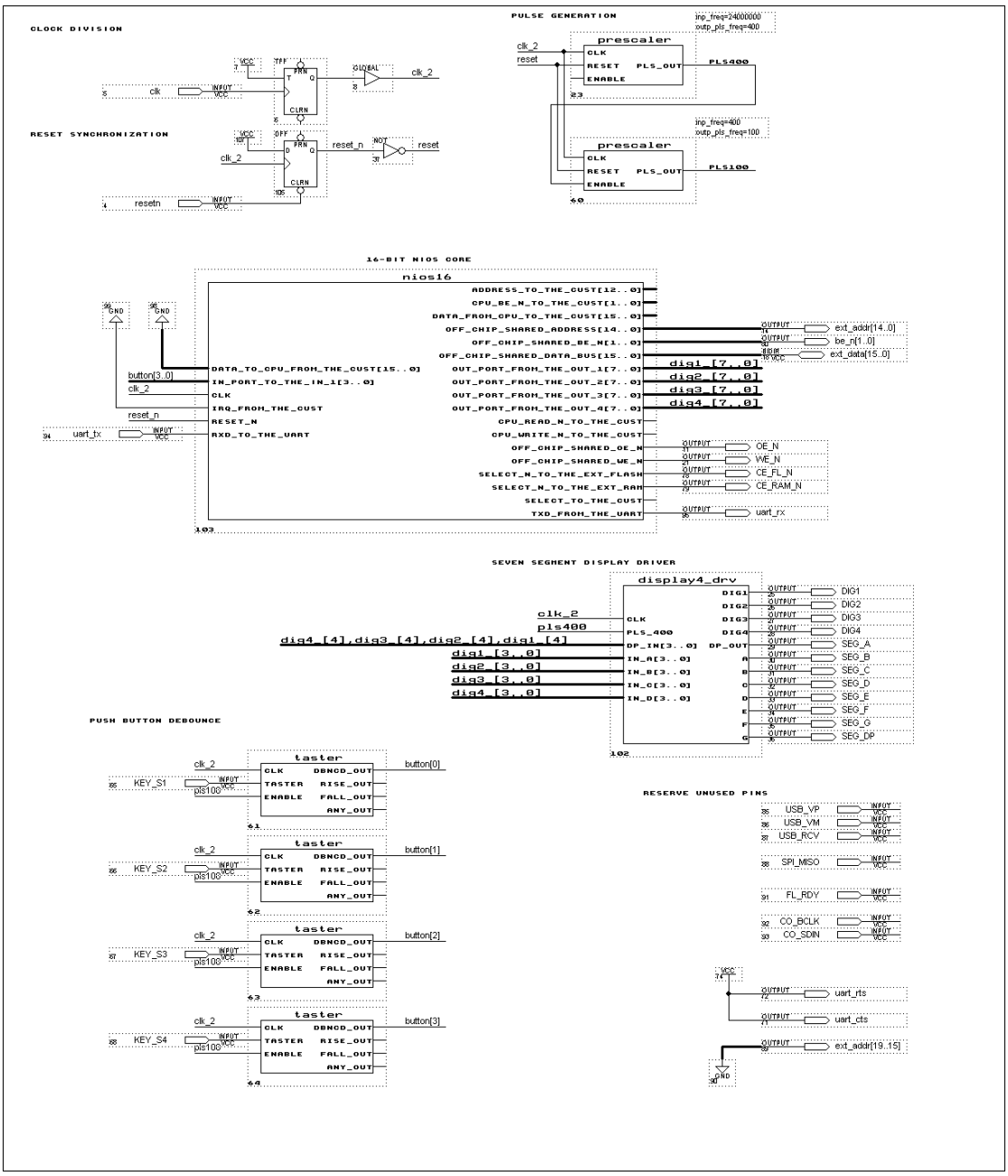
The NIOS software development tools (assembler, C/C++ compiler, linker, builder, debugger…) are part of the Altera SDK (Software Development Kit). In order to develop your own software applications you will either need the EXCALIBUR-NIOS or NIOS-GNUPRO from Altera.



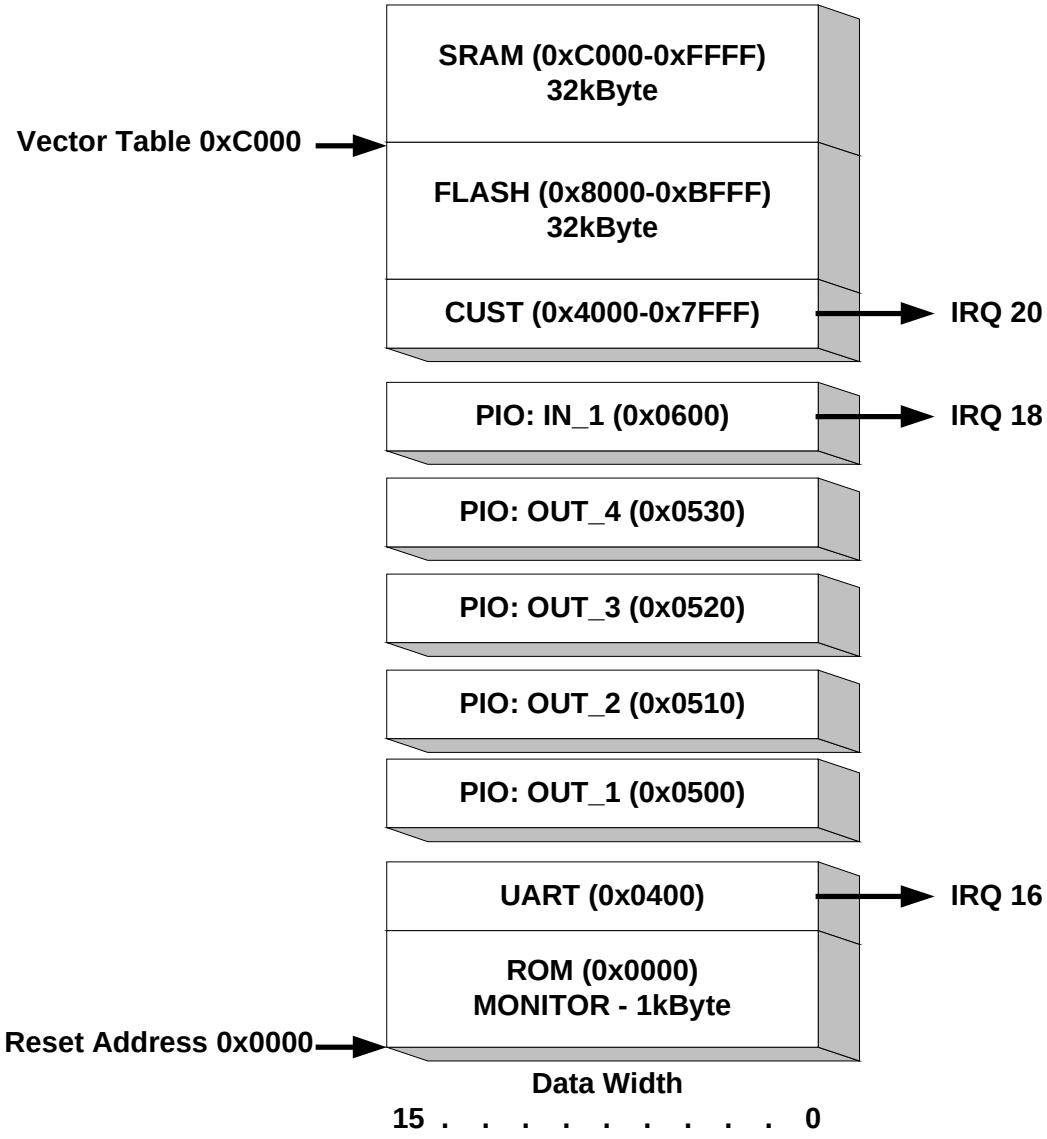
DIGILAB 1Kx208 Demo Design - Block Diagram

MAX+plus II Project

Part of the floppy disk is the following, complete MAX+plus II project. The graphical top-level design file is called “nios_digilab.gdf”



System Address Map
Below is the address map of the SOPC demo design.



System Configuration

The NIOS16 is included as is, a pre-parameterized and pre-synthesized EDIF netlist. You may use this 16-bit NIOS RISC CPU core, connect the parallel I/Os as needed and use the 16-bit interface “CUST” to connect you own custom on-chip logic.

Function	Parameter Name	Setting	Mapping
NIOS16_CPU (CPU CORE)	Architecture	16-bit	
	Size of Address Bus	16-bit	
	Register File Size	256 Registers	
	Internal Shifter Speed	7 bits max. per clock	
	Include Multiply-step unit	False	
MONITOR (ROM)	ROM Size	512 half-words (16-bit)	0x0000 - 0x03FF
	ROM Input File	germsMon16.mif	
UART (UART)	Input Clock Frequency	24 MHz	0x0400 - 0x040F IRQ 16
	Baud Rate	115200 bps	
	Parity, Data Bits, Stop Bits	N,8,1	
OUT_1 (PIO)	PIO width	8 bits	0x0500 - 0x0507
	Type of Pins	Output pins only	
OUT_2 (PIO)	PIO width	8 bits	0x0510 - 0x0517
	Type of Pins	Output pins only	
OUT_3 (PIO)	PIO width	8 bits	0x0520 - 0x0527
	Type of Pins	Output pins only	
OUT_4 (PIO)	PIO width	8 bits	0x0530 - 0x0537
	Type of Pins	Output pins only	
IN_1 (PIO)	PIO width	4 bits	0x0600 - 0x0607 IRQ 18
	Type of Pins	Input pins only	
	Edge Capture Register	Synchronously sample inputs and capture: Falling	
	Interrupt Source	Edge	
CUST (Memory Mapped Peripheral)	Location	On-Chip	0x4000 - 0x7FFF IRQ 20
	Data Bus	16 bits	
	Address Bus	13 bits	
	Fixed number of wait-states	1 Read / 1 Write	
	Interrupt	Yes	
EXT_FLASH (Memory Interface)	Location	Off-Chip	0x8000 - 0xBFFF
	Data Bus	16 bits	
	Address Bus	13 bits	
	Fixed number of wait-states	8 Read / 8 Write	
	Interrupt	No	
EXT_RAM (Memory Interface)	Location	Off-Chip	0xC000 - 0xFFFF
	Data Bus	16 bits	
	Address Bus	13 bits	
	Fixed number of wait-states	0 Read / 0 Write	
	Interrupt	No	

Chapter

6

Work with the Demo Design

The design example that comes with the Digilab has been compiled before and includes a configuration file (nios_digilab.sof).

Hardware Setup

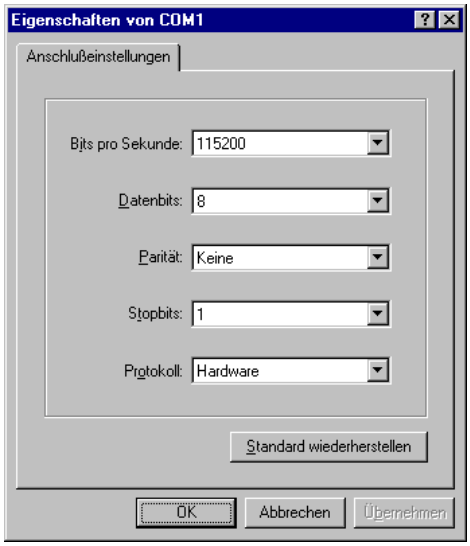
1) Connect the Digilab to your PCs parallel port with the cable provided
2) Connect a power supply with the Digilab board
3) Connect the serial port connector of the DIGILAB to the serial port of your PC, using a standard null-modem cable

Download ACEX 1K Configuartion

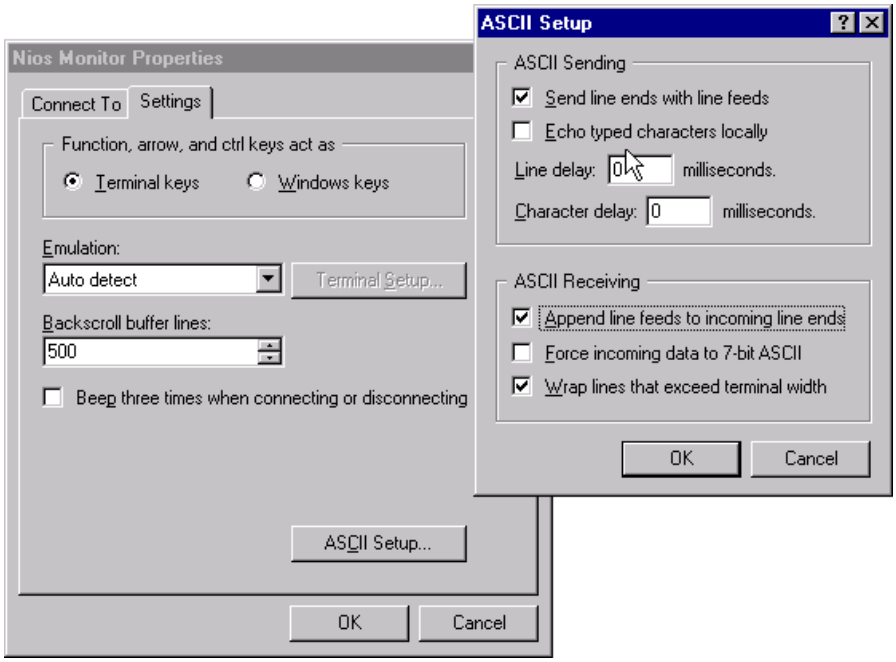
1) Unzip the examples directory on the included floppy disk to your PCs hard disk drive (If you haven't already done so).
2) Start MAX+plus II and select **File/Project/Name**, go to the examples directory, select **nios_digilab.gdf** and choose **OK**.
3) Select **MAX+plus II/Programmer**.
4) Select **JTAG/Multi Device JTAG Chain Setup** and configure the JTAG chain settings. Select "nios_digilab.sof" as configuration file for the ACEX 1K device.
5) Configure the ACEX 1K device.

Connect to the Monitor

1) Run Hyperterminal
   New connection name: Nios Monitor
   Connect using: COM1
   Port settings:



2) Select:
File, Properties, Settings tab, ASCII Setup
Send line ends with line feeds
Append line feeds to incoming lines



Monitor Commands

- **Go**
  Execute a CALL instruction to the specified address.
  Syntax: G<address>
  <address> is any number of hexadecimal digits
  Example: GC100
  Nios runs until done
  To stop Nios, press RESET (S5) button on DIGILAB board

- **Erase**
  Erase Flash Memory
  If the address is within the range of the "flash" ROM, the sector containing that address will be erased
  Syntax: E<address>
  <address> is any number of hexadecimal digits
  Example: E8000

- **Relocate**
  Relocate next download to this address
  Next S-record or I-Hex record will be stored starting at this address
  Syntax: R<address>
  <address> is any number of hexadecimal digits
  Example: R8000

- **Display/Write Memory**
  Display a range of memory
  Write successive 16-bit words to memory
  Fill a range of memory with a 16-bit word

Syntax:	M<address> - <address>	MC000-C100
	M<address>	MC000
	M<address> : <value> <value> <value>	MC000:feff 43 6f5
	M<address> - <address> : <value>	MC000-C100:dead

- **S-Record**
  Accept an S-record
  Syntax: S<S-record data>
  Example: S<218400000 . . . >
  Usage: Terminal programs (e.g. Hyperterm) can download an srec file by "transferring" the file to the COM port

- **I-Hex record**
  Syntax: :<I-Hex record data>
  Example: :800000004
  Usage: Terminal programs (e.g. Hyperterm) can download an I-Hex file by "transferring" the file to the COM port

- **Display the next 16 bytes of memory**
  Syntax: <CR>
  Usage: r0
  #0000: 4A4C 3189 9808 0409 8868 3000 4950 9820
  +
  #0010: 3604 35E5 3466 3413 3414 3415 8917 3000
  +
  #0020: 9806 7F29 891F 3000 890B 35A8 8909 3548

  m0
  #0000: 4A4C 3189 9808 0409 8868 3000 4950 9820
  +
  #0010: 3604 35E5 3466 3413 3414 3415 8917 3000
  +
  #0020: 9806 7F29 891F 3000 890B 35A8 8909 3548

Download the "Hello World" Example Program

- **Run Hyperterminal**
  Connection name: Nios Monitor
  (Connect through COMx, 115000, 8 , n, 1, no flow control)

- **Select:**
  Transfer, Send Text File
  hello_world.srec

- **Execute program:**
  gC100

  #1554002B
  +gC100

  Hello, from Nios!
  Please observe the Digilab...
  99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76
  75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52
  51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28
  27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
  Good bye.

Chapter

7

Using MAX+plus II for your own Designs

Further Documentation

Enclosed is the Altera Digital Library CD-ROM.
On this CD you'll find all current Altera documentation and data sheets. You may also want to check the Altera homepage at http://www.altera.com for more up to date information or newer versions of the MAX+plus II BASELINE software.

<cd-drive>:\Man\Maxiigs.pdf
The CDROM contains the MAX+plus II Getting Started Manual. In Section 2 from page 73 to page 154 you'll find a detailed description of the MAX+plus II software. Section 3, on pages 155 through 276 contains a detailed tutorial that demonstrates the basic features of MAX+plus II.

<cd-drive>:\Ds\ACEX.pdf
There's also a complete data sheet available about ACEX 1K that also includes the EP1K100QC208 device.

<cd-drive>:\Ds\Dsconf.pdf
This data sheet describes the optional FLASH based, re-programmable serial EPROM EPC2.

To start your own design you might want to copy the demo design, which already has all necessary assignments. You can then just modify the top-level graphic design file "nios_digilab.gdf" by deleting existing and entering, respectively connecting new symbols from the various libraries.

Chapter

8

Board Description

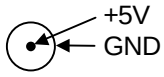
Disable Unused Features

The DIGILAB 1Kx208 Board has various features which need to be disabled when not used. Make sure that you drive the enable and chip select outputs as specified and reserve the listed ACEX 1K inputs, that are driven by external devices.
All unused I/Os in your ACEX 1K design will automatically turn into outputs. There may be contentions when such unused I/Os are driven by external devices.

		ACEX 1K		
Feature	**Signal Name**	**Pin**	**Direction**	**When not used**
RS232	SER_TXD	29	in	reserve as input
	SER_CTS	135	in	reserve as input
USB	USB_VP	128	in	reserve as input
	USB_VM	125	in	reserve as input
	USB_RCV	131	in	reserve as input
Serial EEPROM	SPI_MISO	119	in	reserve as input
SRAM	CE_RAM_N	207	out	drive high
FLASH EPROM	CE_FL_N	104	out	drive high
Audio Chip	CO_BCLK	141	in	reserve as input
	CO_SDIN	144	in	reserve as input

Power Supply

Connector – J30



Connect VCC to the inner pin and GND to the outer shell of the power connector. There are three fixed voltage regulators for VCC-INT @ 2.5V, VCC-IO @ 3.3V and VCC-AUX @ 5V on board. You may supply 7 to 9V unregulated DC.

Configuration

Connector – J31
Use the included parallel port cable to connect your PC's parallel port with the DIGILAB parallel port connector J31. This interface is used to configure the ACEX 1K device or program the EPC2 serial Flash EPROM. Close JP2 to bypass the EPC2 when it is not present. See Chapter 6 for details on how to download a configuration file.

Push the re-configuration push button (S6) to manually restart configuration from the serial EPROM EPC2 (U2).

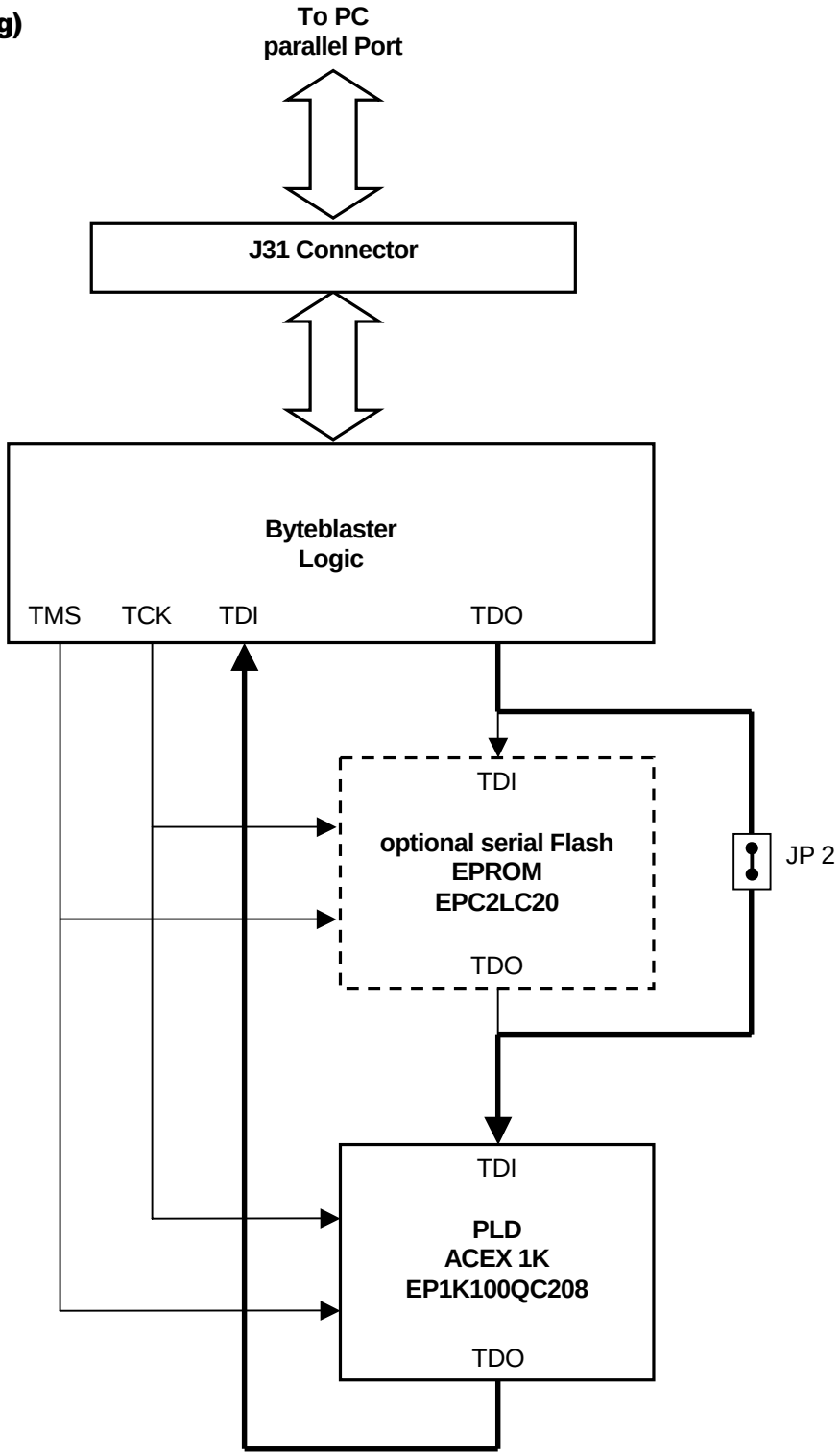
The DIGILAB board features a JTAG chain for ACEX 1K configuration or EPC2 programming. Jumpers JP2 allows the setting of two different modes.

	JP2	
ACEX 1K configuration, no EPC2 installed	closed	default
ACEX 1K configuration and EPC2 programming	open	

LED5 is connected to the CONF_DONE and NSTATUS outputs of the FLEX 10K device and gives you the status of the configuration.

		LED 5
Configuration Error	NSTATUS = low	red
Configuration Successful	CONF_DONE = high	green

JTAG Chain Configuration
(default setting)



Global Reset

There is a global reset switch (S5) which feeds the global reset input (DEV_CLRn) of the ACEX 1K device. This switch is already de-bounced to avoid problems. If you want to use the global reset feature it must be enabled in the Device Settings in the Compiler.

Push Buttons

There are four universal push buttons on board. Default value to the ACEX 1K device is logic high when not pushed and logic low when pushed. These push buttons are not de-bounced.

	S1	**S2**	**S3**	**S4**
Signal Name	KEY_S1	KEY_S2	KEY_S3	KEY_S4
ACEX 1K Pin	71	68	69	65

User LEDs

Eight LEDs (4 dual red/green) can be used for custom functions. LEDs are on, when the corresponding ACEX 1K output is driven low.

	LD1		**LD2**	
	red	**green**	**red**	**gree**
Signal Name	LED1_RT	LED1_GN	LED2_RT	LED2_GN
ACEX 1K Pin	96	19	94	95

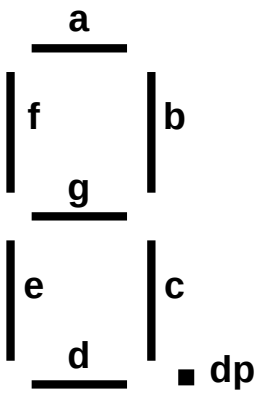
	LD3		**LD4**	
	red	**green**	**red**	**gree**
Signal Name	LED3_RT	LED3_GN	LED4_RT	LED4_GN
ACEX 1K Pin	87	93	90	62

7 Segment Displays

There is a 4-digit 7-segment multiplexed display on the board. Drive low to turn the segment on.

Common Anode	SD4	SD3	SD2	SD1
Signal Name	DIG4	DIG3	DIG2	DIG1
ACEX 1K Pin	113	101	89	83

Segment	Signal Name	ACEX 1K Pin
a	SEG_A	114
b	SEG_B	115
c	SEG_C	120
d	SEG_D	121
e	SEG_E	126
f	SEG_F	112
g	SEG_G	111
dp	SEG_DP	127



VGA Interface

Connector – J7
The ACEX 1K device can drive horizontal and vertical sync. signals, as well as red, green and blue. Since there's no VGA digital to analog conversion on board the three colours may only be turned on or off for each pixel.

		ACEX 1K	
VGA Signal	Signal Name	Pin	Direction
H-Sync	V_HSYNC	143	out
V-Sync	V_VSYNC	142	out
Blue	V_BLUE	139	out
Green	V_GREEN	140	out
Red	V_RED	136	out

RS232 Serial Interface

Connector – J12
The DIGILAB 1Kx208 has a RS232 driver (ADM3222, U12) and an according 9-pin connector on board. The physical interface can be used in conjunction with an UART in the ACEX 1K device e.g. as part of an Excalibur/NIOS embedded processor system.

		ACEX 1K		
RS232 Signal	**Signal Name**	**Pin**	**Direction**	**When not used**
TXD	SER_TXD	29	in	reserve as input
RXD	SER_RXD	28	out	
CTS	SER_CTS	135	in	reserve as input
RTS	SER_RTS	26	out	

USB Interface

Connector – J11
The DIGILAB 1Kx208 has an USB-driver (PDIUSBP11A, U11) and space for an USB-connector. Since there are two different types of USB-connectors (Type A and Type B) none is soldered to the board. You can install the one you need by yourself or leave it unpopulated.

BR3 selects the speed (high or low) for the driver. Depending on the kind of application you want to implement (host or device, high speed or low speed) you need to populate BR4 and BR5 with either 1,5Kohm or 15Kohm resistors to GND or VCC. For details please refer to the Philips USB-driver data sheet.

		ACEX 1K		
USB Signal	**Signal Name**	**Pin**	**Direction**	**When not used**
VMO/FSEO	USB_VMO	134	out	
VPO	USB_VPO	133	out	
OEX	USB_OEX	132	out	
VP	USB_VP	128	in	reserve as input
VM	USB_VM	125	in	reserve as input
RCV	USB_RCV	131	in	reserve as input

Serial EEPROM

There is serial EEPROM (93C46A) on the board. This device can be used to store some user defined, nonvolatile data. For a description and the protocol (serial read and write) please refer to the 93C46A datasheet e.g. from Atmel.

		ACEX 1K		
EEPROM Signal	**Signal Name**	**Pin**	**Direction**	**When not used**
SK	SPI_SCLK	122	out	
DI	SPI_MOSI	116	out	
CS	SEEP_CSX	103	out	
DO	SPI_MISO	119	in	reserve as input

Clocking

There is a quartz-oscillator on board (default 48MHz) which can drive CLK1. Optionally, the clocks can be terminated close to the clock pin of the ACEX 1K device (R12/C59 for CLK1, R11/C58 for CLK2).

	Resistor	**Capacitor**	**ACEX 1K Pin**
CLK 1	R 12	C 59	79
CLK 2	R 11	C 58	183

Optional Clock Termination

Unused clock pins must be tied to a fixed level (GND or VCCIO). CLK1 can be tied to GND by setting JP7, when there's no oscillator on board. CLK2 has a 10k Ohm pull-up resistor.

	JP7	
	Position B-X	**Position X-A**
CLK1 Input (Pin 79)	Tied to GND	Connected to Oscillator

The power supply for the PLLs is critical (affects jitter), therefore the PLL supply is decoupled via a L/C combination. In case of special requirements the connection between VCCINT and VCC_CKLK can be disconnected by removing L1. VCC_CKLK can then be applied from a different, special supply (e.g. special filter etc.).

The PLL lock output is either an user I/O or an output indicating the lock status of the on-chip PLL. This dual purpose pin is connected to LD4_GN. When the lock output is used, a logic high level or LD4/green **off** indicates the PLL has locked.

Dedicated Inputs

All four dedicated input pins have 10k pull-up resistors to VCCIO (3.3V). These inputs are available through J1/J3.

Signal Name	ACEX 1K Pin	Connector
IN78	78	J3-26
IN80	80	J3-28
IN182	182	J1-26
IN184	184	J1-28

SRAM

The DIGILAB 1Kx208 has a fast 256k x 16 on board SRAM (U10). It can be used as external RAM, e.g. for the NIOS embedded processor.

		ACEX 1K		
SRAM Signal	**Signal Name**	**Pin**	**Direction**	**When not used**
CEN	CE_RAM_N	207	out	drive high
UBN	UB_N	75	out	
LBN	LB_N	74	out	
WEN	WE_N	206	out	
OEN	OE_N	204	out	
-	ADR0	102	out	
A8	ADR1	177	out	
A11	ADR2	176	out	
A10	ADR3	179	out	
A9	ADR4	196	out	
A12	ADR5	189	out	
A5	ADR6	191	out	
A6	ADR7	190	out	
A7	ADR8	193	out	
A0	ADR9	197	out	
A1	ADR10	198	out	
A2	ADR11	195	out	
A3	ADR12	192	out	
A4	ADR13	187	out	
A15	ADR14	199	out	
A14	ADR15	200	out	
A13	ADR16	203	out	
A16	ADR17	205	out	
A17	ADR18	202	out	
IO0	D0	160	bidir	
IO1	D1	157	bidir	
IO2	D2	158	bidir	
IO3	D3	159	bidir	
IO4	D4	161	bidir	
IO5	D5	162	bidir	
IO6	D6	164	bidir	
IO7	D7	166	bidir	
IO8	D8	163	bidir	
IO9	D9	167	bidir	
IO10	D10	173	bidir	
IO11	D11	169	bidir	
IO12	D12	170	bidir	
IO13	D13	172	bidir	
IO14	D14	168	bidir	
IO15	D15	174	bidir	

FLASH EPROM

The DIGILAB 1Kx208 has a fast 512k x 16 on board FLASH EPROM (U9).

		ACEX 1K		
Flash Signal	**Signal Name**	**Pin**	**Direction**	**When not used**
CE_N	CE_FL_N	104	out	drive high
WE_N	WE_N	206	out	
OE_N	OE_N	204	out	
RESET_N	GCLR_N	180	out	
RD/BY_N	FL_RDY	88	in	driven by S5
-	ADR0	102	out	
A0	ADR1	177	out	
A1	ADR2	176	out	
A2	ADR3	179	out	
A3	ADR4	196	out	
A4	ADR5	189	out	
A5	ADR6	191	out	
A6	ADR7	190	out	
A7	ADR8	193	out	
A8	ADR9	197	out	
A9	ADR10	198	out	
A10	ADR11	195	out	
A11	ADR12	192	out	
A12	ADR13	187	out	
A13	ADR14	199	out	
A14	ADR15	200	out	
A15	ADR16	203	out	
A16	ADR17	205	out	
A17	ADR18	202	out	
A18	ADR19	175	out	
D0	D0	160	bidir	
D1	D1	157	bidir	
D2	D2	158	bidir	
D3	D3	159	bidir	
D4	D4	161	bidir	
D5	D5	162	bidir	
D6	D6	164	bidir	
D7	D7	166	bidir	
D8	D8	163	bidir	
D9	D9	167	bidir	
D10	D10	173	bidir	
D11	D11	169	bidir	
D12	D12	170	bidir	
D13	D13	172	bidir	
D14	D14	168	bidir	
D15	D15	174	bidir	

Audio Chip

The DIGILAB 1Kx208 has an on-board 18-bit stereo AC97 DSPCodec from Texas Instruments (Part-No.: TLV320AIC27).

Some key features of the chip are:

- 18-Bit Stereo Codec
- S/N Ratio >95 dB
- Multiple Stereo Input Mixer
- Mono and Stereo Volume Control
- Four DAC Channels, Stereo ADC
- Balanced Mixer Architecture
- Variable Rate Audio and Modem Support
- Analog 3D Stereo Enhancement
- Line Level Outputs
- Master/Slave ID Selection
- AC97 Rev. 2.1 Compliant

Refer to the data sheet from TI for further details
(http://www-s.ti.com/sc/psheets/slas253a/slas253a.pdf)

Connector J8
J8 can be used as stereo audio input to the Audio Chip. JP3/JP4 select whether LINE or MIC inputs are driven by connector J8.

	JP3 / JP4	
	Position B-X	**Position X-A**
Audio Input	MIC input	LINE input

Connector J9
J9 is the line output of the Audio Chip.

Jumper JP1
JP1 selects the clock source for the Audio Chip.

	JP1	
	Position B-X	**Position X-A**
Audio Chip Clock Source	CO_CLK from ACEX 1K	On board crystal

		ACEX 1K		
Audio Chip	**Signal Name**	**Pin**	**Direction**	**When not used**
SDATOUT	CO_SDOUT	148	out	
BITCLK	CO_BCLK	141	in	reserve as input
SDATIN	CO_SDIN	144	in	reserve as input
SYNC	CO_SYNC	150	out	
RESETB	CO_RESET	147	out	
XTLIN	CO_CLK	149	out	

User Connector J6

This connector can be used to connect standard components or sub-modules to the DIGILAB 1Kx208. J6A conforms to the IDE standard.

J6B

1	GND	2	VCC5V
3	GND	4	J6_B4
5	J6_B5	6	J6_B6
7	J6_B7	8	J6_B8
9	J6_B9	10	J6_B10
11	J6_B11	12	J6_B12
13	J6_B13	14	J6_B14

J6C

1	VIAUX	2	GND
3	VREF	4	GND
5	GND	6	VCC3V3
7	GND	8	VCC3V3
9	GND	10	CLK_OSC
11	GND	12	CLK1
13	GND	14	CLK2
15	GND	16	N/C
17	GND	18	N/C
19	GND	20	N/C

J6A

1	GCLR_N	2	GND
3	J6_A3	4	J6_A4
5	J6_A5	6	J6_A6
7	J6_A7	8	J6_A8
9	J6_A9	10	J6_A10
11	J6_A11	12	J6_A12
13	J6_A13	14	J6_A14
15	J6_A15	16	J6_A16
17	J6_A17	18	J6_A18
19	GND	20	N/C
21	J6_A21	22	GND
23	J6_A23	24	GND
25	J6_A25	26	GND
27	J6_A27	28	J6_A28
29	J6_A29	30	GND
31	J6_A31	32	J6_A32
33	J6_A33	34	GND
35	J6_A35	36	J6_A36
37	J6_A37	38	J6_CSN
39	J6_A39	40	GND

User Connectors J1-J4

All ACEX 1K pins are accessible through connectors J1-J4. You can use these as test points, to connect your own IOs or build daughter cards that can be plugged onto the DIGILAB 1Kx208.

J1								
Connector Pin	ACEX 1K Pin		Connector Pin	ACEX 1K Pin		Connector Pin	ACEX 1K Pin	
		Signal			Signal			Signal
54		VCC3V3	53		USER3	52	208	IO208NCS
51	207	CE_RAM_N	50	206	WE_N	49	205	ADR17
48	204	OE_N	47	203	ADR16	46	202	ADR18
45	201	VCCINT	44	200	ADR15	43	199	ADR14
42	198	ADR10	41	197	ADR9	40	196	ADR4
39	195	ADR11	38	194	VCCIO	37	193	ADR8
36	192	ADR12	35	191	ADR6	34	190	ADR7
33	189	ADR5	32	188	GND	31	187	ADR13
30	186	IO186DOE	29	185	VCCINT	28	184	IN184
27	183	CLK2	26	182	IN182	25	181	GND
24	180	GCLR_N	23	179	ADR3	22	178	VCCIO
21	177	ADR1	20	176	ADR2	19	175	ADR19
18	174	D15	17	173	D10	16	172	D13
15	171	GND	14	170	D12	13	169	D11
12	168	D14	11	167	D9	10	166	D7
9	165	VCCIO	8	164	D6	7	163	D8
6	162	D5	5	161	D4	4	160	D0
3	159	D3	2	158	D2	1	157	D1

User Connector J2

J2								
Connector Pin	ACEX 1K Pin		Connector Pin	ACEX 1K Pin		Connector Pin	ACEX 1K Pin	
		Signal			Signal			Signal
54		VCC3V3	53		USER4	52	52	NSTATUS
51	51	TRST	50	50	TMS	49	49	GND
48	48	VCCINT	47	47	J6_A8	46	46	J6_A7
45	45	J6_A10	44	44	J6_A9	43	43	GND
42	42	VCCIO	41	41	J6_A12	40	40	J6_A11
39	39	J6_A14	38	38	J6_A13	37	37	J6_A16
36	36	J6_A15	35	35	GND	34	34	VCCIO
33	33	VCCINT	32	32	GND	31	31	J6_A18
30	30	J6_A17	29	29	SER_TXD	28	28	SER_RXD
27	27	J6_A21	26	26	SER_RTS	25	25	J6_A23
24	24	J6_A28	23	23	GND	22	22	VCCIO
21	21	VCCINT	20	20	GND	19	19	LED1_GN
18	18	J6_A28	17	17	J6_A27	16	16	RNBSY
15	15	J6_A29	14	14	J6_A31	13	13	J6_A32
12	12	J6_A36	11	11	J6_A33	10	10	CLKUSR
9	9	J6_A39	8	8	J6_A37	7	7	J6_A35
6	6	GND	5	5	VCCIO	4	4	TDO
3	3	NCEO	2	2	CONFDONE	1	1	TCK

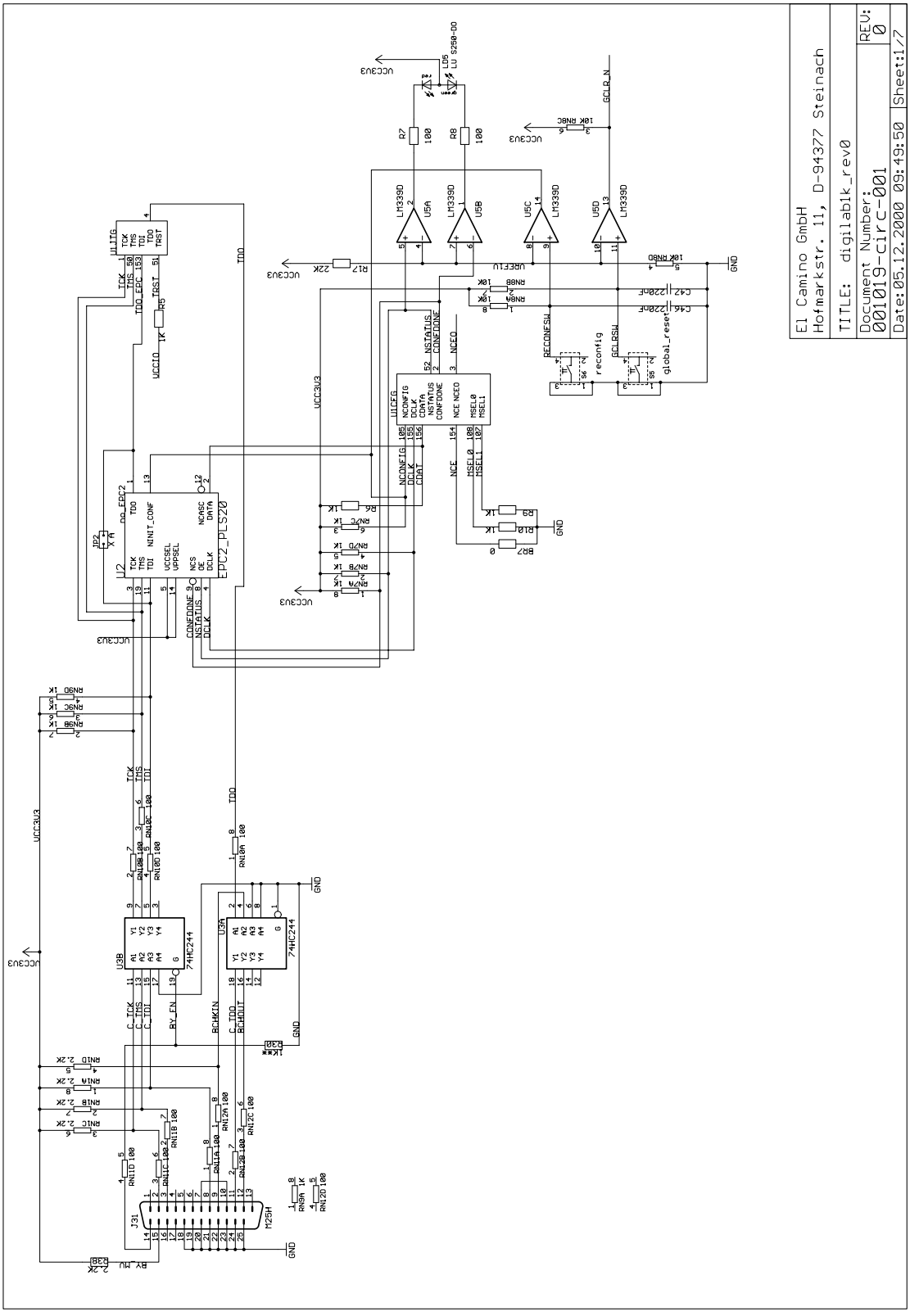
User Connector J3

J3								
Connector Pin	ACEX 1K Pin		Connector Pin	ACEX 1K Pin		Connector Pin	ACEX 1K Pin	
		Signal			Signal			Signal
54		VCC3V3	53		USER1	52	104	CE_FL_N
51	103	SEEP_CSX	50	102	ADR0	49	101	DIG3
48	100	SPARE100	47	99	SPARE99	46	98	VCCIO
45	97	SPARE97	44	96	LED1_RT	43	95	LED2_GN
42	94	LED2_RT	41	93	LED3_GN	40	92	J6_B9
39	91	VCCINT	38	90	LED4_RT	37	89	DIG2
36	88	FL_RDY	35	87	LED3_RT	34	86	J6_B10
33	85	J6_B11	32	84	VCCIO	31	83	DIG1
30	82	GND	29	81	GND	28	80	IN80
27	79	CLK1	26	78	IN78	25	77	VCC_CKLK
24	76	GND	23	75	UB_N	22	74	LB_N
21	73	J6_B12	20	72	VCCINT	19	71	KEY_S1
18	70	J6_B13	17	69	KEY_S3	16	68	KEY_S2
15	67	J6_B14	14	66	VCCIO	13	65	KEY_S4
12	64	J6_B7	11	63	J6_B6	10	62	LED4_GN
9	61	J6_B8	8	60	J6_A5	7	59	GND
6	58	J6_B5	5	57	J6_A6	4	56	J6_CSN
3	55	J6_B4	2	54	J6_A3	1	53	J6_A4

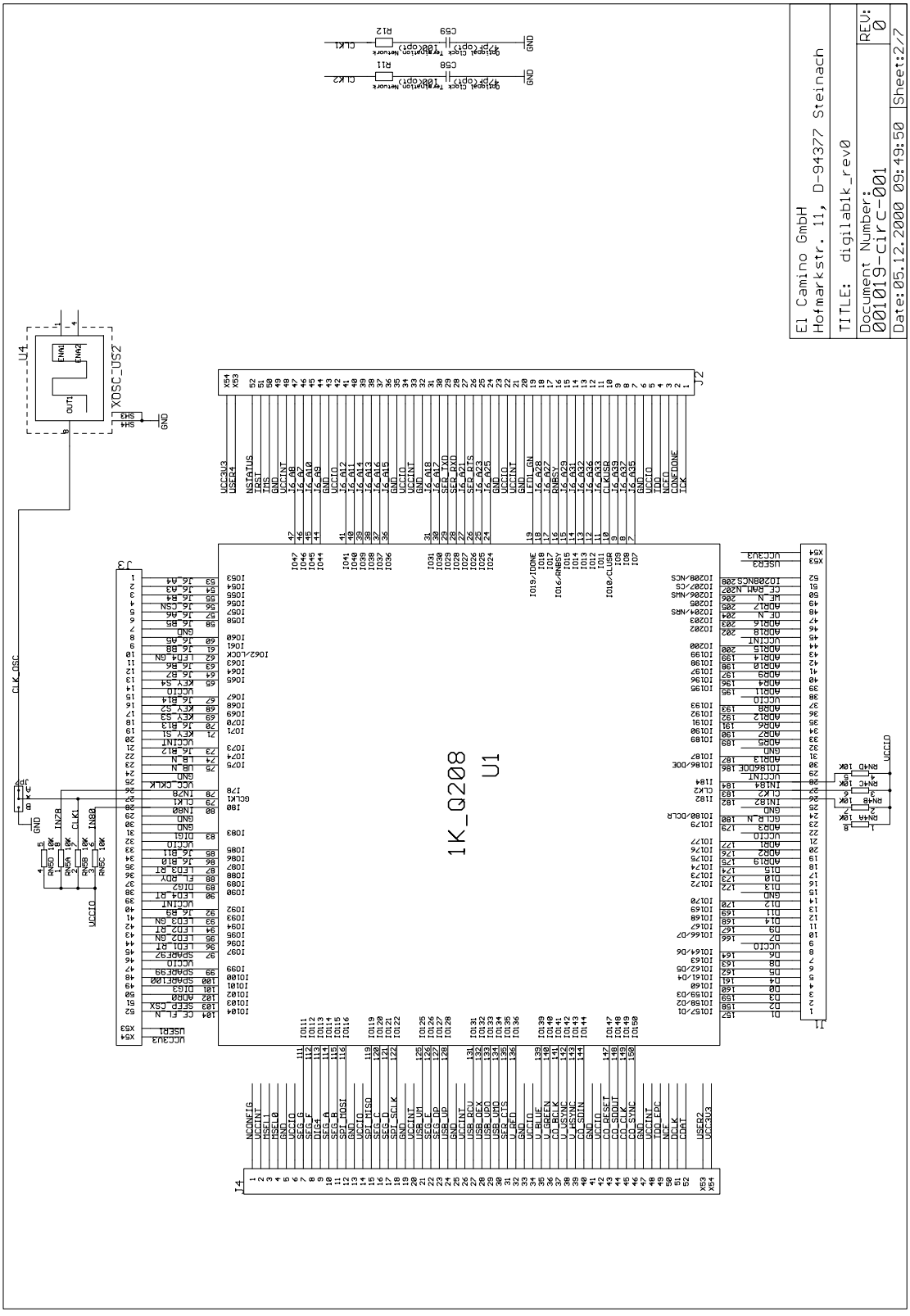
User Connector J4

J4								
Connector Pin	ACEX 1K Pin		Connector Pin	ACEX 1K Pin		Connector Pin	ACEX 1K Pin	
		Signal			Signal			Signal
54		VCC3V3	53		USER2	52	156	CDAT
51	155	DCLK	50	154	NCE	49	153	TDO_EPC
48	152	VCCINT	47	151	GND	46	150	CO_SYNC
45	149	CO_CLK	44	148	CO_SDOUT	43	147	CO_RESET
42	146	VCCIO	41	145	GND	40	144	CO_SDIN
39	143	V_HSYNC	38	142	V_VSYNC	37	141	CO_BCLK
36	140	V_GREEN	35	139	V_BLUE	34	138	VCCIO
33	137	GND	32	136	V_REG	31	135	SER_CTS
30	134	USB_VMO	29	133	USB_VPO	28	132	USB_OEX
27	131	USB_RCV	26	130	VCCINT	25	129	GND
24	128	USB_VP	23	127	SEG_DP	22	126	SEG_E
21	125	USB_VM	20	124	VCCINT	19	123	GND
18	122	SPI_SCLK	17	121	SEG_D	16	120	SEG_C
15	119	SPI_MISO	14	118	VCCIO	13	117	GND
12	116	SPI_MOSI	11	115	SEG_B	10	114	SEG_A
9	113	DIG4	8	112	SEG_F	7	111	SEG_G
6	110	VCCIO	5	109	GND	4	108	MSEL0
3	107	MSEL1	2	106	VCCINT	1	105	NCONFIG

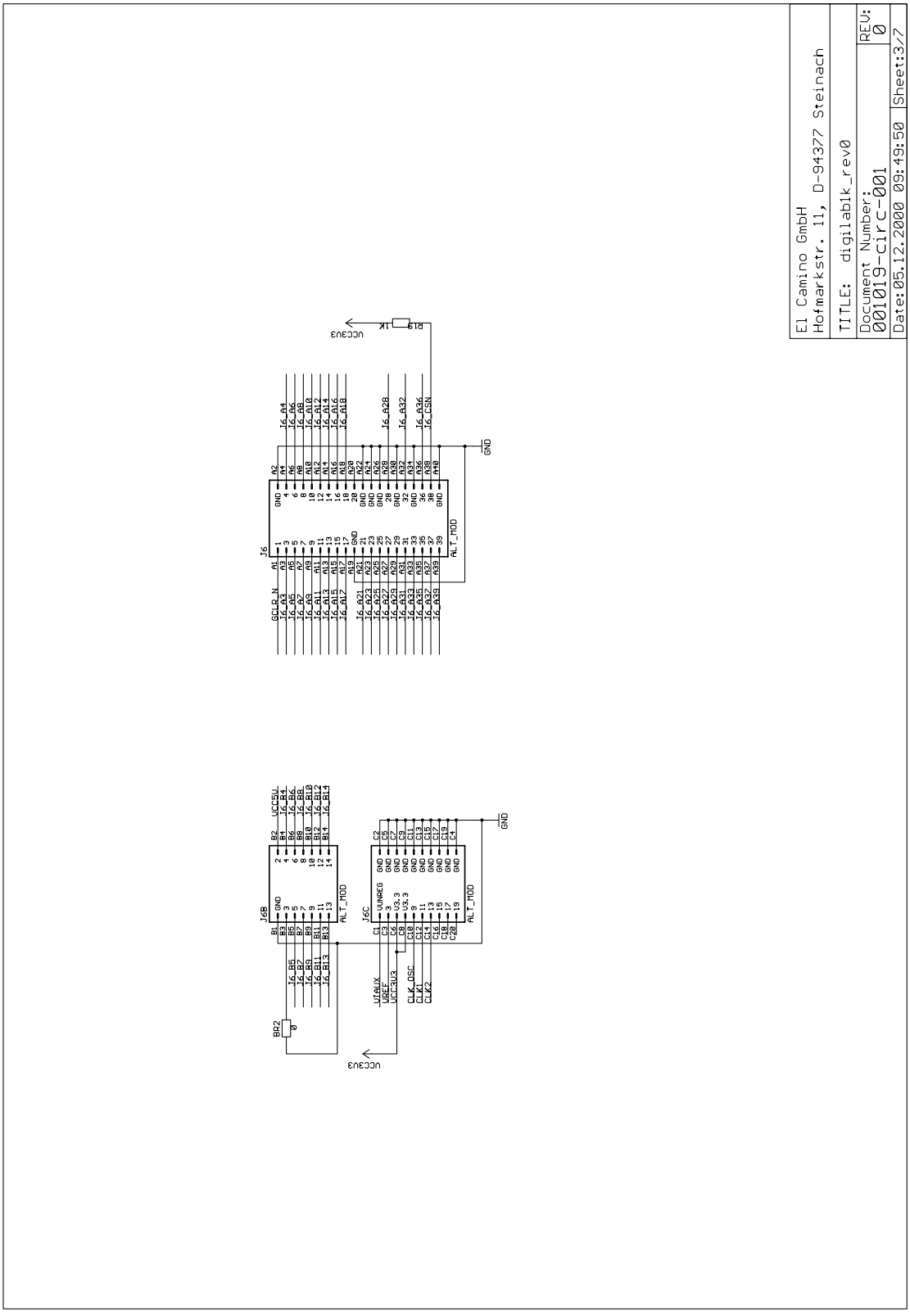
Board, Schematic, Page 1



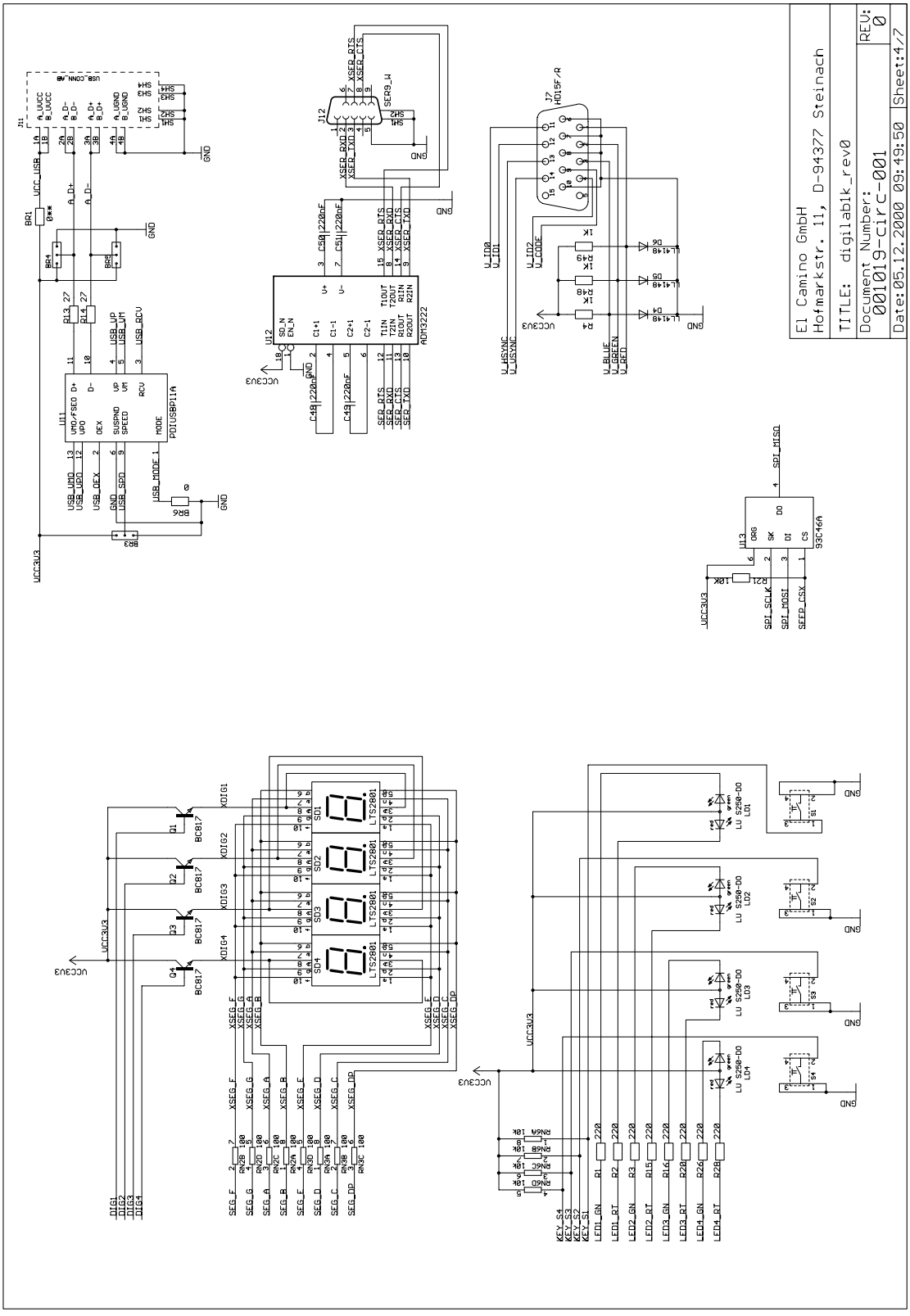
Board, Schematic, Page 2



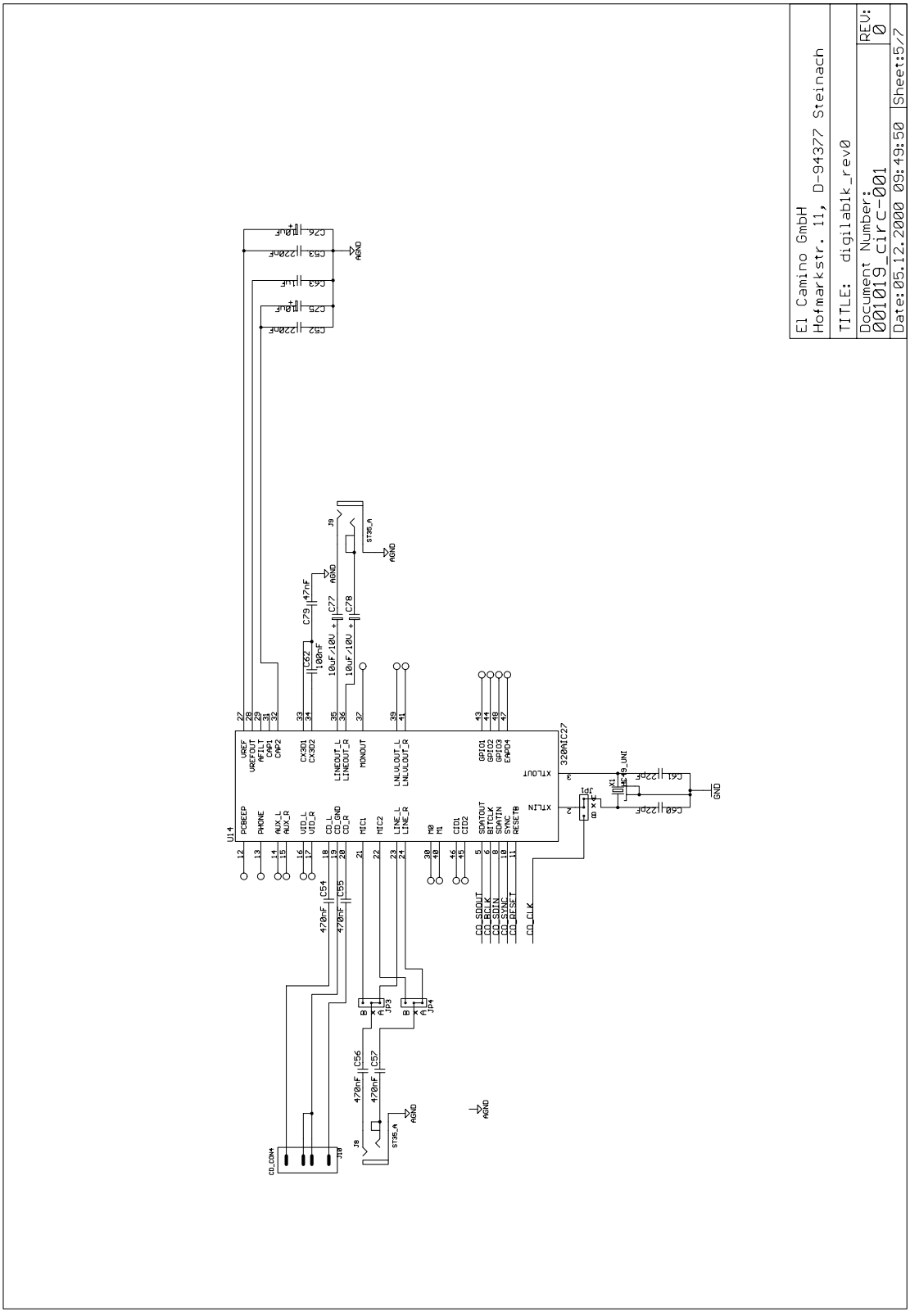
Board, Schematic, Page 3



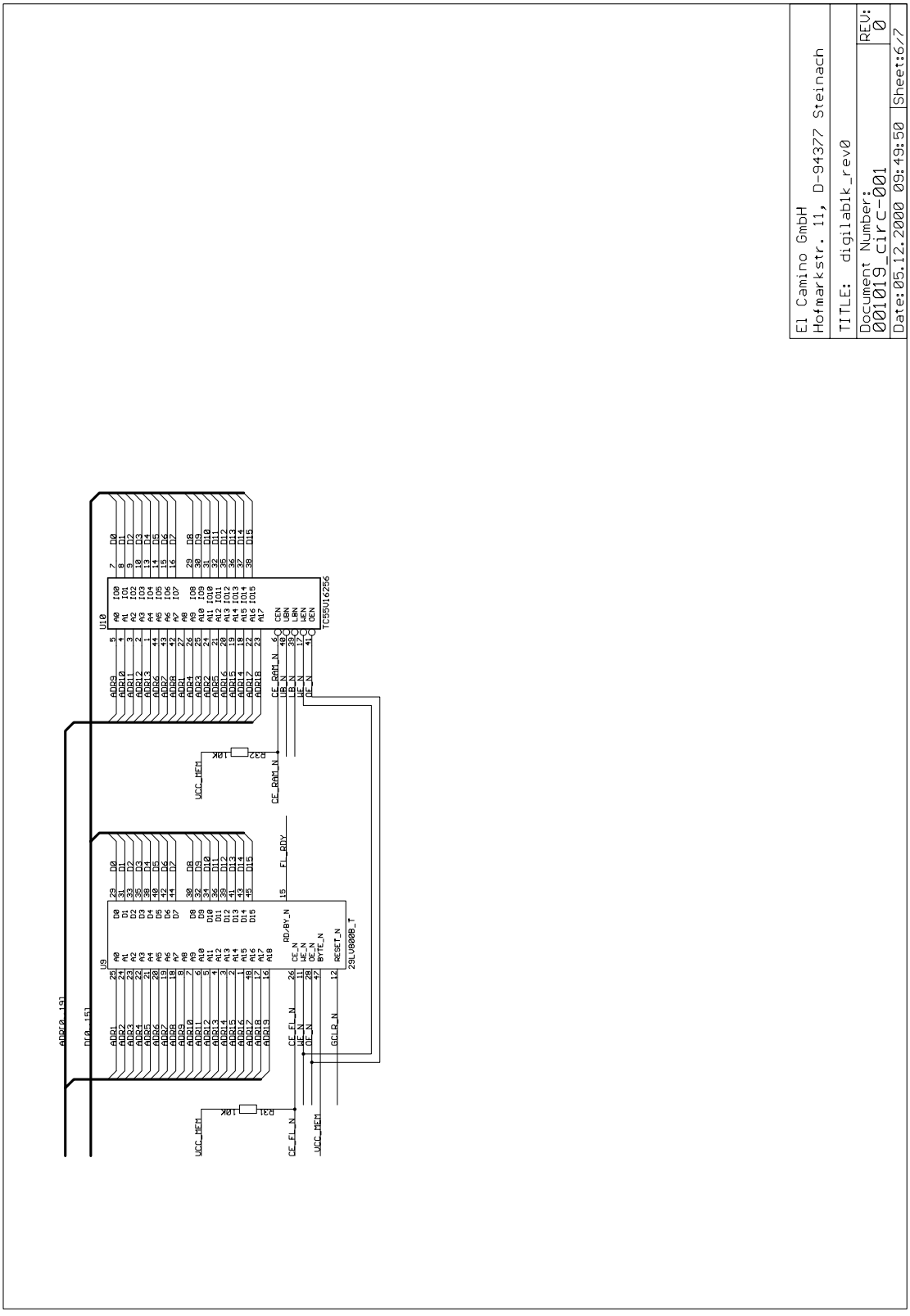
Board, Schematic, Page 4



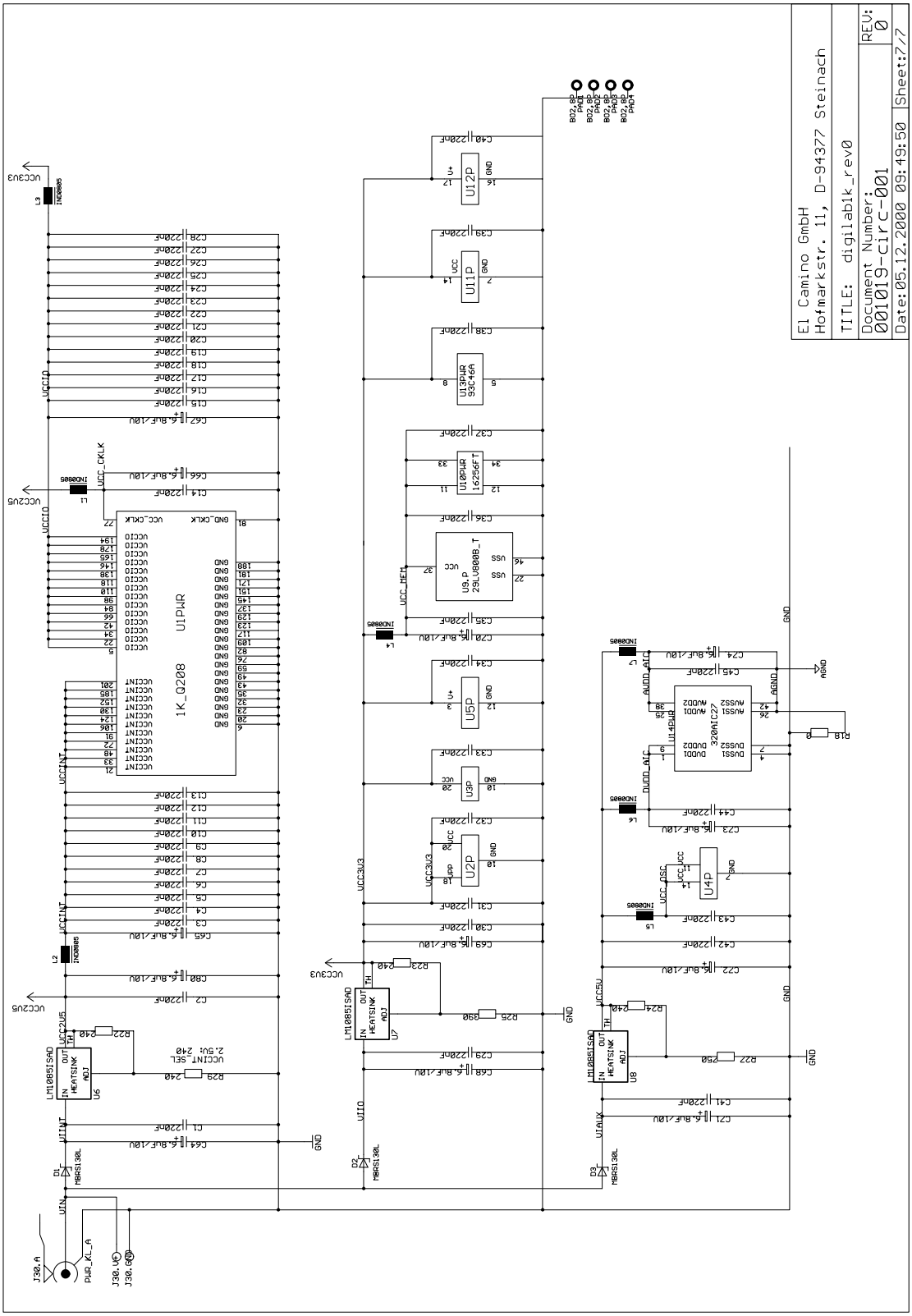
Board, Schematic, Page 5



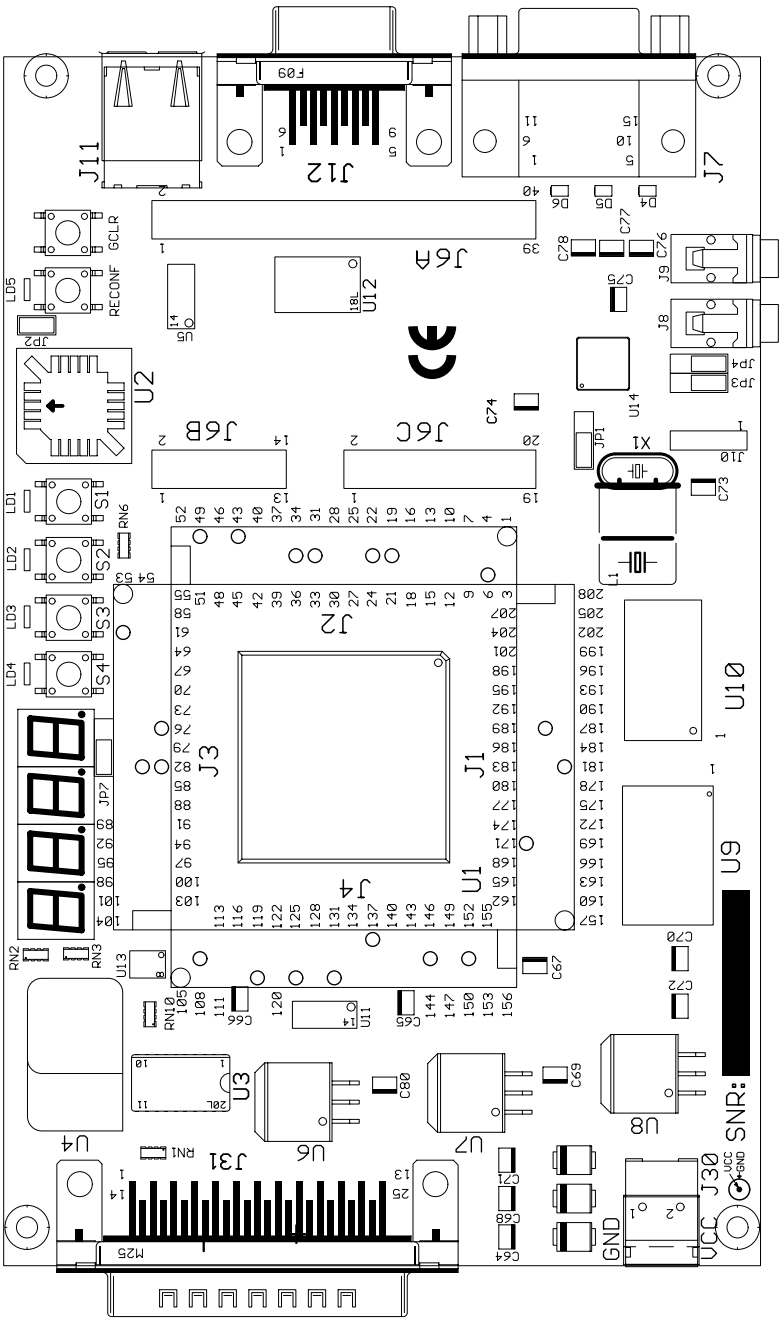
Board, Schematic, Page 6



Board, Schematic, Page 7



Board, Components Top Side



Board, Components Bottom Side