Voltage Translation (5 V, 3.3 V, 2.5 V, 1.8 V), Switching Standards, and Bus Contention

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Contents

List of Illustrations

Abstract

Voltage translation is required because many analog devices operate at 5-V V_{CC}, but most digital products operate at 3.3-V V_{CC}, or lower. Interfaces between devices must consider issues such as driver and receiver switching compatibility and bus contention. Texas Instruments (TI™) offers a variety of products that provide translation among 5-V, 3-V, 2.5-V, and 1.8-V devices.

Introduction

In today's applications there are many mixed-voltage designs that require voltage translation between different levels. Many analog products still operate at 5-V V_{CC}, whereas, most digital products have migrated to 3.3-V V_{CC}, or lower. TI's logic devices are ideal for these types of situations. This application report explains how to utilize TI logic products for both CMOS and TTL voltage translations.

Switching Compatibility Between Drivers and Receivers

To have switching compatibility between a driver and a receiver, the output of the driver must be compliant with the input of the receiver. To establish a low signal at the receiver, V_{OL} of the driver should be less than or equal to V_{IL} of the receiver. To establish a high signal at the receiver, V_{OH} of the driver should be greater than or equal to V_{IH} of the receiver (see Figure 1).

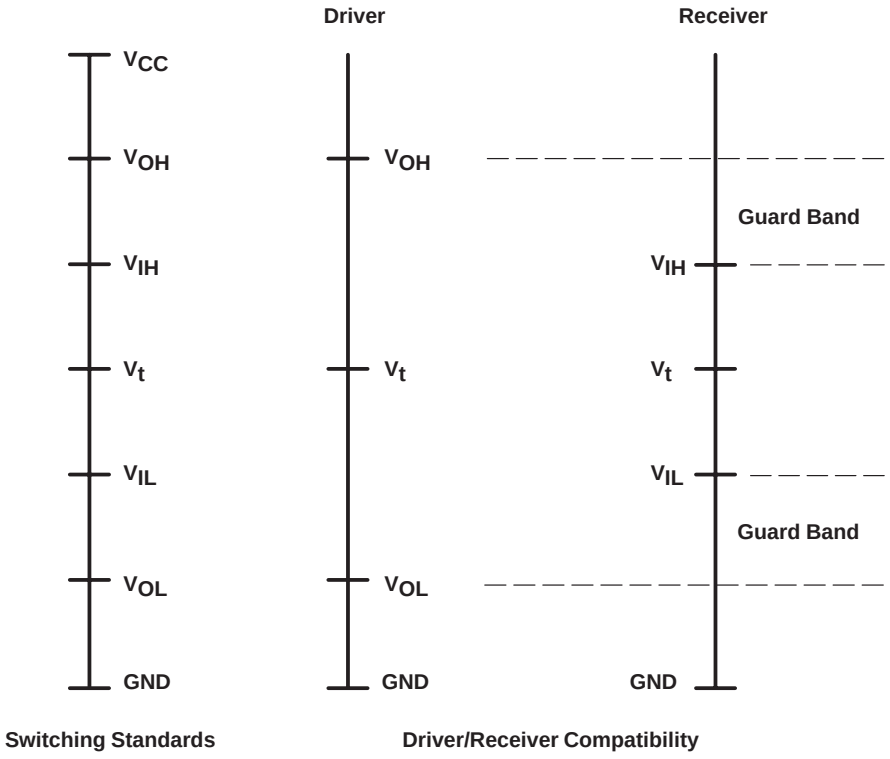

Figure 1. Switching Standards

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The guard band is the difference between the V_{OH} of the driver and the V_{IH} of the receiver and the difference between the V_{OL} of the driver and the V_{IL} of the receiver.

The threshold voltage (V_t) is the transition voltage where both the PMOS and NMOS transistors of the input stage may be turned on at the same time. At this level there is no valid signal level, and the device is unstable.

For CMOS devices, when both transistors are fully and/or partially turned on, there is a low-resistance current path from V_{CC} to ground that results in high power dissipation. When switching from low to high or high to low, the voltage passes through the threshold; however, it is not recommended that the input voltage of the receiver remains at the threshold region. This may cause a high surge of current drain that can damage the input and destroy the device (see Figure 2). A good practice is to keep the signal levels at the recommended operating conditions (above V_{IH} or below V_{IL} of the receiver).

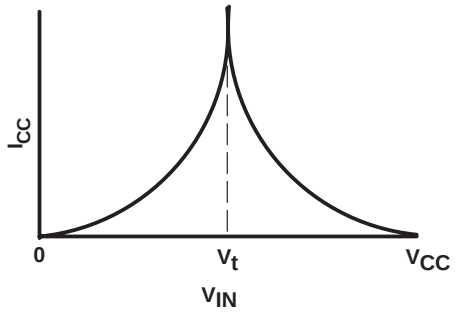


Figure 2. V_{IN} vs I_{CC}

As shown in Figure 2, the current consumption is the lowest at V_{IN} equal to 0 V or V_{CC}, and highest at the threshold voltage (V_t). Therefore, the power dissipation is lower when input voltages are at V_{CC} or ground. Refer to I_{CC} and ΔI_{CC} specification in the data sheet.

Product Families and Switching Standards

Figure 3 shows the switching standards for TI logic families.

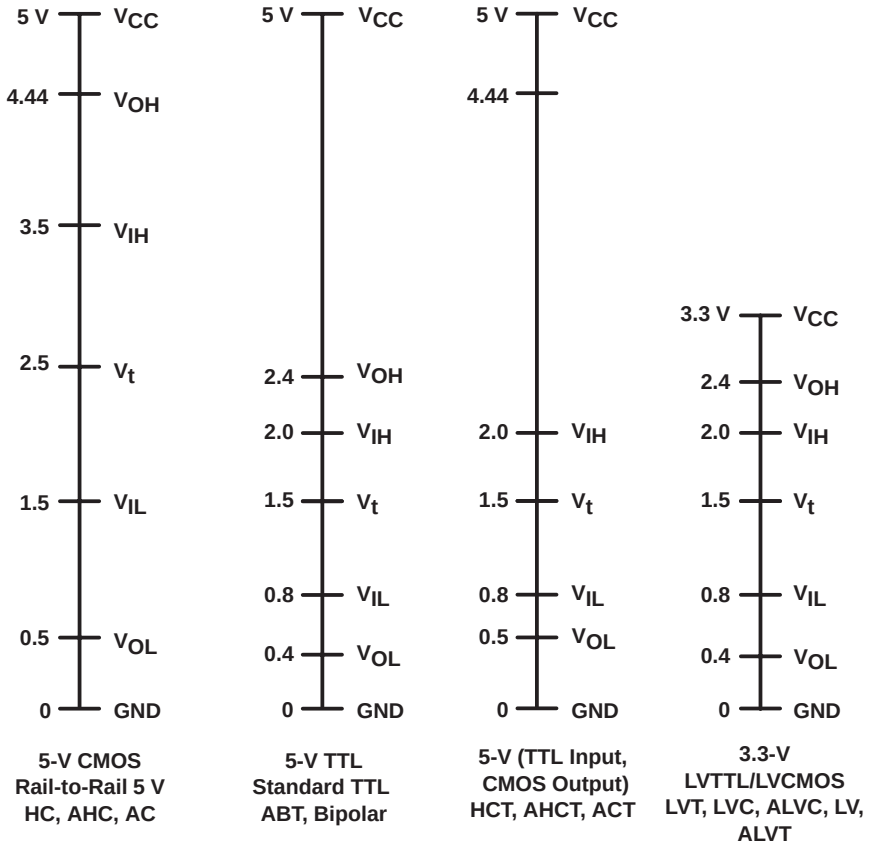


Figure 3. Comparison of Switching Standards

Frequently asked questions about switching standards are:

Do 3.3-V LVTTL and 3.3-V LVCMOS have the same switching standards?

Yes, 3.3-V LVTTL and 3.3-V LVCMOS have the same switching standards.

Which switching standards are compatible?

5-V TTL and 3.3-V (LVTTL and LVCMOS) have the same switching standards for V_{OL}, V_{IL}, V_{IH}, and V_{OH}. The only difference is V_{CC}.

Is 5-V CMOS compatible with 5-V TTL or 3.3-V LVTTL/LVCMOS?

In most cases, no, because V_{IH} for 5-V CMOS is 3.5 V. The exceptions are the HCT, AHCT, and ACT devices, which have TTL-input and CMOS-output compatibility.

Where do TI logic families fit in?

5-V CMOS inputs and outputs:	HC, AHC, and AC
5-V TTL inputs and outputs:	ABT and bipolar
5-V TTL inputs and 5-V CMOS outputs:	AHCT, HCT, and ACT
3.3-V CMOS and LVTTL:	LVC, ALVC, LV, LVT, ALVT, AVC, and AHC

Unidirectional Voltage Translations

Voltage Translation From 3.3-V LVTTL/LVCMOS to 5-V TTL

Because all TI 3.3-V logic devices are output compatible with 5-V TTL, this voltage translation can be done with TI 3.3-V families, such as LVT, LVC, ALVC, LV, ALVT, AHC, HC, and AVC (see Figure 4).

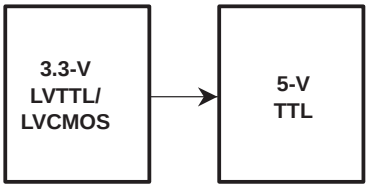


Figure 4. 3.3-V LVTTL/LVCMOS to 5-V TTL

Voltage Translation From 5-V TTL to 3.3-V LVTTL/LVCMOS

Because the 5-V TTL and 3.3-V LVTTL/LVCMOS switching standards are compatible, except for the V_{CC}, this translation can be done with TI 3.3-V logic families that have 5-V tolerant inputs, such as LVC, AHC, LVT, and ALVT. These logic families do not have a diode to V_{CC}, which was formerly used for electrostatic-discharge (ESD) protection (see Figure 5).

The diode to V_{CC} results in a current conduction at 3.3 V + 0.5 V_{be}. The resulting effects from the diode are:

- Clamping the driving signal at 3.3 V plus the diode drop
- Pulling the 3.3-V supply to a higher voltage (which may violate the data-sheet specification)
- Powering up a device that was intended to be powered down

Therefore, TI's 5-V-tolerant low-voltage families do not have this diode to V_{CC} and can be used in this voltage translation. They have other methods for ESD protection.

TI's CBTD or CBT with an external diode also can be used for 5-V TTL to 3.3-V LVTTL/LVCMOS translation.

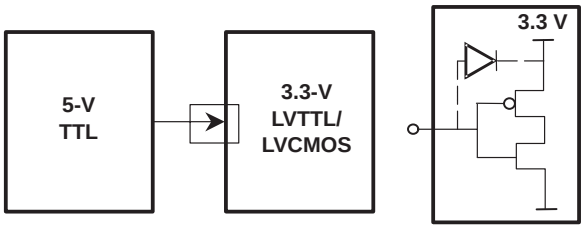


Figure 5. 5-V TTL to 3.3-V LVTTL/LVCMOS

Voltage Translation From 5-V CMOS to 3.3-V LVTTL/LVCMOS

This voltage translation can be done if the TI 3.3-V logic device is 5-V tolerant on the inputs, such as LVC, AHC, LVT, and ALVT (see Figure 6).

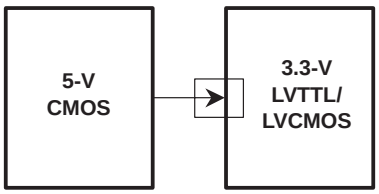


Figure 6. 5-V CMOS to 3.3-V LVTTL/LVCMOS

Voltage Translation From 3.3-V LVTTL/LVCMOS to 5-V CMOS

The 5-V CMOS V_{IH} is 3.5 V, which is above the V_{OH} of the 3.3-V devices. Therefore, a standard 3.3-V device cannot achieve this type of translation. TI has split-rail transceivers that have two voltage supplies, one on the A port and one on the B port, that allow for translation from 3.3-V LVTTL/LVCMOS to 5-V CMOS devices. The 8-bit LVCC3245A and LVCC4245A transceivers have configurable rails on the B port. The LVCC3245A A port can operate between 2.3-V and 3.6-V V_{CC}. The configurable B port can operate between 3-V and 5.5-V V_{CC}. The LVCC4245A A port operates between 4.5-V and 5.5-V V_{CC}, and the configurable B port operates between 2.7-V and 5.5-V V_{CC}. TI also offers 16-bit SN74ALVC164245 transceivers in which the A port has a 5-V V_{CC} and the B port has a 3.3-V V_{CC} (see Figure 7).

TI also has 5-V logic families (AHCT, HCT, and ACT) that have TTL inputs and CMOS outputs. Therefore, these devices can interface 3.3-V outputs to 5-V CMOS inputs (see Figure 7).

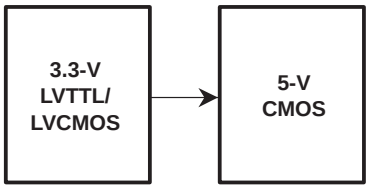
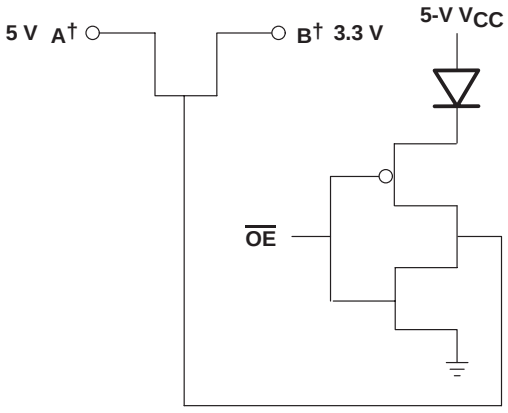


Figure 7. 3.3-V LVTTL/LVCMOS to 5-V CMOS

Bidirectional Voltage Translation

Voltage Translation From 3.3 V to 5-V TTL and From 5-V TTL to 3.3 V Using CBT or CBTD

This type of bidirectional translation (from A to B or B to A) can be done with TI's SN74CBT bus switches, using an external diode, or SN74CBTD bus switches that have the diode integrated internally. This method is suitable for voltage translation and bus-isolation applications. For example, with TI's 5-V V_{CC} SN74CBTD3384 bus switch (see Figure 8), the conditions are such that there are no pulldown resistors, and there is a minimal current passing through the FET.



† A can be 3.3 V, and B can be 5 V.

Figure 8. CBTD Bus Switch

The diode drop between V_{CC} and the PMOS gate is 0.7 V, which brings the voltage at the source to 4.3 V. With a 5-V input on the A side, the V_{gs} drop across the N channel is approximately 1.0 V, hence, the B side is translated to about 3.3 V. The typical V_{CC} vs V_{OH} graph is shown in Figure 9 and is provided in the data sheets for various temperatures and currents. In this example, the maximum voltage that can pass from B to A is 3.3 V. If a voltage less than 3.3 V is applied at B, the same voltage results on the A side. If a voltage greater than 3.3 V is applied at B, it is limited to 3.3 V on the A side. The V_{IH} min for 5-V TTL is 2.0 V. Therefore, as long as the voltage at B complies with 5-V TTL switching standards, this device can translate in both directions. Utilizing a bus switch for voltage translations also has the advantage of very fast propagation delay time.

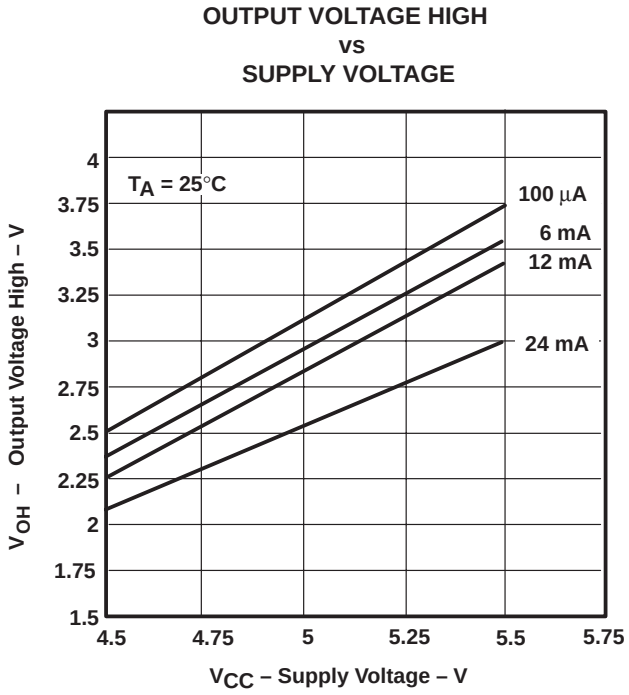


Figure 9. Typical V_{OH} vs V_{CC}

Voltage Translation From 3.3 V to 5-V TTL and 5-V TTL to 3.3 V Using TI 5-V-Tolerant Transceivers

TI's low-voltage logic transceivers that are 5-V input and output tolerant, such as LVT, ALVT, and most LVC devices, can be used for bidirectional voltage translation between 3 V and 5-V TTL when buffering is required, and added delay is not critical to the application (see Figure 10). Output tolerance is specified as output voltage (V_O) or as the voltage range applied to any output in the high-impedance or power-off state (refer to the absolute maximum ratings in the data sheet for more information).

See the *Bus Contention* section of this application report.

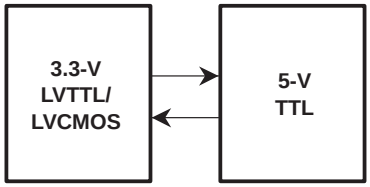


Figure 10. Translation Between 3.3 V and 5-V TTL

Voltage Translation From 3.3-V LVTTL/LVCMOS to 5-V CMOS and From 5-V CMOS to 3.3 V

Because 5-V CMOS switching standards have a $V_{IH(min)}$ of 3.5 V, TI split-rail devices, SN74LVCC4245A, SN74LVCC3245/A, and SN74ALVC164245 transceivers are the method of bidirectional voltage translation between 3.3-V and 5-V CMOS (see Figure 11).

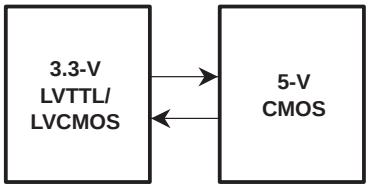


Figure 11. Translation Between 3.3-V and 5-V CMOS

Voltage Translation Between 3.3 V, 2.5 V, and 1.8 V

The switching standards allow for voltage translation between 2.5 V and 3.3 V. Voltage translation between 3.3 V and 2.5 V also is permissible if the 2.5-V device is 3.3-V input tolerant. Voltage translation between 1.8 V and 3.3 V is not possible because the 3.3-V V_{IH} min is 2.0 V, which is not in range for a 1.8-V V_{CC} device. Voltage translation from 1.8 V to 2.5 V also is not possible because the V_{IH} min for a 2.5-V V_{CC} device is 1.7 V (see Figure 12).

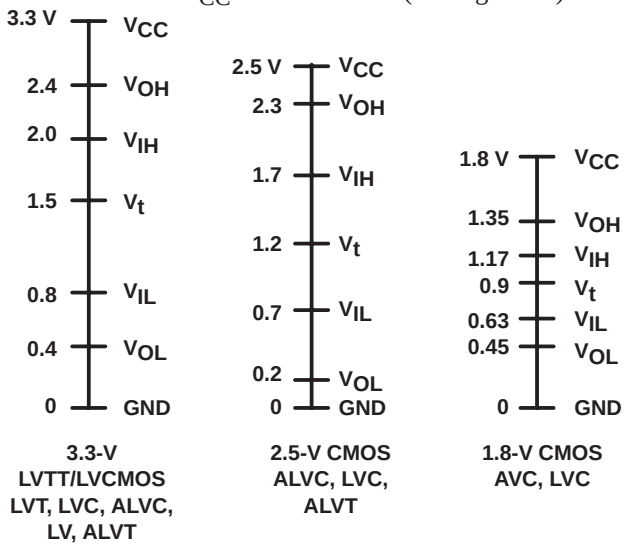


Figure 12. Comparison of Low-Voltage Switching Standards

Bus Contention

TI data sheets specify the maximum continuous current through a single output or through V_{CC} and GND. These values are absolute maximum ratings, which are stress ratings, not recommended operating conditions. These specifications most likely are exceeded when bus contention occurs.

Figure 13 shows a bus-contention situation between two devices driving the same bus. One has low-level output and the other has high-level output. This happens when drivers that have different enable and disable delays get on and off the same bus. This produces a short between the drivers, creating a current surge that may damage the devices. Typically, logic devices cannot withstand these high-current shorts that usually exceed the absolute maximum ratings of the device.

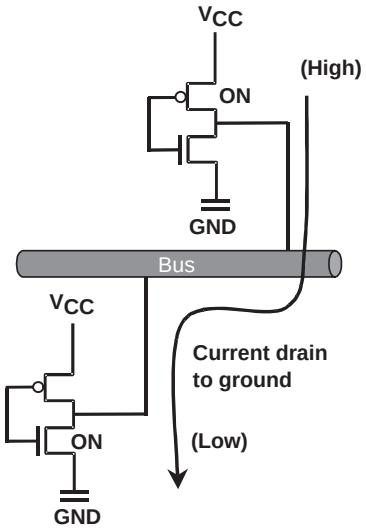


Figure 13. Bus Contention

If V_{CC} = 5 V and the resistance through the p and n channels of the transistors is about 10 Ω per output:

$$I = \frac{V}{R} = \frac{5\ V}{10\ \Omega} = 0.5\ A\ \text{per output} \quad (1)$$

Another high-current situation that may damage the device occurs when a 3.3-V device is at a high level and the output is pulled up to a higher voltage, such as 5 V (see Figure 14). Properly sizing the pullup resistor is very important. Using a pullup resistor of proper value limits the current to an allowable level. The device will not be damaged; however, there will be additional power dissipation from the current path through the 3.3-V device to V_{CC}.

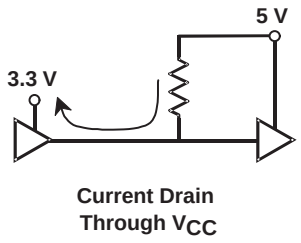


Figure 14. 3.3-V Driver Pulled to a Higher V_{CC}

The ALVT family has the auto3-state feature that automatically turns off the p-channel of the logic device to stop the current flow to V_{CC} (see Figure 15). This feature is specified in the absolute maximum ratings table of the ALVT data sheet as the voltage range applied to any output in the high state (-0.5 V to 7 V).

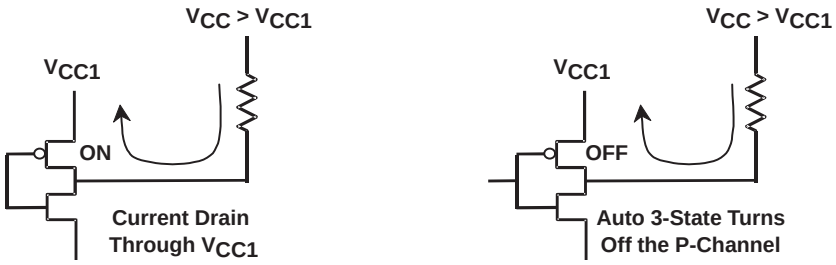


Figure 15. Auto3-State

Conclusion

Voltage translation from 5 V to 3 V, 3 V to 2.5 V, and vice versa, can be done with a wide variety of TI logic products. 3.3-V and 2.5-V logic can translate to 1.8 V, if the 1.8-V device is 2.5-V and 3.3-V tolerant. However, due to switching standards, 1.8-V logic currently cannot be translated upward to 2.5 V and 3.3 V with the existing families. Newer families are being developed to handle voltage translations of these levels.

Acknowledgment

The authors of this application report are Susan Feodorov and Ramzi Ammar.

Glossary

A

ABT	Advanced BiCMOS technology
AC/ACT	Advanced CMOS logic
AHC/AHCT	Advanced high-speed CMOS logic
ALVC	Advanced low-voltage CMOS technology
ALVT	Advanced low-voltage BiCMOS technology

C

CBT	Crossbar technology
CMOS	Complementary metal-oxide semiconductor

L

LS	Low-power Schottky logic
LV	Low-voltage CMOS technology
LVC	Low-voltage CMOS technology
LVCMOS	Low-voltage CMOS
LVT	Low-voltage BiCMOS technology
LVTTL	Low-voltage TTL (3.3-V power supply and interface levels)

V

V_{CC}	Supply voltage
V_{IH}	High-level input voltage
V_{IL}	Low-level input voltage
V_{IN}	Input voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_{OLP}	Low-level output voltage peak
V_{OLV}	Low-level output voltage valley
V_t	Threshold voltage