

datasheet name:

ADA-LVDS-RX-TWIN



name:

date:

build: Oliver Reiners

05.04.04

checked: A. Niederholz

16.04.04

approved: Oliver Reiners

16.04.04

SPEC.: ADA-LVDS-RX-TWIN

REV: 1.0

ES&S
CONNECTING THE WORLD

ADA-LVDS-RX-TWIN

Receiver board LVDS18/24 to TTL18

with



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1. functional description

This LVDS Receiver decodes a LVDS 18 or 24 BIT signal to a 18 BIT TTL-digital output. To connect the TTL-display it uses the ES&S standard connector ESDCI for different 18 BIT TTL display's from several manufacturers. Please refer to ESDCI® adapter's.

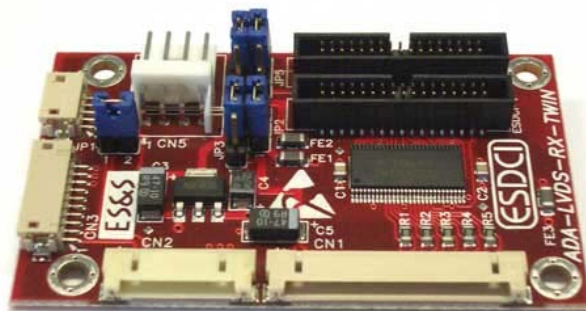
The power source for the receiver and the display may be switched (depending from the available source) by jumpers JP2-JP5 to different standard values. The jumper settings are explained in app B.

To be compatible with both LVDS standards 18 and 24 Bit there are two ESDCI® connectors mounted. One is used if the input is 18 Bit LVDS, the other one is used while using 24 Bit LVDS. The binary structure is different (MSB's and LSB's) so please check.

Additional there are several ways of loop-through-wires to ease up connection with inverter and optional hardware like USB or TOUCH-screens. Please refer to app. A.

The BRT-control may also be influenced by an external custom made regulator (JP1/CN4) which may be connected to CN4

2. adapter pictures



ESDCI® cable and adapters like shown are separate order parts !

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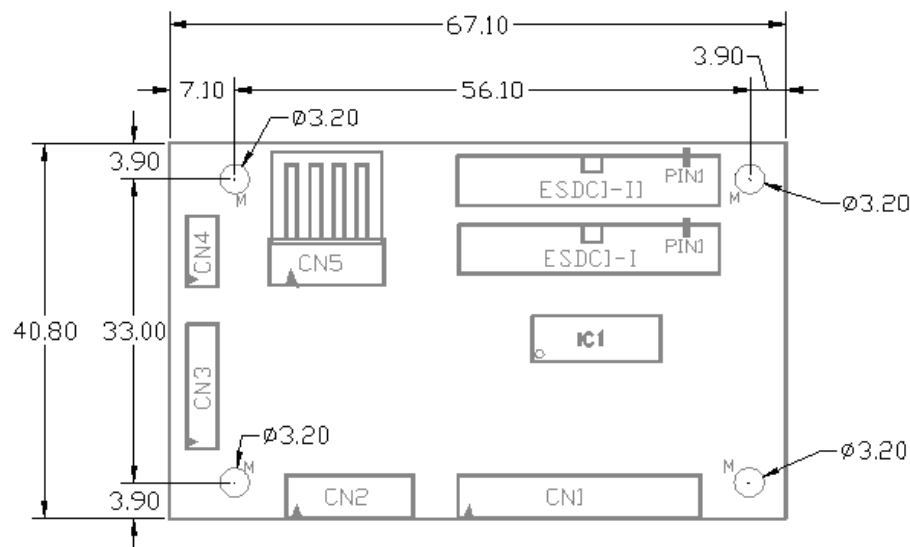
3. material definition

used material:

	mounted	corresponding	UL-Style
ESDCI-I/II	STE-C44-34-B-S-1	STE-A32-34	UL94V0
CN1	DF14-20P-1.25H	DF14-20S-1.25C	UL94V0
CN2	DF14-10P-1.25H	DF14-10S-1.25C	UL94V0
CN3	DF13-10P-1.25H	DF13-10S-1.25C	UL94V0
CN4	DF13-05P-1.25H	DF13-05S-1.25C	UL94V0
CN5	1x4 2.54mm male	various	UL94V0

4. dimension

Module size: 67.10 (H) x 40.80 (V) x 9.0 (D)



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5. electrical connection

ADA-LVDS-RX-TWIN					
CN1: LVDS Input		ESDCI-I/II: to display		CN3: Power Output	
pin	signal	pin	signal	pin	signal
1	Vcc 3.3V	1		1	BLEN
2	Vcc 3.3V	2		2	BRT
3	GND	3	GND	3	Vcc 5V
4	GND	4	CLK	4	Vcc 5V
5	Vcc 5V	5	HSYNC	5	GND
6	Vcc 5V	6	VSYNC	6	GND
7	OPT1	7	GND	7	GND
8	OPT2	8	R0	8	Vcc 12V
9	OPT3	9	R1	9	Vcc 12V
10	OPT4	10	R2	10	Vcc 12V
11	RX0-	11	R3	CN4: optional BRT	
12	RX0+	12	R4	pin	signal
13	RX1-	13	R5	1	BRT out
14	RX1+	14	GND	2	BRT in
15	RX2-	15	G0	3	Vcc 5V
16	RX2+	16	G1	4	GND
17	RXCLK-	17	G2	5	Vcc 12V
18	RXCLK+	18	G3	CN5: loop through	
19	RX3-	19	G4	pin	signal
20	RX3+	20	G5	1	OPT1
CN2: Power Input		21	GND	2	OPT2
pin	signal	22	B0	3	OPT3
1	BLEN	23	B1	4	OPT4
2	BRT	24	B2		
3	Vcc 5V	25	B3		
4	Vcc 5V	26	B4		
5	GND	27	B5		
6	GND	28	GND		
7	GND	29	ENAB		
8	Vcc 12V	30	Vcc		
9	Vcc 12V	31	Vcc		
10	Vcc 12V	32	R/L		
		33	U/D		

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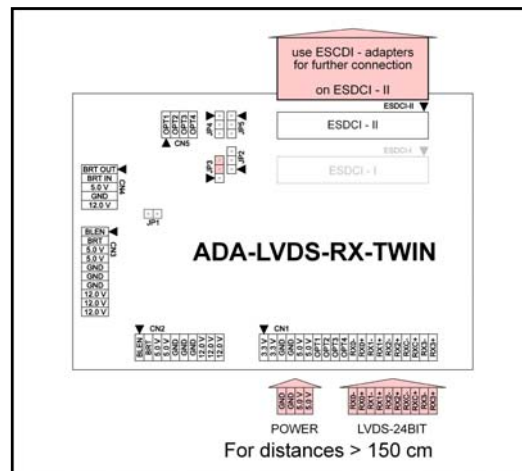
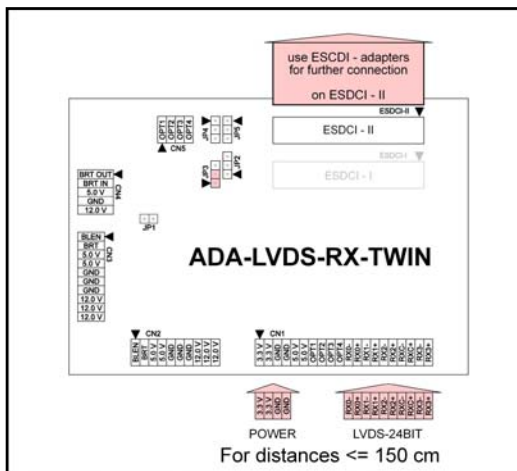
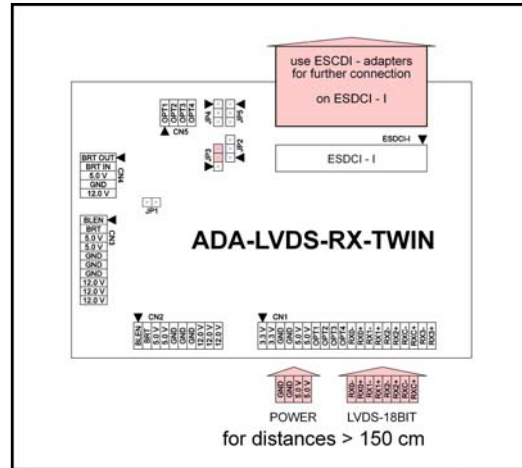
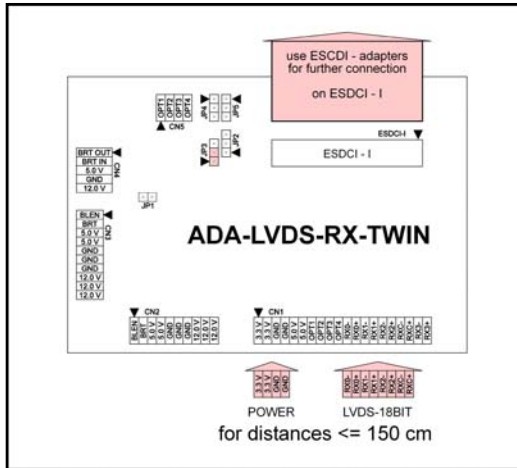
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A. connection diagram's



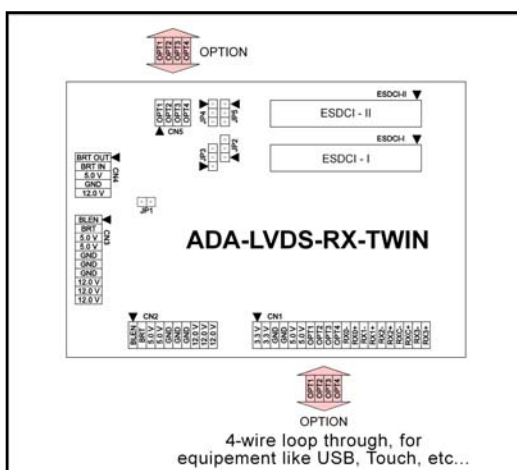
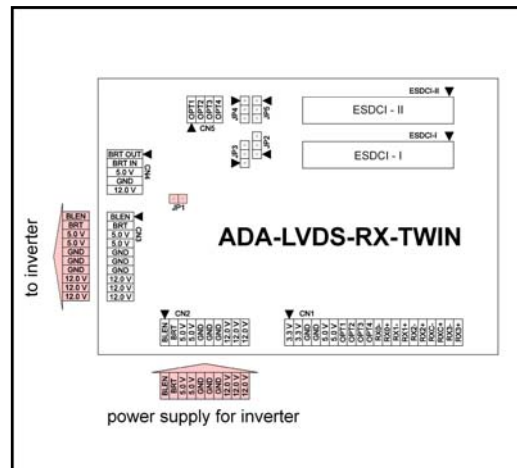
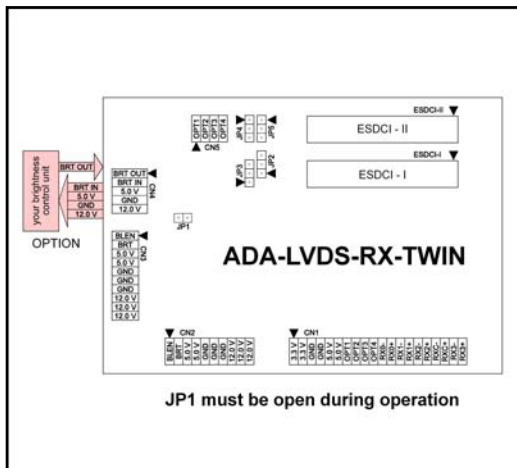
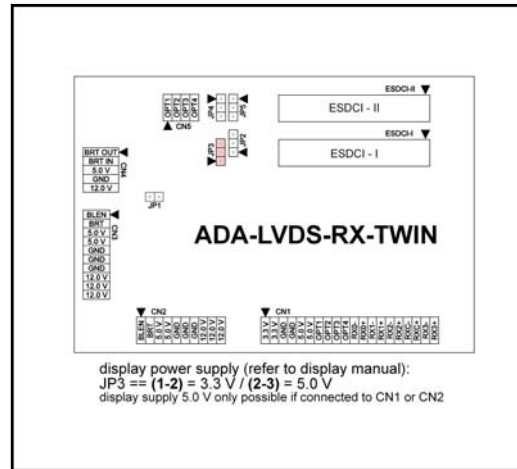
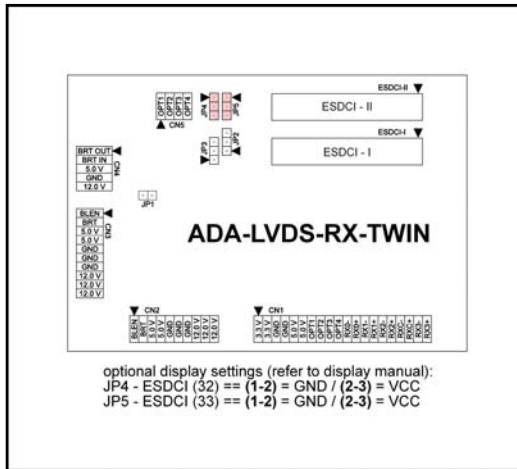
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B. jumper settings

ADA-LVDS-RX-TWIN configuration settings	
JP1	BRT-control
1-2 closed	external via CN5
1-2 open	loop through CN3/CN4
JP2	DISPLAY Vcc
1-2 closed	Vcc 3.3 V
2-3 closed	Vcc 5.0 V
JP3	LVDS Vcc source
1-2 closed	external 3.3 V via CN1
2-3 closed	generated 3.3 V on board
JP4	option pin 31
1-2 closed	GND
2-3 closed	Vcc
JP5	option pin 30
1-2 closed	GND
2-3 closed	Vcc

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