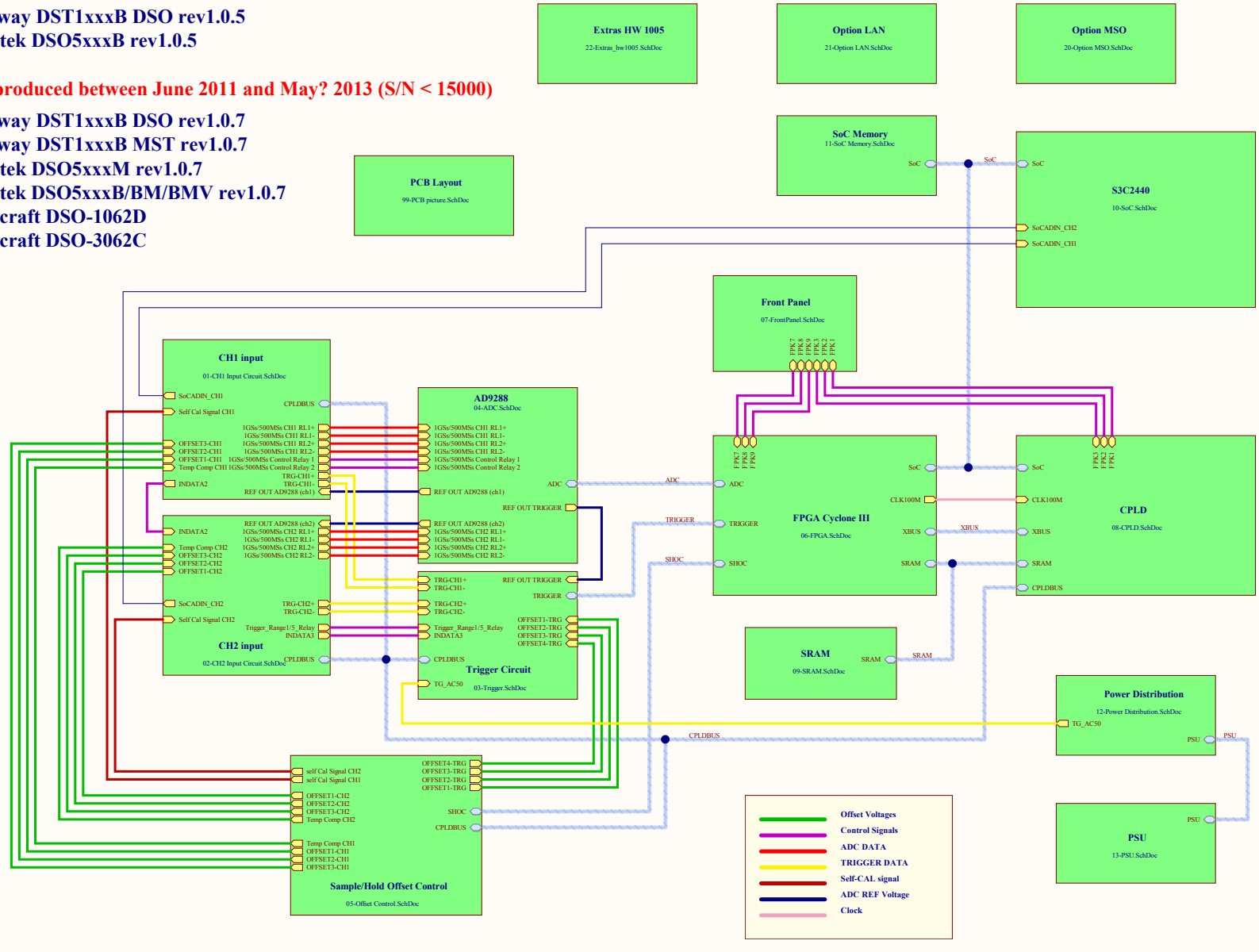
DSOs produced between Feb 2011 and June 2011

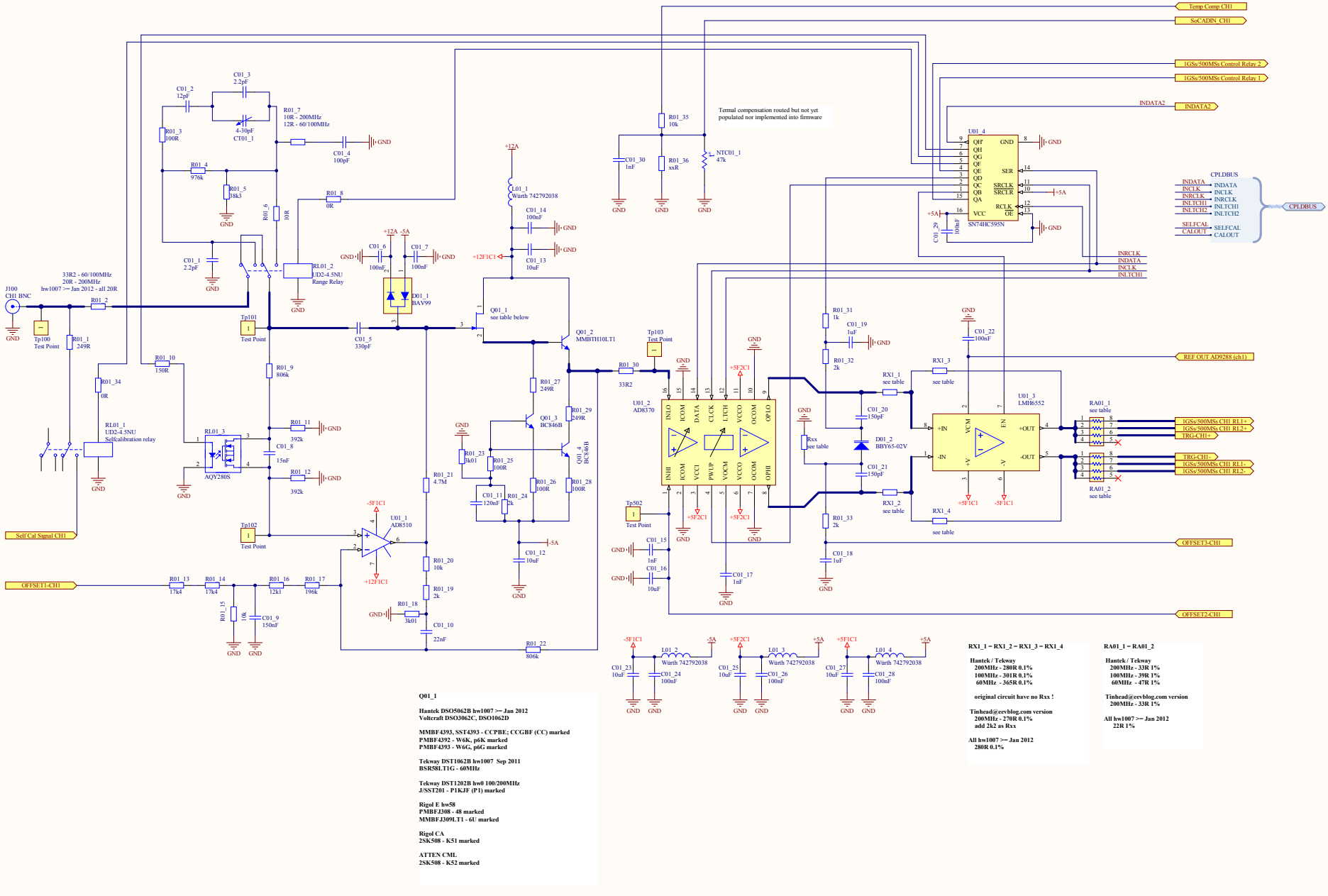
- Tekway DST1xxxB DSO rev1.0.5
- Hantek DSO5xxxB rev1.0.5

DSOs produced between June 2011 and May? 2013 (S/N < 15000)

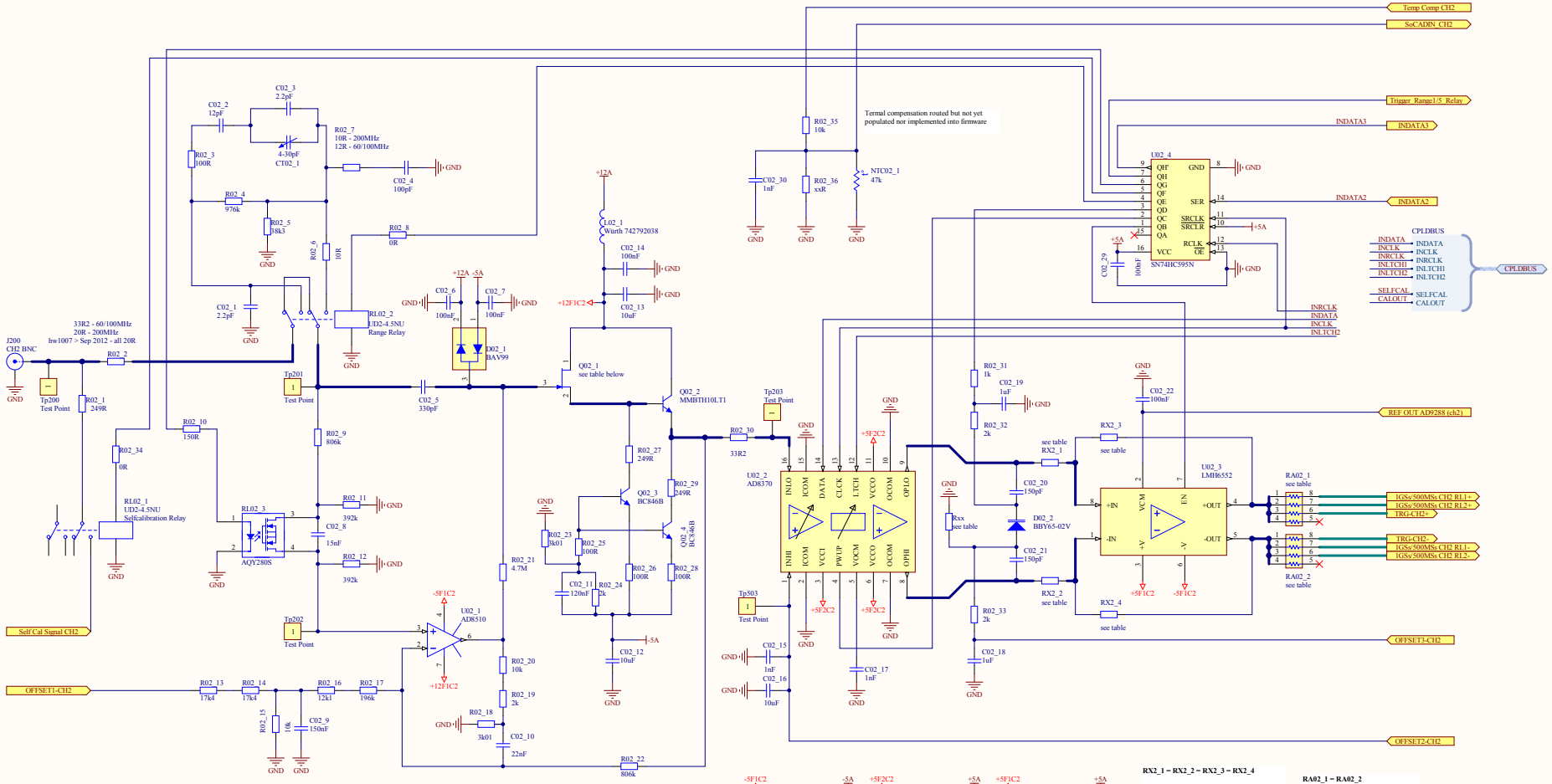
- Tekway DST1xxxB DSO rev1.0.7
- Tekway DST1xxxB MST rev1.0.7
- Hantek DSO5xxxM rev1.0.7
- Hantek DSO5xxxB/BM/BMV rev1.0.7
- Voltcraft DSO-1062D
- Voltcraft DSO-3062C



CH1 Input Circuit



CH2 Input Circuit



Q02_1

Hantek DSO5062B hw1007 >= Jan 2012
Volteraft DSO3062C, DSO1062D

MMBF4393, SST4393 - CCPBE; CCGBF (CC) marked
PMBF4392 - W6K, p6K marked
PMBF4393 - W6G, p6G marked

Tekway DST1062B hw1007 Sep 2011
BSR58LT1G - 60MHz

Tekway DST1202B hw0 100/200MHz
J/SST201 - P1KJF (P1) marked

Rigol E hw58
PMBFJ308 - 48 marked
MMBFJ309LT1 - 6U marked

Rigol CA
2SK508 - K51 marked

ATTEN CML
2SK508 - K52 marked

RX2_1 = RX2_2 = RX2_3 = RX2_4

Hantek / Tekway
200MHz - 280R 0.1%
100MHz - 301R 0.1%
60MHz - 365R 0.1%

original circuit have no Rxx !

Tinhead@eevblog.com version
200MHz - 270R 0.1%
add 2k2 as Rxx

All hw1007 >= Jun 2012
280R 0.1%

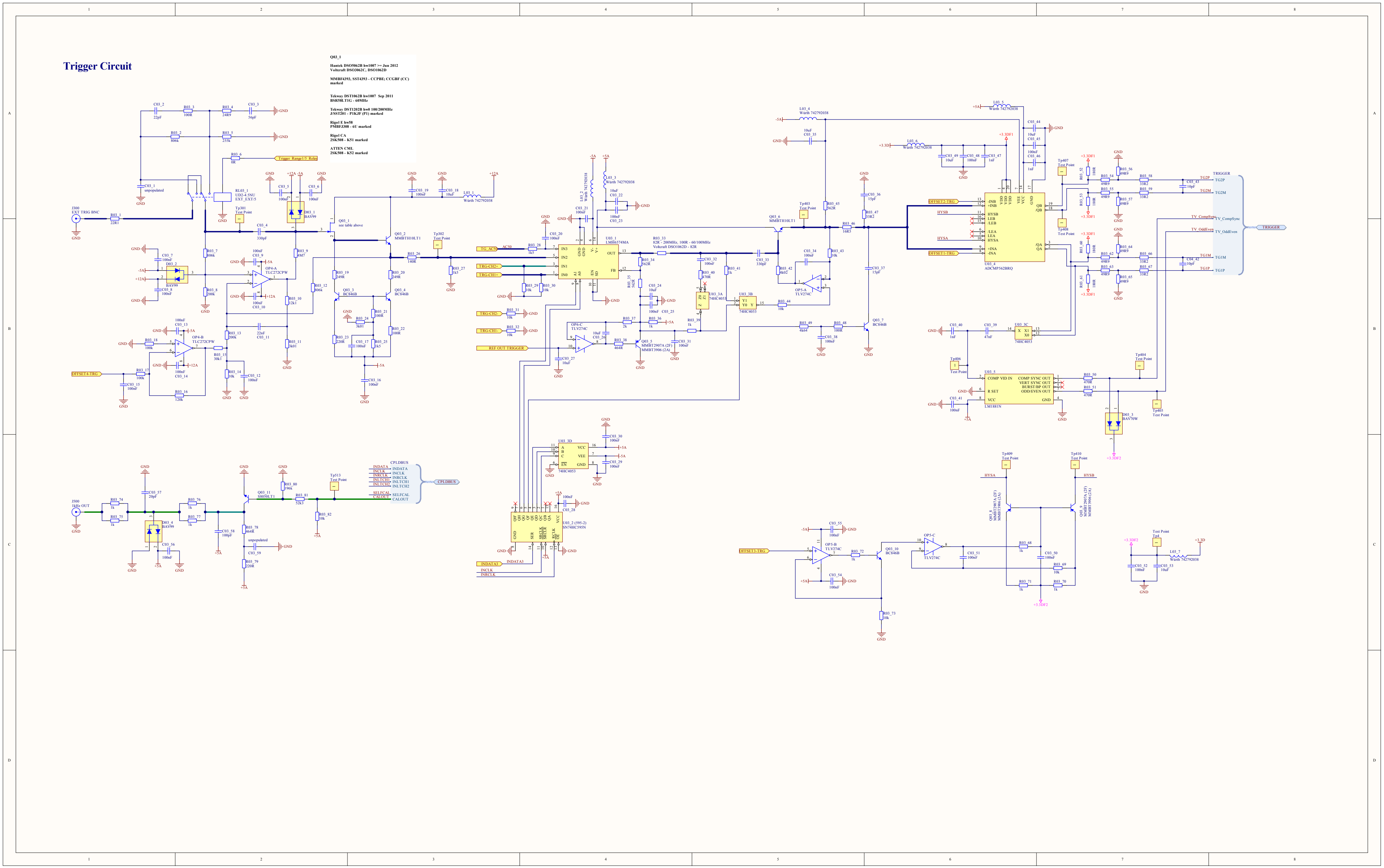
RA02_1 = RA02_2

Hantek / Tekway
200MHz - 33R 1%
100MHz - 39R 1%
60MHz - 47R 1%

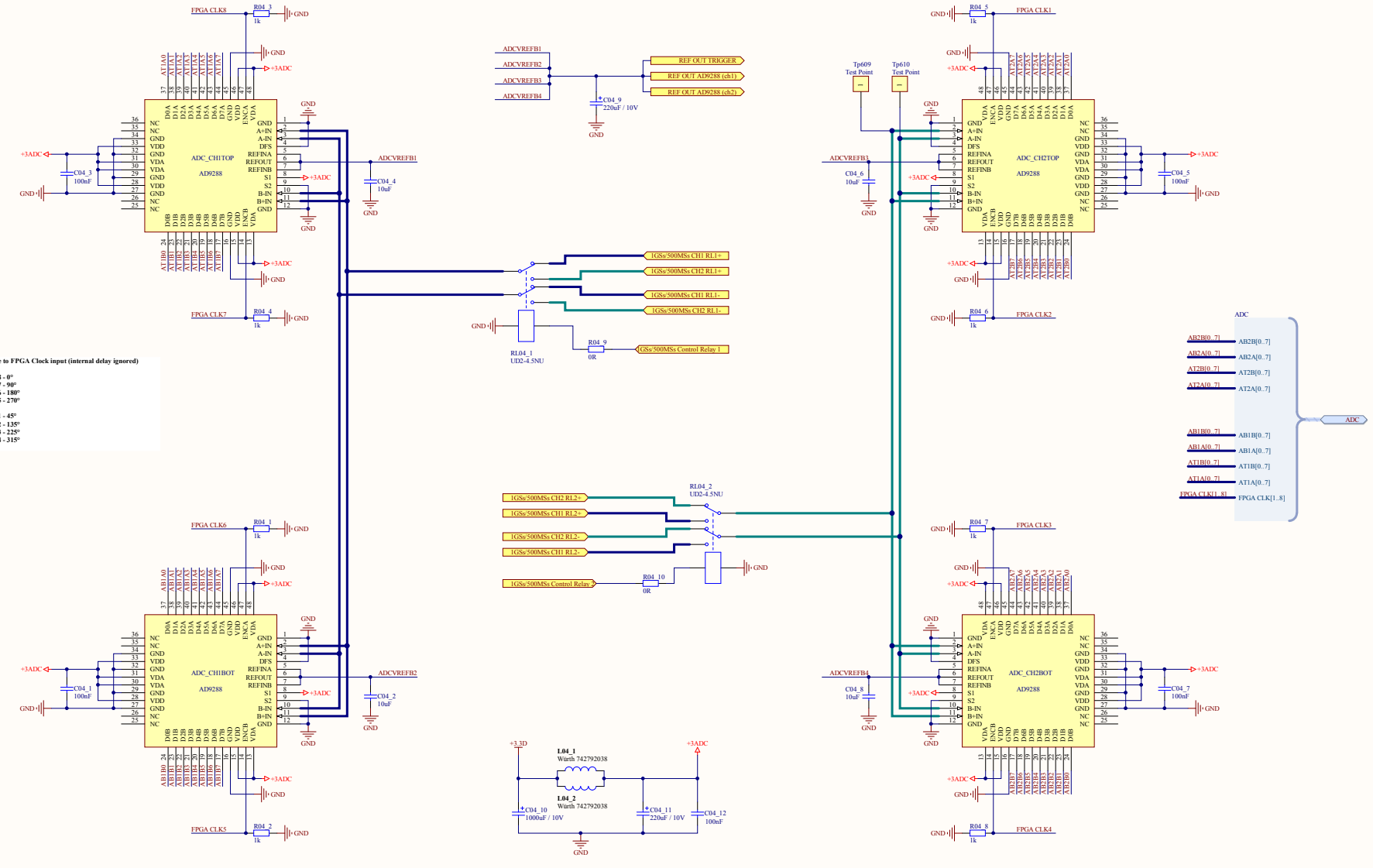
Tinhead@eevblog.com version
200MHz - 33R 1%

All hw1007 >= Jun 2012
22R 1%

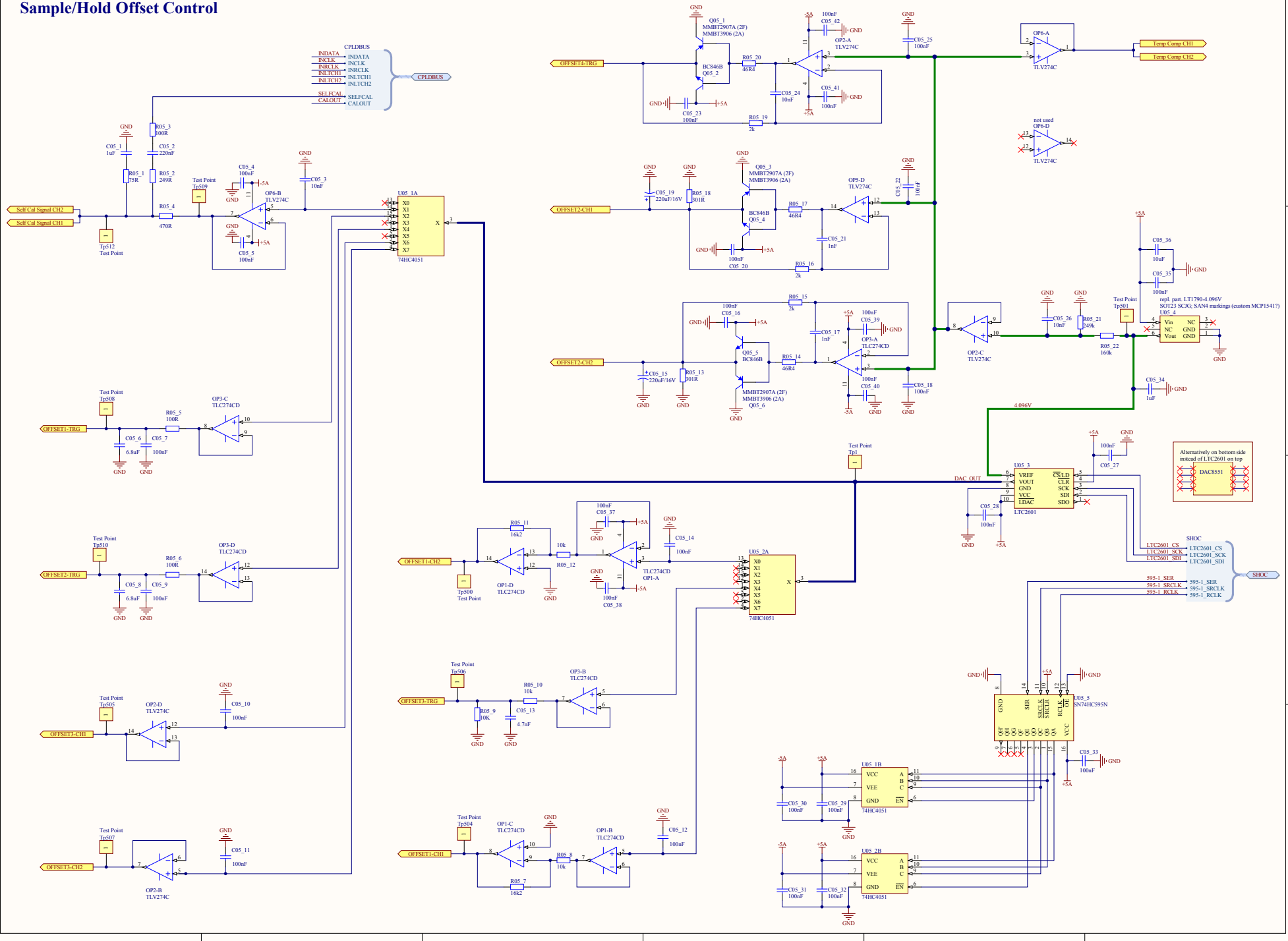
Trigger Circuit



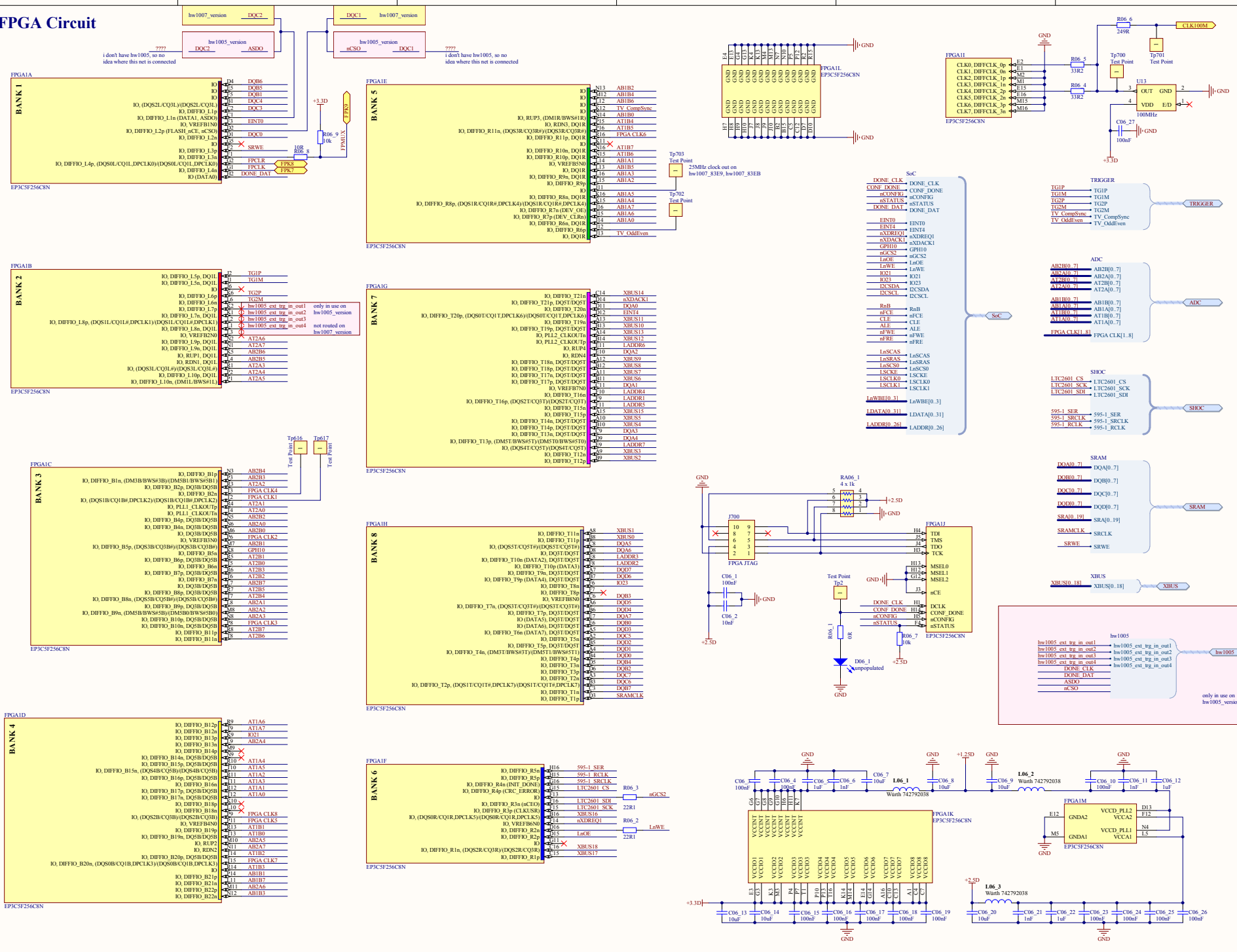
ADC Circuit


Clocks relative to FPGA Clock input (internal delay ignored)
FPGA Clock 8 - 0°
FPGA Clock 7 - 90°
FPGA Clock 6 - 180°
FPGA Clock 5 - 270°
FPGA Clock 1 - 45°
FPGA Clock 2 - 135°
FPGA Clock 3 - 225°
FPGA Clock 4 - 315°
ADC_CH1TOP
ADC_CH1BOT
ADC_CH2TOP
ADC_CH2BOT
AD9288
ADCVREFB1
ADCVREFB2
ADCVREFB3
ADCVREFB4
REF OUT TRIGGER
REF OUT AD9288 (ch1)
REF OUT AD9288 (ch2)
1GSs/500MSs CH1 RL1+
1GSs/500MSs CH2 RL1+
1GSs/500MSs CH1 RL1-
1GSs/500MSs CH2 RL1-
1GSs/500MSs Control Relay 1
1GSs/500MSs CH2 RL2+
1GSs/500MSs CH1 RL2+
1GSs/500MSs CH2 RL2-
1GSs/500MSs CH1 RL2-
1GSs/500MSs Control Relay 2
RL04_1 UD2-4.5NU
RL04_2 UD2-4.5NU
L04_1 Würth 742792038
L04_2 Würth 742792038
Tp609 Test Point
Tp610 Test Point
ADC

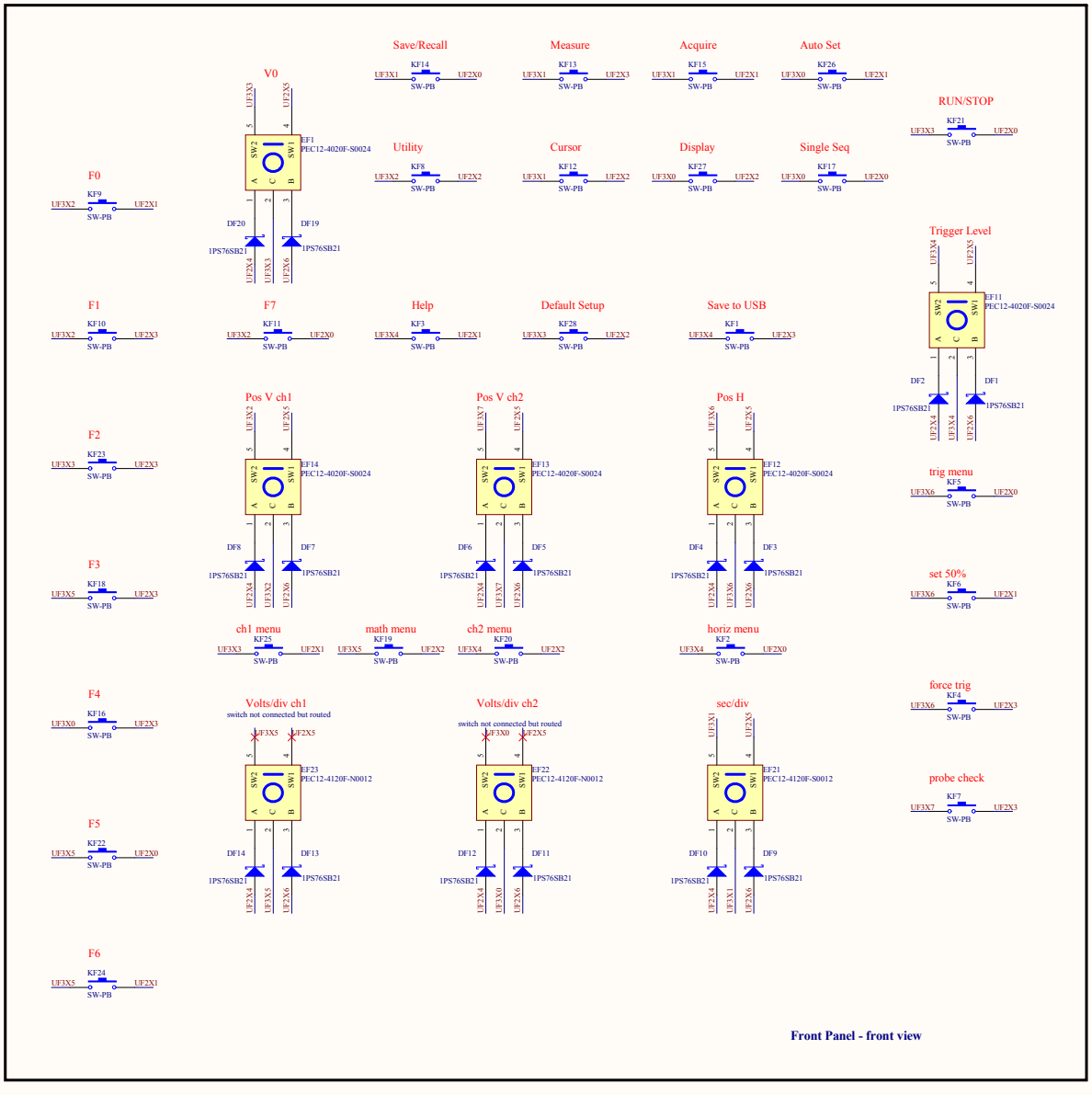
Sample/Hold Offset Control

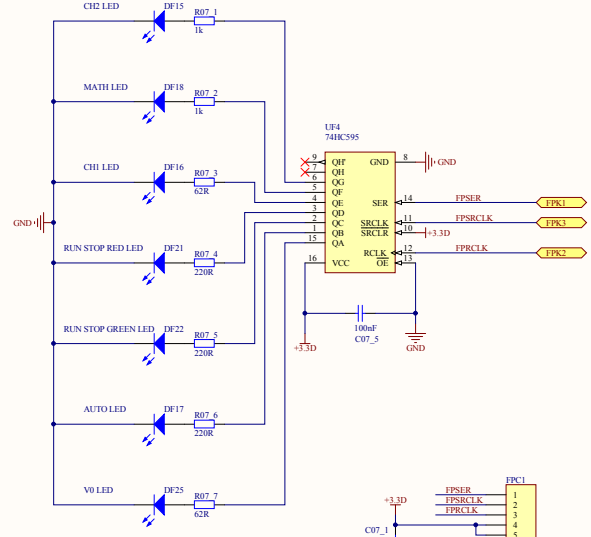


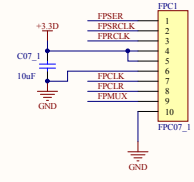
FPGA Circuit

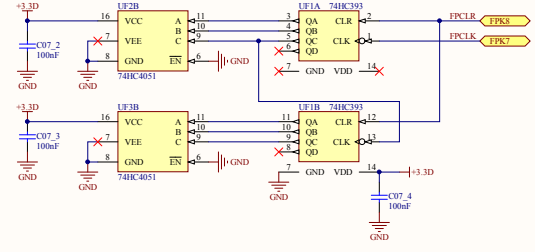


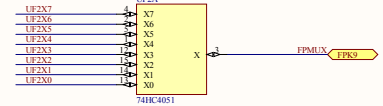
Front Panel Circuit

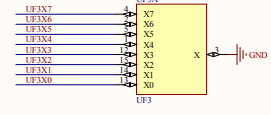




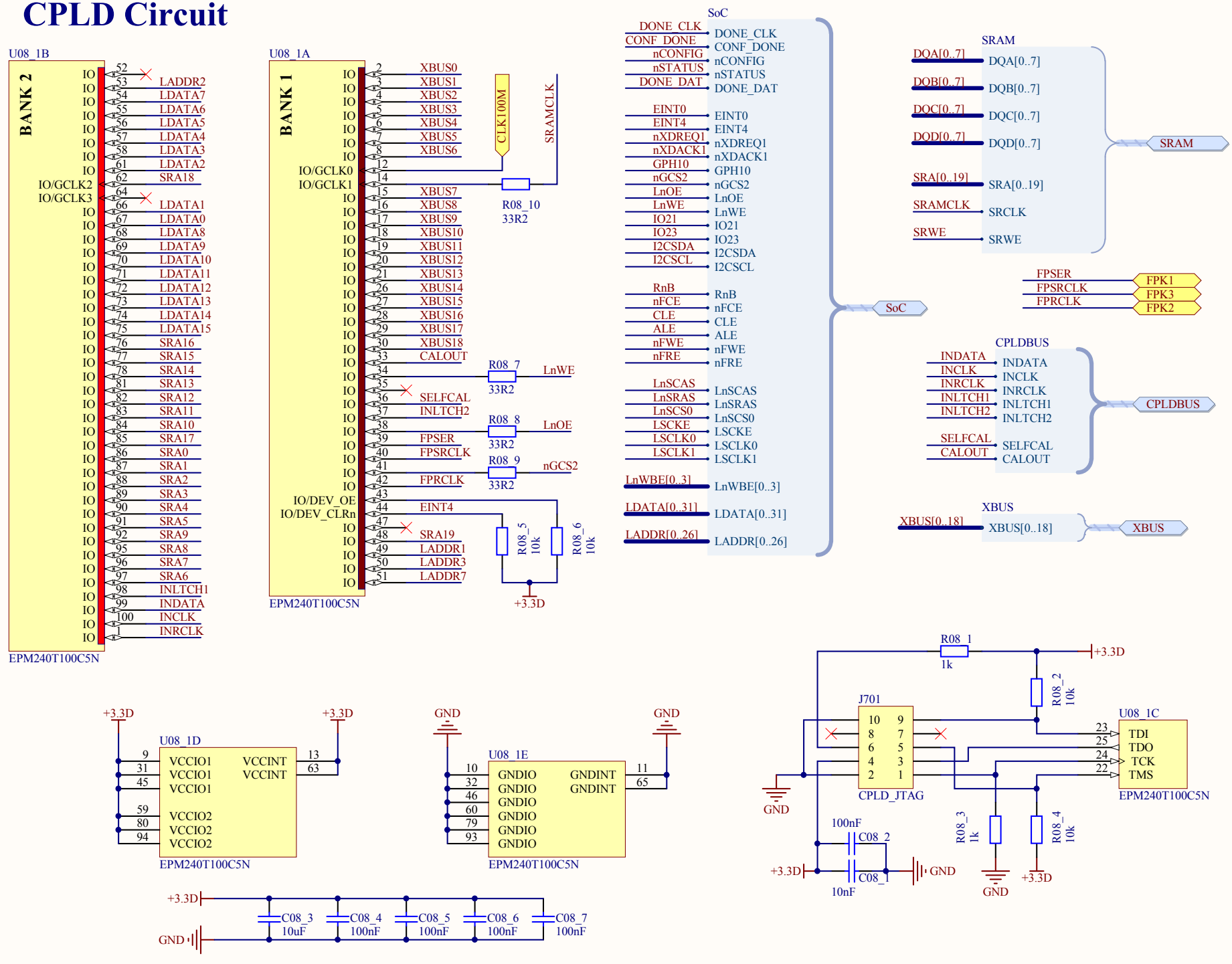




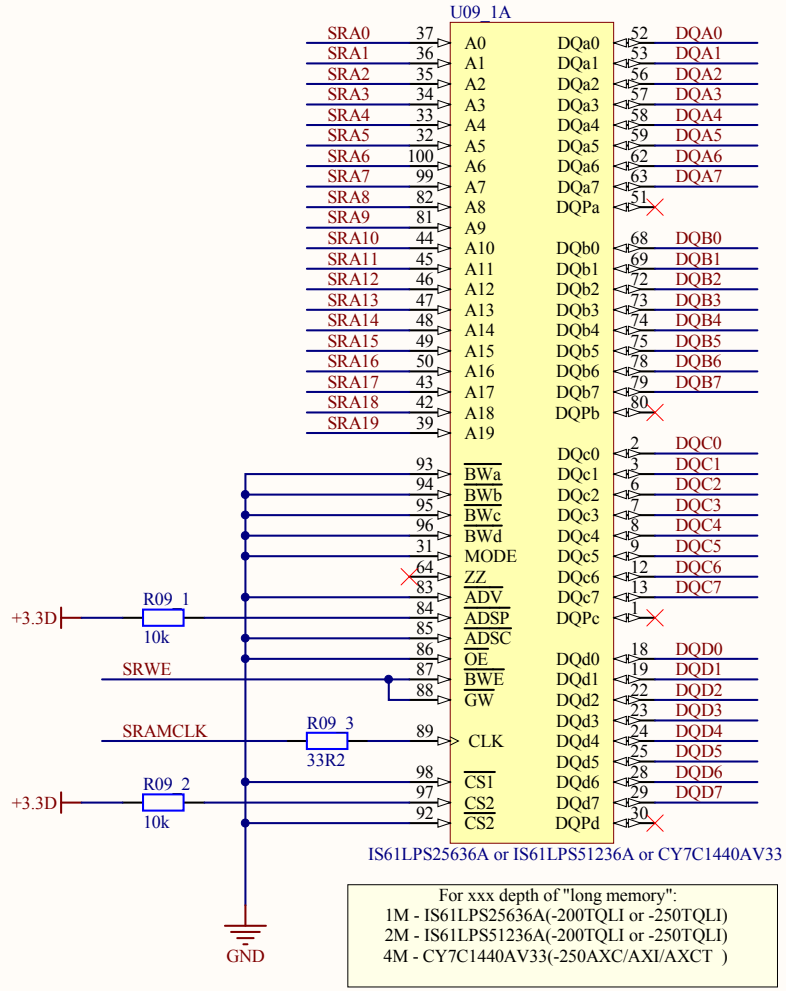


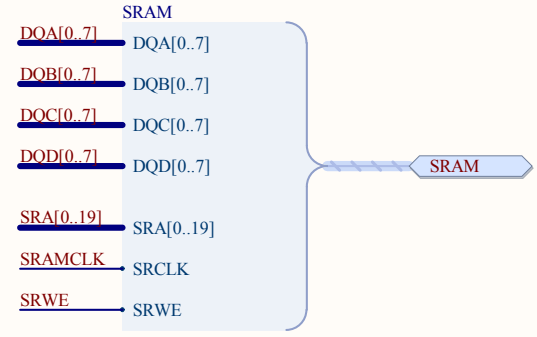


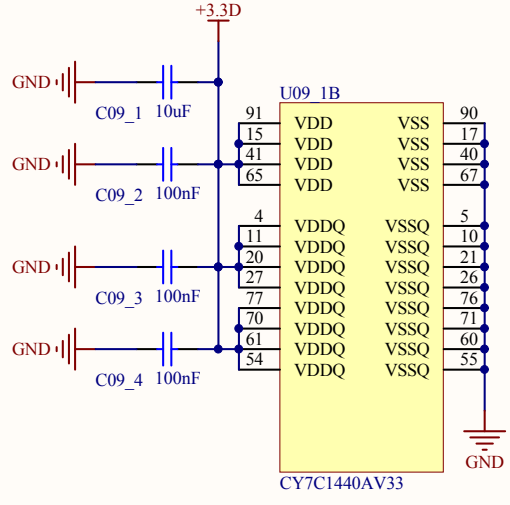
CPLD Circuit

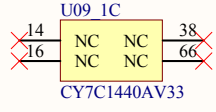


SRAM Circuit

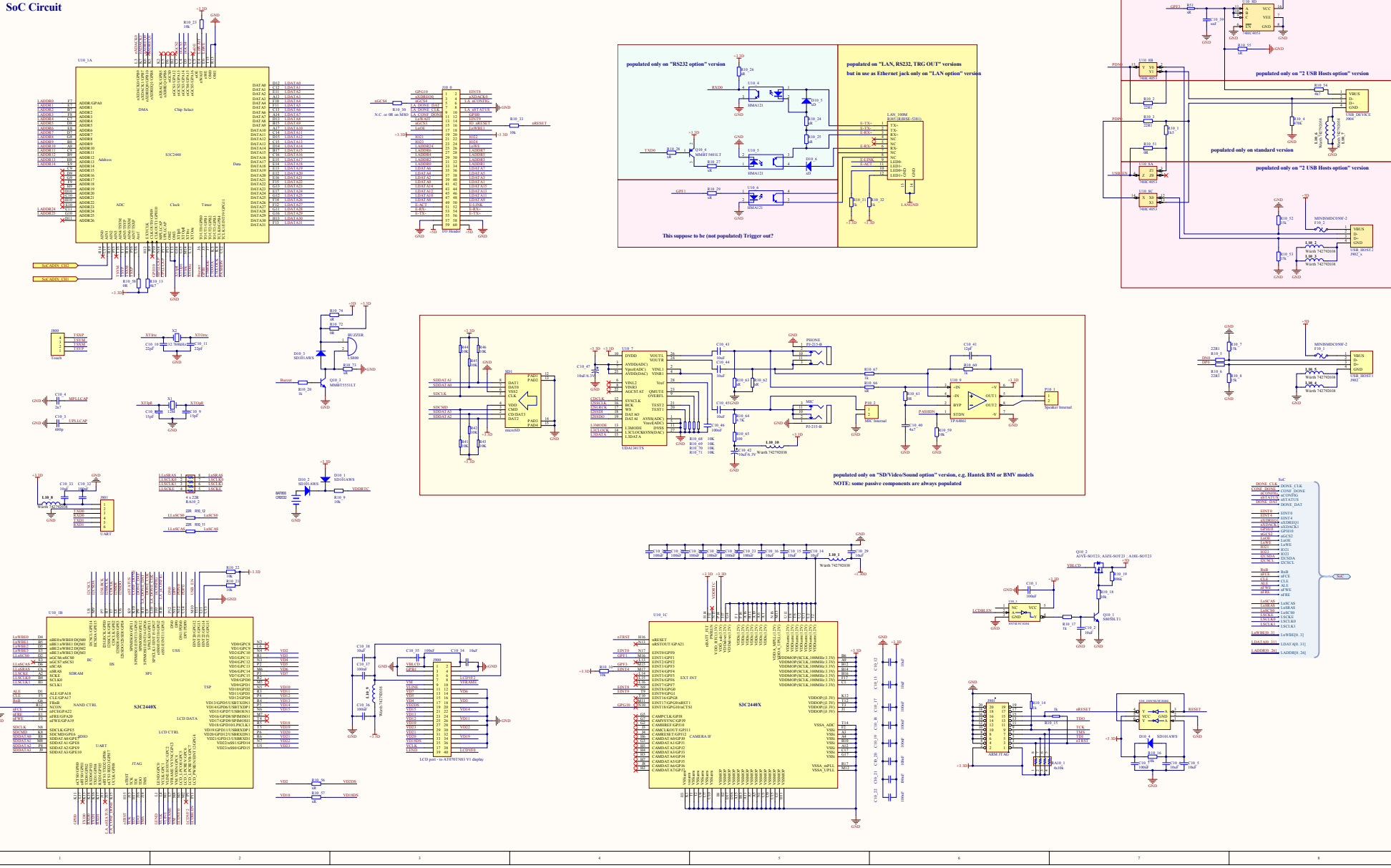




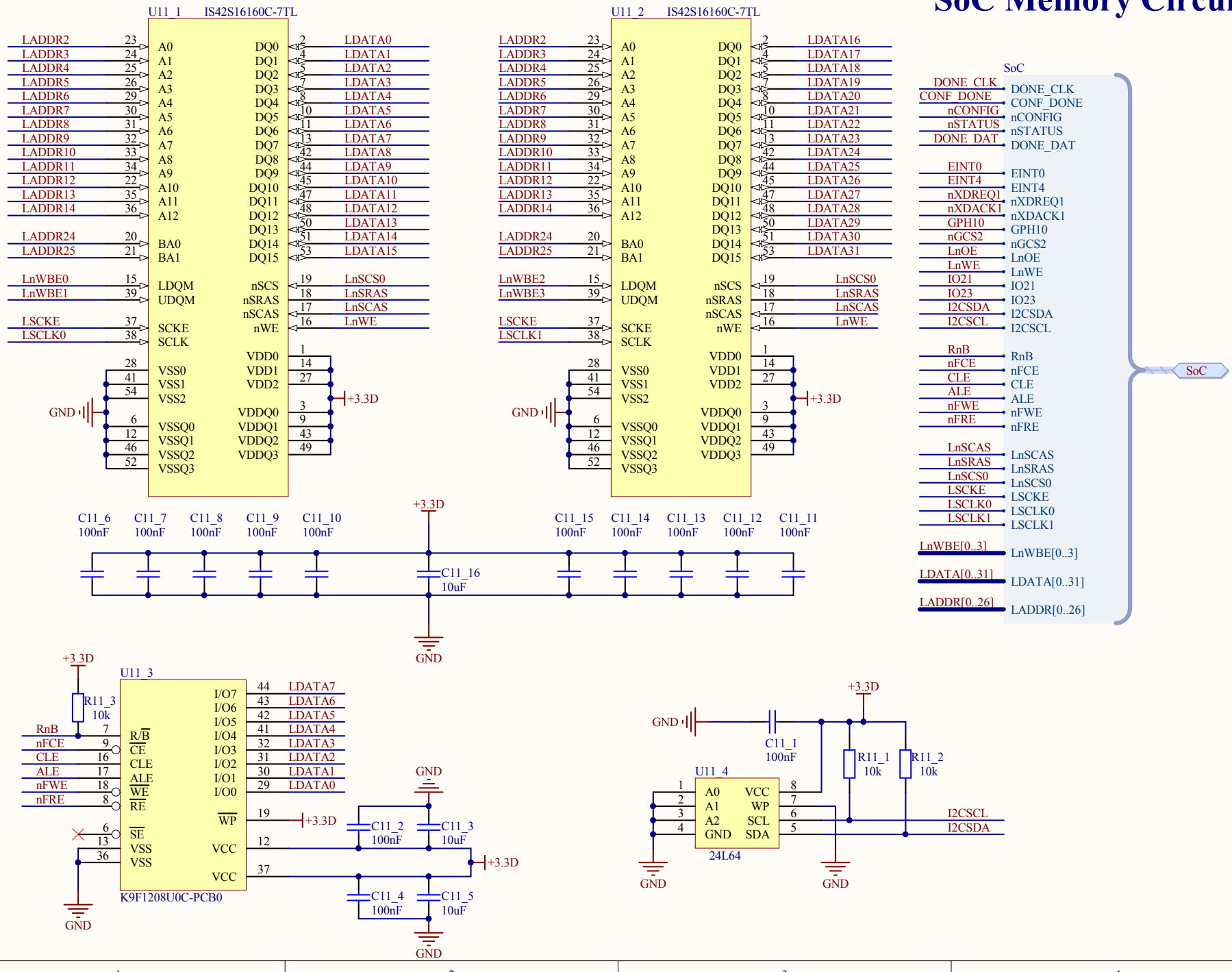




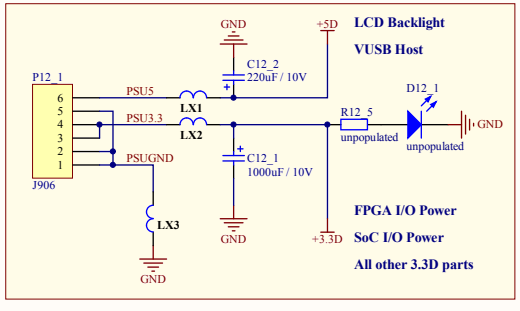
SoC Circuit

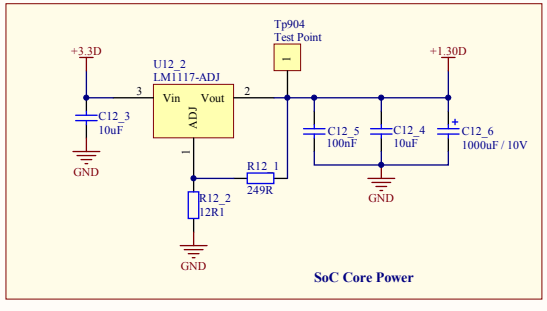

populated only on "RS232 option" version
populated on "LAN, RS232, TRG OUT" versions
but in use as Ethernet jack only on "LAN option" version
This suppose to be (not populated) Trigger out?
populated only on "2 USB Hosts option" version
populated only on standard version
populated only on "2 USB Hosts option" version
populated only on "SD/Video/Sound option" version, e.g. Hantek BM or BMV models
NOTE: some passive components are always populated
S3C2440X
S3C2440A
SoC

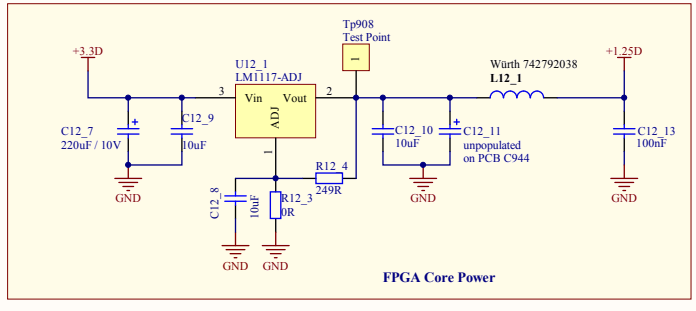
SoC Memory Circuit

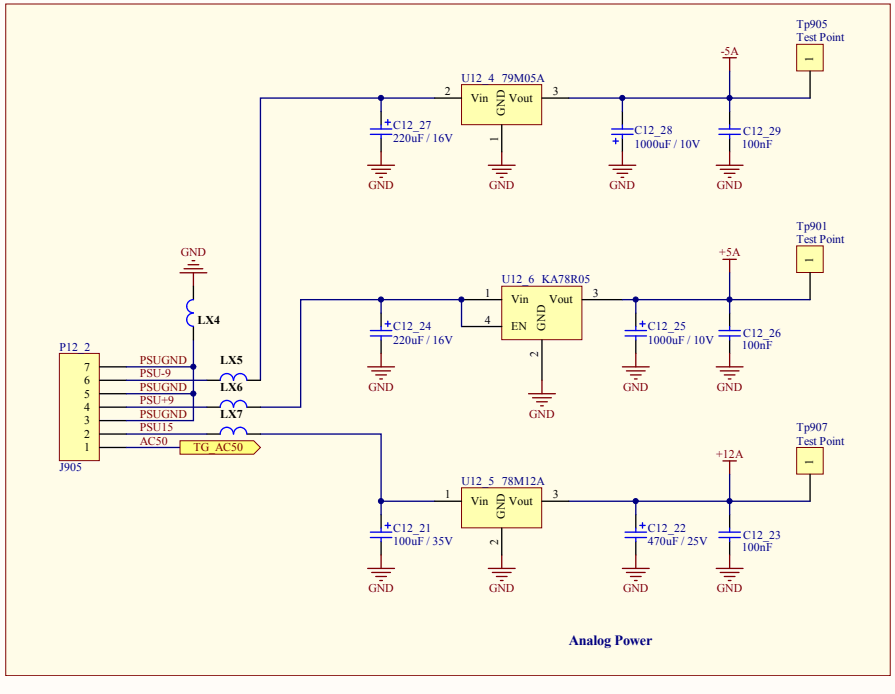


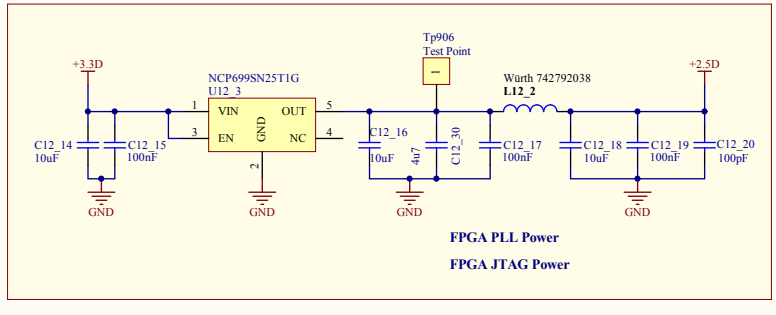
Power Distribution Circuit

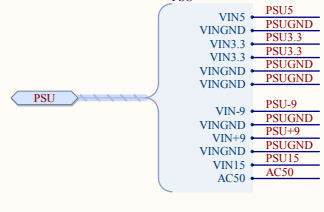




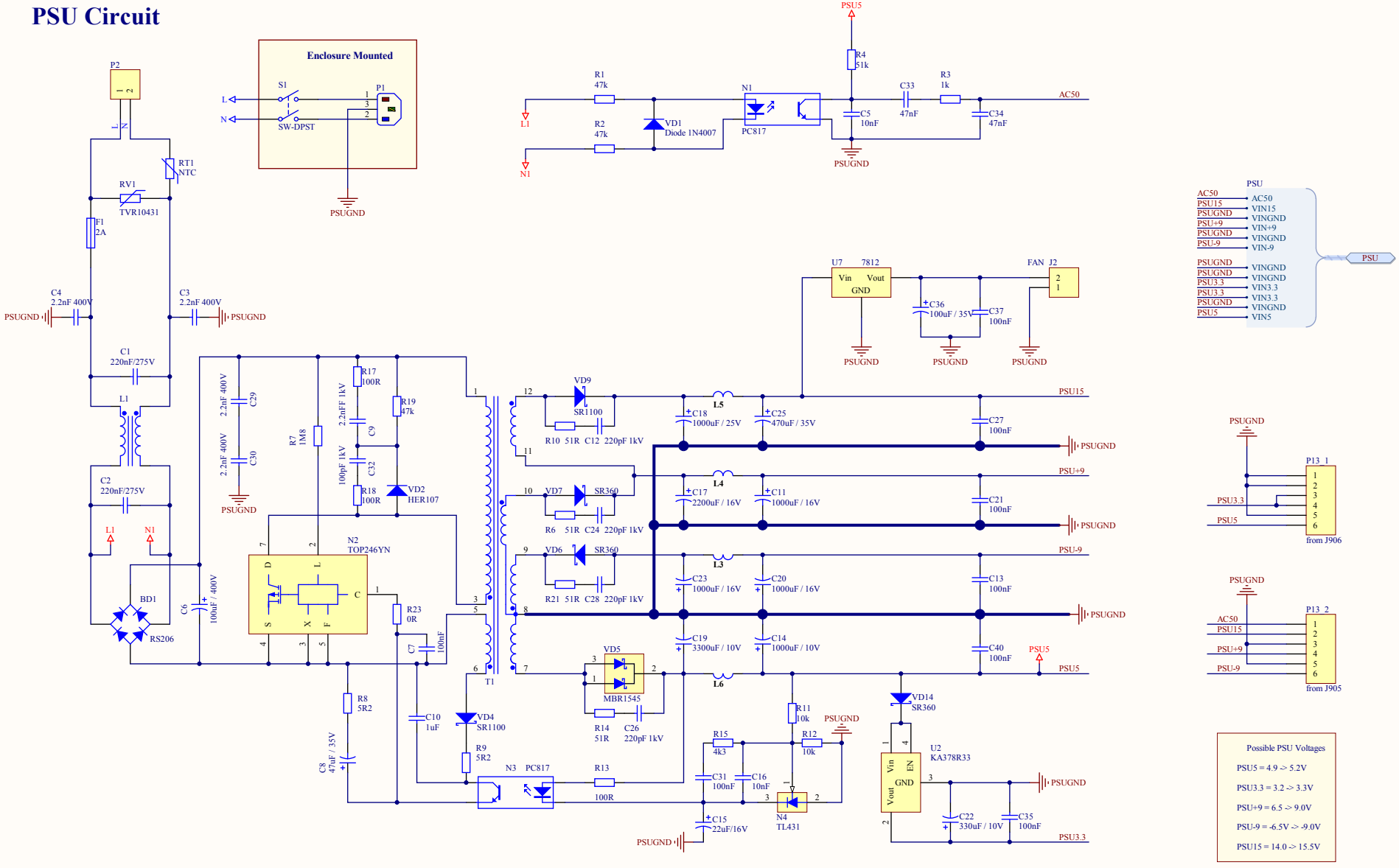


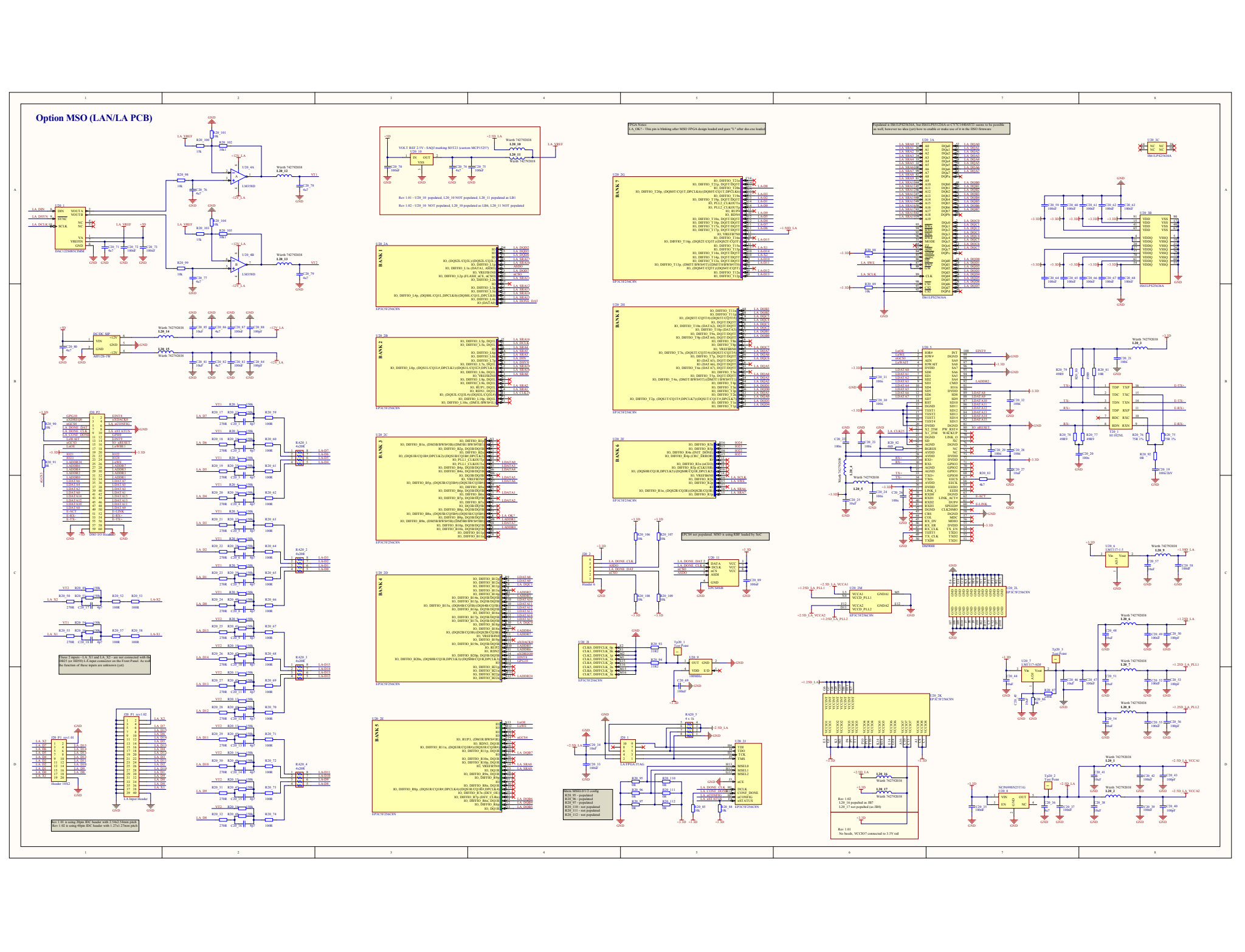




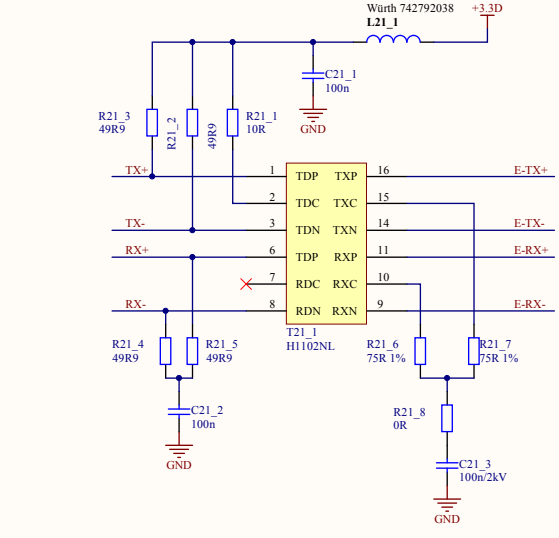


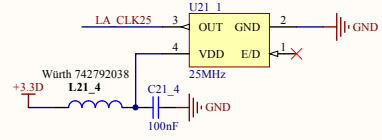
PSU Circuit

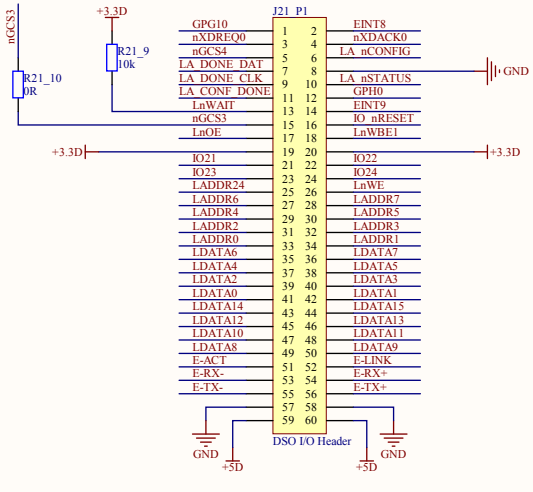

Enclosure Mounted
P2
S1
SW-DPST
P1
PSUGND
RT1
NTC
RV1
TVR10431
F1
2A
C4
2.2nF 400V
C3
2.2nF 400V
C1
220nF/275V
C2
220nF/275V
L1
N1
BD1
RS206
C6
100uF / 400V
C29
C30
R7
1M8
R17
100R
R18
100R
R19
47k
C9
C32
VD2
HER107
N2
TOP246YN
R23
0R
C7
100nF
R8
5R2
C8
47uF / 35V
C10
1uF
VD4
SR1100
R9
5R2
T1
R1
47k
R2
47k
VD1
Diode 1N4007
N1
PC817
R4
51k
C33
47nF
R3
1k
C5
10nF
C34
47nF
AC50
PSU5
U7
7812
Vin
Vout
GND
C36
100uF / 35V
C37
100nF
FAN
J2
VD9
SR1100
R10 51R C12 220pF 1kV
VD7
SR360
R6 51R C24 220pF 1kV
VD6
SR360
R21 51R C28 220pF 1kV
VD5
MBR1545
R14
51R
C26
220pF 1kV
L5
L4
L3
L6
C18
1000uF / 25V
C25
470uF / 35V
C17
2200uF / 16V
C11
1000uF / 16V
C23
1000uF / 16V
C20
1000uF / 16V
C19
3300uF / 10V
C14
1000uF / 10V
C27
100nF
C21
100nF
C13
100nF
C40
100nF
PSU15
PSU+9
PSU-9
PSU5
R11
10k
R12
10k
R15
4k3
C31
100nF
C16
10nF
N3
PC817
R13
100R
N4
TL431
C15
22uF/16V
VD14
SR360
U2
KA378R33
Vin
EN
GND
Vout
C22
330uF / 10V
C35
100nF
PSU3.3
PSU
AC50
PSU15
PSUGND
PSU+9
PSUGND
PSU-9
PSUGND
PSUGND
PSU3.3
PSU3.3
PSUGND
PSU5
VIN15
VINGND
VIN+9
VINGND
VIN-9
VINGND
VINGND
VIN3.3
VIN3.3
VINGND
VIN5
P13_1
from J906
P13_2
from J905
Possible PSU Voltages
PSU5 = 4.9 -> 5.2V
PSU3.3 = 3.2 -> 3.3V
PSU+9 = 6.5 -> 9.0V
PSU-9 = -6.5V -> -9.0V
PSU15 = 14.0 -> 15.5V

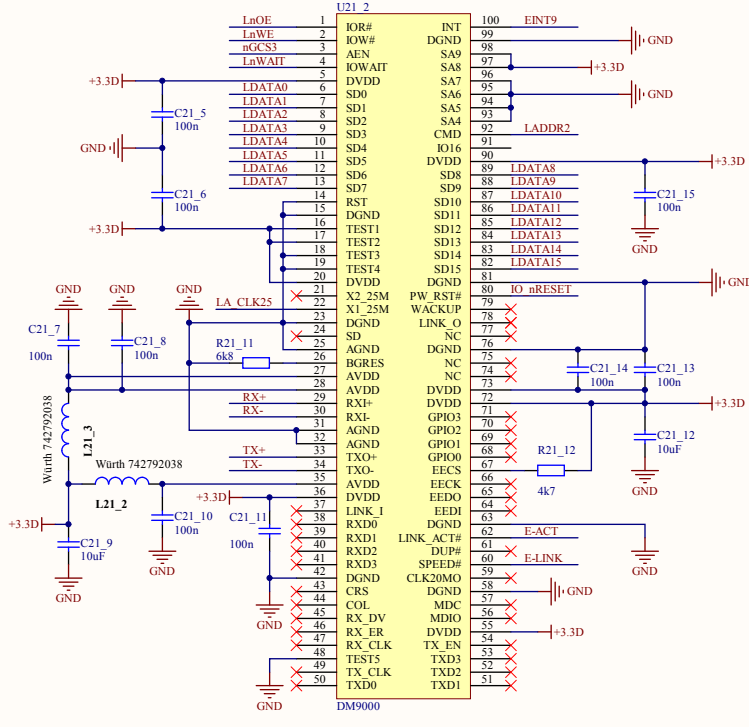

Option MSO (LAN/LA PCB)
FPGA Notes:
LA_OK? - This pin is blinking after MSO FPGA design loaded and goes "L" after dso.exe loaded
Populated in IS61LPS25616A, but IS61LPS51236A or CY7C1440AV33 seems to be possible as well, however no idea (yet) how to enable or make use of it in the DSO firmware
VOLT REF 2.5V - SAQ/ marking SOT23 (custom MCP1525?)
Rev 1.01 - U20_10 populated, L20_10 NOT populated, L20_11 populated as LB1
Rev 1.02 - U20_10 NOT populated, L20_10 populated as LB6, L20_11 NOT populated
PCS9 not populated. MSO is using RBF loaded by SoC
Header 8
Header 10X2
LA Input Header
Rev 1.01 is using 20pin IDC header with 2.54x2.54mm pitch
Rev 1.02 is using 40pin IDC header with 1.27x1.27mm pitch
Rev 1.02
L20_16 populated as JB7
L20_17 not populated (as JB8)
Rev 1.01
No beads, VCCIO7 connected to 3.3V rail
Micro MSO 8/32 config
R20_95 - populated
R20_96 - populated
R20_97 - not populated
R20_110 - not populated
R20_111 - not populated
R20_112 - not populated

Option LAN

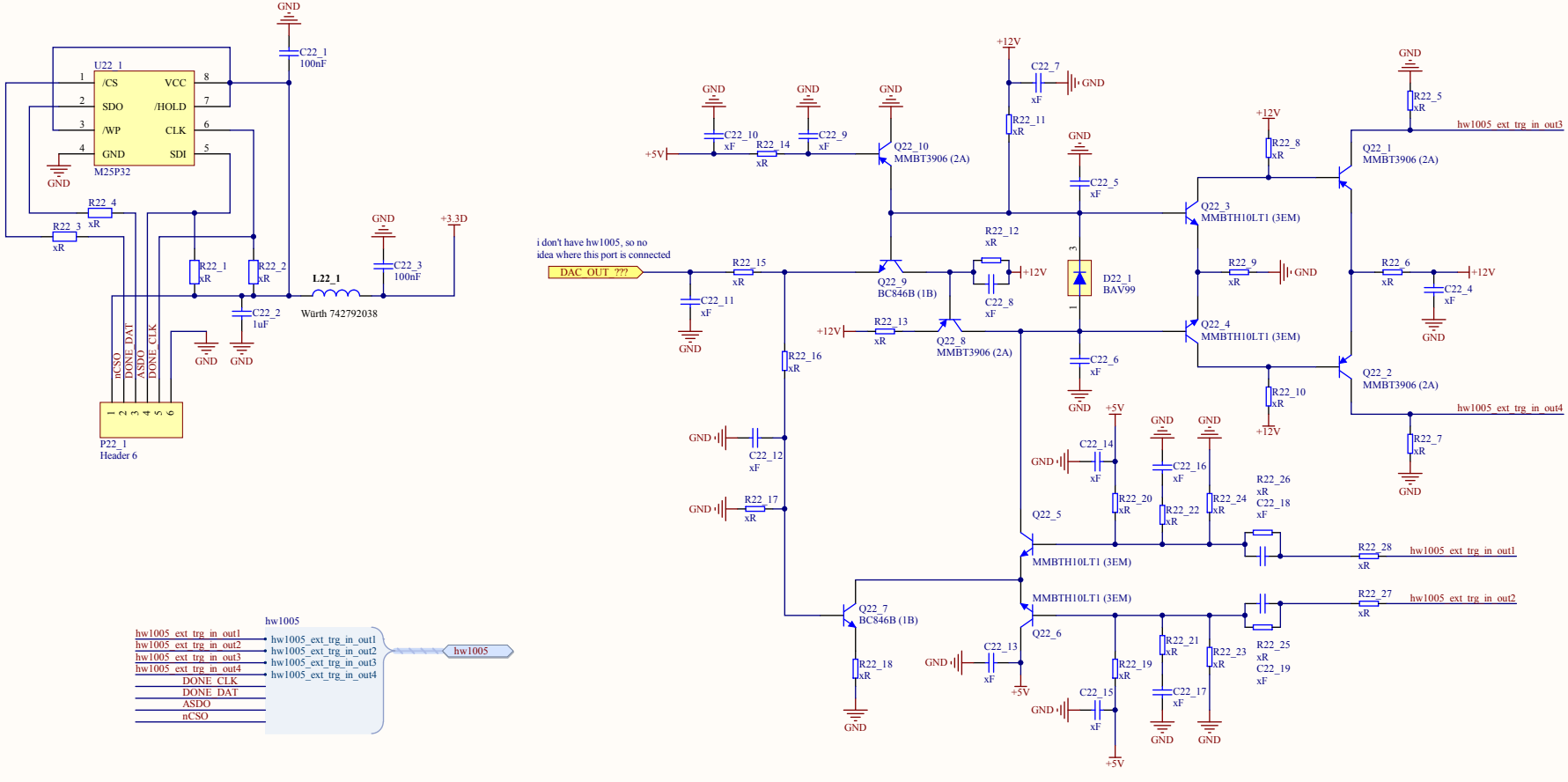

Würth 742792038
L21_1
+3.3D
C21_1
100n
GND
R21_3
49R9
R21_2
49R9
R21_1
10R
TX+
TX-
RX+
RX-
TDP TXP
TDC TXC
TDN TXN
TDP RXP
RDC RXC
RDN RXN
E-TX+
E-TX-
E-RX+
E-RX-
T21_1
H1102NL
R21_4
49R9
R21_5
49R9
R21_6
75R 1%
R21_7
75R 1%
C21_2
100n
R21_8
0R
C21_3
100n/2kV


U21_1
LA_CLK25
OUT GND
VDD E/D
25MHz
GND
Würth 742792038
L21_4
+3.3D
C21_4
100nF


J21_P1
nGCS3
+3.3D
R21_9
10k
R21_10
0R
GPG10
nXDREQ0
nGCS4
LA_DONE_DAT
LA_DONE_CLK
LA_CONF_DONE
LnWAIT
nGCS3
LnOE
IO21
IO23
LADDR24
LADDR6
LADDR4
LADDR2
LADDR0
LDATA6
LDATA4
LDATA2
LDATA0
LDATA14
LDATA12
LDATA10
LDATA8
E-ACT
E-RX-
E-TX-
EINT8
nXDACK0
LA_nCONFIG
LA_nSTATUS
GPH0
EINT9
IO_nRESET
LnWBE1
IO22
IO24
LnWE
LADDR7
LADDR5
LADDR3
LADDR1
LDATA7
LDATA5
LDATA3
LDATA1
LDATA15
LDATA13
LDATA11
LDATA9
E-LINK
E-RX+
E-TX+
GND
+5D
DSO I/O Header


U21_2
LnOE
LnWE
nGCS3
LnWAIT
LDATA0
LDATA1
LDATA2
LDATA3
LDATA4
LDATA5
LDATA6
LDATA7
IOR#
IOW#
AEN
IOWAIT
DVDD
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
RST
DGND
TEST1
TEST2
TEST3
TEST4
DVDD
X2_25M
X1_25M
DGND
SD
AGND
BGRES
AVDD
AVDD
AVDD
RXI+
RXI-
AGND
AGND
TXO+
TXO-
AVDD
DVDD
LINK_I
RXD0
RXD1
RXD2
RXD3
DGND
CRS
COL
RX_DV
RX_ER
RX_CLK
TEST5
TX_CLK
TXD0
INT
DGND
SA9
SA8
SA7
SA6
SA5
SA4
CMD
IO16
DVDD
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
DGND
PW_RST#
WACKUP
LINK_O
SD
NC
DGND
NC
NC
DVDD
DVDD
GPIO3
GPIO2
GPIO1
GPIO0
EECS
EECK
EEDO
EEDI
DGND
LINK_ACT#
DUP#
SPEED#
CLK20MO
DGND
MDC
MDIO
DVDD
TX_EN
TXD3
TXD2
TXD1
DM9000
EINT9
LADDR2
LDATA8
LDATA9
LDATA10
LDATA11
LDATA12
LDATA13
LDATA14
LDATA15
IO_nRESET
E-ACT
E-LINK
LA_CLK25
RX+
RX-
TX+
TX-
R21_11
6k8
R21_12
4k7
C21_5
100n
C21_6
100n
C21_7
100n
C21_8
100n
C21_9
10uF
C21_10
100n
C21_11
100n
C21_12
10uF
C21_13
100n
C21_14
100n
C21_15
100n
Würth 742792038
L21_3
Würth 742792038
L21_2
+3.3D
GND

hw1005 extra circuits



all these parts on this sheet are not populated, but i reversed the circuit from pictures and "restored" their function