KS0093

26 COM / 80 SEG DRIVER & CONTROLLER FOR STN LCD

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Ver. 0.4

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KS0093 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Jun.1998
0.1	Miss typed contents changed	Jan.1999
0.2	RESETB pin V_{IL},V_{IH} added	Mar.1999
0.3	VDD change (2.4V~5.5V -> 2.4V~3.6V)	Nov.1999
0.4	VDD change (2.4V~3.6V -> 2.4V~5.5V)	Dec.1999

CONTENTS

INTRODUCTION

The KS0093 is an LCD driver and controller LSI for liquid crystal dot matrix character display systems. It can display 2 or 3 lines of 16 characters with 5 x 8 dots format. It is capable of interfacing various microprocessors, supporting the 4-bit, 8-bit parallel modes and the clock synchronized serial mode. Voltage converter, oscillator, voltage regulator, voltage follower and bias circuit are built in the IC. The double height character mode and line vertical scroll functions are supported.

FEATURES

Driver Outputs

- Common outputs: 26 common
- Segment outputs: 80 segment

Applicable Panel Size

Font	Display	Duty	Contents of outputs
5 x 8	2-line x 16 characters	1 / 17	2 x 16 characters + 80 icons
	3-line x 16 characters	1 / 25	3 x 16 characters + 80 icons

Internal Memory

- Character Generator ROM (CGROM): 10,240 bits (256 characters x 5 x 8 dots)
- Character Generator RAM (CGRAM): 320 bits (8 characters x 5 x 8 dots)
- Display Data RAM (DDRAM): 512 bits (16 characters x 4 lines)
- Segment Icon RAM (ICONRAM): 80 bits (80 icons)

MPU Interface

- No busy MPU interface (no busy check or no execution waiting time)
- 8-bit parallel interface mode: 68-series and 80-series are available.
- 4-bit parallel interface mode: 68-series and 80-series are available.
- Serial interface mode: 4 pins clock synchronized serial interface

Function Set

- Various instruction set: display control, power save, power control, etc.
- COM / SEG bi-directional (4-type LCD application available)
- H/W reset (RESETB)

Built-in Analog Circuit

- Internal RC oscillator circuit or external clock
- Electronic volume for contrast control (32 steps)
- Voltage converter / voltage regulator / voltage follower & bias circuit

Low Power Operation

- Sleep mode operation (5μA Max.)
- Normal mode operation (80μA Max.)

Operating Voltage Range

- Power supply voltage (V_{DD}): 2.4V ~ 5.5V
- LCD driving voltage (V_{LCD} = V0 - V_{SS}): 6.0V Max.

Package Type

- Gold bumped chip or TCP

BLOCK DIAGRAM

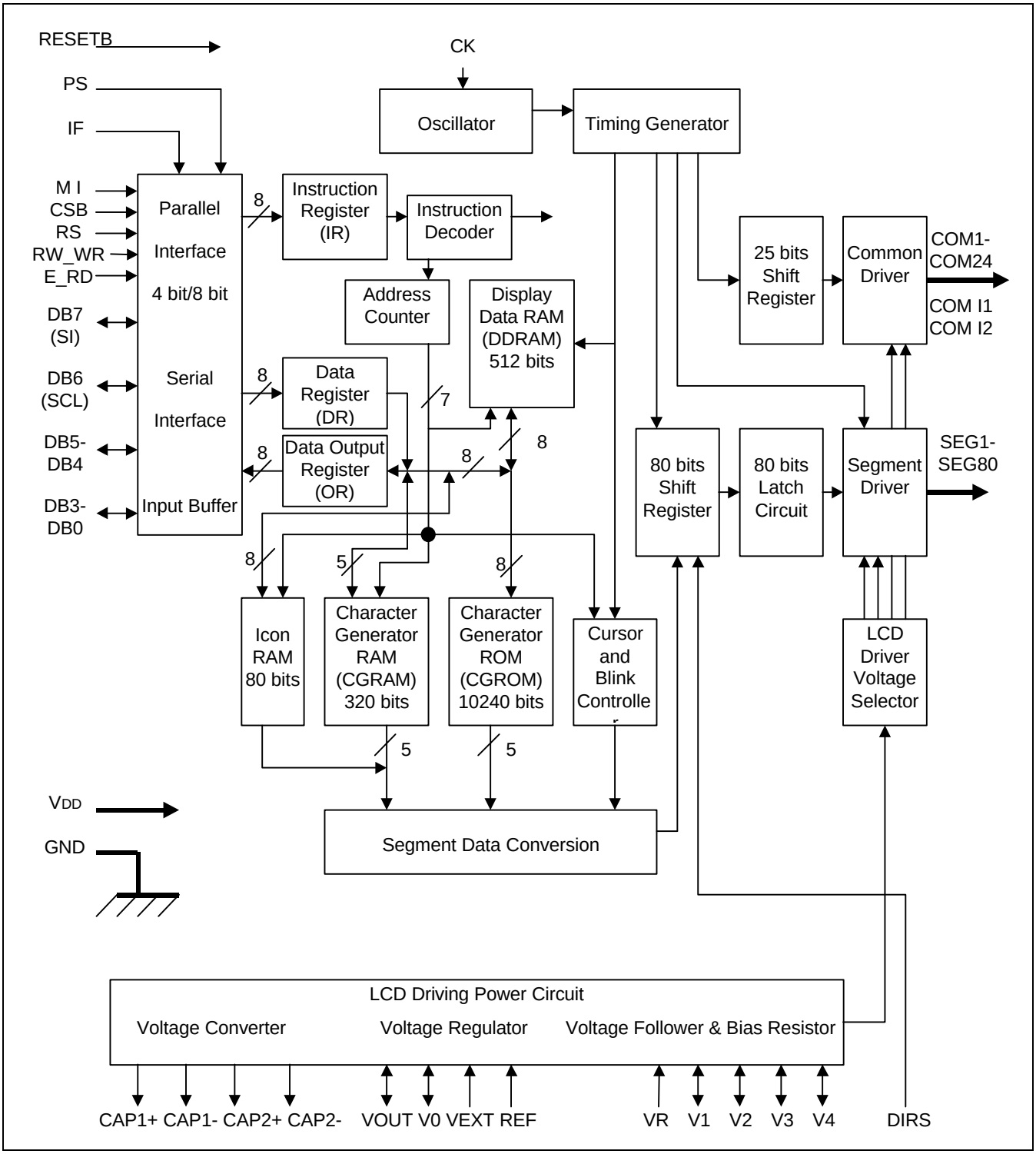


Figure 1. Block Diagram

PAD CONFIGURATION

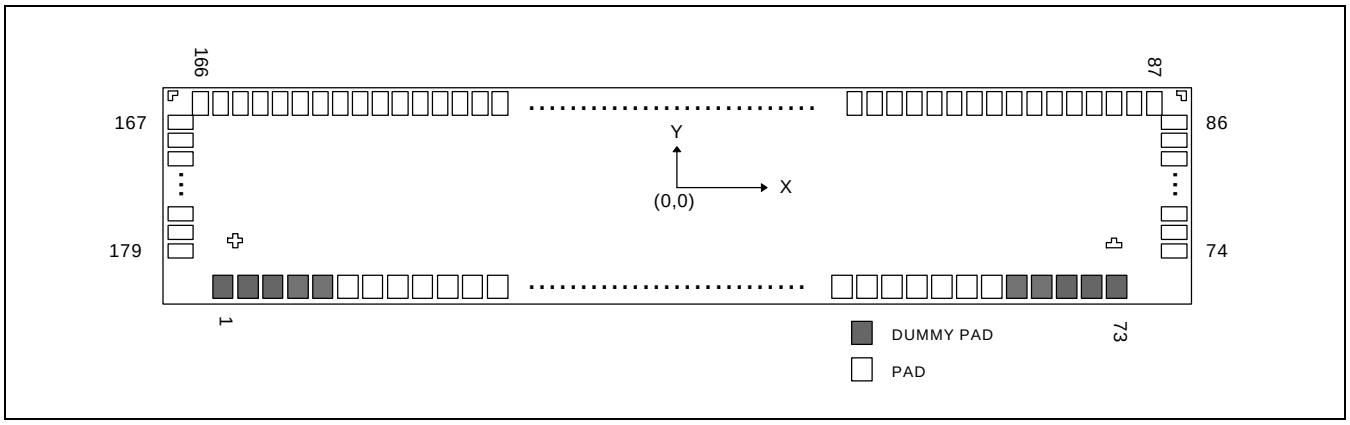
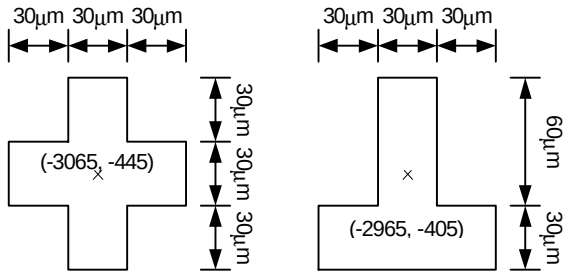


Figure 2. Pad Configuration

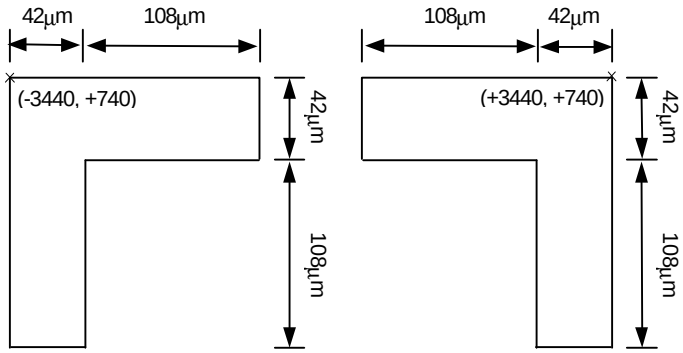
Table 1. KS0093 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	7020	1620	µm
Pad pitch	1 ~ 73	90		
	74 ~ 179	80		
Bumped pad size	1 ~ 73	60	100	
	74 ~ 86	100	50	
	87 ~ 166	50	100	
	167 ~ 179	100	50	
Bumped pad height	All pad	17		

COG Align Key Coordinate



ILB Align Key Coordinate



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PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	DUMMY	-3240	-700	61	PS	2160	-700	121	SEG35	440	700
2	DUMMY	-3150	-700	62	VDD	2250	-700	122	SEG36	360	700
3	DUMMY	-3060	-700	63	IF	2340	-700	123	SEG37	280	700
4	DUMMY	-2970	-700	64	VSS	2430	-700	124	SEG38	200	700
5	DUMMY	-2880	-700	65	MI	2520	-700	125	SEG39	120	700
6	RS	-2790	-700	66	VDD	2610	-700	126	SEG40	40	700
7	VSS	-2700	-700	67	RESETB	2700	-700	127	SEG41	-40	700
8	RW_WR	-2610	-700	68	TEST	2790	-700	128	SEG42	-120	700
9	VDD	-2520	-700	69	DUMMY	2880	-700	129	SEG43	-200	700
10	E_RD	-2430	-700	70	DUMMY	2970	-700	130	SEG44	-280	700
11	CSB	-2340	-700	71	DUMMY	3060	-700	131	SEG45	-360	700
12	DB7	-2250	-700	72	DUMMY	3150	-700	132	SEG46	-440	700
13	DB6	-2160	-700	73	DUMMY	3240	-700	133	SEG47	-520	700
14	DB5	-2070	-700	74	COMI1	3400	-520	134	SEG48	-600	700
15	DB4	-1980	-700	75	COM1	3400	-440	135	SEG49	-680	700
16	DB3	-1890	-700	76	COM2	3400	-360	136	SEG50	-760	700
17	DB2	-1800	-700	77	COM3	3400	-280	137	SEG51	-840	700
18	DB1	-1710	-700	78	COM4	3400	-200	138	SEG52	-920	700
19	DB0	-1620	-700	79	COM5	3400	-120	139	SEG53	-1000	700
20	VDD	-1530	-700	80	COM6	3400	-40	140	SEG54	-1080	700
21	VDD	-1440	-700	81	COM7	3400	40	141	SEG55	-1160	700
22	VDD	-1350	-700	82	COM8	3400	120	142	SEG56	-1240	700
23	VSS	-1260	-700	83	COM17	3400	200	143	SEG57	-1320	700
24	VSS	-1170	-700	84	COM18	3400	280	144	SEG58	-1400	700
25	VSS	-1080	-700	85	COM19	3400	360	145	SEG59	-1480	700
26	V4	-990	-700	86	COM20	3400	440	146	SEG60	-1560	700
27	V4	-900	-700	87	SEG1	3160	700	147	SEG61	-1640	700
28	V3	-810	-700	88	SEG2	3080	700	148	SEG62	-1720	700
29	V3	-720	-700	89	SEG3	3000	700	149	SEG63	-1800	700
30	V2	-630	-700	90	SEG4	2920	700	150	SEG64	-1880	700
31	V2	-540	-700	91	SEG5	2840	700	151	SEG65	-1960	700
32	V1	-450	-700	92	SEG6	2760	700	152	SEG66	-2040	700
33	V1	-360	-700	93	SEG7	2680	700	153	SEG67	-2120	700
34	V0	-270	-700	94	SEG8	2600	700	154	SEG68	-2200	700
35	V0	-180	-700	95	SEG9	2520	700	155	SEG69	-2280	700
36	V0	-90	-700	96	SEG10	2440	700	156	SEG70	-2360	700
37	V0	0	-700	97	SEG11	2360	700	157	SEG71	-2440	700
38	VR	90	-700	98	SEG12	2280	700	158	SEG72	-2520	700
39	VR	180	-700	99	SEG13	2200	700	159	SEG73	-2600	700
40	VOUT	270	-700	100	SEG14	2120	700	160	SEG74	-2680	700
41	VOUT	360	-700	101	SEG15	2040	700	161	SEG75	-2760	700
42	CAP2-	450	-700	102	SEG16	1960	700	162	SEG76	-2840	700
43	CAP2-	540	-700	103	SEG17	1880	700	163	SEG77	-2920	700
44	CAP2+	630	-700	104	SEG18	1800	700	164	SEG78	-3000	700
45	CAP2+	720	-700	105	SEG19	1720	700	165	SEG79	-3080	700
46	CAP1-	810	-700	106	SEG20	1640	700	166	SEG80	-3160	700
47	CAP1-	900	-700	107	SEG21	1560	700	167	COMI2	-3400	440
48	CAP1+	990	-700	108	SEG22	1480	700	168	COM24	-3400	360
49	CAP1+	1080	-700	109	SEG23	1400	700	169	COM23	-3400	280
50	VEXT	1170	-700	110	SEG24	1320	700	170	COM22	-3400	200
51	VSS	1260	-700	111	SEG25	1240	700	171	COM21	-3400	120
52	VSS	1350	-700	112	SEG26	1160	700	172	COM16	-3400	40
53	VSS	1440	-700	113	SEG27	1080	700	173	COM15	-3400	-40
54	REF	1530	-700	114	SEG28	1000	700	174	COM14	-3400	-120
55	DIRS	1620	-700	115	SEG29	920	700	175	COM13	-3400	-200
56	VDD	1710	-700	116	SEG30	840	700	176	COM12	-3400	-280
57	VDD	1800	-700	117	SEG31	760	700	177	COM11	-3400	-360
58	VDD	1890	-700	118	SEG32	680	700	178	COM10	-3400	-440
59	CK	1980	-700	119	SEG33	600	700	179	COM9	-3400	-520
60	VSS	2070	-700	120	SEG34	520	700				

PIN DESCRIPTION

POWER SUPPLY

Table 3. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td rowspan="2">Power</td><td>Power supply
Connect to MPU power supply pin.</td></tr>
<tr><td>VSS</td><td>0V (GND)</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>Bias voltage level for LCD driving
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the built-in power circuit is active and internal 1/5 bias resistors are used.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table>
When the built-in power circuit is active and internal 1/4 bias resistors are used.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/4 bias</td><td>(3/4) x V0</td><td colspan="2">(2/4) x V0</td><td>(1/4) x V0</td></tr>
</table>
</td></tr>
</table>

LCD DRIVER SUPPLY

Table 3. Pin Description (Continued)

Name	I/O	Description
CAP1+	O	Capacitor + connecting pin for the internal voltage converter
CAP1-	O	Capacitor - connecting pin for the internal voltage converter
CAP2+	O	Capacitor + connecting pin for the internal voltage converter
CAP2-	O	Capacitor - connecting pin for the internal voltage converter
VOUT	I/O	DC/DC voltage converter output (7.2V)
VR	I	Voltage adjust pin This pin gives a voltage between V0 and VSS by resistance-division of voltage.
VEXT	I	External reference voltage for internal regulator (instead of the internal VREF, 2V) REF = "Low (VSS)": VEXT is not used (open). REF = "High (VDD)": VEXT is reference input voltage of internal voltage regulator.
REF	I	Select the input voltage of internal voltage regulator REF = "Low (VSS)": The input voltage of internal Voltage regulator is the internal VREF(2V). REF = "High (VDD)": The input voltage of internal Voltage regulator is the voltage of VEXT.

SYSTEM CONTROL

Table 3. Pin Description (Continued)

Name	I/O	Description
CK	I	External clock input. It must be fixed to "High" or "Low" when the internal oscillation circuit is used. In case of the external clock mode, CK is used as the clock and OS bit should be OFF.
MI	I	MPU interface selection input MI = "Low": 80-series MPU MI = "High": 68-series MPU
PS	I	Parallel / serial selection input When PS = "Low": serial mode When PS = "High": 4-bit / 8-bit bus mode
IF	I	Interface data length selection pin for parallel data input When PS = "Low" IF = "Low" or "High": serial interface mode When PS = High IF = "Low": 4-bit bus mode IF = "High": 8-bit bus mode
DIRS	I	SEG direction selection input When DIRS = "Low" SEG1 → SEG2 → SEG79 → SEG80 When DIRS = "High" SEG80 → SEG79 → SEG2 → SEG1

MPU INTERFACE

Table 3. Pin Description (Continued)

Name	I/O	Description
RESETB	I	Reset input KS0093 is initialized while RESETB is low.
CSB	I	Chip selection input KS0093 is selected while CSB is low.
RS	I	Register selection input When RS = "Low", instruction register When RS = "High", data register.
RW_WR	I	In 80-series MPU interface mode This pin is connected to WR pin of MPU and is a active low write signal In 68-series MPU interface mode This pin is connected to R/W pin of MPU When RW_WR = "Low", write mode When RW_WR = "High", read mode
E_RD	I	In 80-series MPU interface mode This pin is connected to RD pin of MPU and is a active low read signal In 68-series MPU interface mode This pin is connected to E pin of MPU and enable read or write command according to RW_WR signal.

Table 3. Pin Description (Continued)

Name	I/O	Description
DB0 ~ DB3 DB4 ~ DB5 DB6 (SCL), DB7 (SI)	I/O	When 8-bit bus mode, used as bi-directional data bus DB0 ~ DB7 During 4-bit bus mode, only DB4 ~ DB7 are used. In this case DB0 ~ DB3 pins are not used. When serial mode, DB6 (SCL) is used as serial clock input pin and DB7 (SI) is used as serial data input pin.

LCD DRIVER OUTPUTS

Table 3. Pin Description (Continued)

Name	I/O	Description
COM1 ~ COM24	O	Common signal output for driving LCD
COMI1, COMI2	O	Common signal output for icon display These are the same signal but the name is different.
SEG1 ~ SEG80	O	Segment signal output for driving LCD

TEST

Table 3. Pin Description (Continued)

Name	I/O	Description
TEST	I	Test pin This pin is not used for normal operation. TEST: Open

NOTE: **DUMMY – These pins should be opened (floated).**

FUNCTION DESCRIPTION

SYSTEM INTERFACE

KS0093 has two kinds of interface type with MPU: bus mode, serial mode. Serial or bus mode is selected by PS pin. In bus mode, 4-bit bus or 8-bit bus is selected by IF pin, and 68 series MPU or 80 series MPU is selected by MI pin.

Table 4. Various Kinds of MPU Interface according to PS, MI and IF

PS	MI	IF	CSB	RS	RW_WR	E_RD	DB0~DB3	DB4~DB5	DB6	DB7
Bus mode (H)	68 series (H)	8 bit (H)	CSB	RS	R/$\overline{W}$	E	DB0~DB3	DB4~DB5	DB6	DB7
		4 bit (L)	CSB	RS	R/$\overline{W}$	E	*(1)	DB4~DB5	DB6	DB7
	80 series (L)	8 bit (H)	CSB	RS	$\overline{WR}$	$\overline{RD}$	DB0~DB3	DB4~DB5	DB6	DB7
		4 bit (L)	CSB	RS	$\overline{WR}$	$\overline{RD}$	*	DB4~DB5	DB6	DB7
Serial mode (L)	(H)/(L)(2)	(H)/(L)	CSB	RS	(H)/(L)	(H)/(L)	*	*	SCL	SI

NOTES:
1. Don't care (high, low or open)
2. Fixed high (V_{DD}) or low (V_{SS})

PS: "High" = bus mode, "Low" = serial mode
MI: "High" = 68-series MPU, "Low" = 80-series MPU
IF: "High" = 8 bit mode, "Low" = 4 bit mode (PS: "High")
CSB: "High" = chip is not selected, "Low" = chip is selected
RS: "High" = data register, "Low" = instruction register
RW_WR: Read / Write indicating signal in 68 mode or active low signal for enabling write in 80 mode
E_RD: Active high signal for enabling command is 68 mode or active low signal for enabling read in 80 mode.
SCL (DB6): Serial clock input
SI (DB7): Serial data input

Interface with MPU in Parallel Mode (PS = "High")

During writing operation, two 8-bit registers, data register (DR) and instruction register (IR), are used. The data register (DR) is used as temporary data storage place for being written into DDRAM / CGRAM / ICONRAM and one of these RAMs is selected by RAM address setting instruction. The Instruction register (IR) is used only to store instruction code transferred from MPU. To select DR or IR register, RS input pin is used.

During reading operation, 8-bit register, output data register (OR) is used. The output data register (OR) is used as temporary data storage place for being read from DDRAM / CGRAM / ICONRAM and one of these RAMs is selected by RAM address setting instruction. After RAM address setting, first reading is a dummy cycle in 8-bit bus mode (figure 3, 4). The valid data comes from second reading. In 4-bit bus mode, after RAM address setting, first and second reading are dummy cycles (figure 5, 6). The valid data comes from third reading. The dummy read make the address counter (AC) increased by 1. So it is recommended to set address again before writing. The instruction read cycle is not supported and it is regarded as a no operation cycle.

In 4-bit bus mode, it is needed to transfer 4-bit data (through DB7~DB4) by two times. The high order bits (for 8-bit mode DB7~DB4) are written before the low order bits (for 8-bit mode DB3~DB0) in write and low order bits (for 8-bit mode DB3~DB0) are read before the high order bits (for 8-bit mode DB7~DB4) in read transaction. The DB0~DB3 pins are floated in this 4-bit bus mode. After RESETB resets, KS0093 considers first 4-bit data from MPU as the high order bits.

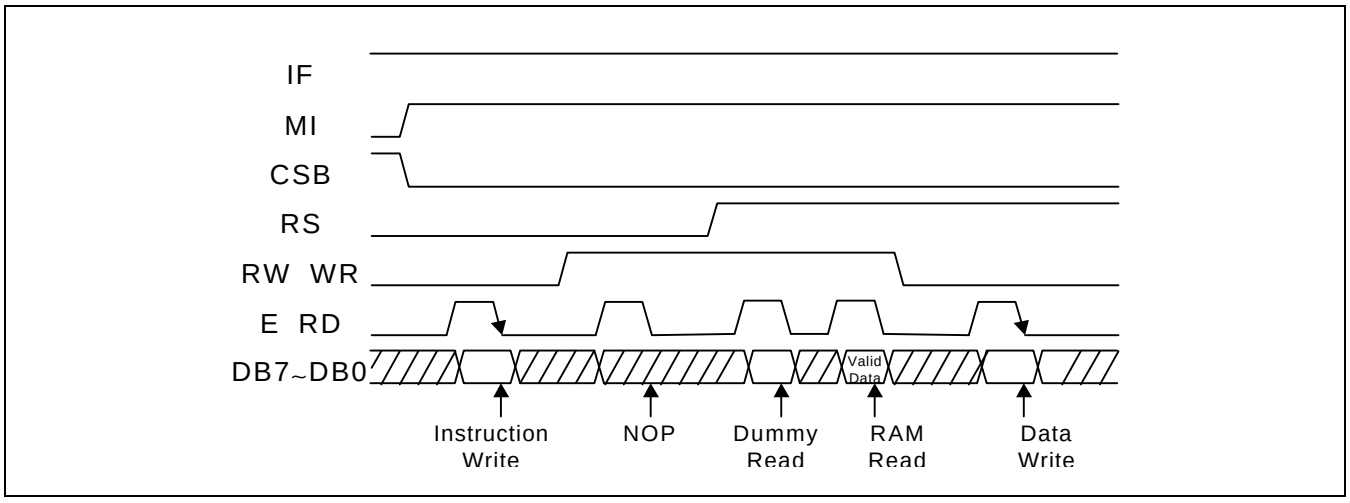

Figure 3. Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (68-series MPU Mode)

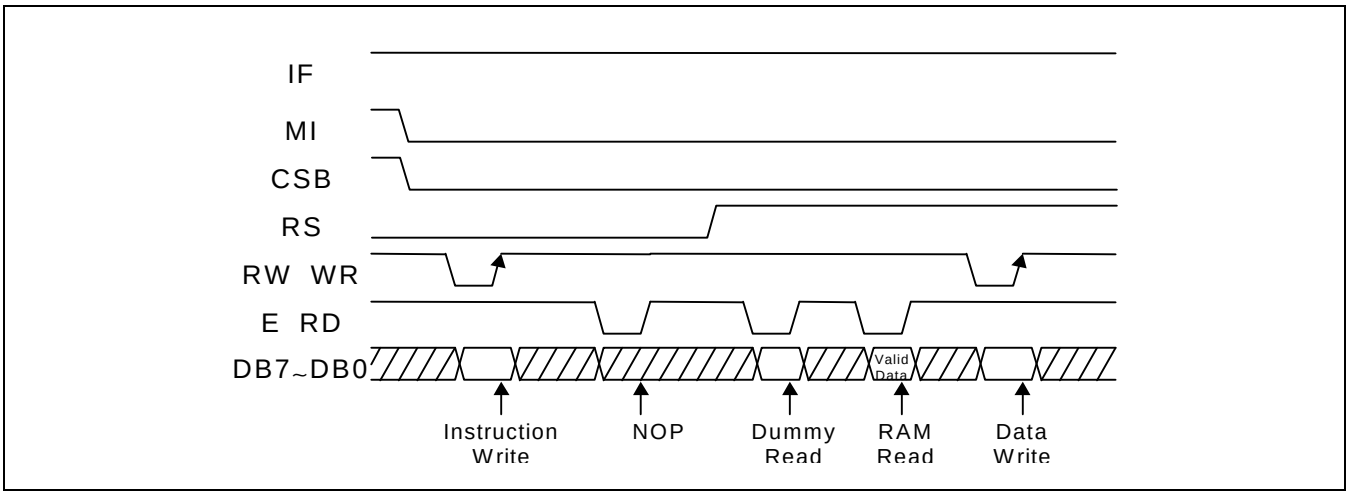

Figure 4. Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (80-series MPU Mode)

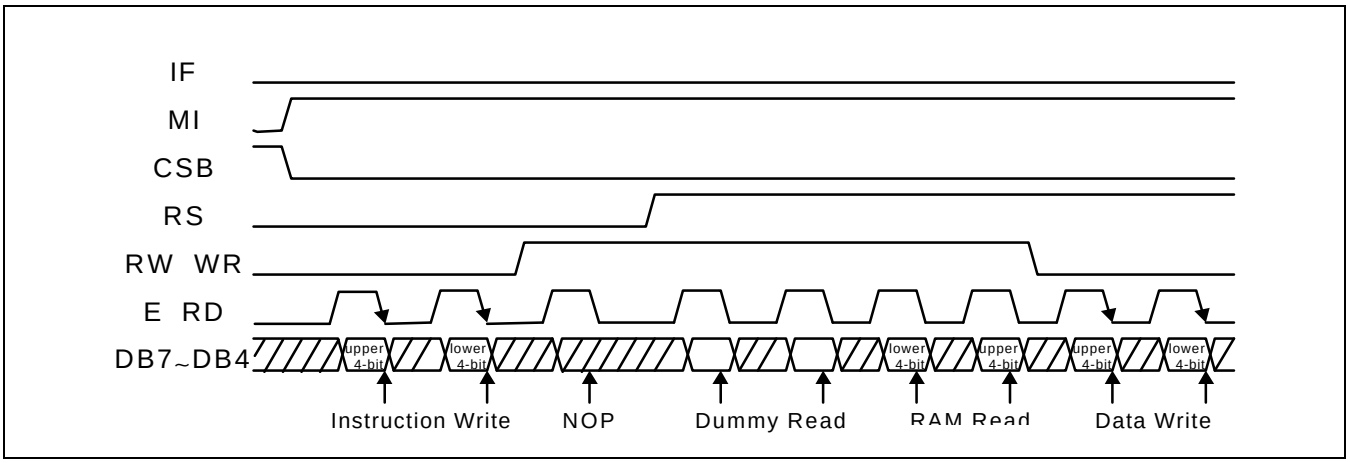

Figure 5. Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (68-series MPU Mode)

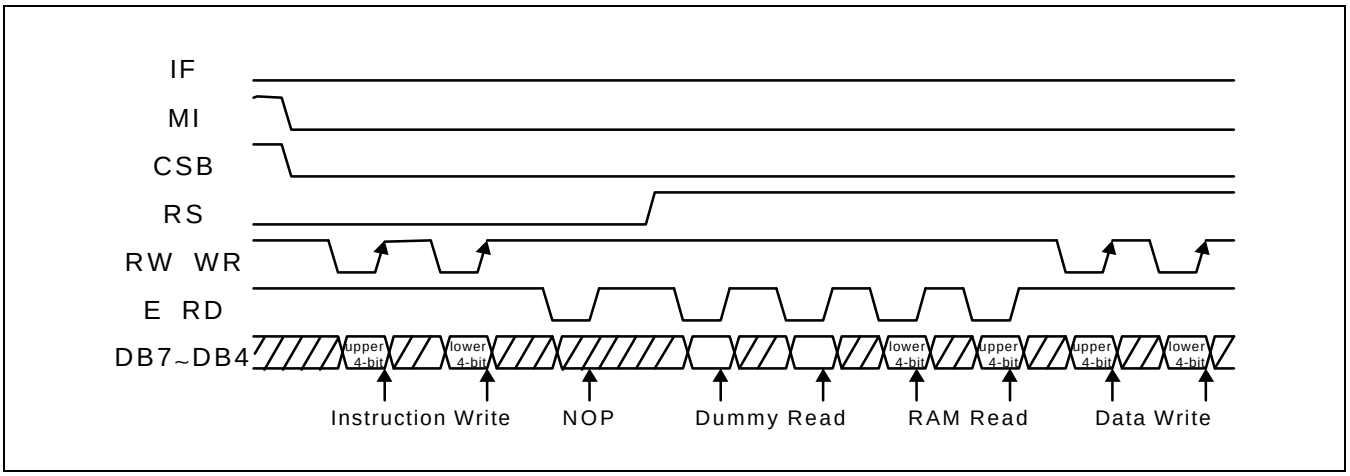

Figure 6. Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (80-series MPU Mode)

Interface with MPU in Serial Mode (PS = "Low")

When PS input pin is "Low", clock synchronized serial interface mode is selected. At this time, five ports, RESETB (reset input), SCL (DB6, synchronizing transfer clock), SI (DB7, serial input data), RS (register selection input) and CSB(chip selection input) are used.

By setting CSB to "Low", KS0093 can receive SCL input. If CSB is set to "High", KS0093 resets the internal 8-bit shift register and 3-bit counter. Serial data is input in the order of "D7, D6, D5, D4, D3, D2, D1, D0" from the serial data input pin (SI = DB7) at the rising edge of serial clock (SCL = DB6).

At the rising edge of the 8th serial clock, the serial data (D7-D0) is converted into 8 bit bus mode data. The RS input of the DR/IR selection is latched at the rising edge of the 8th serial clock (SCL).

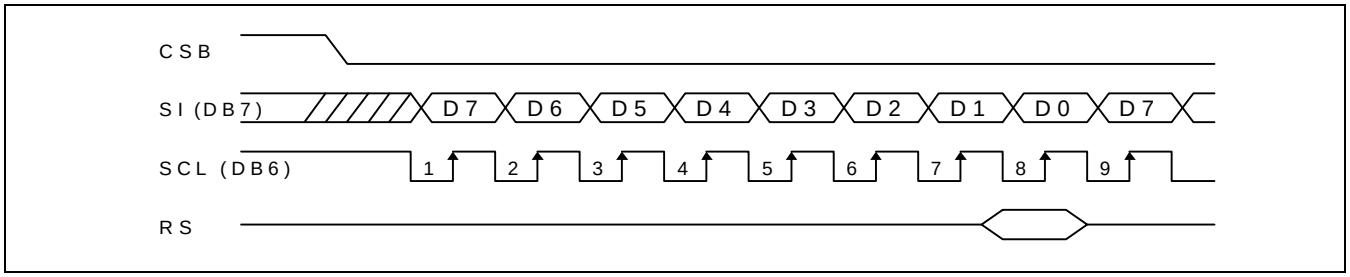

Figure 7. Timing Diagram of Serial Data Transfer

ADDRESS COUNTER (AC)

Address Counter (AC) in KS0093 stores DDRAM/ CGRAM/ ICONRAM address. After writing into or reading from DDRAM / CGRAM / ICONRAM, AC is automatically increased by 1. The address counter is only one and stores the address among DDRAM / CGRAM / ICONRAM.

DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 64 x 8 bits (Max. 64 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number.

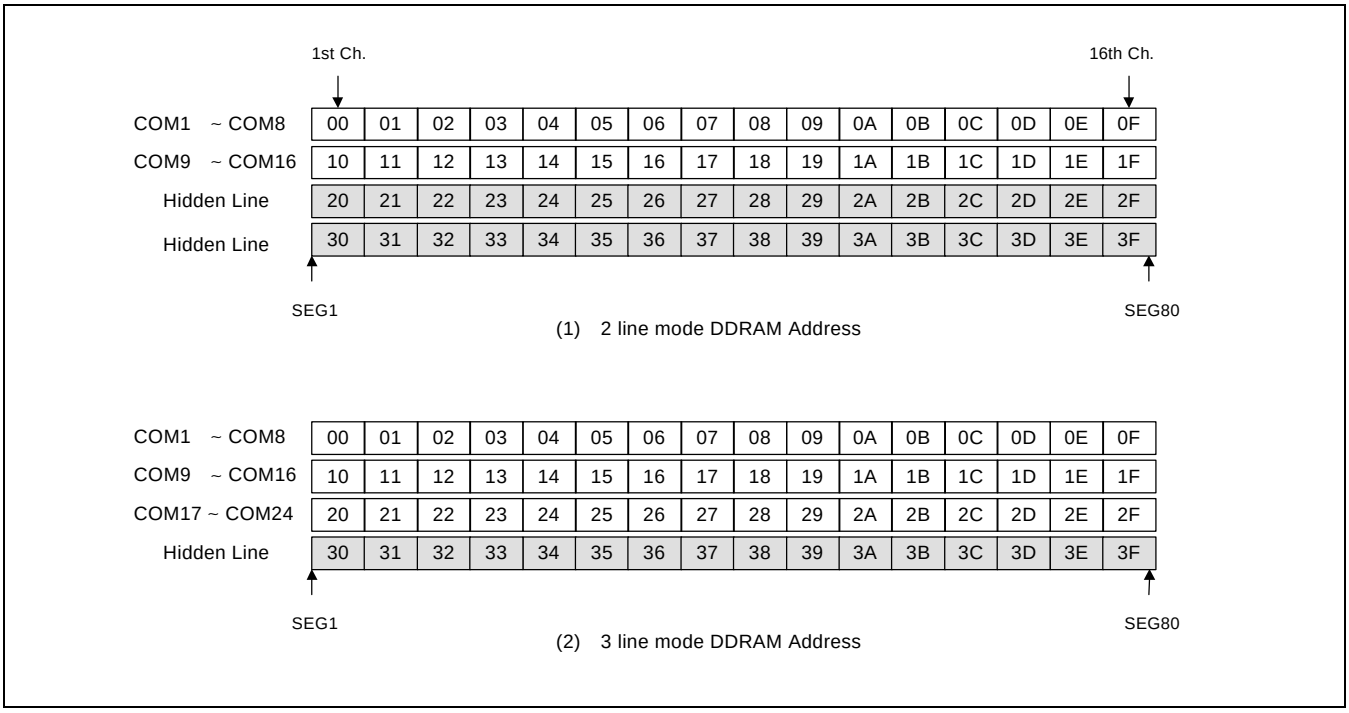

Figure 8. DDRAM Address

CHARACTER GENERATOR ROM (CGROM)

CGROM has 5 x 8-dot 256 characters. The CG bit of the instruction table selects the 8 characters (00h ~ 07h) of CGROM or CGRAM.

Table 5. CGROM Character Code (00)

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CHARACTER GENERATOR RAM (CGRAM)

CGRAM has up to 5 x 8-dot 8 characters. By writing font data to CGRAM, user defined character can be used. CGRAM can be written regardless of CG bit.

Table 6. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character code (DDRAM data)	DD/CGRAM address	CGRAM data	Pattern number
D7 D6 D5 D4 D3 D2 D1 D0	A6 A5 A4 A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 0 0 0 0 (00h)	1 0 0 0 0 0 0 1 0 0 0 0 0 1 1 0 0 0 0 1 0 1 0 0 0 0 1 1 1 0 0 0 1 0 0 1 0 0 0 1 0 1 1 0 0 0 1 1 0 1 0 0 0 1 1 1	- - - 0 1 0 1 0 - - - 1 0 1 0 1 - - - 0 1 0 1 0 - - - 1 0 1 0 1 - - - 0 1 0 1 0 - - - 1 0 1 0 1 - - - 0 1 0 1 0 - - - 1 0 1 0 1	Pattern 1
0 0 0 0 0 0 0 1 (01h)	1 0 0 1 0 0 0 1 0 0 1 0 0 1 1 0 0 1 0 1 0 1 0 0 1 0 1 1 1 0 0 1 1 0 0 1 0 0 1 1 0 1 1 0 0 1 1 1 0 1 0 0 1 1 1 1	- - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 1 1 1 1 1	Pattern 2
0 0 0 0 0 0 1 0 (02h)	1 0 1 0 0 0 0 1 0 1 0 0 0 1 1 0 1 0 0 1 0 1 0 1 0 0 1 1 1 0 1 0 1 0 0 1 0 1 0 1 0 1 1 0 1 0 1 1 0 1 0 1 0 1 1 1	- - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0	Pattern 3
0 0 0 0 0 0 1 1 (03h)	1 0 1 1 0 0 0 1 0 1 1 0 0 1 1 0 1 1 0 1 0 1 0 1 1 0 1 1 1 0 1 1 1 0 0 1 0 1 1 1 0 1 1 0 1 1 1 1 0 1 0 1 1 1 1 1	- - - 0 1 1 1 0 - - - 1 0 1 0 1 - - - 1 1 0 1 1 - - - 1 0 1 0 1 - - - 0 1 1 1 0 - - - 1 1 1 1 1 - - - 1 1 1 1 1 - - - 1 1 1 1 1	Pattern 4

Table 6. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM) (continued)

Character code (DDRAM data)	DD/CGRAM address	CGRAM data	Pattern number
D7 D6 D5 D4 D3 D2 D1 D0	A6 A5 A4 A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 0 1 0 0 (04h)	1 1 0 0 0 0 0 1 1 0 0 0 0 1 1 1 0 0 0 1 0 1 1 0 0 0 1 1 1 1 0 0 1 0 0 1 1 0 0 1 0 1 1 1 0 0 1 1 0 1 1 0 0 1 1 1	- - - 1 1 0 1 1 - - - 1 0 0 0 1 - - - 0 0 0 0 0 - - - 1 0 0 0 1 - - - 1 1 0 1 1 - - - 1 1 1 1 1 - - - 1 1 1 1 1 - - - 1 1 1 1 1	Pattern 5
0 0 0 0 0 1 0 1 (05h)	1 1 0 1 0 0 0 1 1 0 1 0 0 1 1 1 0 1 0 1 0 1 1 0 1 0 1 1 1 1 0 1 1 0 0 1 1 0 1 1 0 1 1 1 0 1 1 1 0 1 1 0 1 1 1 1	- - - 1 1 1 1 1 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 0 0 0 0 0	Pattern 6
0 0 0 0 0 1 1 0 (06h)	1 1 1 0 0 0 0 1 1 1 0 0 0 1 1 1 1 0 0 1 0 1 1 1 0 0 1 1 1 1 1 0 1 0 0 1 1 1 0 1 0 1 1 1 1 0 1 1 0 1 1 1 0 1 1 1	- - - 0 0 1 1 0 - - - 0 0 1 1 0 - - - 0 0 1 1 0 - - - 0 0 1 1 0 - - - 0 0 1 1 0 - - - 0 0 1 1 0 - - - 0 0 1 1 0 - - - 0 0 1 1 0	Pattern 7
0 0 0 0 0 1 1 1 (07h)	1 1 1 1 0 0 0 1 1 1 1 0 0 1 1 1 1 1 0 1 0 1 1 1 1 0 1 1 1 1 1 1 1 0 0 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	- - - 0 0 0 0 0 - - - 1 0 0 0 1 - - - 1 1 0 1 1 - - - 1 0 0 0 1 - - - 0 0 0 0 0 - - - 1 0 0 0 1 - - - 1 1 0 1 1 - - - 1 1 1 1 1	Pattern 8

NOTE: "-" - Don't care

SEGMENT ICON RAM (ICONRAM)

ICONRAM has segment control data and segment pattern data. COMI1 and COMI2 are the same signal but the name is different. So the icons on the same SEG are displayed at the same time. The number of icons is 80.

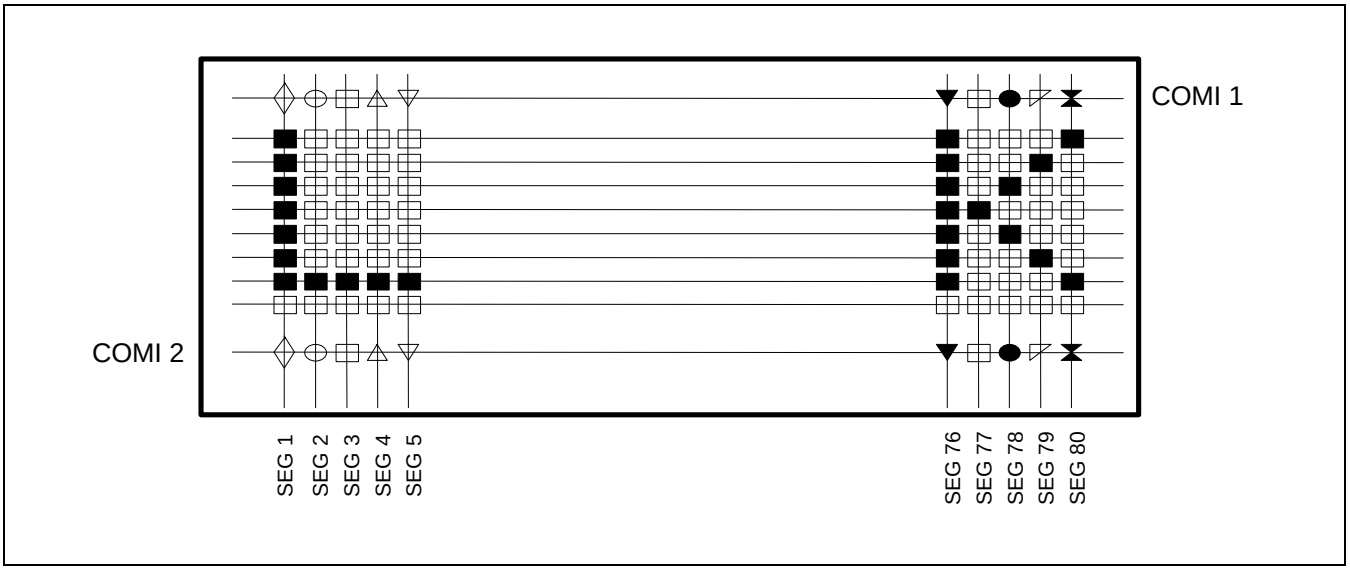


Figure 9. Relationship between ICONRAM and Icon Display

Table 7. Relationship between ICONRAM Address and Display Pattern

ICONRAM address	ICONRAM bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	-	-	-	S1	S2	S3	S4	S5
01h	-	-	-	S6	S7	S8	S9	S10
02h	-	-	-	S11	S12	S13	S14	S15
. .	. .	. .	. .	. .	. .	. .	. .	. .
0Dh	-	-	-	S66	S67	S68	S69	S70
0Eh	-	-	-	S71	S72	S73	S74	S75
0Fh	-	-	-	S76	S77	S78	S79	S80

NOTE: "-" - Don't care

LOW POWER CONSUMPTION MODE

KS0093 provides with sleep mode for saving power consumption during standby period.

Sleep Mode (Power Save Bit ON, Oscillation Bit OFF)

To enter the sleep mode, the power circuit and oscillation circuit should be turned off by using the power save command and the power control command. This mode helps to save power consumption by reducing current to reset level.

1. Liquid Crystal Display Output
   COM1 ~ COM24, COMI1, COMI2: V_{SS} level
   SEG1 ~ SEG80: V_{SS} level

2. Data written in DDRAM, CGRAM, ICONRAM and registers are remained as previous value.

3. Operation mode is retained the same as it was prior to execution of the sleep mode.
   All internal circuits are stopped.

4. Power Circuit and Oscillation Circuit
   The built-in power supply circuit and oscillation circuit are turned off by power save command and power control command.

LCD DRIVER CIRCUIT

LCD Driver circuit has 26 common and 80 segment signals for driving LCD. Data from ICONRAM/ CGRAM/ CGROM are transferred to 80-bit segment register serially, and then they are stored to 80-bit shift latch. In case of 2-line display mode, COM1 ~ COM16, COMI1 and COMI2 have 1/17 duty, and in 3-line mode, COM1 ~ COM24, COMI1 and COMI2 have 1/25 duty ratio. SEG bi-directional function is selected by DIRS input pin, and COM shift direction is selected by function set instruction "S" bit.

Table 8. SEG Data Shift Direction

DIRS pin	SEG data shift direction
Low	SEG1 → SEG2 → SEG3 ..... SEG78 → SEG79 → SEG80
High	SEG80 → SEG79 → SEG78 ..... SEG3 → SEG2 → SEG1

Table 9. COM Data Shift Direction

Line mode	S	COM data shift direction
2-line mode	0 (left)	COM1 → COM2 ..... COM15 → COM16 → COMI1 (COMI2)
	1 (right)	COMI1 (COMI2) → COM16 → COM15 ..... COM2 → COM1
3-line mode	0 (left)	COM1 → COM2 ..... COM23 → COM24 → COMI1 (COMI2)
	1 (right)	COMI1 (COMI2) → COM24 → COM23 ..... COM2 → COM1

INSTRUCTION DESCRIPTION

Table 10. Instruction Table

Instruction	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Return home	0	0	0	0	0	0	0	1	-	DDRAM address is set to 00h from AC and the cursor returns to 00h position The contents of DDRAM are not changed.
Double height mode	0	0	0	0	0	1	0	DH2	DH1	Double height mode DH2, DH1 = 00: normal display (default) 01: COM1 ~ COM16 is a double height, COM17~COM24 is normal 10: 1) 2-line mode : normal display 2) 3-line mode : COM1~COM8 is normal, COM9 ~ COM24 is a double height 11: normal display
Power save	0	0	0	0	0	1	1	OS	PS	Power save / oscillation circuit ON / OFF OS = 0: oscillator OFF (default) 1: oscillator ON PS = 0: power save OFF (default) 1: power save ON
Function set	0	0	0	0	1	0	N	S	CG	Display line mode N = 0: 2-line display mode (default) 1: 3-line display mode shifting direction of COM. S = 0: 1) 2-line mode: COM1 -> COM16 (default) 2) 3-line mode: COM1 -> COM24 (default) 1: 1) 2-line mode: COM16 -> COM1 2) 3-line mode: COM24 -> COM1 Select CGRAM or CGROM CG = 0: CGROM (default) 1: CGRAM
Line shift mode	0	0	0	0	1	1	0	LS2	LS1	Determination of the DDRAM line which is displayed at the first line at LCD LS2, LS1 = 00: DDRAM line 1 shows at the first line of LCD (default). 01: DDRAM line 2 shows at the first line of LCD. 10: DDRAM line 3 shows at the first line of LCD. 11: DDRAM line 4 shows at the first line of LCD
Bias control	0	0	0	0	1	1	1	-	BS	Determination of bias BS = 0: 1/5 bias (default) 1: 1/4 bias
Power control	0	0	0	1	0	0	VC	VR	VF	LCD power control VC = 0: voltage converter OFF (default) 1: voltage converter ON VR = 0: voltage regulator OFF (default) 1: voltage regulator ON VF = 0: voltage follower OFF (default) 1: voltage follower ON

Table 10. Instruction Table (Continued)

Instruction	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display control	0	0	0	1	0	1	C	B	D	Cursor / blink / display ON / OFF C = 0: cursor OFF (default), 1: cursor ON B = 0: blink OFF (default), 1: blink ON D = 0: display OFF (default), 1: display ON
DD/CGRAM address set	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	DDRAM / CGRAM address range: DDRAM 00h ~ 3Fh CGRAM 40h ~ 7Fh
ICONRAM address set	0	0	1	0	IA4	IA3	IA2	IA1	IA0	ICONRAM address, electronic volume and test byte address range: ICONRAM 00h ~ 0Fh EV 10h (electronic volume byte), TE 11h (test byte)
Write Data	1	D7	D6	D5	D4	D3	D2	D1	D0	Write DDRAM / CGRAM / ICONRAM
Read Data	1	D7	D6	D5	D4	D3	D2	D1	D0	Read DDRAM / CGRAM / ICONRAM or registers data (NOTE1)
NOP	0	0	0	0	0	0	0	0	0	Non-operation Instruction
Test	0	0	0	1	1	*	*	*	*	Don't use this Instruction.

NOTES:

1. "-": Don't care
2. "*": Don't use
3. Instruction execution time depends on the internal process time of KS0093, therefore it is necessary to provide a time larger than one MPU interface cycle time (tc) between execution of two successive instructions.

Return Home

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	-

Return Home instruction field makes cursor return home.
DDRAM address is set to 00h from AC and the cursor returns to 00h position. The contents of DDRAM are not changed.

Double Height Mode

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	DH2	DH1

Double Height mode instruction field selects double height line type.
DH2, DH1 = 00: normal display line mode (default)
01: COM1 ~ COM16 is a double height,
COM17 ~ COM24 is normal
10: 1) 2-line mode: normal display
2) 3-line mode: COM1 ~ COM8 is normal
COM9 ~ COM24 is a double height
11: normal display

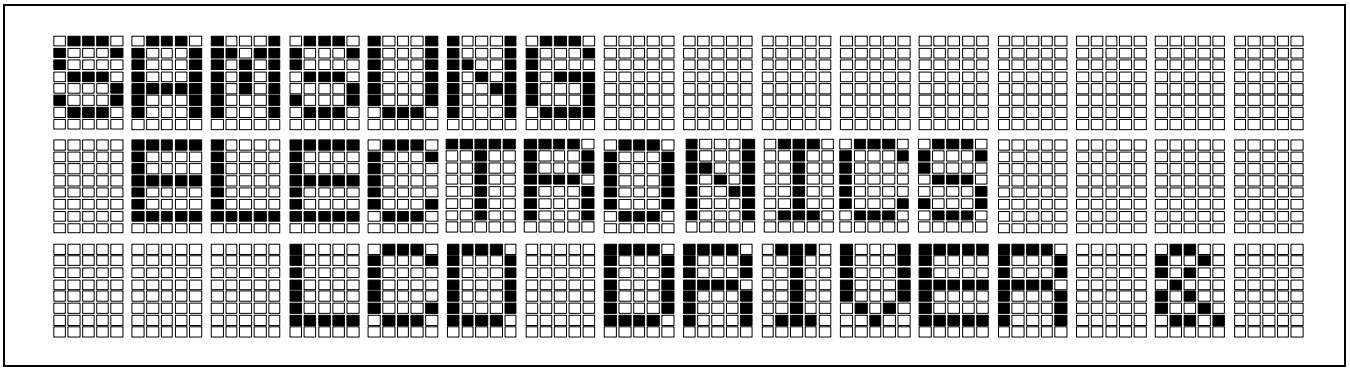


Figure 10. 3 Line Normal Mode Display (DH2, DH1 = 00)

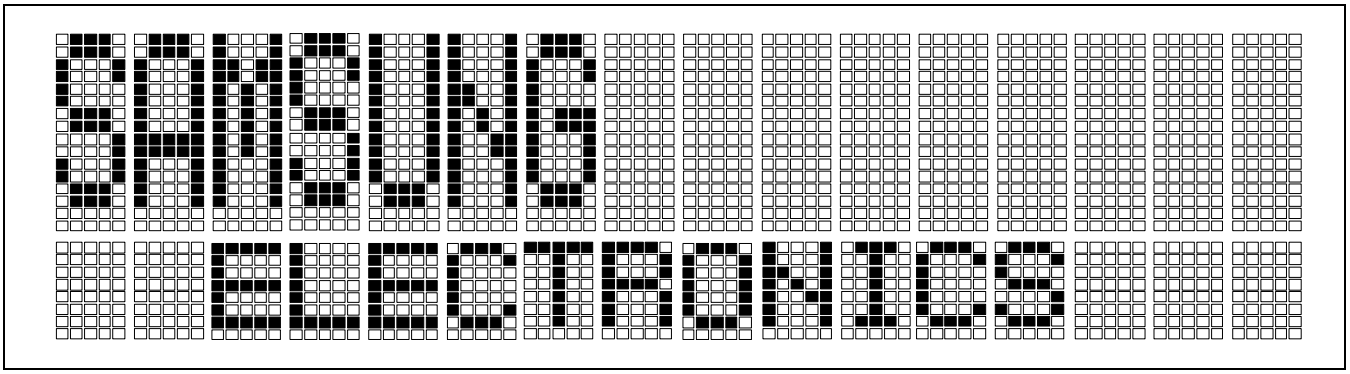


Figure 11. COM1 ~ 16 is a Double Height Line, COM17 ~ 24 is Normal (DH2, DH1 = 01)

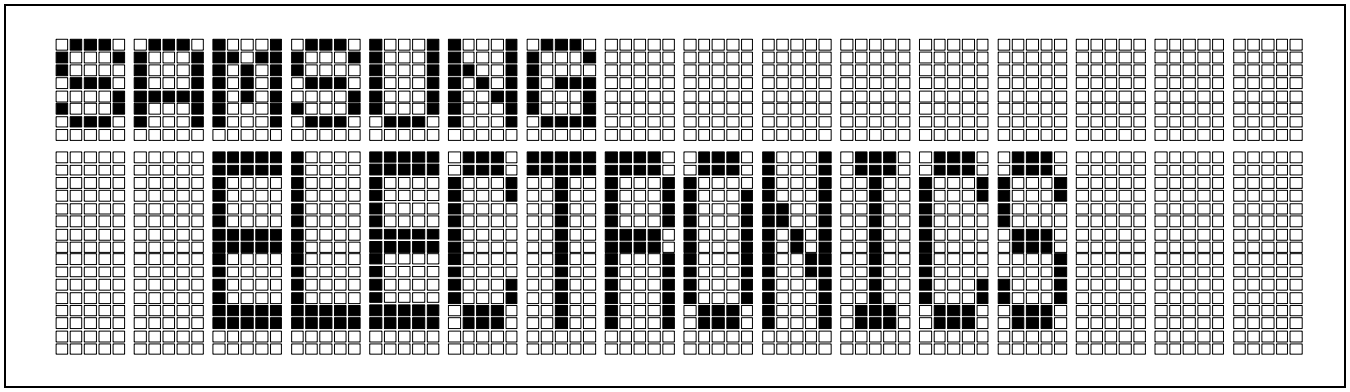


Figure 12. COM1 ~ 8 is Normal, COM9 ~ COM24 is a Double Height Line (DH2, DH1 = 10)

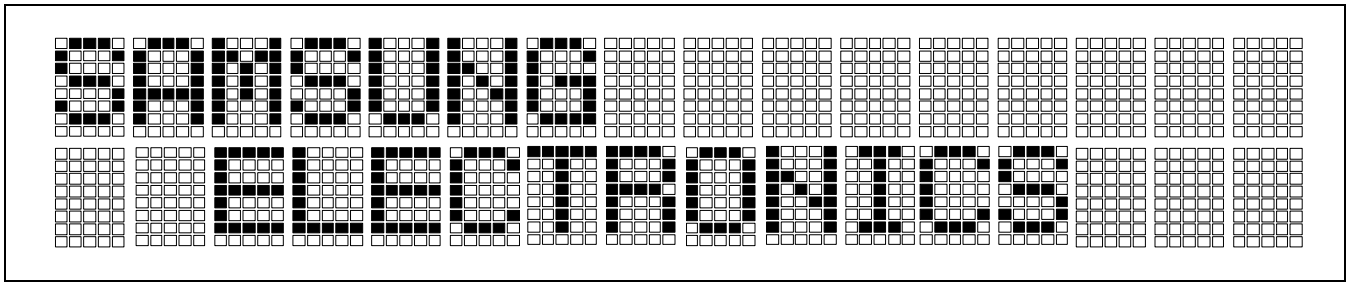


Figure 13. 2-line Normal Mode Display (DH2, DH1 = 00)

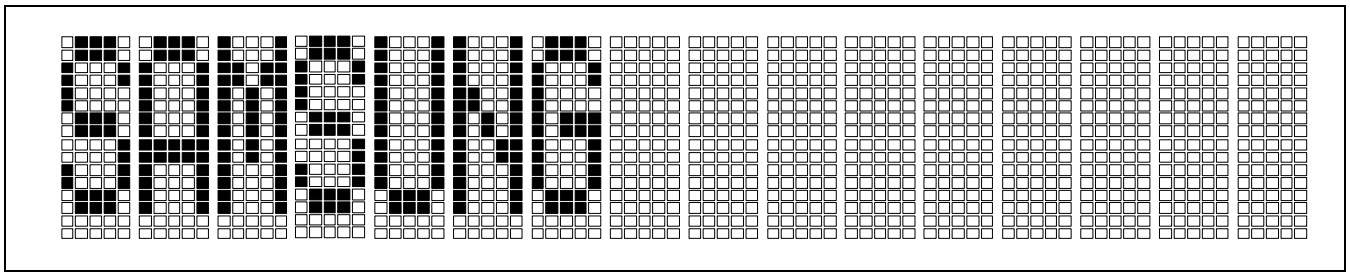


Figure 14. COM1 ~ 16 is a Double Height Line (DH2, DH1 = 01)

Power Save Set

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	OS	PS

Power Save instruction field is used to control the oscillator and to set or to reset the power save mode.

OS: oscillator ON / OFF control Bit
When OS = "High", oscillator is turned ON
When OS = "Low", oscillator is turned OFF (default)

PS: power save ON / OFF control bit
When PS = "High", power save mode is turned ON
When PS = "Low", power save mode is turned OFF (default)

Function Set

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	N	S	CG

N: display line mode Instruction field selects 2 line or 3 line display mode
When N = "High", 3 line display mode
When N = "Low", 2 line display mode (default)

S: data shift direction of common
S sets the shift direction of common display data
When S = "High", COM right shift
When S = "Low", COM left shift (default)
(refer to table 9)

CG: CGRAM enable bit
When CG = "High", CGRAM can be accessed and you can use this RAM for eight special character area. (00h - 07h = **CGRAM** font display)

When CG = "Low", CGRAM is disabled. CGROM (00h~07h) can be accessed and the additional current consumption is saved by using this mode (default). (00h - 07h = **CGROM** font display)

Line Shift Mode

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	LS2	LS1

Line Shift mode instruction field selects the DD RAM to be displayed in first line.

LS2, LS1 = 00: DDRAM line 1 shows at the first line of LCD (default).
01: DDRAM line 2 shows at the first line of LCD.
10: DDRAM line 3 shows at the first line of LCD.
11: DDRAM line 4 shows at the first line of LCD.

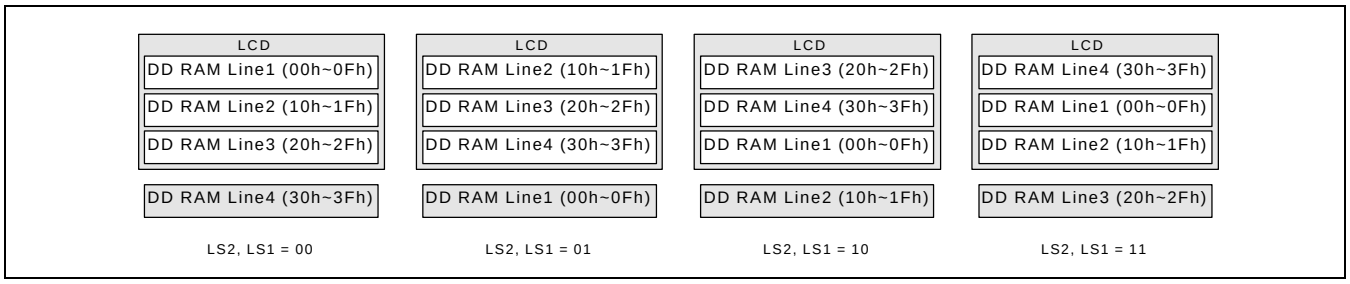


Figure 15. Line Shift Mode Display at 3 Line LCD

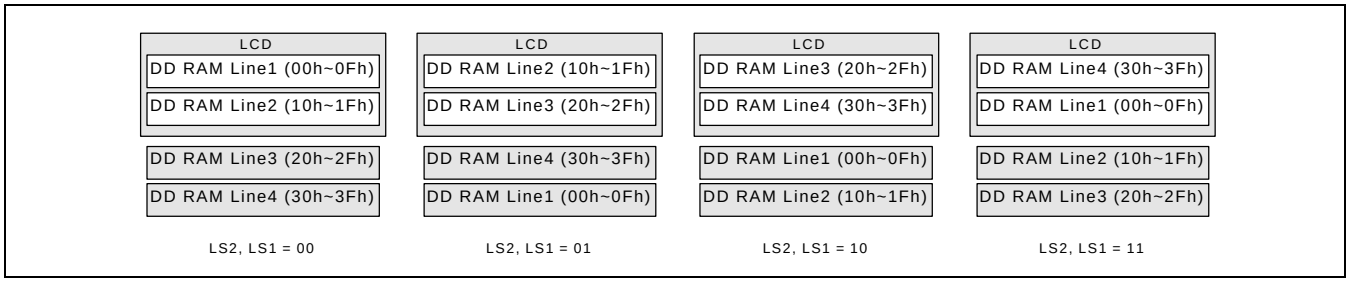


Figure 16. Line Shift Mode Display at 2 Line LCD

Bias Control

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	-	BS

Bias Control instruction field sets LCD bias voltages generated internally.
This bit is used when the internal voltage follower is ON.

BS = 0: 1/5 bias (default)
1: 1/4 bias (V2 = V3)

Power Control Set

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	VC	VR	VF

Power Control instruction field sets voltage regulator/ converter/ follower on / off.

VC: voltage converter circuit control bit
When VC= "High", voltage converter is turned ON.
When VC = "Low", voltage converter is turned OFF (default).

VR: voltage regulator circuit control bit
When VR = "High", voltage regulator is turned ON.
When VR = "Low", voltage regulator is turned OFF (default).

VF: voltage follower circuit control bit
When VF = "High", voltage follower is turned ON.
When VF = "Low", voltage follower is turned OFF (default).

*NOTE: The oscillation circuit must be turned on for the voltage converter circuit to be active.

Display Control

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	C	B	D

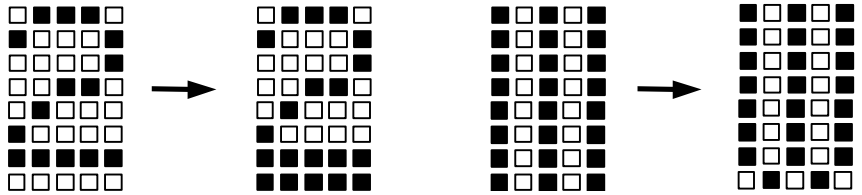
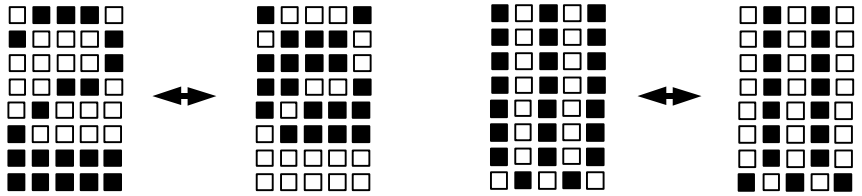
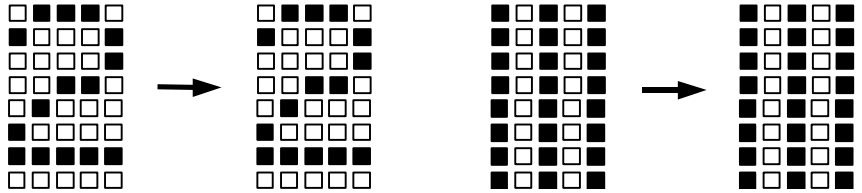
Display Control instruction field controls cursor / blink / display ON / OFF.

C: cursor ON / OFF control bit
When C = "High", cursor is turned ON.
When C = "Low", cursor is disappeared in current display (default).

B: cursor blink ON / OFF control bit
When C = "High" and B = "High", KS0093 make LCD alternate between inverting display character and normal display character at the cursor position with about a half second.
On the contrary, if C = "Low", only a normal character is displayed regardless of "B" flag.
When B = "Low", blink is OFF (default).

D: display ON / OFF control bit
When D = "High", entire display is turned ON.
When D = "Low", display is turned OFF, but display data are remained in DDRAM (default).

Table 11. Cursor Attributes

C, B	Display state
1, 0	
1, 1 (Blinking mode)	
0, 0 0, 1	

DD/CG RAM Address Set

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

DD/CG RAM Address Set instruction field sets DDRAM / CGRAM address.

Before writing / reading data into / from the RAM, set the address by RAM Address Set instruction. Next, when data are written / read in succession, the address is automatically increased by 1. After accessing 7Fh, the address of AC is 00h.

The address ranges are 00h ~ 7Fh.

Table 12. DD/CG RAM Address Mapping

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00h	DDRAM line 1 (00h ~ 0Fh)															
10h	DDRAM line 2 (10h ~ 1Fh)															
20h	DDRAM line 3 (20h ~ 2Fh)															
30h	DDRAM line 4 (30h ~ 3Fh)															
40h	CGRAM (pattern 0)								CGRAM (pattern 1)							
50h	CGRAM (pattern 2)								CGRAM (pattern 3)							
60h	CGRAM (pattern 4)								CGRAM (pattern 5)							
70h	CGRAM (pattern 6)								CGRAM (pattern 7)							

ICONRAM Address Set

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	IA4	IA3	IA2	IA1	IA0

ICONRAM Address Set instruction field sets ICONRAM / Registers address.

Before writing/reading data into/from the ICON RAM, set the address by ICONRAM Address Set instruction. Next, when data are written/read in succession, the address is automatically increased by 1. The 5 icons at a time can blink, if C and B bits of the display instructions are enabled. The blink attributes of ICON are same as the cursor blink. For accessing DD/CGRAM, the DD/CGRAM Address Set instruction should be set before. After accessing 0Fh, the address of ICONRAM address is 00h. The ICONRAM address ranges are 00h ~ 1Fh.

Table 13. ICONRAM Address Mapping

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00h	ICON RAM (00h ~ 0Fh)															
10h	EV	TE	Reserved													

EV: electronic volume register (10h) - default (00000)
TE: test register (Do not use) (11h)
When the EV and TE registers are written, the address counter (AC) is not increased.

Write Data

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	D7	D6	D5	D4	D3	D2	D1	D0

This instruction field make KS0093 write binary 8-bit data to DDRAM / CGRAM / ICONRAM or register. The RAM address to be written into is determined by previous DD/CGRAM Address Set or ICONRAM Address Set instruction. After writing operation, the address is automatically increased by 1.

Read Data

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	D7	D6	D5	D4	D3	D2	D1	D0

DDRAM / CGRAM / ICONRAM data read instruction.

Each RAM is selected by address set instruction. And then you can read the RAM data. You can get correct RAM data from second read transaction. The first read data after setting RAM address is dummy data, so the correct RAM data come from the second read transaction. After reading operation, the address is increased by 1 automatically.

INITIALIZING & POWER SAVE MODE SETUP

HARDWARE RESET

When RESETB pin = "Low", KS0093 can be initialized as the following state.

(1) Control display ON / OFF instruction
C = 0: cursor OFF
B = 0: blink OFF
D = 0: display OFF

(2) Power save set instruction
OS = 0: oscillator OFF
PS = 0: power save OFF

(3) Power control set instruction
VR = 0: voltage regulator OFF
VC = 0: voltage converter OFF
VF = 0: voltage follower OFF

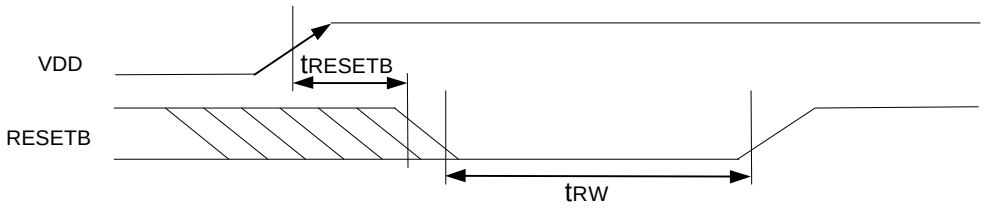
(4) Function set instruction
N = 0: 2 line display mode
S = 0: COM left shift
CG = 0: CGRAM is not used.

(5) Return Home
Address counter = 00h

(6) Electronic contrast control register: 10h = (0, 0, 0, 0, 0)

(7) In case of 4-bit interface mode selection
KS0093 considers the first 4-bit data from MPU as the high order bits.

*NOTE: If initialization is not done by the RESETB pin at application, unknown condition might result. Then you can initialize by instruction.

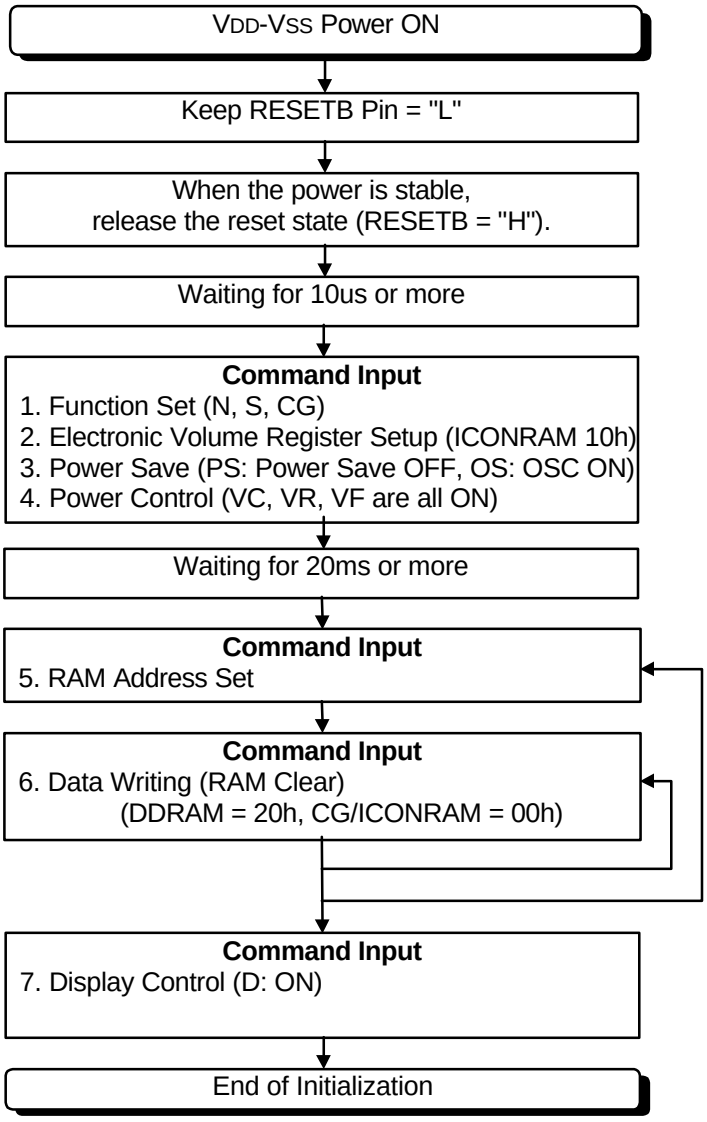


RESET pulse width	t_{RW}	10µs
RESET start time	t_{RESETB}	50ns

Figure 17. RESET Timing

INITIALIZING AND POWER SAVE SETUP

Initializing by Instruction



NOTE:

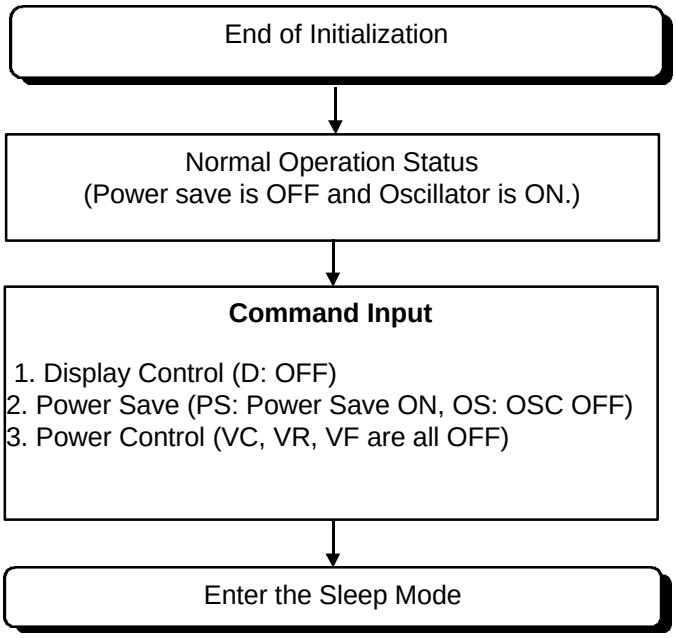
At command 5 and 6, the internal RAM should be cleared.
To clear DDRAM, Set address at 00h (first DDRAM) and then write 20h (space character code) 64 times

To clear CGRAM, set address at 40h (first CGRAM) and then write 00h (null data) 64 times

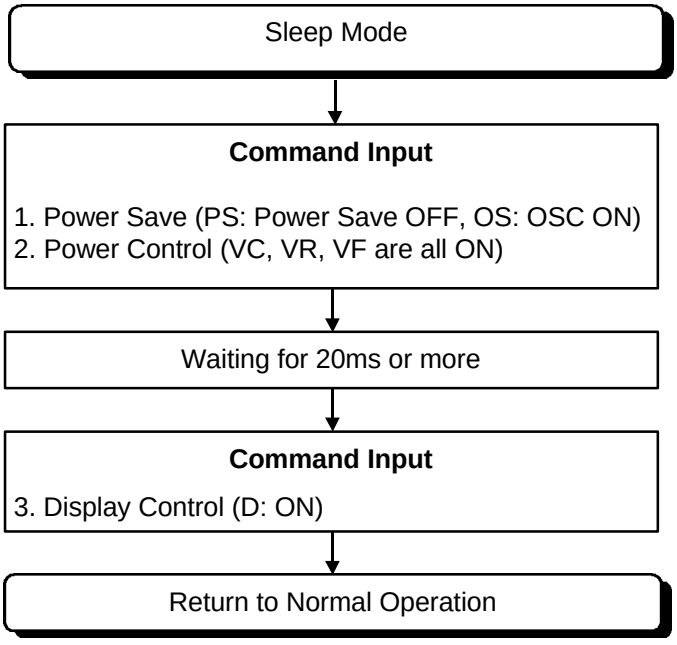
To clear ICONRAM, set ICONRAM address at 00h (first ICONRAM) and then write 00h (null data) 16 times.

Sleep Mode Set or Release by Instruction

a) Sleep Mode Set

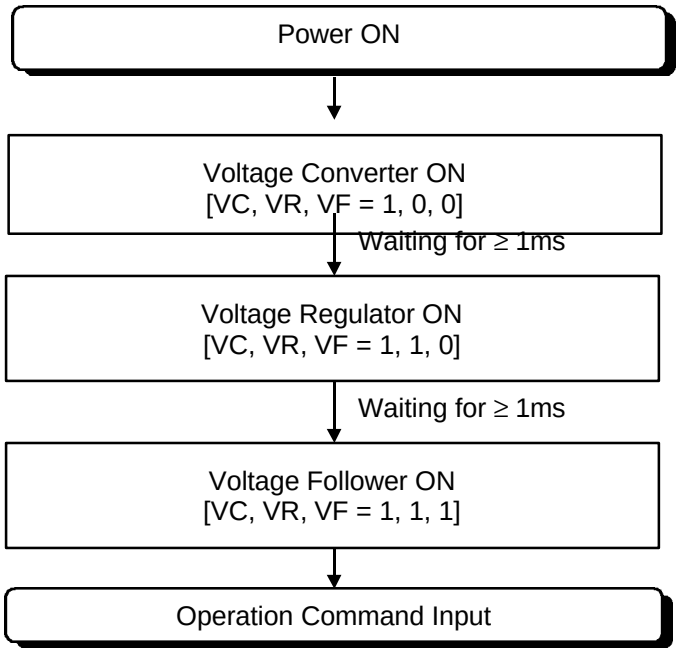


b) Sleep Mode Release

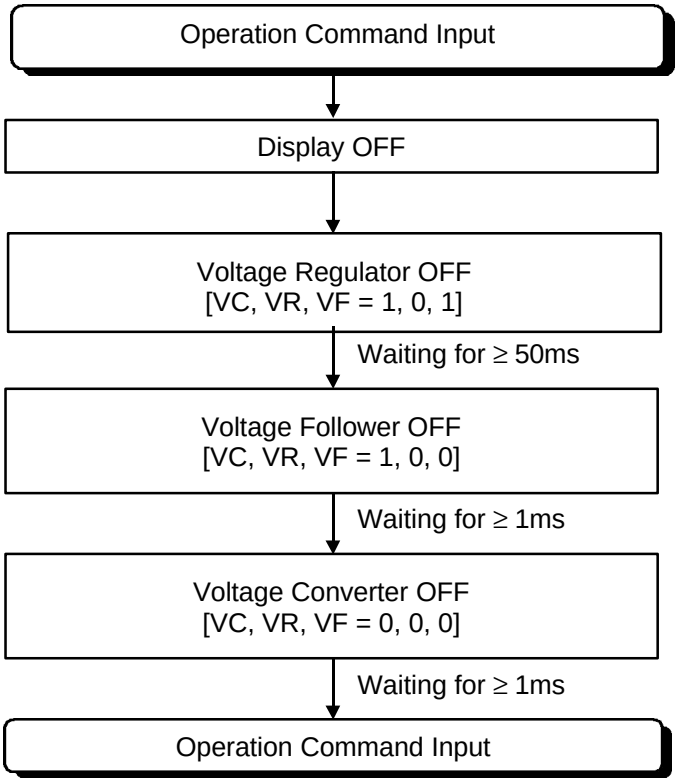


Recommendation of Power ON / OFF Sequence

a) Power ON Sequence



b) Power OFF Sequence



LCD DRIVING POWER SUPPLY CIRCUIT

The Power Supply Circuit produces LCD panel driving voltage at low power consumption. The LCD Driving Power Supply circuit consists of Voltage converter, Voltage regulator, and Voltage follower. It is controlled by power control instruction. Table 14 shows how the LCD Driving Power Supply circuit works by power control instruction sets.

Table 14. Power Supply Control Mode Set

VC VR VF	Voltage converter	Voltage regulator	Voltage follower	VOUT pin	VR pin	V0, V1, V2, V3, V4 pin
1 1 1	Enable	Enable	Enable	Internal voltage output	Used for voltage adjustment	Internal voltage output
0 1 1	Disable	Enable	Enable	External voltage input	Used for voltage adjustment	Internal voltage output
0 0 1	Disable	Disable	Enable	Open	Open	V1~V4: internal voltage output V0: external voltage input
0 0 0	Disable	Disable	Disable	Open	Open	V0~V4: external voltage input

NOTE: SEC recommendation is to use only the case listed above table.

VOLTAGE CONVERTER

The Voltage Converter circuit generates positive 4-time voltage of 1.8V that is generated internally. VOUT is generated from the voltage converter. And this conversion voltage is used in the built-in Voltage regulator circuit. This application circuit is same as 3-times DC/DC converter.

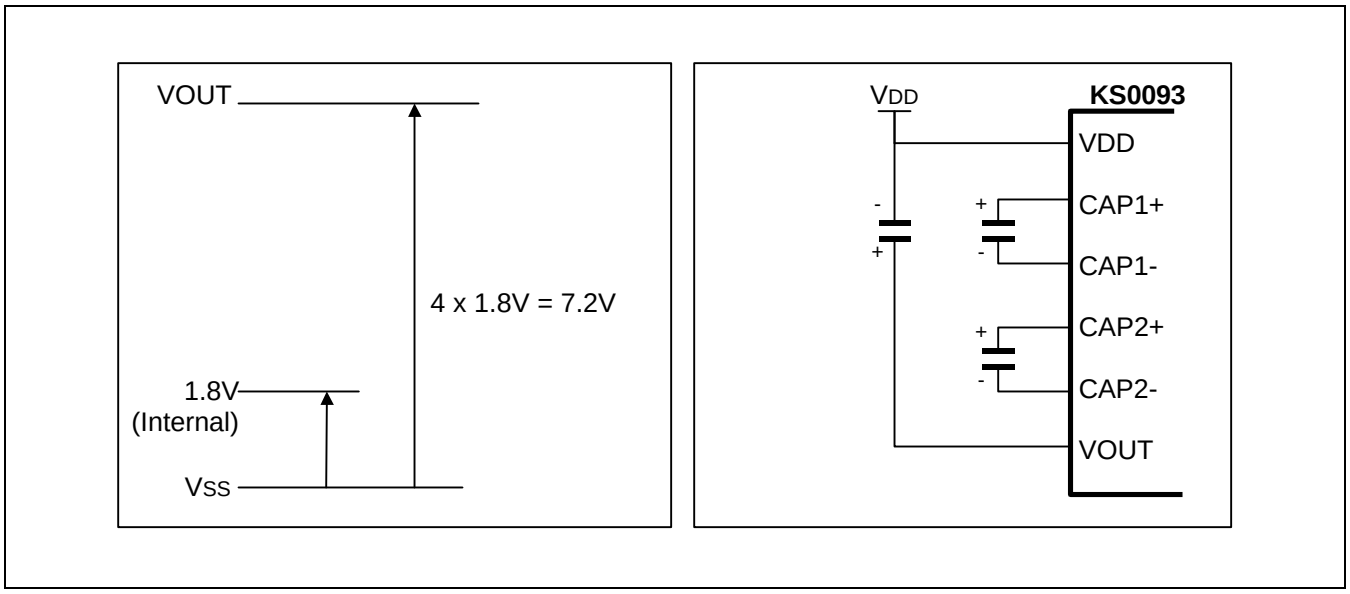


Figure 18. DC/DC Converter Output and Circuit

VOLTAGE REGULATOR

The Voltage Regulator circuit is used to obtain an appropriate LCD panel driving voltage. This voltage is obtained by adjusting resistors Ra and Rb as shown in equation (1) or (2), and by setting electronic contrast control data bits, see equation (3) or (4).

The potential of V0 Pin can be adjusted within VOUT - V_{REF}. V_{REF} is the internal constant voltage source of the chip and this value is 2.0V in the condition $V_{DD} \geq 2.4V$

The REF selects which voltage is used for voltage regulator between the external VEXT and the internal V_{REF}.

- Voltage regulation by adjusting resistors Ra, Rb

When REF is "Low"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{REF} \quad \text{--- (1)}$$

When REF is "High"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times VEXT \quad \text{--- (2)}$$

The internal V_{REF} of voltage regulator has the temperature compensation function, and the temperature coefficient is about 0.0%/°C.

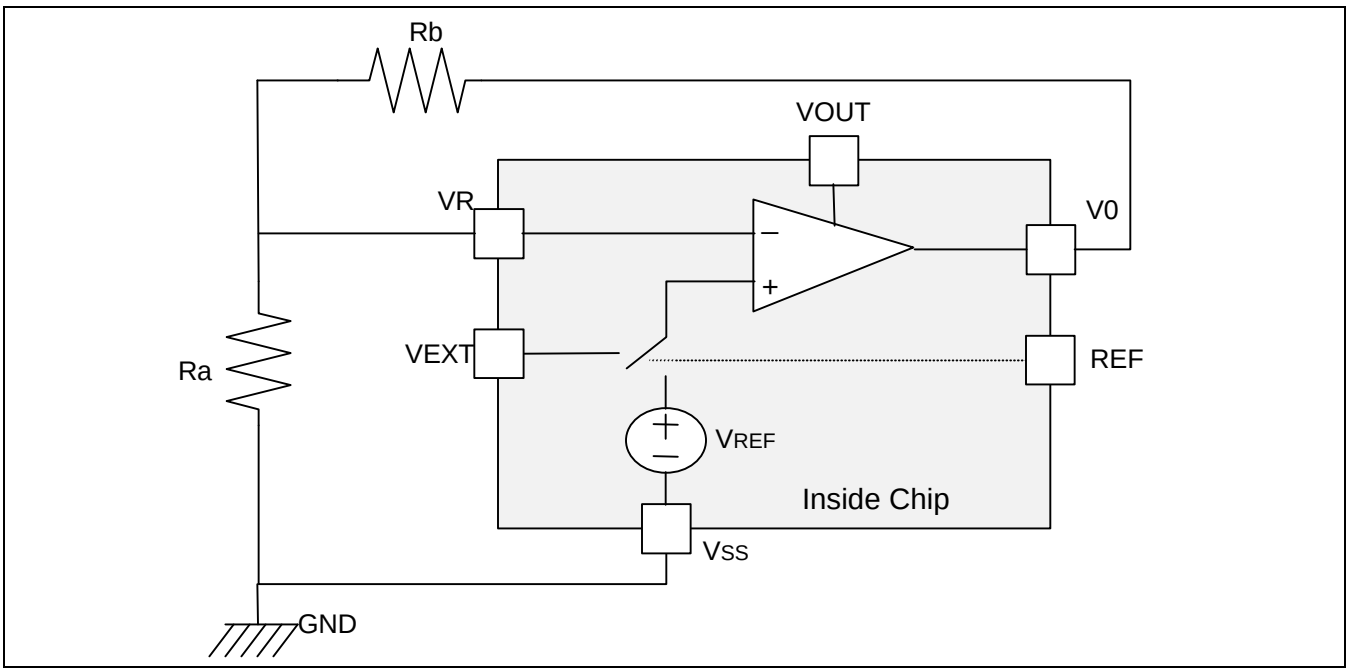


Figure 19. Voltage Regulator Circuit

ELECTRONIC CONTRAST CONTROL (32 STEPS)

Electronic Contrast Control data bits is 10h = (C4, C3, C2, C1, C0). Voltage regulation is adjusted as 32-contrast step according to the value of Electronic Contrast Control data bits. LCD drive voltage V0 has one of 32 voltage values if 5-bit data is set to the electronic contrast control register (ICONRAM address 10h). When using the Electronic Contrast Control function, you need to turn the voltage regulators on using power control instruction.

When REF = "Low"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad \text{--- (3)}$$

$V_{EV} = V_{REF} - n\alpha$ (n = 0, 1, 2, ..., 30, 31)

$\alpha = V_{REF} / 150$

When REF = "High"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad \text{--- (4)}$$

$V_{EV} = VEXT - n\alpha$ (n = 0, 1, 2, ..., 30, 31)

$\alpha = VEXT / 150$

Table 15. Electronic Contrast Control Register

No.	C7	C6	C5	C4	C3	C2	C1	C0	nα	V0	Contrast
1	-	-	-	0	0	0	0	0	0α (default)	Maximum	High
2	-	-	-	0	0	0	0	1	1α	.	.
3	-	-	-	0	0	0	1	0	2α	.	.
4	-	-	-	0	0	0	1	1	3α	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
31	-	-	-	1	1	1	1	0	30 α	.	.
32	-	-	-	1	1	1	1	1	31α	Minimum	Low

("-": Don't care)

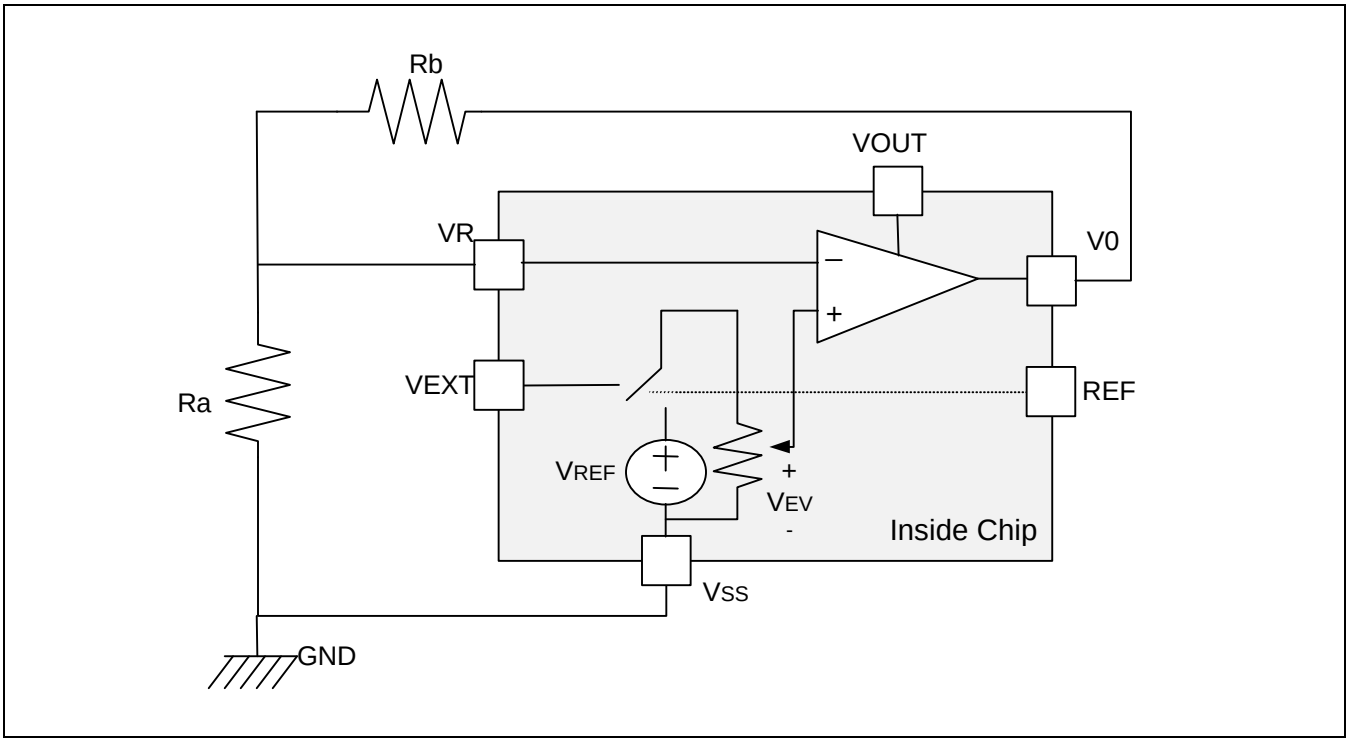


Figure 20. Electronic Contrast Control Circuit

VOLTAGE GENERATOR CIRCUIT

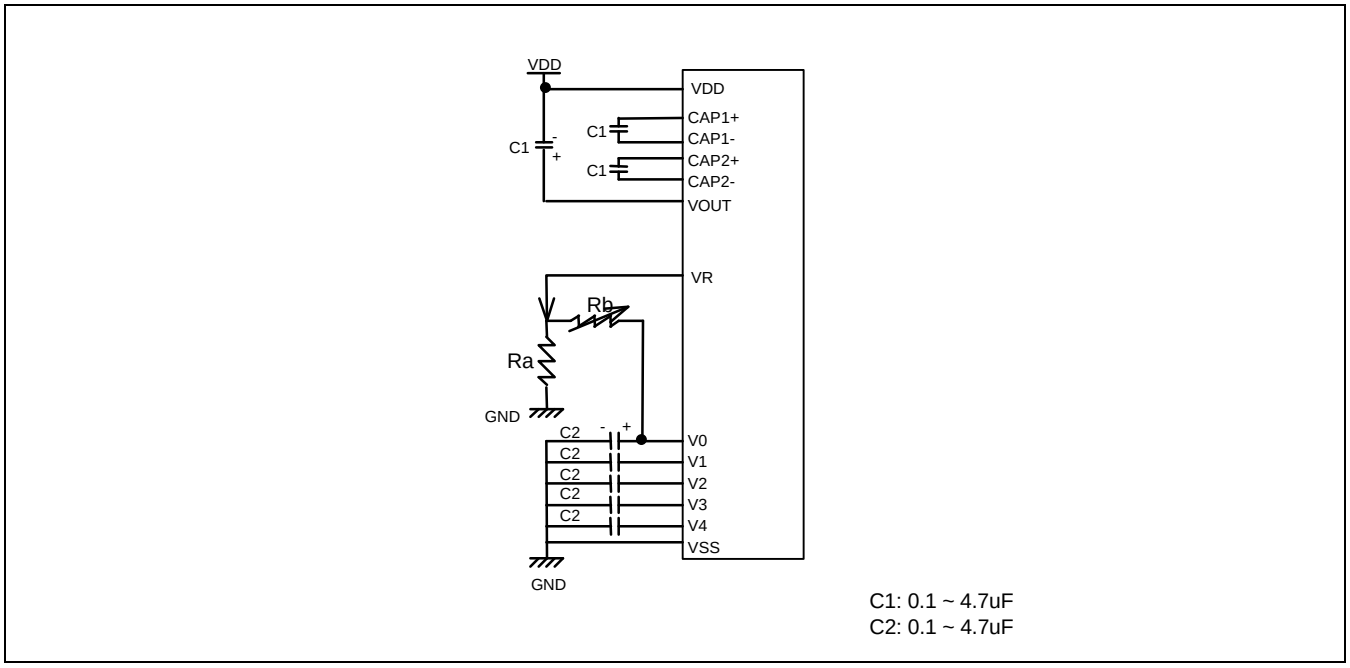


Figure 21. When Built-in Power Supply is used (VC, VR, VF = 1, 1, 1)

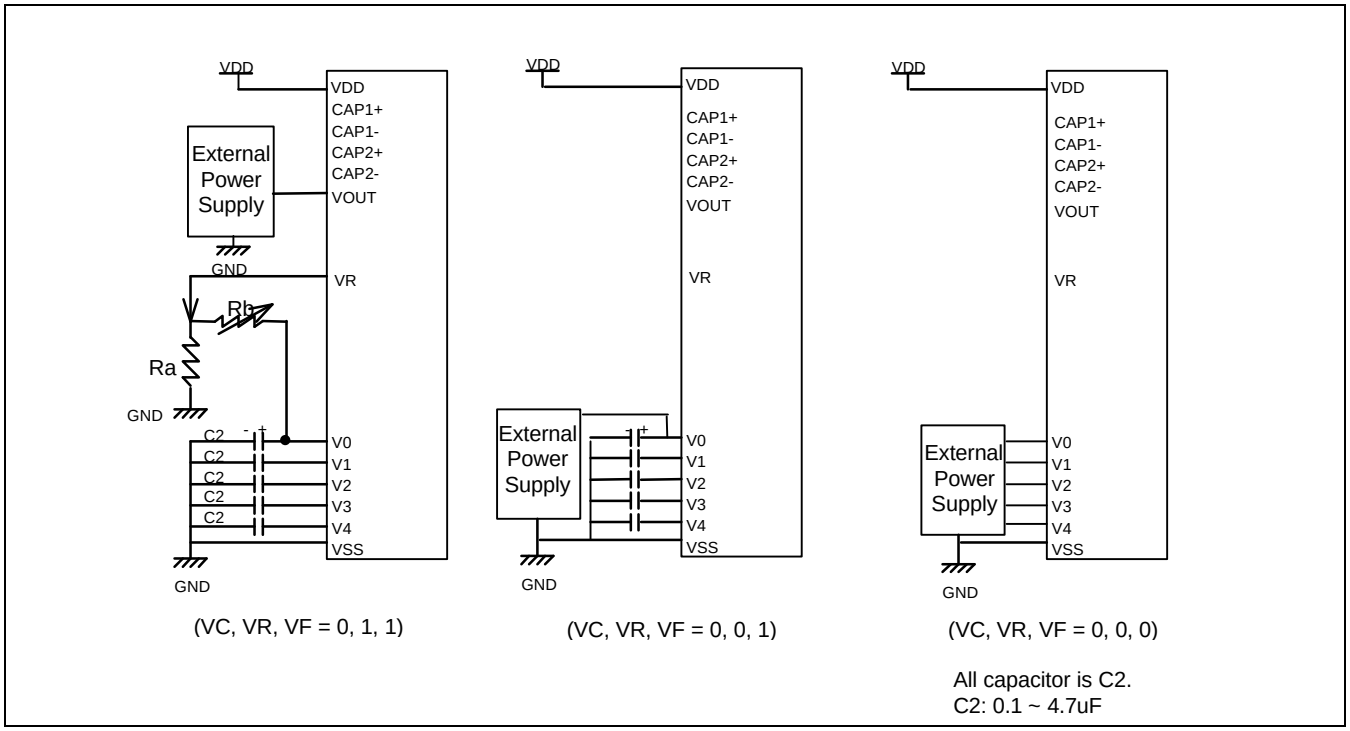


Figure 22. When External Power Supply is used

MPU INTERFACE

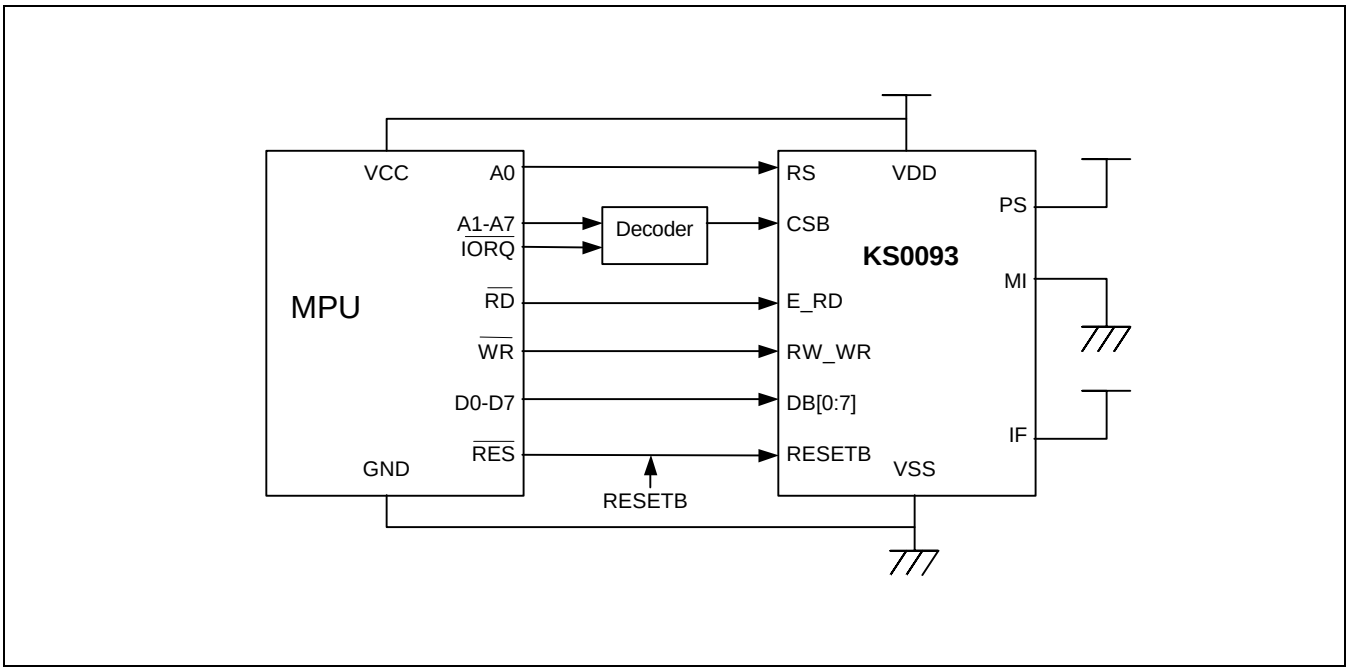


Figure 23. Parallel Interfacing with 8080-series Microprocessors

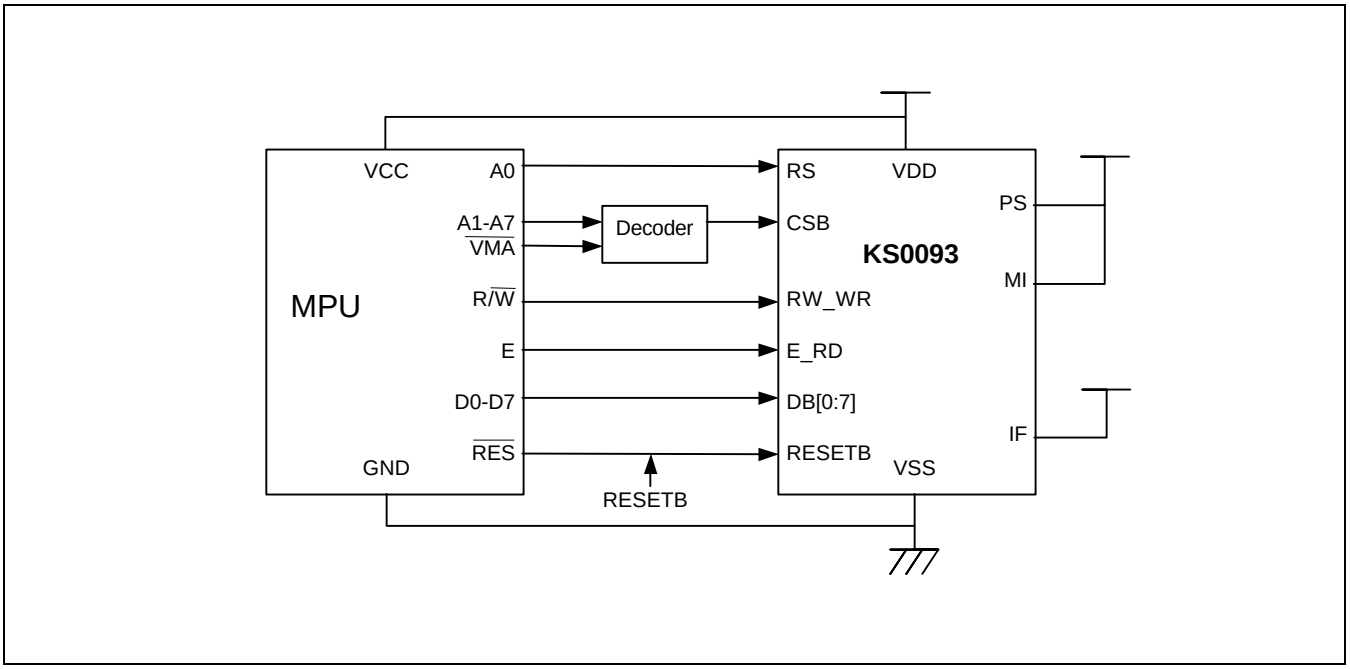


Figure 24. Parallel Interfacing with 6800-series Microprocessors

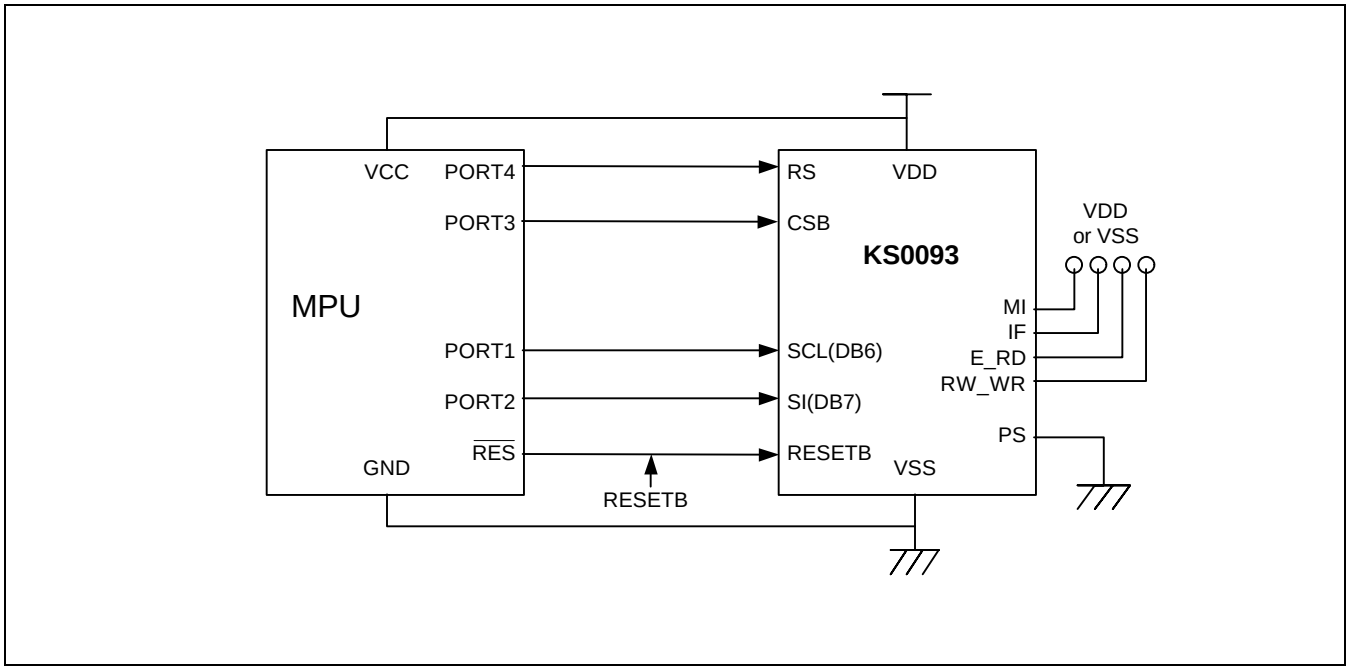
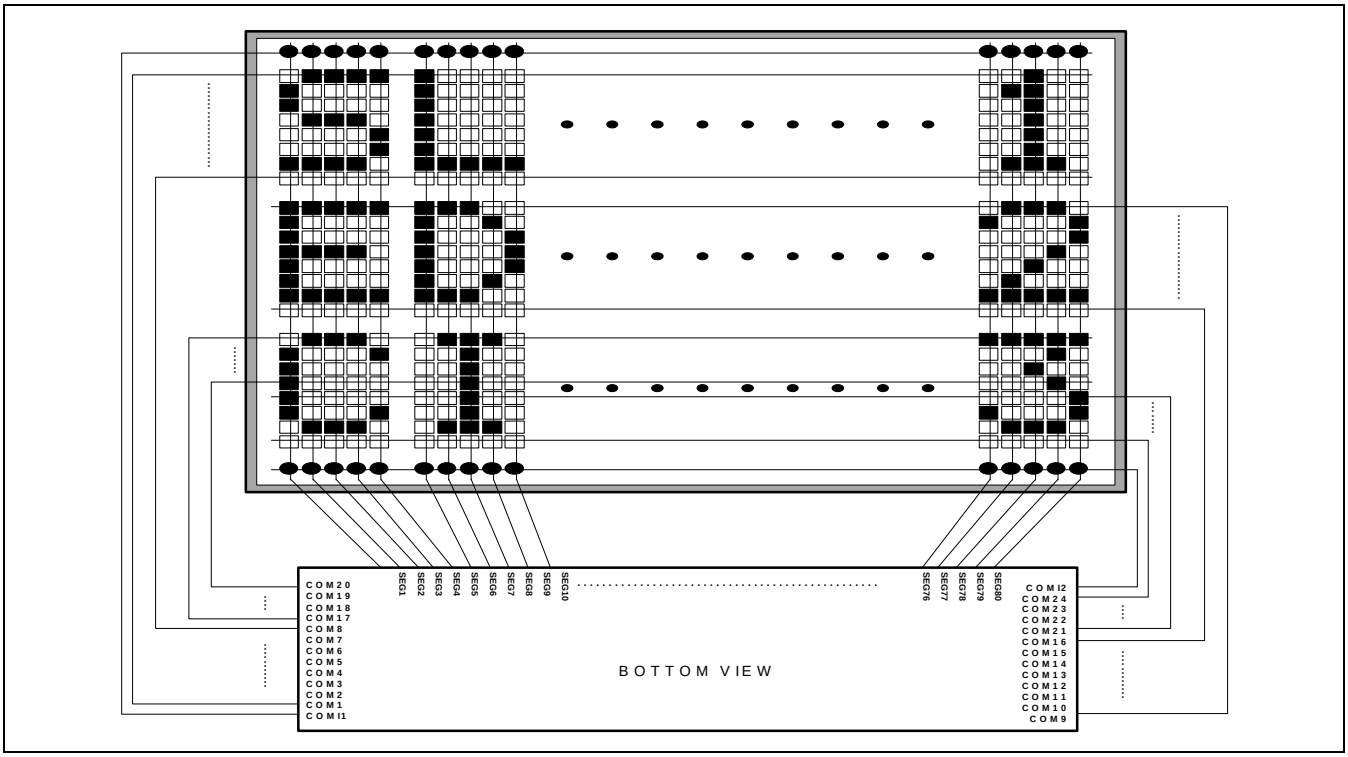


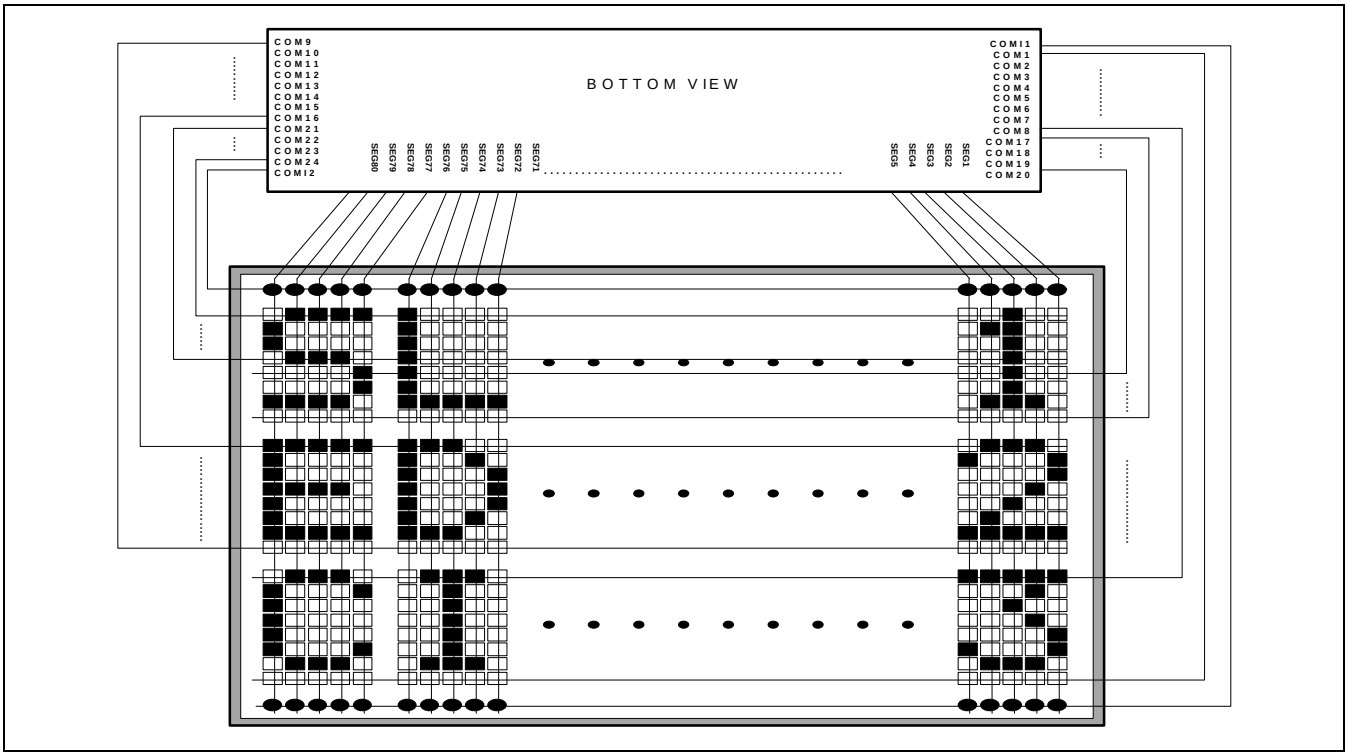
Figure 25. Clock Synchronized Serial Interfacing with any Microprocessors

APPLICATION INFORMATION FOR LCD PANEL

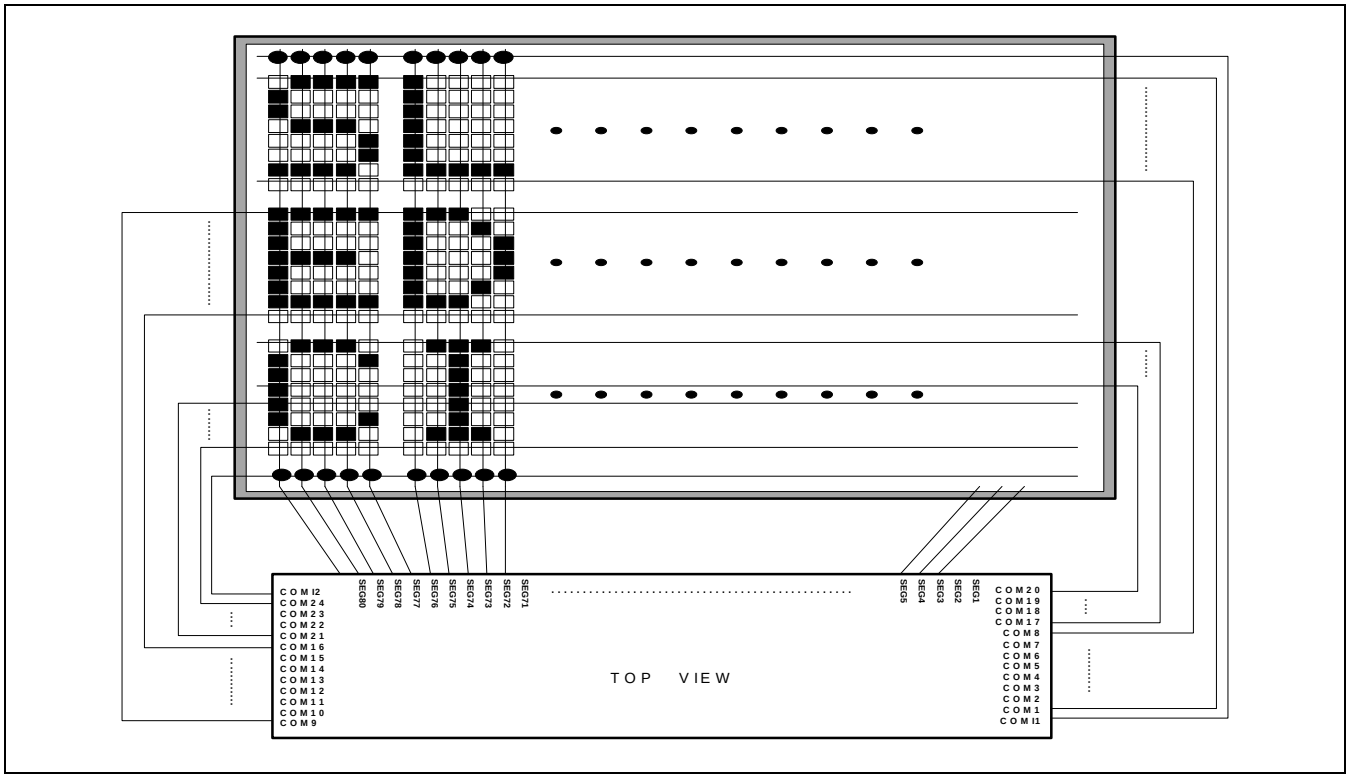
Chip Bottom & Lower View (S bit = "0", DIRS = "0")



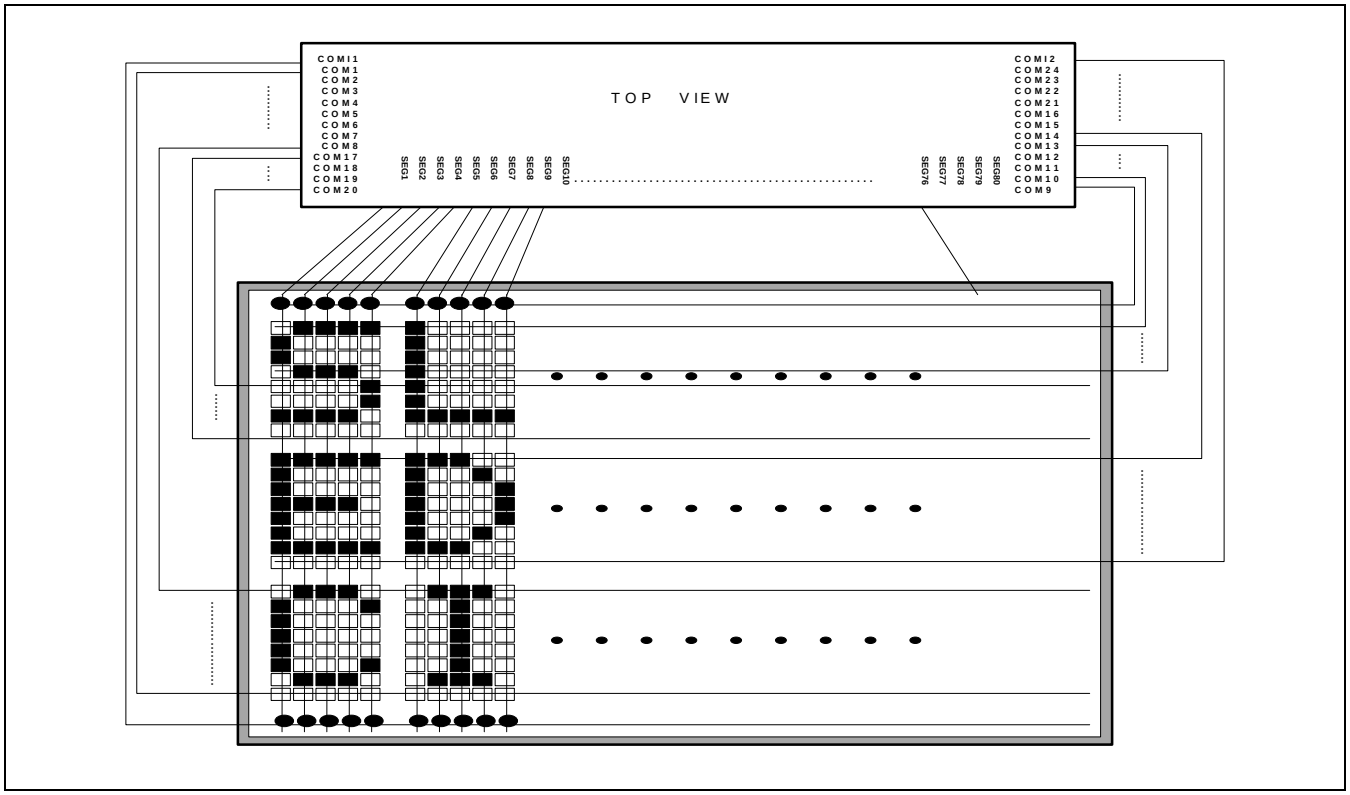
Chip Bottom & Upper View (S bit = "1", DIRS = "1")



Chip Top & Lower View (S bit = "0", DIRS = "1")



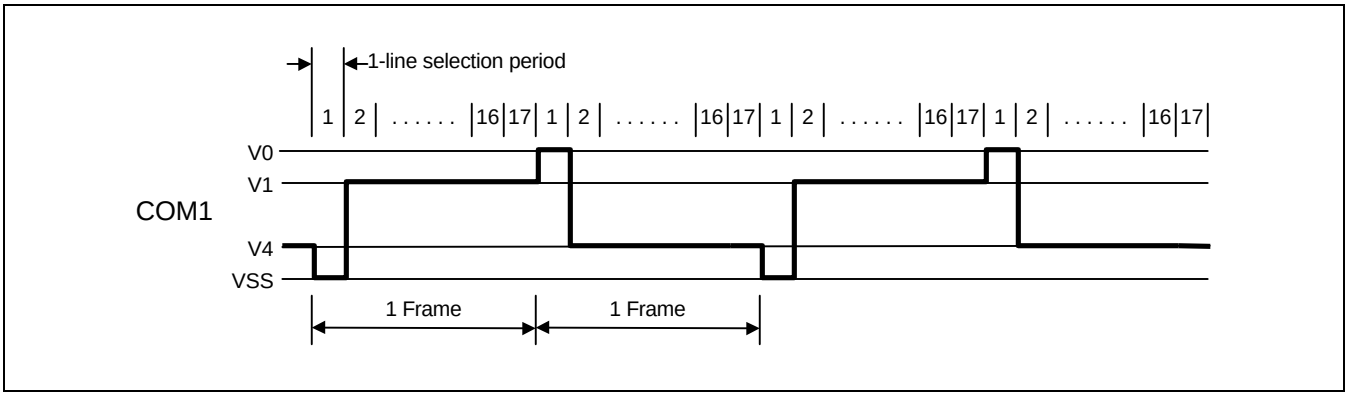
Chip Top & Upper View (S bit = "1", DIRS = "0")



SAMSUNG ELECTRONICS

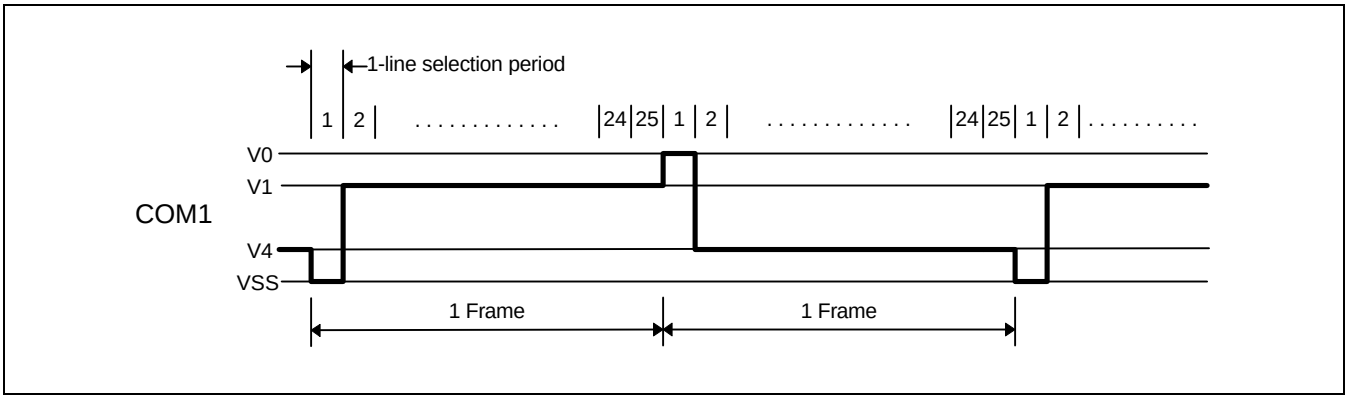
FRAME FREQUENCY

1/17 Duty (2-line mode)



1-line Selection Period = 16 Clocks
One Frame = 16 x 17 x 36.8 µs = 10.0 ms (1 Clock = 36.8 µs at fOSC =27.2 kHz)
Frame Frequency = 1 / 10.0 ms = 100 Hz

1/25 Duty (3-line mode)



1-line Selection Period = 16 Clocks
One Frame = 16 x 25 x 25 µs = 10.0 ms (1 Clock = 25 µs at fOSC =40 kHz)
Frame Frequency = 1 / 10.0 ms = 100 Hz

MAXIMUM ABSOLUTE RATINGS

Table 16. Maximum Absolute Ratings

Characteristic	Symbol	Value	Unit
Power supply voltage (1)	V_{DD}	-0.3 to + 7.0	V
Power supply voltage (2)	VOUT, V0	-0.3 to + 8.0	V
Power supply voltage (3)	V1, V2, V3, V4	-0.3 to V0	V
Input voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating temperature	T_{OPR}	-30 to +85	^{o}C
Storage temperature	T_{STG}	-55 to +125	^{o}C

NOTES:

1. All the voltage levels are based on VSS = 0V.
2. Voltage greater than above may damage the circuit.
   Voltage level: VOUT ≥ V0 ≥ VDD ≥ VSS
3. Voltage level: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Table 17. DC Characteristics

(V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage		V_{DD}	-	2.4	-	3.6	V
Supply current (V_{DD} = 3V, Ta = 25 °C)		I_{DD1}	Display operation V_{LCD} = 6V without load No access from MPU	-	-	80	µA
		I_{DD2}	Access operation from MPU (fcyc = 200kHz)	-	-	500	
		I_{DDS1}	Sleep operation without load oscillator OFF, power save ON	-	-	5	
Input voltage (1)		V_{IH}	-	0.7V_{DD}		V_{DD}	V
		V_{IL}	-	V_{SS}		0.3V_{DD}	
Output voltage		V_{OH}	I_{OH} = -1mA, V_{DD} = 2.4V	V_{DD}-0.4			V
		V_{OL}	I_{OL} = 1mA, V_{DD} = 2.4V			0.4	
Input leakage current		I_{IZ}	V_{IN} = 0V to V_{DD}	-1	-	1	µA
Output leakage current		I_{OZ}	V_{IN} = 0V to V_{DD}	-3		3	µA
R_{ON} resistance		R_{COM}	Io = ±50µA	-	-	5	kΩ
		R_{SEG}	Io = ±50µA	-	-	10	
Frame frequency (internal OSC)		f_{FR}	V_{DD} = 3V, Ta = 25 °C	70	100	130	Hz
Voltage converter	Conversion efficiency	V_{EF}	RL = ∞	95	99	-	%
	Output voltage	V_{OUT}	Ta = 25 °C, C = 1µF	6.9	7.2	7.5	V
Voltage regulator reference voltage		V_{REF}	Ta = 25 °C	1.94	2.0	2.06	V
LCD driving voltage		V_{LCD}	V_{LCD} = V0 - V_{SS}	4.0	-	6.0	

NOTE:

1. RESETB pin is schmitt input (0.8VDD ≤ VIH ≤ VDD, VSS ≤ VIL ≤ 0.2VDD).

Table 18. DC Characteristics

(V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage		V_{DD}	-	3.6	-	5.5	V
Supply current (V_{DD} = 5V, Ta = 25 °C)		I_{DD1}	Display operation V_{LCD} = 6V without load No access from MPU	-	-	100	µA
		I_{DD2}	Access operation from MPU (fcyc = 200kHz)	-	-	1000	
		I_{DDS1}	Sleep operation without load oscillator OFF, power save ON	-	-	10	
Input voltage (1)		V_{IH}	-	0.7V_{DD}		V_{DD}	V
		V_{IL}	-	V_{SS}		0.3V_{DD}	
Output voltage		V_{OH}	I_{OH} = -1mA, V_{DD} = 4.0V	V_{DD}-0.4			V
		V_{OL}	I_{OL} = 1mA, V_{DD} = 4.0V			0.4	
Input leakage current		I_{IZ}	V_{IN} = 0V to V_{DD}	-1	-	1	µA
Output leakage current		I_{OZ}	V_{IN} = 0V to V_{DD}	-3		3	µA
R_{ON} resistance		R_{COM}	Io = ±50µA	-	-	5	kΩ
		R_{SEG}	Io = ±50µA	-	-	10	
Frame frequency (internal OSC)		f_{FR}	V_{DD} = 5V, Ta = 25 °C	70	100	130	Hz
Voltage converter	Conversion efficiency	V_{EF}	RL = ∞	95	99	-	%
	Output voltage	V_{OUT}	Ta = 25 °C, C = 1µF	6.9	7.2	7.5	V
Voltage regulator reference voltage		V_{REF}	Ta = 25 °C	1.94	2.0	2.06	V
LCD driving voltage		V_{LCD}	V_{LCD} = V0 - V_{SS}	4.0	-	6.0	

NOTE:

1. RESETB pin is schmitt input (0.8VDD ≤ VIH ≤ VDD, VSS ≤ VIL ≤ 0.2VDD).

AC CHARACTERISTICS

Parallel Write Interface (68 Mode)

(V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	T_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
E_RD pulse width high	T_{WH}	450	-	-	
E_RD pulse width low	T_{WL}	150	-	-	
RS and CSB setup time	t_{SU1}	60	-	-	
RS and CSB hold time	t_{H1}	30	-	-	
DB setup time	t_{SU2}	100	-	-	
DB hold time	t_{H2}	50	-	-	

(V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	T_C	350	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
E_RD pulse width high	T_{WH}	250	-	-	
E_RD pulse width low	T_{WL}	150	-	-	
RS and CSB setup time	t_{SU1}	40	-	-	
RS and CSB hold time	t_{H1}	10	-	-	
DB setup time	t_{SU2}	40	-	-	
DB hold time	t_{H2}	10	-	-	

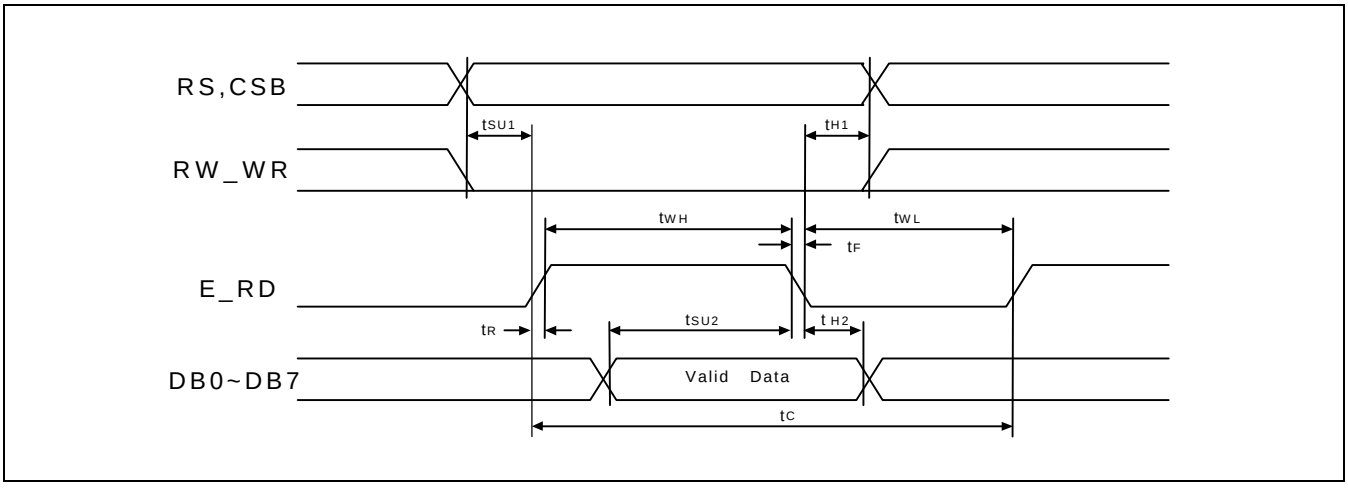


Figure 26. Write Timing Diagram (68-series)

Parallel Read Interface (68 Mode)

(V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
E_RD pulse width high	t_{WH}	450	-	-	
E_RD pulse width low	t_{WL}	150	-	-	
RS and CSB setup time	t_{SU}	60	-	-	
RS and CSB hold time	t_H	30	-	-	
DB output delay time	t_D	100	-	-	
DB output hold time	t_{DH}	50	-	-	

(V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
E_RD pulse width high	t_{WH}	450	-	-	
E_RD pulse width low	t_{WL}	150	-	-	
RS and CSB setup time	t_{SU}	60	-	-	
RS and CSB hold time	t_H	30	-	-	
DB output delay time	t_D	100	-	-	
DB output hold time	t_{DH}	50	-	-	

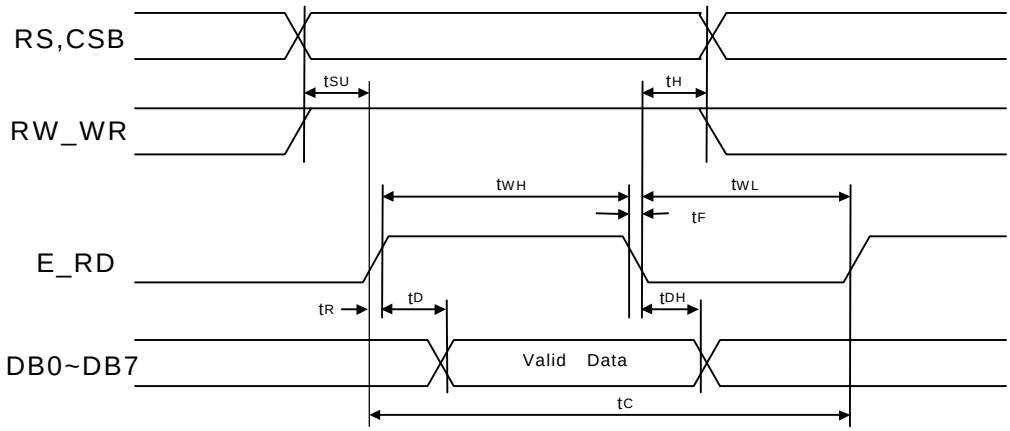


Figure 27. Read Timing Diagram (68-seres)

Parallel Write Interface (80 Mode)

(V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
RW_WR cycle time	t_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
RW_WR pulse width high	t_{WH}	150	-	-	
RW_WR pulse width low	t_{WL}	450	-	-	
RS and CSB setup time	t_{SU1}	60	-	-	
RS and CSB hold time	t_{H1}	30	-	-	
DB setup time	t_{SU2}	100	-	-	
DB hold time	t_{H2}	50	-	-	

(V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
RW_WR cycle time	t_C	350	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
RW_WR pulse width high	t_{WH}	100	-	-	
RW_WR pulse width low	t_{WL}	250	-	-	
RS and CSB setup time	t_{SU1}	40	-	-	
RS and CSB hold time	t_{H1}	10	-	-	
DB setup time	t_{SU2}	40	-	-	
DB hold time	t_{H2}	10	-	-	

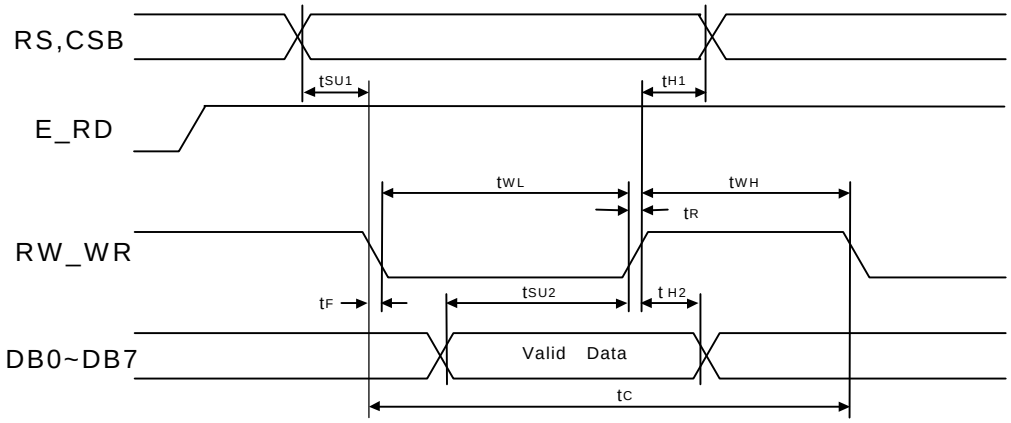


Figure 28. Write Timing Diagram (80-series)

Parallel Read Interface (80 Mode)

(V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
E_RD pulse width high	t_{WH}	150	-	-	
E_RD pulse width low	t_{WL}	450	-	-	
RS and CSB setup time	t_{SU}	60	-	-	
RS and CSB hold time	t_H	30	-	-	
DB output delay time	t_D	100	-	-	
DB output hold time	t_{DH}	50	-	-	

(V_{DD} = 3.6V to 5.5V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
E_RD pulse width high	t_{WH}	150	-	-	
E_RD pulse width low	t_{WL}	450	-	-	
RS and CSB setup time	t_{SU}	60	-	-	
RS and CSB hold time	t_H	30	-	-	
DB output delay time	t_D	100	-	-	
DB output hold time	t_{DH}	50	-	-	

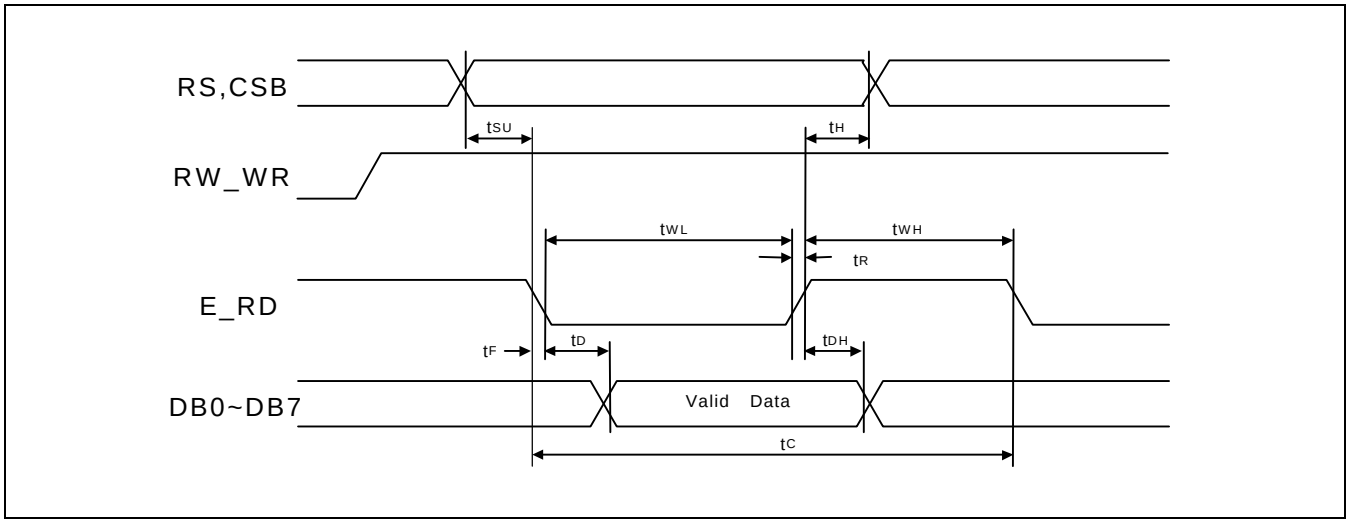


Figure 29. Read Timing Diagram (80-series)

Clock Synchronized Serial Mode

(V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min	Typ	Max	Unit
SCL clock cycle time	t_C	1000	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
SCL clock width (high, low)	t_W	300	-	-	
CSB setup time	t_{SU1}	150	-	-	
CSB hold time	t_{H1}	700	-	-	
RS data setup time	t_{SU2}	50	-	-	
RS data hold time	t_{H2}	300	-	-	
SI data setup time	t_{SU3}	50	-	-	
SI data hold time	t_{H3}	50			

(V_{DD} = 2.4V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min	Typ	Max	Unit
SCL clock cycle time	t_C	600	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
SCL clock width (high, low)	t_W	200	-	-	
CSB setup time	t_{SU1}	100	-	-	
CSB hold time	t_{H1}	400	-	-	
RS data setup time	t_{SU2}	50	-	-	
RS data hold time	t_{H2}	200	-	-	
SI data setup time	t_{SU3}	40	-	-	
SI data hold time	t_{H3}	40			

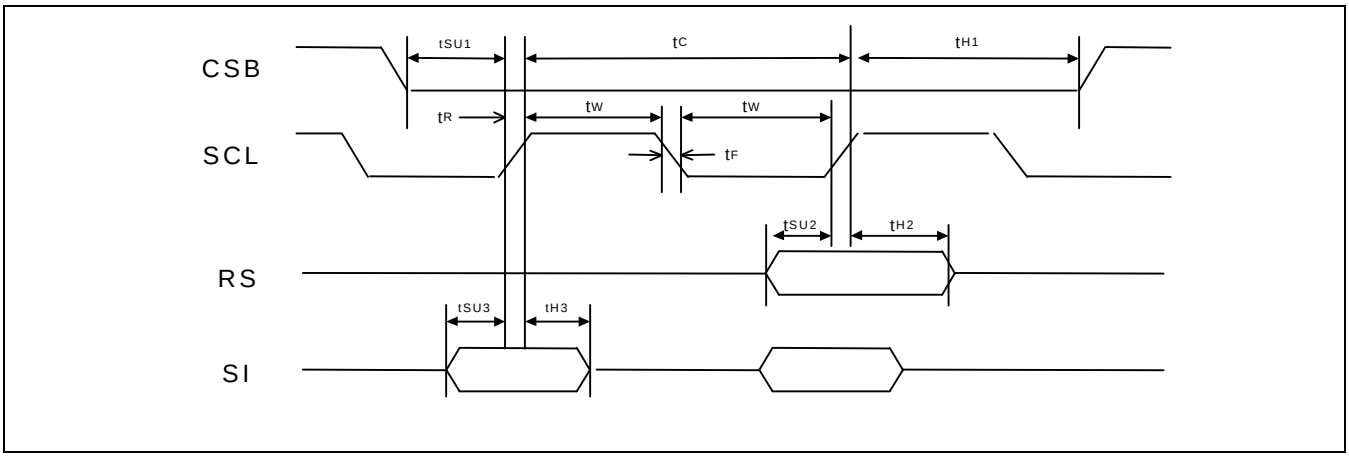


Figure 30. Clock Synchronized Serial Interface Mode Timing Diagram