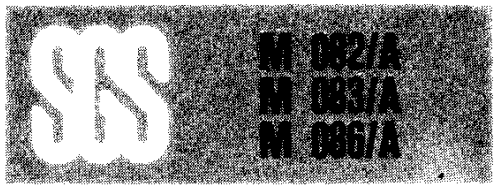
MOS INTEGRATED CIRCUITS



PRELIMINARY DATA

TONE GENERATOR

- SINGLE POWER SUPPLY
- WIDE SUPPLY VOLTAGE OPERATING RANGE
- LOW POWER DISSIPATION < 500 mW
- 13 (M082/A, M083/A) OR 12 (M086/A) TONE OUTPUTS
- HIGH OUTPUT DRIVE CAPABILITY
- HIGH ACCURACY OF OUTPUT FREQUENCIES: ERROR LESS THAN ± 0.069%
- INPUT PROTECTED AGAINST STATIC CHARGES
- LOW INTERMODULATION

The M082/A, M083/A and M086/A are monolithic tone generators specifically designed for electronic organs. The only difference between the M082, M083, M086 and the M082A, M083A, M086A is the maximum input clock frequency, which is 4500 KHz for the standard types and 2500 KHz for the "A" types. Constructed on a single chip using low threshold N-channel silicon gate technology they are supplied in a 16 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

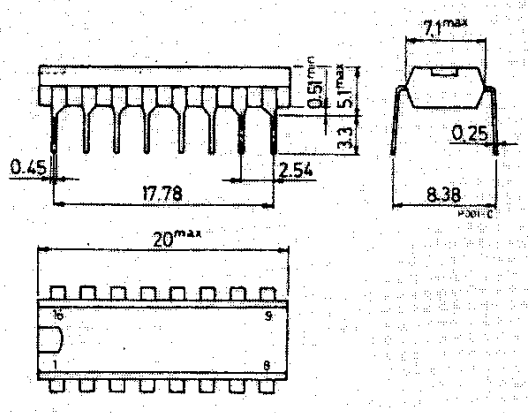
V_i	Voltage on any pin relative to V_{SS} (GND)	+20 to -0.3	V
T_{op}	Operating temperature	0 to 50	°C
T_{stg}	Storage temperature	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

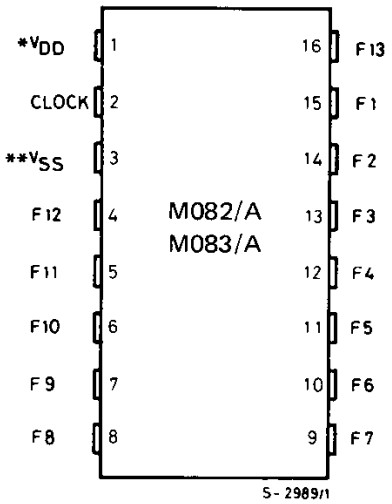
ORDERING NUMBERS: M082B1 M082A B1
M083B1 M083A B1
M086B1 M086A B1

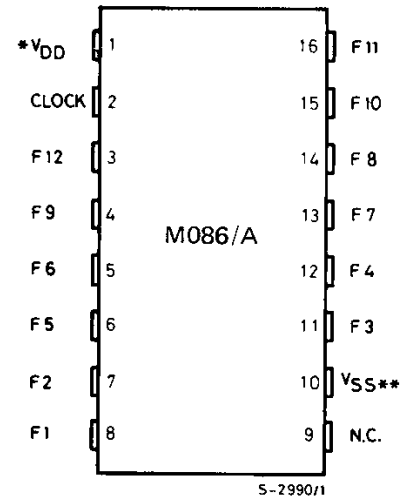
MECHANICAL DATA

Dimensions in mm



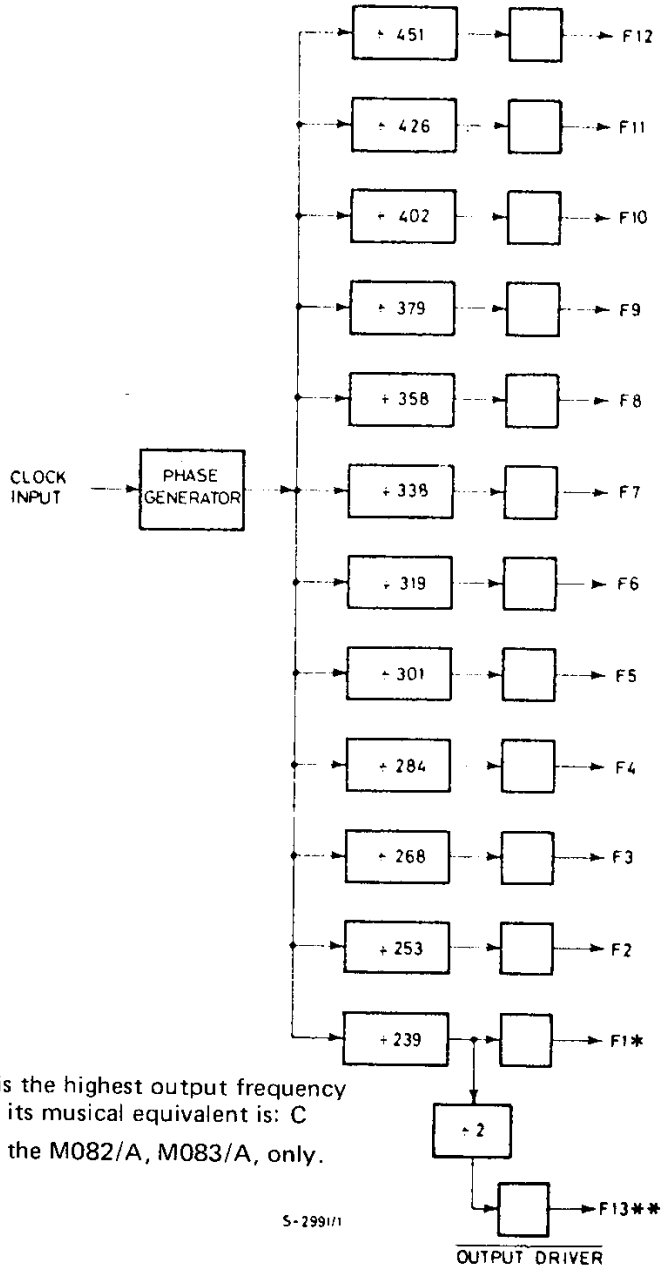
PIN CONNECTIONS





* V_{DD} is the highest supply voltage
** V_{SS} is the lowest supply voltage

BLOCK DIAGRAM



* F1 is the highest output frequency and its musical equivalent is: C
** For the M082/A, M083/A, only.

RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		+10	+12	+14	V

ELECTRICAL CHARACTERISTICS ($0°C \leq T_{amb} \leq 50°C$; $V_{SS}=0V$; $V_{DD}=+10V$ to $+14V$ unless otherwise specified)

Parameter		Test conditions	Values			Unit	Fig.
			Min.	Typ.	Max.		
V_{IL}	Input clock, low		V_{SS}		$V_{SS}+1$	V	1
V_{IH}	Input clock, high		$V_{DD}-1$		V_{DD}	V	
t_r, t_f	Input clock rise and fall times 10% to 90%	4.5 MHz			30	ns	1
t_{on}, t_{off}	Input clock on and off times	4.5 MHz		111		ns	1
C_I	Input capacitance			5	10	pF	
V_{OH}	Output high	0.75 mA	$V_{DD}-1.5$		V_{DD}	V	2
V_{OL}	Output low	0.70 mA	V_{SS}		$V_{SS}+1$	V	2
t_{ro}, t_{fo}	Output rise and fall times 500 pF load		250		2500	ns	3
t_{on}, t_{off}	Output duty cycle	M 082		30		%	
		M 083, M 086		50			
I_{DD}	Supply current			24	35	mA	*
f_I	Input clock frequency	M082, M083, M086	100	4000.48	4500	kHz	
f_I	Input clock frequency	M082A, M083A, M086A	100	2000.24	2500	kHz	

* Output unloaded.

Fig. 1 Input clock waveform

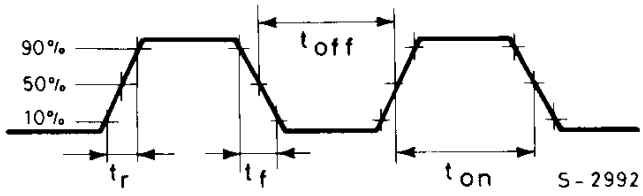
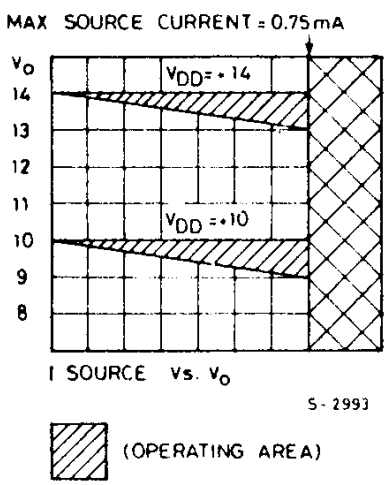


Fig. 2 - Output signal d.c. loading



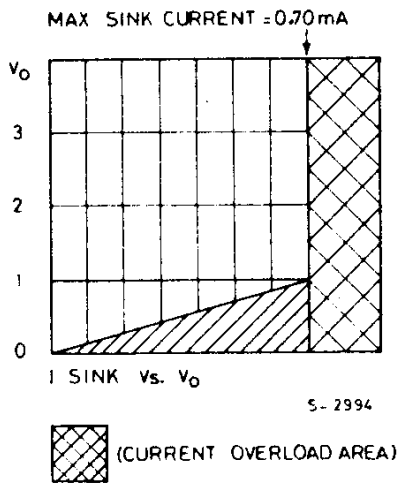
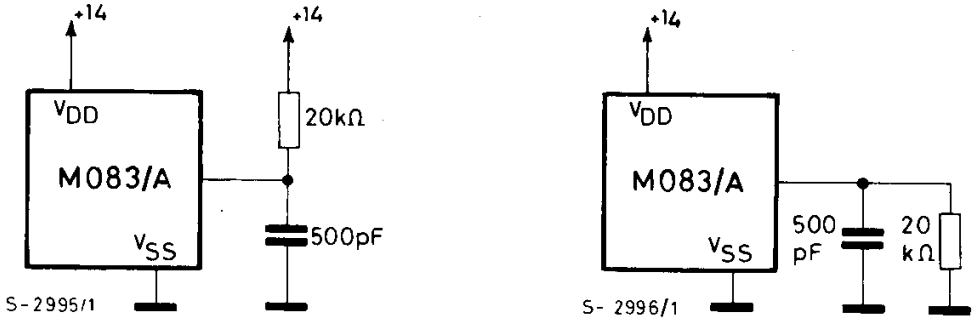
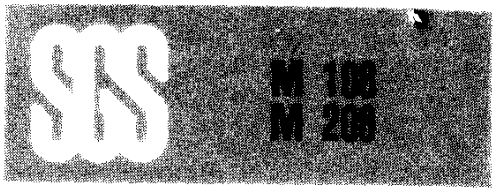


Fig. 3 - Output loading



MOS INTEGRATED CIRCUITS



PRELIMINARY DATA

SINGLE CHIP ORGAN (SOLO + ACCOMPANIMENT)

- SIMPLE KEY SWITCH REQUIREMENTS FOR 61 KEYS, IN A MATRIX OF 12 x 6
- LOW TIME REQUIRED FOR A SCANNING CYCLE OF 576 μsec.
- ACCEPTANCE OF ALL KEYS PRESSED
- TWO KEYBOARD FORMATS: 61 KEYS (SOLO) OR 24+37 (M108), 17+44 (M208) KEYS (ACC. + SOLO) WITH POSSIBILITY OF AUTOMATIC CHORDS OF THE "ACCOMPANIMENT" SECTION
- TOP OCTAVE SYTHESIZER INCORPORATED FOR GENERATION OF 3 "FOOTAGES"
- MORE THAN ONE CHIP CAN BE EMPLOYED WITH SYNCHRONIZATION THROUGH THE RESET INPUT
- SEPARATED ANALOG OUTPUTS (FOR EACH FOOT) FOR "SOLO", "ACC." AND "BASS" SECTIONS (SQUARE WAVE 50% D.C.) WITH AVERAGE VALUE CONSTANT
- INTERNAL ANTI-BOUNCE CIRCUITS
- KEY DOWN AND TRIGGER OUTPUTS FOR "SOLO", "ACC." AND "BASS" SECTIONS
- SUSTAIN FOR THE LAST KEYS RELEASED IN THE "SOLO" SECTION
- CHOICE OF OPERATING MODE IN "ACC." SECTION
  - MANUAL, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEYS (FREE CHORDS WITH ALTERNATE BASS)
  - AUTOMATIC, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEY (PRIORITY TO THE LEFT FOR AUTOMATIC CHORDS AND BASS ARPEGGIO)
- MULTIPLE CHOICE POSSIBILITY ON THE CHORDS IN AUTOMATIC MODE
  - MAJOR OR MINOR THIRD
  - WITH OR WITHOUT SEVENTH
- LOW DISSIPATION OF $\leqslant$ 600 mW
- STANDARD SINGLE SUPPLY OF +12V $\pm$ 5%
- INPUTS PROTECTED FROM ELECTROSTATIC DISCHARGES

The M108 and M208 are realized on a single monilithic chip using N-channel silicon gate technology. They are available in a 40 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Source supply voltage	-0.3 to +20 V
V_i **	Input voltage	-0.3 to +20 V
I_o	Output current (at any pin)	3 mA
T_{stg}	Storage temperature	-65 to 150 °C
T_{op}	Operating temperature	0 to 50 °C

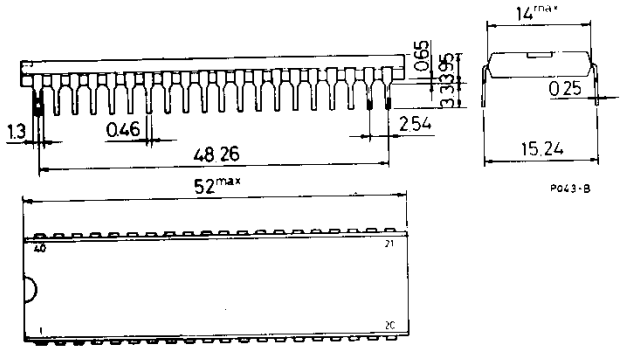
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** This voltage is with respect to V_{SS} (GND) pin voltage.

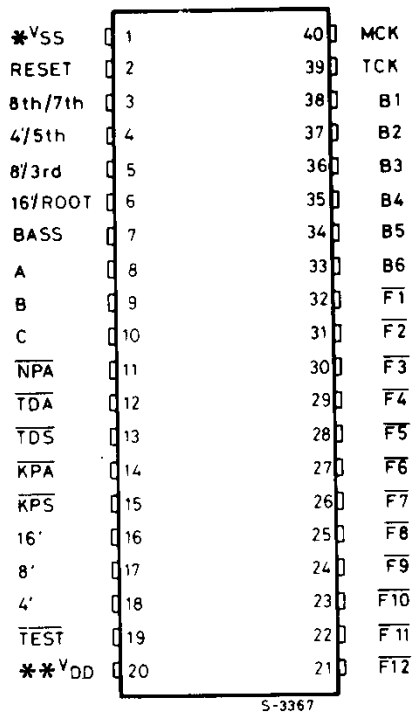
ORDERING NUMBERS: M 108 B1 for dual in-line plastic package
M 208 B1 for dual in-line plastic package

MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package

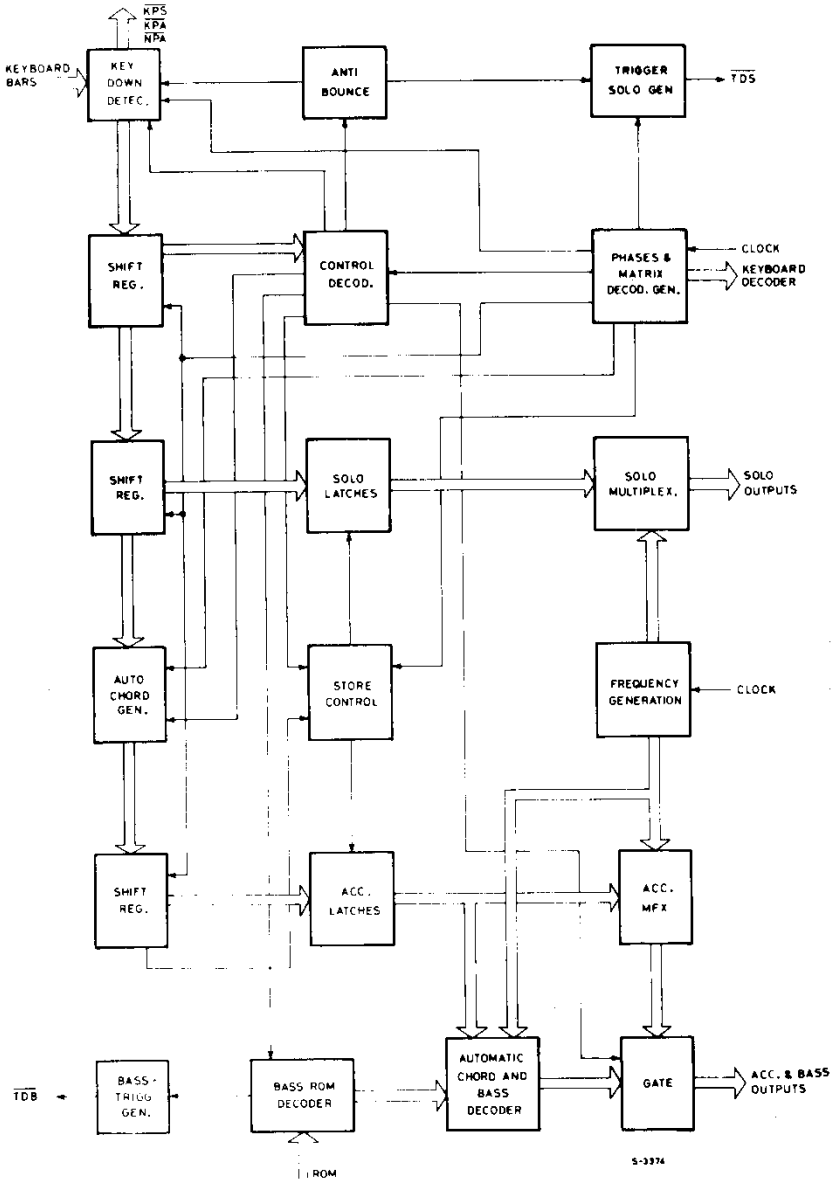


PIN CONNECTIONS



* V_{SS} is the lowest supply voltage
** V_{DD} is the highest supply voltage

BLOCK DIAGRAM



GENERAL CHARACTERISTICS

The caracteristics of the M208 are similar to those of the M108; the only difference is the keyboard split, which is 24+37 for the M108 and 17+44 for the M208 when used in "accompaniment + solo" mode.

The circuit comprises:

a) 2 pins for clock input: one for the matrix scanning, the other for the incorporated T.O.S.; by connecting both the clock inputs to the same matrix scanning clock (1000.12 KHz), the three "footages" generated are 16', 8' and 4'.

b) 6 inputs from the octave bars (keyboard and control scanning

c) 3 multiplexed data inputs for addressing the bass selection. These inputs normally come from the outputs of an external memory (negative or positive logic with control inside the chip)

d) 8 signal outputs divided by section: 3 for the "SOLO" section (16', 8', 4'), 4 for the "ACC." section (16' or root, 8' or 3rd, 4' or 5th, 8th/7th according to operating mode), 1 for the bass

e) 12 outputs for the matrix scanning

f) 5 "trigger" and "key down" outputs: $\overline{KPS}$ (key pressed "SOLO"), $\overline{TDS}$ (trigger decay "SOLO"), $\overline{KPA}$ (key pressed "ACC."), $\overline{NPA}$ (pitch present in "ACC." outputs), $\overline{TDB}$ (trigger decay "BASS") respectively. These outputs, in conjunction with an external time constant, allow the formation of the envelope of the sustain and percussion effects. The duration of the trigger pulses is $\cong$ 9 msec.

g) 1 input (reset) to synchronize the device or more than one device (with the same keyboard scanning and using a single contact per key).
The reset action, provided by an external circuit, is of the "POWER ON RESET" (high active) type and its duration must be $\cong$ 0.5 msec.

h) 1 $\overline{TEST}$ pin (in use it must be connected to V_{DD})

i) 2 supply pins.

MATRIX ORGANIZATION (Keyboard and controls)

M108/208 Matrix outputs	M108/208 Octave bar inputs					
	B_1	B_2	B_3	B_4	B_5	B_6
$\overline{F_1}$	C_1	C_2	C_3	C_4	C_5	C_6
$\overline{F_2}$	C_1#	C_2#	C_3#	C_4#	C_5#	7th OFF/7th ON
$\overline{F_3}$	D_1	D_2	D_3	D_4	D_5	3rd+/3rd-
$\overline{F_4}$	D_1#	D_2#	D_3#	D_4#	D_5#	Sust. OFF/Sust. ON
$\overline{F_5}$	E_1	E_2	E_3	E_4	E_5	$\overline{Latch}$/Latch
$\overline{F_6}$	F_1	F_2	F_3	F_4	F_5	Man/Auto
$\overline{F_7}$	F_1#	F_2#	F_3#	F_4#	F_5#	61/24 + 37 (17 + 44)
$\overline{F_8}$	G_1	G_2	G_3	G_4	G_5	Antibounce ON/Antibounce OFF
$\overline{F_9}$	G_1#	G_2#	G_3#	G_4#	G_5#	ROM Low/ROM High
$\overline{F_{10}}$	A_1	A_2	A_3	A_4	A_5	————
$\overline{F_{11}}$	A_1#	A_2#	A_3#	A_4#	A_5#	————
$\overline{F_{12}}$	B_1	B_2	B_3	B_4	B_5	————

C_1 is the first key on the left, O_6 is the last key on the right of the keyboard.

The main feature of this chip is the possibility of formating the keyboard either with 61 keys (only "SOLO" without automatism) or separating it into two sections ("ACCOMPANIMENT + SOLO") with the possibility of chord and bass automatic in the first section.

FEATURES

a) The "61/24 + 37" (17 + 44) control chooses the keyboard operating mode, i.e. the whole keyboard dedicated to "SOLO" or 24 (17) keys dedicated to "ACCOMPANIMENT" and 37 (44) to "SOLO".

b) The "Man/Auto" control, which operates only in case of "ACC.+ SOLO", chooses the manual or the automatic accompaniment.

c) The "Sust OFF/Sust ON" allows the storage of the "SOLO" section and handles the whole keyboard or 37 (44) keys depending on the operating mode.

d) The "$\overline{\text{Latch}}$/Latch" similarly allows the storage of the "ACC." section and operates in "ACC.+ SOLO" only.

e) The "3rd+/3rd-" which operates only in case of "ACC.+ SOLO" and "AUTOMATIC", changes the automatic chord generated from major to minor or viceversa.

f) The "7th OFF/7th ON" adds the seventh to the automatic chord generated.

g) The "Antibounce ON/Antibounce OFF" disables the antibounce circuit which is usually enabled.

h) The "ROM Low/ROM High" selects between ROMs with return to "1" (Low active) or with return to "0" (High active). Usually the chip is enabled for ROMs with return to "1" (Low active).

"SOLO" Operation

In this case the chip recognizes the whole keyboard as "SOLO" and does not read the controls which concern the "ACC.+ SOLO" operation.
The chip identifies all the keys pressed and transfers to the outputs of each section (ACC. and SOLO) the analog sum of corresponding pitches.
The outputs are current generators with average value constant, therefore it is sufficient to connect the pins to one load and send the signals on to the filters.
In the case of "Sustain OFF" each new key pressed or released is accepted or deleted in a time $\leqslant 576\ \mu$sec.
In the case of "Sustain ON" the chip has a different operation according to whether the new key (keys) is pressed or released: each new key pressed is always accepted in a time $\leqslant 576\ \mu$sec., whereas each key released is deleted with a delay of 73 msec. and only if there are still keys pressed.
In fact, if after the 73 msec. there are no keys pressed, the last key (or keys) released remains stored until new keys are pressed.
In this mode it is possible to have Sustain, with external envelope shaping, for the last keys (or key) released.
The pitch envelope is controlled by a D.C. signal $\overline{\text{KPS}}$ (any key pressed) and there is also an A.C. signal $\overline{\text{TDS}}$ (trigger decay "SOLO") which provides a pulse whenever a key is pressed.
An appropriate antibounce circuit, inside the chip, solves the problems associated with the keyboard contacts.

"SOLO + ACCOMPANIMENT" Operation

In this case the chip identifies the "ACCOMPANIMENT" on the first 24 (17) keys on the left, and the "SOLO" on the remaining 37 (44) keys and reads all the controls which concern the "ACC." section. The "SOLO" function is identical to "61 keys" mode, but for the "ACC." section there are two possibilities:

A) **MANUAL**
The chip identifies which keys are pressed in the "ACC." section, and transfers to the "ACC." outputs the analog sum of the corresponding pitches.
The "ACC." section is fully independent of the "SOLO" section and the signals (if there is no "LATCH") remain at the output only while the keys are pressed even if there is "SUSTAIN ON".

The "BASS" section gives at the bass output an alternating bass between the first on the left and the first on the right of the keys pressed in the "ACC." section; the pitch switching timing is dependent on an external ROM (3 bits).
The "LATCH" control stores the last keys released and the output signals, including the bass output, remain until new keys are pressed.
The $\overline{TDB}$ (trigger decay "BASS") output gives a pulse corresponding to every output change; there are also two D.C. signals, $\overline{KPA}$ (any key pressed accompaniment) and $\overline{NPA}$ (pitches in output accompaniment) relative only to the "ACC." section.
The first of these signals (analogous to $\overline{KPS}$) concerns the keyboard and does not consider the "LATCH" condition.
The second on the contrary concerns the "ACC." output and considers the "LATCH" condition.

B) **AUTOMATIC**

The chip recognizes in the "ACC." section only the first on the left of the keys pressed and, according to the setting of the following controls, produces a major or minor chord with or without seventh only the 4' footage but with separated outputs for root, third, fifth and eighth (or seventh if the chord is with seventh).
The bass section gives the bass arpeggio among root, third, fourth, fifth, sixth, seventh and eighth with pitch switching dependent on an external ROM (3 bits).
In automatic mode the two octaves of the "ACC." section inside the chip are connected in parallel both for the chord and for the bass; therefore by pressing anyone of the two keys of the same note the chip generates the same chord.
The "LATCH" control stores the major chord and the bass pitches (until new keys are pressed); the modification of the chord stored (from major to minor, addition of seventh) is always possible by operating the proper controls: by releasing these controls the chord becomes major again.
It is possible to delete the stored pitches both is manual and in "AUTOMATIC" mode by a $\overline{Latch}$ control signal.
Once again there are $\overline{KPA}$, $\overline{NPA}$, and $\overline{TDB}$ information; however the $\overline{TDB}$ pulse, which normally appears at each arrival of the ROM codes, does not appear if there are no pitches in the "ACC." (and bass) outputs or, in the case of alternate bass (in manual mode) if the codes indicate conditions of indifference.

RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		11.4	12	12.6	V

BASS TRUTH TABLES

LOW ACTIVE

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
1	1	1	No change	No change
1	1	0	Root	1st on the left
1	0	1	3rd	– – –
1	0	0	4th	– – –
0	1	1	5th	1st on the right
0	1	0	6th	– – –
0	0	1	7th	– – –
0	0	0	8th	– – –

HIGH ACTIVE

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
0	0	0	No change	No change
0	0	1	Root	1st on the left
0	1	0	3rd	– – –
0	1	1	4th	– – –
1	0	0	5th	1st on the right
1	0	1	6th	– – –
1	1	0	7th	– – –
1	1	1	8th	– – –

STATIC ELECTRICAL CHARACTERISTICS (Positive Logic, V_{DD}= +10 to +14V, V_{SS}= 0V, T_{amb}= 0 to 50°C unless otherwise specified)

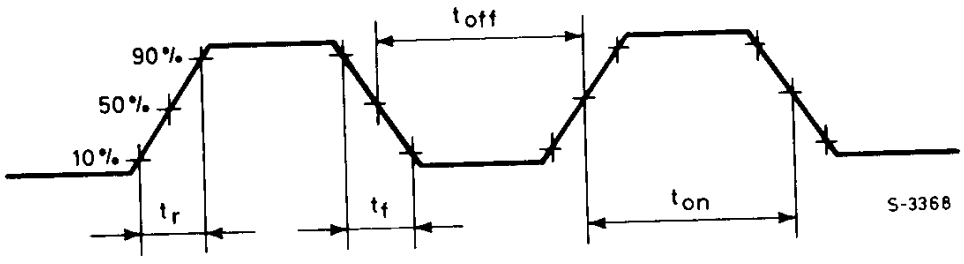
Parameter		Test conditions	Min.	Typ.	Max.	Unit
INPUT SIGNALS						
V_{IH}	Input high voltage	Note 1	V_{DD}-1		V_{DD}	V
		Note 2	4		18	V
		Note 3	V_{DD}-2		V_{DD}	V
V_{IL}	Input low voltage	Note 1	V_{SS}		V_{SS}+1	V
		Note 2	V_{SS}		V_{SS}+0.6	V
		Note 3	V_{SS}		V_{SS}+2	V
I_{LI}	Input leakage current	V_I= +14V T_{amb}= 25°C			10	µA
LOGIC SIGNAL OUTPUTS						
R_{ON}	Output resistance with respect to V_{SS}			300	500	Ω
R_{ON}	Output resistance with respect to V_{DD}	V_{OUT}= V_{DD}-1 (driver off)		15	25	kΩ
V_{OH}	Output high voltage		V_{DD}-0.4		V_{DD}	V
V_{OL}	Output low voltage			V_{SS}+0.2	V_{SS}+0.4	V
POWER DISSIPATION						
I_{DD}	Supply current	T_{amb}= 25°C		30	45	mA
ANALOG SIGNAL OUTPUTS (the external load must be connected to $V_{DD}/2$)						
I_{OH}	Output current with respect to $V_{DD}/2$	Outputs loaded with 1 KΩ resistor versus $V_{DD}/2$	35	50	70	µA
I_{OL}	Output current with respect to V_{SS}	Outputs loaded with 1 KΩ resistor versus $V_{DD}/2$	-35	-50	-70	µA

Note 1 : Refers only to the clock inputs.
Note 2 : Refers only to the inputs from the external memory.
Note 3 : Refers only to the reset input.

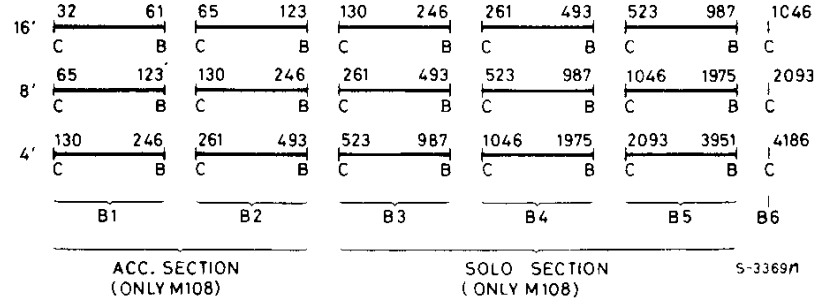
DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
MASTER CLOCK INPUT						
f_i	Input clock frequency			1000.12		KHz
t_r, t_f	Input clock rise and fall time 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	1000 KHz		500		ns
T.O.S. CLOCK INPUT						
f_i	Input clock frequency		100	1000.12	2500	KHz
t_r, t_f	Input clock rise and fall times 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	2000 KHz		250		ns
$\overline{TDS}$ and $\overline{TDB}$ OUTPUTS						
t_{on}	Pulse duration	1000 KHz		9.216		ms
t_r, t_f	Outputs rise and fall times 10% to 90%	1000 KHz		100		ns

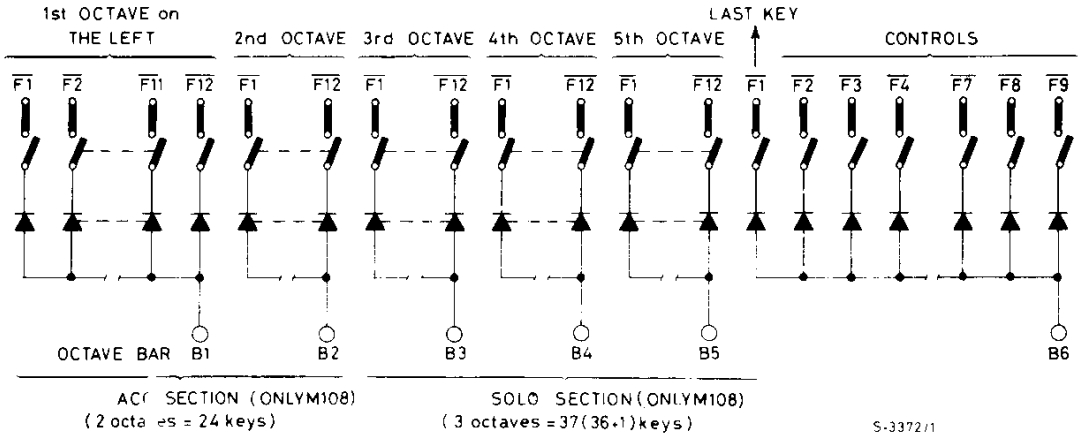
INPUT CLOCK WAVEFORM



FREQUENCY RANGE OF EACH OCTAVE (16', 8', 4' footages)

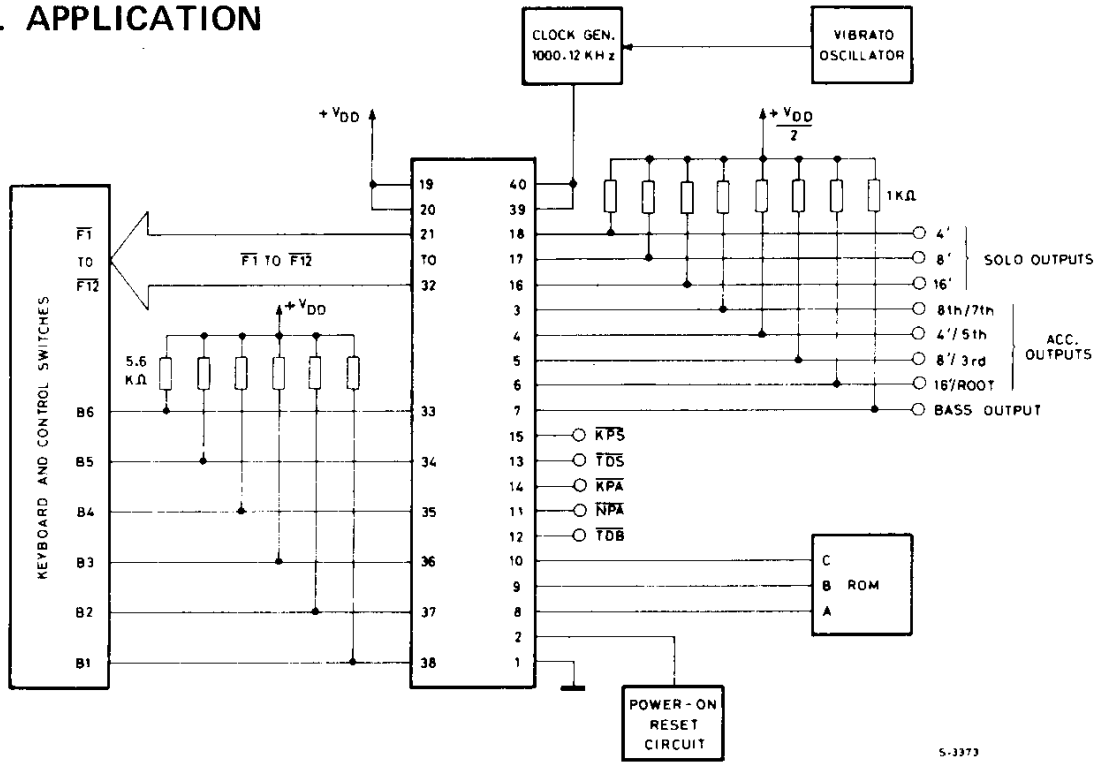


CONNECTION OF THE KEYBOARD AND CONTROL SWITCHES

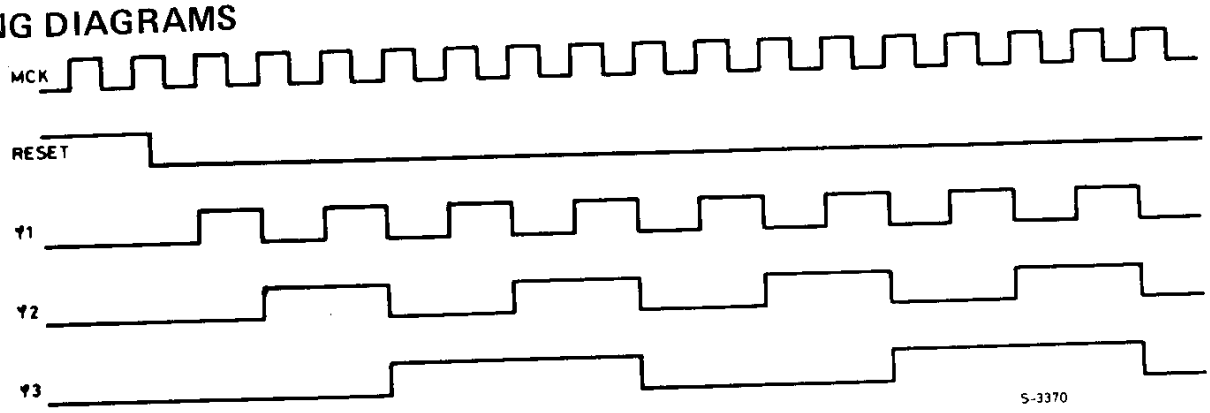


Note: The switch "OPEN" corresponds to "KEY NOT PRESSED" or "CONTROL IN THE FIRST CONDITION" (see the drawing "MATRIX ORGANIZATION").

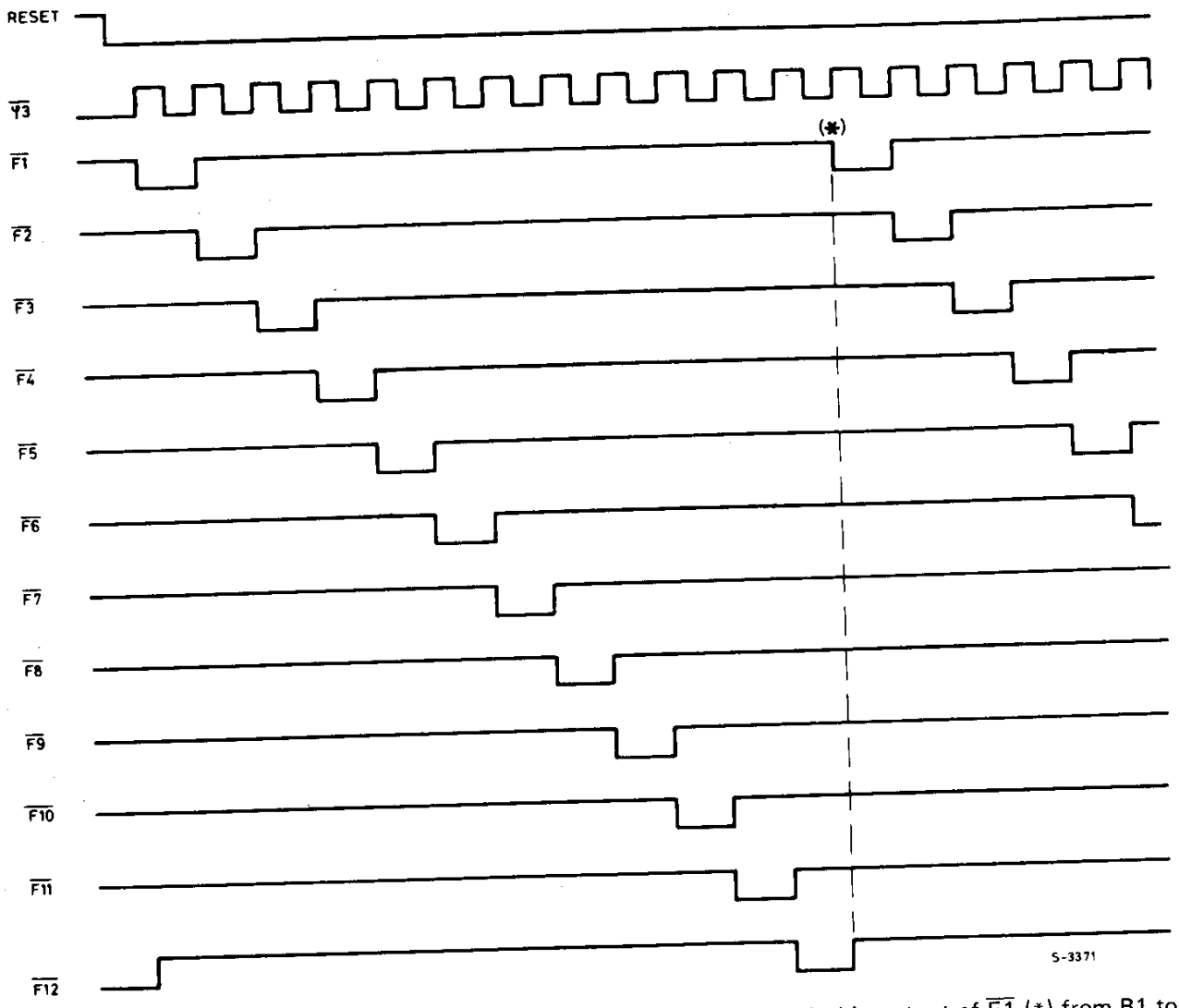
TYPICAL APPLICATION



TIMING DIAGRAMS

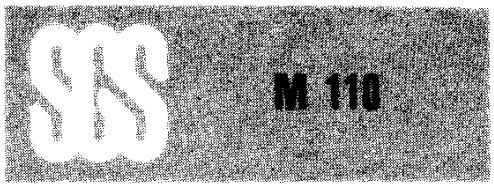


Note: MCK is the master clock input (matrix scanning), $\varphi 1, \varphi 2, \varphi 3$ are internal phases to generate $\overline{F1} \div \overline{F12}$.



Note: The matrix scanning starts (after the power on reset) at the second arrival in output of $\overline{F1}$ (*) from B1 to B6 in continuous sequence.

MOS INTEGRATED CIRCUIT



PRELIMINARY DATA

MONOPHONIC SYNTHESIZER

- LOW POWER DISSIPATION < 500 mW TYP.
- N-CHANNEL SILICON GATE PROCESS
- DIGITAL PORTAMENTO EFFECT
- EXTERNAL CONTROL (WITH RC) OF THE PORTAMENTO SPEED IN THE 100 μs to 150 ms RANGE FOR EACH HALF TONE
- EXTERNAL OSCILLATOR FOR PORTAMENTO (EXT. OSC.)
- STANDARD SUPPLY (12V, GND)
- MATRIX ORGANIZATION 12 x 6 WITH 61 POSITIONS FOR THE KEYBOARD AND 6 COMMANDS
- RESET INPUT FOR FREQUENCY CLAMP
- PRIORITY LEFT OR RIGHT OF THE PRESSED KEYS
- 3 CODED OUTPUTS FOR THE OCTAVE INFORMATION OF THE PLAYING FREQUENCY
- 2 TRIGGER SIGNALS $\overline{TP}$ AND $\overline{TS}$ FOR PERCUSSION AND KEY PRESSED
- 1 OUTPUT WITH DC CURRENT PROPORTIONAL TO THE PLAYING FREQUENCY
- 1 OUTPUT WITH PULSE FOR FALLING EDGE OF THE EXTERNAL SAWTOOTH WAVEFORM (20 μs)
- SAWTOOTH WAVEFORM SELECTABLE (4', 8', 16', 32')
- PROVISION FOR OBTAINING SAWTOOTH WAVEFORMS WITH FEW EXTERNAL COMPONENTS ON THE 4', 8', 16', 32' FOOTAGES
- 1 OUTPUT WITH FOOT AND DUTY CYCLE ON FOLLOWING COMMANDS
- 4 OUTPUTS WITH 50% DUTY CYCLE (2', 4', 8', 16')

The M110 is realized on a single monolithic silicon chip using low threshold N-channel silicon gate MOS technology. It is available in a 40 lead plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.3 to 20	V
V_I	Input voltage	-0.3 to 20	V
I_o	Output current (at any output pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 50	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

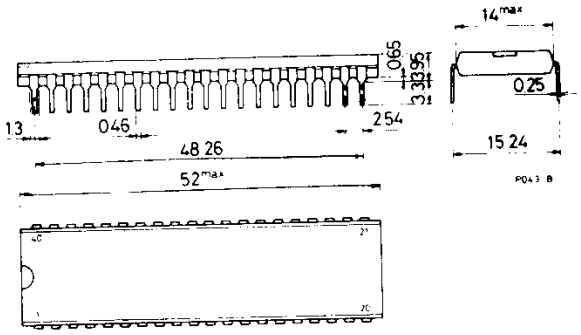
** All voltages are with respect to V_{SS} (GND).

ORDERING NUMBER: M110 B1 for dual in-line plastic package

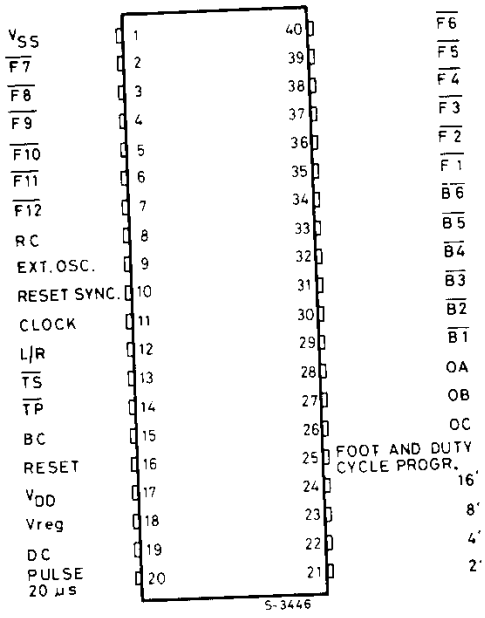
M 110

MECHANICAL DATA (dimensions in mm)

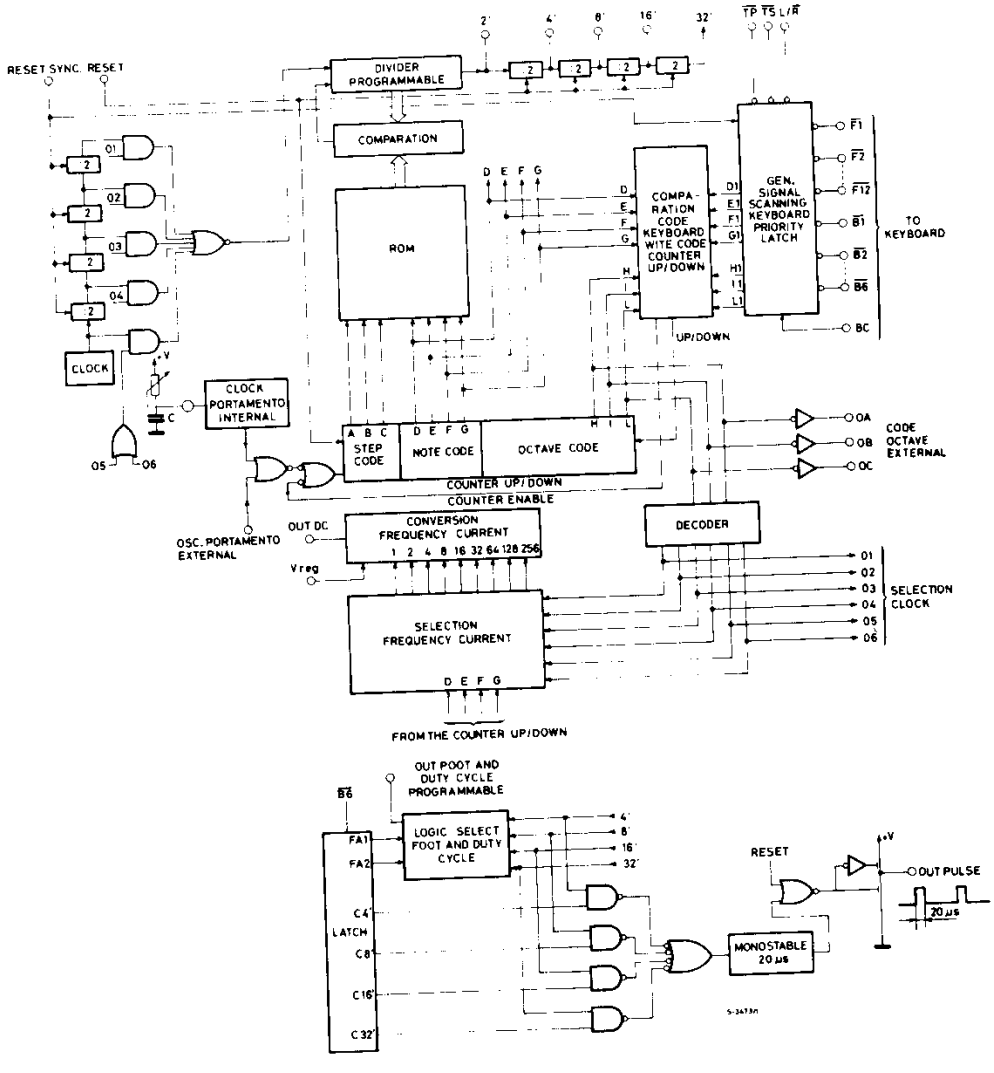
Dual in-line plastic package (40 lead)



PIN CONNECTIONS



BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (V_{DD} = 12V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 50°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK INPUT (pin 11)						
V_{IH}	Clock high voltage		V_{DD}-1		V_{DD}	V
V_{IL}	Clock low voltage		V_{SS}		V_{SS}+1	V
DATA INPUTS (pin 9, 10, 12, 15, 16, 29, 30, 31, 32, 33, 34)						
V_{IH}	Input high voltage		V_{DD}-2		V_{DD}	V
V_{IL}	Input low voltage		V_{SS}		V_{SS}+2	V
I_L	Input leakage current	V_i = 12.6V T_{amb} = 25°C			10	μA
DATA OUTPUTS (pin 13, 14, 21, 22, 23, 24, 25, 26, 27, 28) (2, 3, 4, 5, 6, 7, 35, 36, 37, 38, 39, 40 with external pull-up)						
R_{OUT}	Output res. to V_{SS} Output res. to V_{DD}	for $V_o = V_{DD} - 1$ (driver OFF)		300 15	500 25	Ω KΩ
V_{OH}	Output high voltage		V_{DD}-0.4		V_{DD}	V
V_{OL}	Output low voltage			V_{SS}+0.2	V_{SS}+0.4	V
POWER DISSIPATION						
I_{DD}	Supply current	T_{amb} = 25°C		30	50	mA
INTERNAL OSCILLATOR (pin 8)						
RC external		C = 4.7 nF R = 2.2MΩ(*) C = 4.7 nF R = 1 KΩ(*)		0.07 125		KHz
OUTPUT PULSE 20 μs (pin 20)						
V_{OH}	Output high voltage	I_{OH} = 0	8	9		V
V_{OL}	Output low voltage	I_{OL} = 300 μA	V_{SS}		V_{SS}+0.3	V
R_{OUT}	Output res. to V_{SS} Output res. to V_{DD}	for V_o = 6V		0.5 5	1 8	KΩ

(*) Max. admissible value of R = 2.2 MΩ; min. admissible value of R = 1 KΩ.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{DD} = 12V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 50 °C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK INPUT (pin 11)						
f_i	Input clock frequency		1600	2000.240	2500	KHz
t_r, t_f	Input clock rise and fall time 10 to 90%				40	ns
t_{on}, t_{off}	Input clock ON and OFF times	2 MHz	200	250		ns

GENERAL CHARACTERISTICS

The circuit includes:

Pin 2, 3, 4, 5, 6, 7, 35, 36, 37, 38, 39, 40

$\overline{F1}$ to $\overline{F12}$: outputs for selection of notes with 22 KΩ external pull-up. The maximum allowable external capacity must be < 500 pF. When not selected these outputs are at the high state (+12V).

Pin 29, 30, 31, 32, 33, 34

$\overline{B1}$ to $\overline{B6}$: inputs for selection of octave with 5.6 KΩ external pull-up so that these are at the high state when not selected.

Pin 12

L/R input for selecting priority to the left or right.

- if priority to the right is selected the note relative to the key farthest to the right of those pressed is supplied at the output
- priority to the left gives the possibility of choosing one key out of the first 12 pressed, starting from the left
- the internal pull-up is between 200 and 350 KΩ.

Pin 15

BC: input for selecting priority key in the case of priority to the left.

Pin 11

Clock: input frequency for generating notes.
(The internal logic of the system provides a precision equal to that of the TOS-M087-M083).

Pin 9, 8

Ex Osc-RC of Clock for portamento:

- an external oscillator with square wave can be connected at the first input (pin 9) limiting the max. frequency to 160 KHz. The duty cycle can be as desired provided that the minimum duration of the "0" and of the "1" is 2 μs.
- the 2nd input (pin 8) foresees the use of an external RC with the possibility of varying the frequency of the internal oscillator by regulating R.
  The maximum frequency value which can be measured on the pin must have a period T = 6 μsec. With values of R = 2.2 MΩ (potentiometer) and C = 4.7 nF, we obtain $T_{min} \simeq 8$ μs and $T_{max} \simeq 14$ ms. The corresponding portamento time between the 2 keys at the two extremes of the keyboard is: min. time ≃ 7 ms, max. time ≃ 12 sec.
- the portamento time between 2 semitones can be defined by applying the following formula:

  Portamento time = 16 x oscillator frequency period

  The two oscillators must not be switched on simultaneously; use of one must exclude the other. The pin for the oscillator not in use is connected to V_{SS}.
- The portamento time between 2 keys is proportional to the distance between them; this means that the law of portamento/keys variation is linear.

GENERAL CHARACTERISTICS (continued)

Pin 10

Reset Sync.: input required when several SGS-ATES devices are used, all having the same type of scanning, so that only one contact need be used per key. Ohterwise it is connected to V_{SS}.

Pin 16

Reset input (active high) active on outputs 2', 4', 8', 16', output with foot duty cycle programmable, output pulse 20 μs.

Pin 28, 27, 26

OA-OB-OC: used in binary code of the octave to which the note selected belongs. The highest weight code is relative to the lowest octave. The 3 outputs are of the push-pull type.

Pin 25

Output with foot and duty cycle programmable; digital output with possibility of 4 functions: 8', 12.5%, 8' 25%, 16' 6.25%, 16' 12.5%.
Only one function can be selected at a time with the commands inserted in the matrix of the keyboard (push-pull).

Pin 20

Output 20 μs pulse: output for zeroing the sawtooth whose duration is between 16 and 24 μs at 2 MHz of clock (push-pull).

Pin 13

$\overline{TS}$: output of key pressed: high in absence of keys pressed, low in presence of keys pressed (push-pull).

Pin 14

$\overline{TP}$; output of priority key; high in absence of keys inserted, low in priority conditions (in this case the output goes to zero for a time equal to 8 ± 0.6 ms with clock 2 MHz) (push-pull).

– The conditions required to make a pulse appear at this exit are:
a) insertion of at least 1 key
b) insertion of a new priority key
c) release of a priority key when another key pressed previously acquires priority.

Pin 21, 22, 23, 24

2'-4'-8'-16': square wave outputs (push-pull) with 50% of duty cycle on 4 different footages: 2', 4', 8', 16' corresponding to the following max frequencies: 8372 Hz; 4186 Hz; 2093 Hz; 1046 Hz.
These outputs switch on the rise front.

Pin 19

DC: output which generates a current proportional to the frequency output therefore exponential with the position of the key.

Pin 18

Vreg: input necessary for calibration of current (OUT DC) and amplitude of sawtooth for different devices.

GENERAL INFORMATION

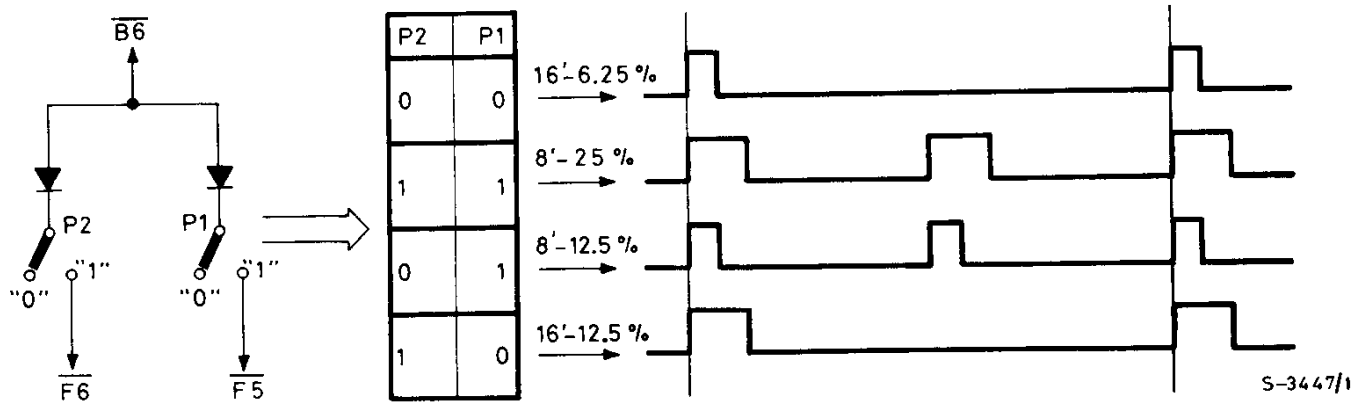
- Updating of a key between insertion and relative output information occurs in 0.5 ms.
- On release of all the keys pressed the last key released in order of time is memorized: consequently the relative frequency (on the 4 footages) and current (OUT DC) are memorized at the output.
- Each internal between 2 adjacent semitones is divided into 8 frequencies.
- The ratio between two contiguous frequencies is $\simeq \sqrt[96]{2.}$

Binary representation of octave codes

OA	OB	OC	
1	1	1	lowest octave
0	1	1	
1	0	1	
0	0	1	
1	1	0	
0	1	0	highest octave

Function with selectable foot and duty cycle

Selection of one of the 4 possible functions occurs via commands connected to the diode matrix of the keyboard.

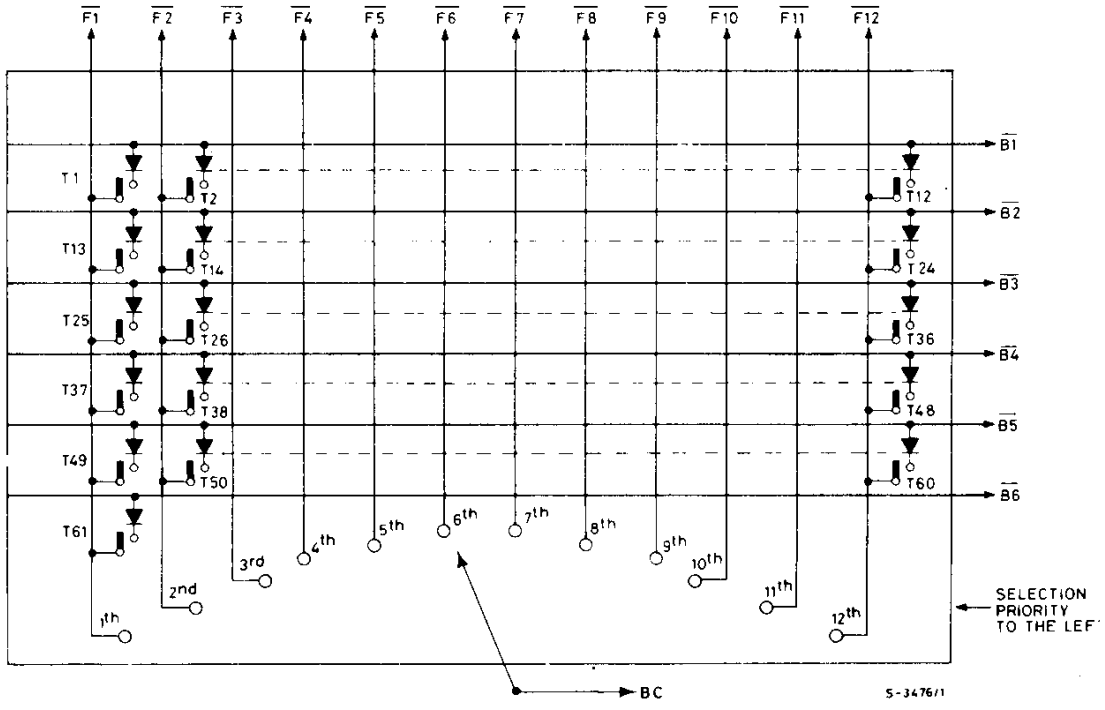


MATRIX ORGANIZATION (Keyboard and controls)

M110 matrix output	M110 Octave bar inputs						Selection for the priority on the left
	$\overline{B1}$	$\overline{B2}$	$\overline{B3}$	$\overline{B4}$	$\overline{B5}$	$\overline{B6}$	BC
$\overline{F1}$	(*) C1	C2	C3	C4	C5	(*) C6	1st key on the left
$\overline{F2}$	C1#	C2#	C3#	C4#	C5#		2nd key on the left
$\overline{F3}$	D1	D2	D3	D4	D5		3rd key on the left
$\overline{F4}$	D1#	D2#	D3#	D4#	D5#		4th key on the left
$\overline{F5}$	E1	E2	E3	E4	E5	P1 (***)	5th key on the left
$\overline{F6}$	F1	F2	F3	F4	F5	P2 (***)	6th key on the left
$\overline{F7}$	F1#	F2#	F3#	F4#	F5#		7th key on the left
$\overline{F8}$	G1	G2	G3	G4	G5		8th key on the left
$\overline{F9}$	G1#	G2#	G3#	G4#	G5#	(**) sawtooth 32'	9th key on the left
$\overline{F10}$	A1	A2	A3	A4	A5	(**) sawtooth 16'	10th key on the left
$\overline{F11}$	A1#	A2#	A3#	A4#	A5#	(**) sawtooth 8'	11th key on the left
$\overline{F12}$	B1	B2	B3	B4	B5	(**) sawtooth 4'	12th key on the left

(*) C1 is the first key on the left; C6 is the last key on the right of the keyboard.
(**) This control selects the correct pulse of the sawtooth generated by OUT DC (pin n° 19).
(***) P1 and P2 are the controls for the output with foot and duty cycle programmable.

12 x 6 MATRIX



If the device is used with selection of the first key to the left connect the control bar BC to V_{SS}.
For different priorities of the first key to the left connect BC to the selection frequency for the selected priority key. In this case BC must have a pull-up of 5.6 KΩ.
The selection sequence is: $\overline{F1}$ selects the first key to the left.

⋮

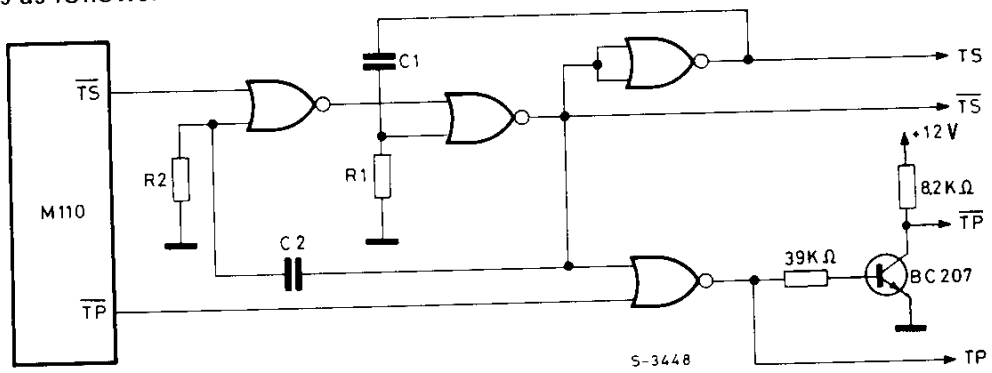
$\overline{F12}$ selects the twelfth key to left.

POWER ON RESET

The device must have an external circuit for the power-on reset (pin 16) high active. In the application diagram a power-on reset time of 0.5 sec is used and the circuit also connects, when active, the $\overline{B1}$ bar to V_{SS}.

ANTIBOUNCE CIRCUIT

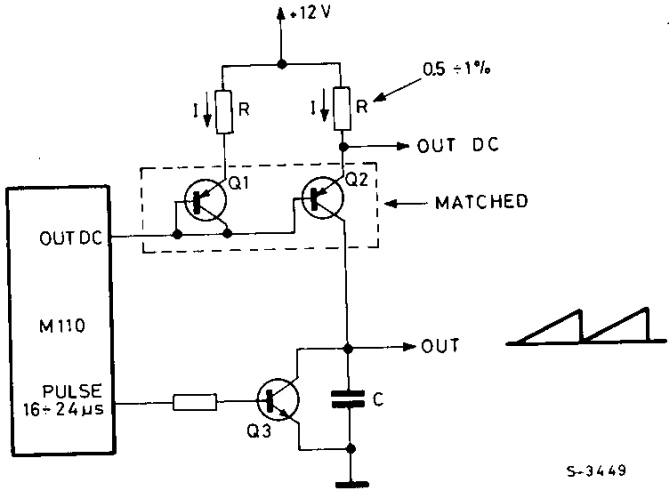
The antibounce circuit eliminates bounce caused by the contact springs of the keyboard. The bounce may supply wrong information at outputs $\overline{TS}$ and $\overline{TP}$.
The diagram is as follows:



The antibounce time can be regulated by acting on constants R1-C1 (antibounce on pressing a key) and R2-C2 (antibounce on release of key). In the application diagram of the device an antibounce of 18 ms is established C1 = C2 = 18 nF and R1 = R2 = 1 MΩ. The time constants must not however be 12 ms.
The antobounce circuit supplies the high or low active priority key and key pressed outputs compatible with the technical requirements requested.

GENERATION OF SAWTOOTH

The four sawtooth signals (4', 8', 16', 32' corresponding, for the last key on the right, to 4186 Hz; 2093 Hz; 1046 Hz, 523 Hz) are analog and are obtained by loading (with constant current) and unloading four external capacitors. A current mirror of the type shown below is produced.



– The reference of the sawtooth is V_{SS}.

– The best results are obtained using T1 and T2 matched with h_{FE} high while resistances R must have 0.5 to 1% precision.
The maximum variation in the amplitude of the sawtooth (over the whole keyboard) is ± 4%.

CALIBRATION

a) Press key 61.

b) Regulate Vreg until OUT DC is 9V (± 3%).

c) In these conditions the sawtooth assumes an amplitude of 4V and Vreg= 5V ± 30%.

d) In these conditions value of R must be 1600 Ω.

e) The OUT DC voltage must not fall below 9V (± 3%); this means that the maximum voltage excursion between the 1st and 61st key is 3V.

f) If OUT DC excursions lower than 3V are required for the whole keyboard, the value of R must be reduced in proportion to the new value of OUT DC.
let us consider come practical values of OUT DC:

OUT DC	R
3 V	1600 Ω
2 V	1066 Ω
1.5 V	800 Ω

values of R proportional to OUT DC

– This rule must be applied to avoid frequency/voltage linearity errors.

– The value of R must be between 100 to 1600 Ω.

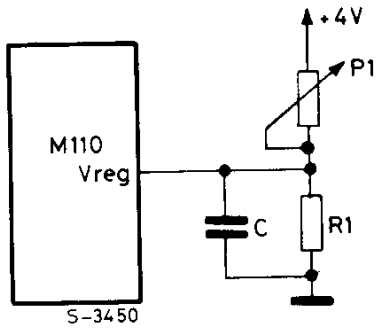
– The current/frequency conversion and therefore the variation in amplitude of the sawtooth for the whole keyboard have a precision of 4%.

– When the value of R and the maximum value of OUT DC have been established the latter can be maintained constant for any device simply by acting on Vreg.

– The resistive divider from which the Vreg is taken should be established respecting the following rules:

1) P1//R1 < 5 KΩ

2) $\frac{P1\ max}{R1} = 4$ to 5

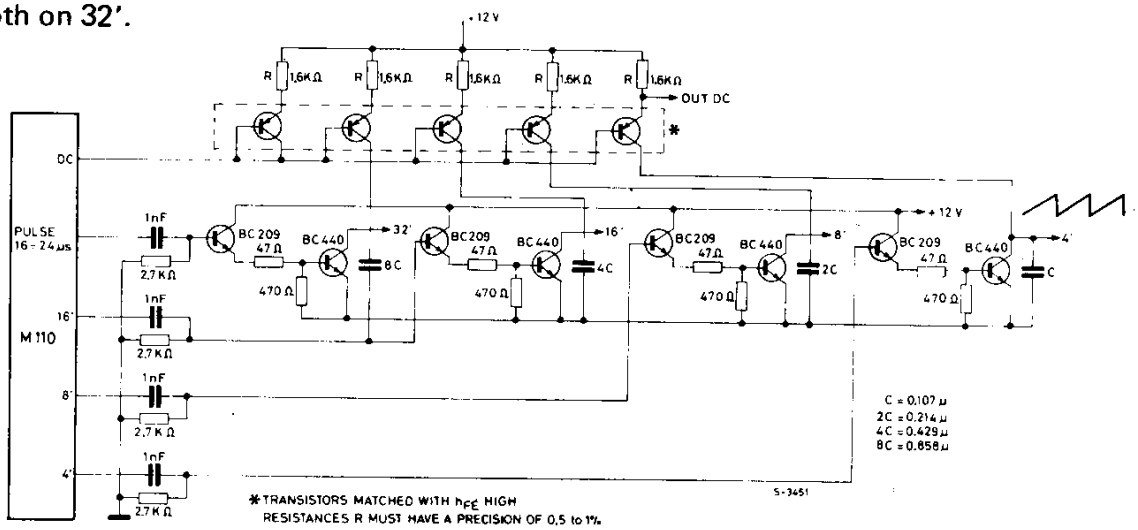


The values suggested for the four capacitances are respectively:

4'C = 0.107 μF; 9'C = 0.214 μF; 16'C = 0.429 μF; 32'C = 0.858 μF.

Outputs with simultaneous sawtooth on footages 4', 8', 16', 32'

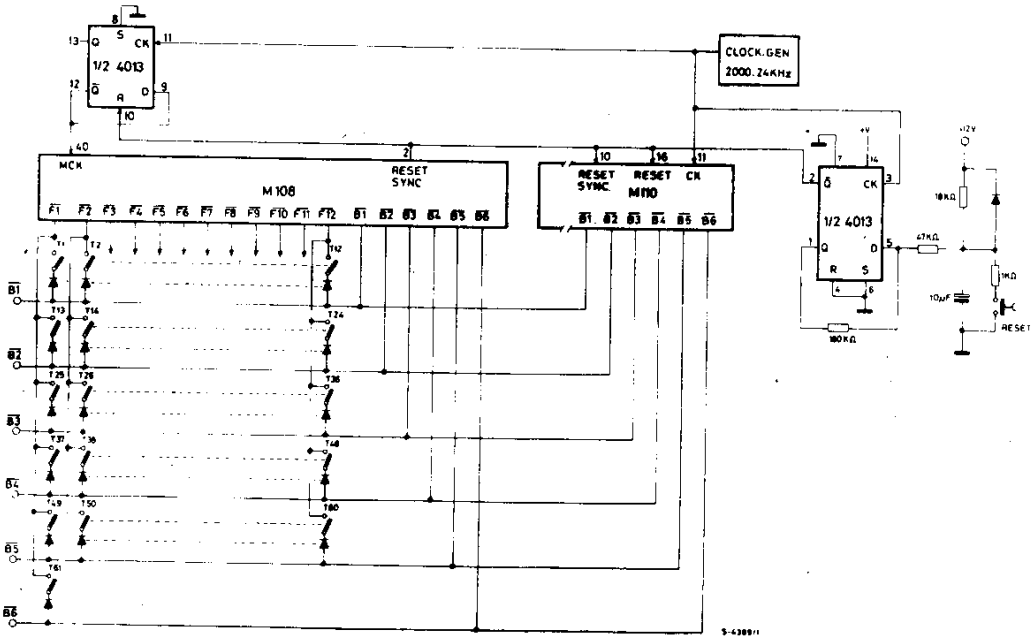
- The sawtooth can also be obtained simultaneously on 4 different footages: the diagram to be used is shown below.
- The zeroing pulses for 4', 8', 16' pulses are obtained by means of the rising fronts of the relative square wave outputs; for 32' however the 20 μs pulse is used, with the command for selection of the sawtooth on 32'.



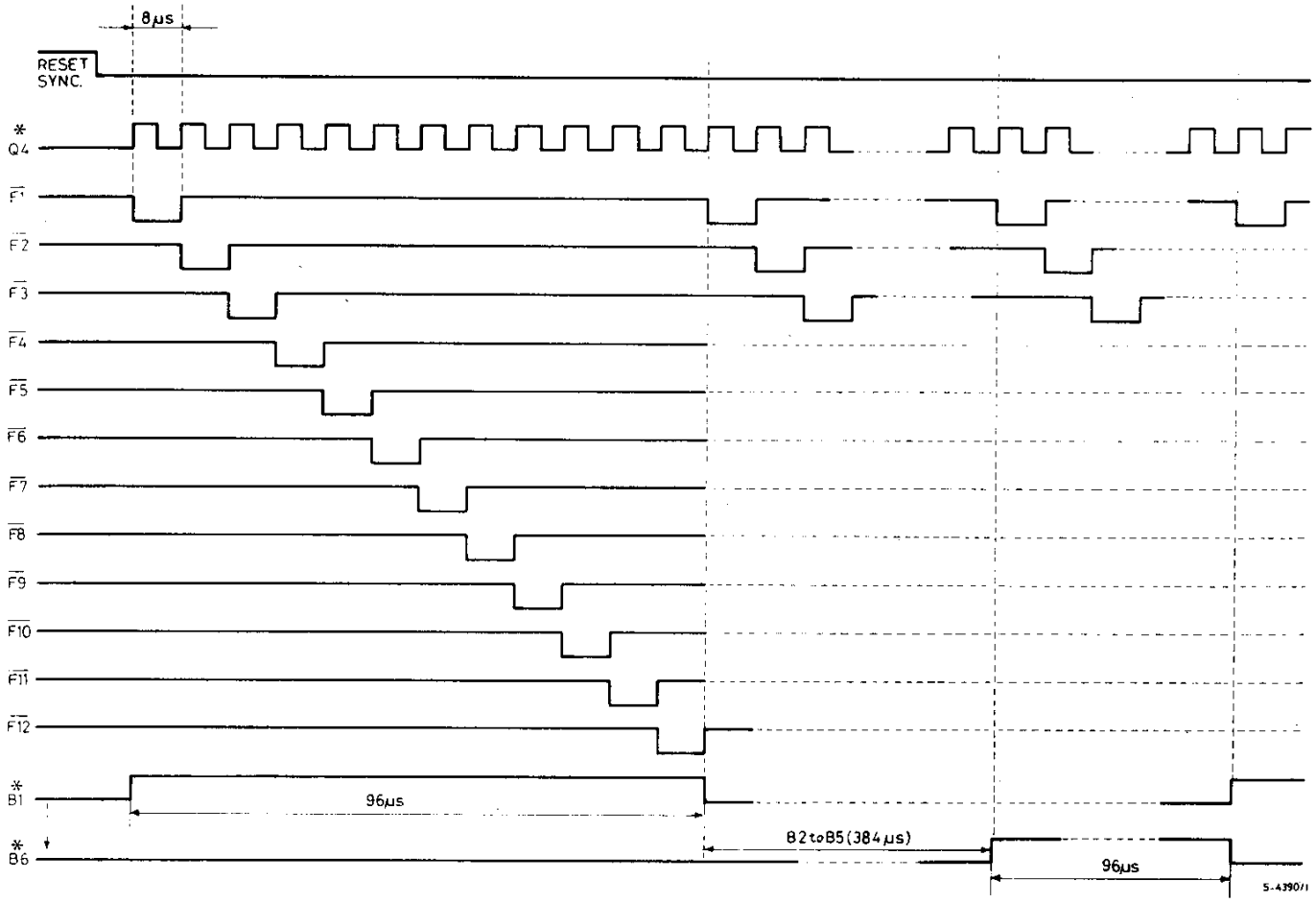
USE OF THE M108 AND M110 SIMULTANEOUSLY WITH ONLY ONE CONTACT FOR KEY

Application

The M108 and the M110 have the same connection with the keyboard therefore only one contact per key is sufficient to drive both the devices: one is the master, with outputs $\overline{F1}$ to $\overline{F12}$ connected to the keyboard switches, the other is the slave and will receive the information in bus $\overline{B1}$ to $\overline{B6}$ together with the master.
The synchronization is made by the reset (sync.) pin.

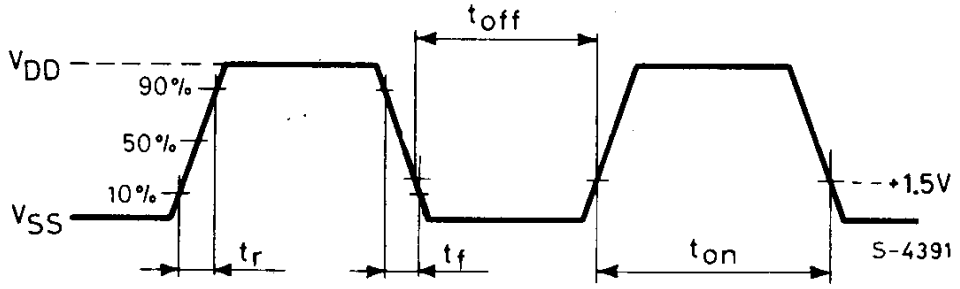


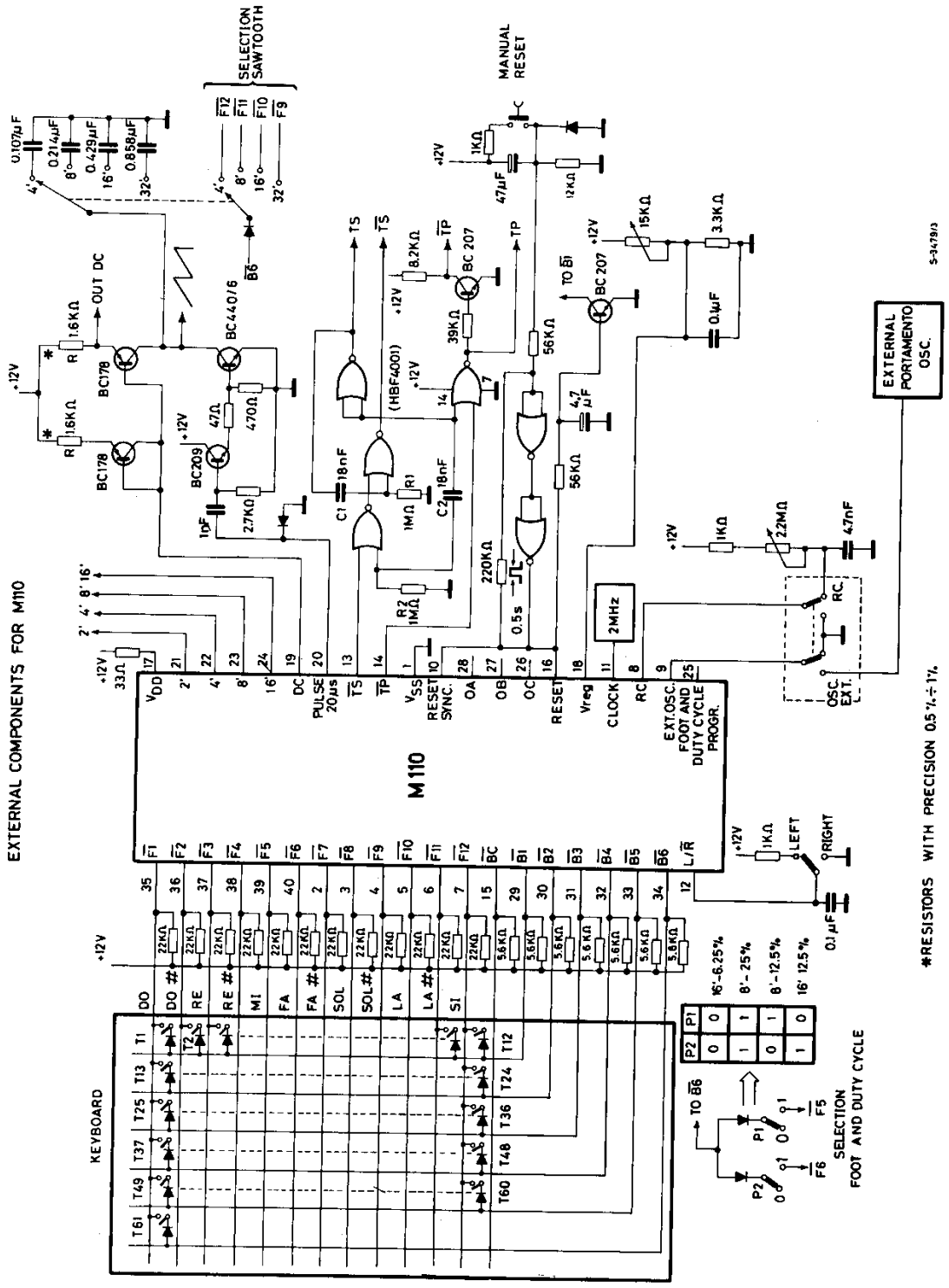
TIMING DIAGRAMS (KEYBOARD SCANNING)



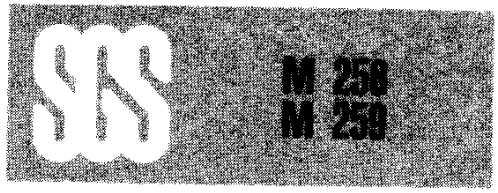
*Signals inside the M110

INPUT CLOCK WAVEFORM (pin 11)




EXTERNAL COMPONENTS FOR M110
M 110
KEYBOARD
SELECTION FOOT AND DUTY CYCLE
*RESISTORS WITH PRECISION 0.5 %÷ 1%
EXTERNAL PORTAMENTO OSC.
SELECTION SAWTOOTH
MANUAL RESET
OUT DC
2MHz
LEFT
RIGHT
16'-6.25%
8'-25%
8'-12.5%
16' 12.5%

MOS INTEGRATED CIRCUITS



PRELIMINARY DATA

RHYTHM GENERATORS

- 16 PROGRAMMABLE RHYTHMS (CODED FOR THE M258; ALSO AVAILABLE IN COMBINATION FOR THE M259
- 16 OUTPUTS (2 SECTIONS BY 8)
- MASK PROGRAMMABLE RESET COUNTS (24 or 32)
- DOWN BEAT OUT
- SYNC OUT
- EXTERNAL RESET
- TWO CHIP SELECTS (CS1, CS2) FOR SEPARATE TRISTATE CONDITION OF THE TWO OUTPUT SECTIONS
- INTERNAL PULL-UP ON THE INPUTS
- OPEN DRAIN OUTPUTS WITH RETURN TO "1" STATUS
- CHOICE BETWEEN RETURN TO "1" OR NOT ON 8 OUTPUTS (OUT 1, 2, 3, 4, 9, 10, 11, 12) SEPARATELY
- ONLY ONE POWER SUPPLY (+5V)
- VERY LOW POWER CONSUMPTION (150 mW TYP.)

The M258, M259 are monolithic rhythm generators specifically designed for electronic organs and other musical instruments.
Constructed on a single chip using MOS N-channel silicon gate technology, they are supplied in a 28 lead for (M258) or 40 lead for (M259) dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Source supply voltage	-0.3 to +7	V
V_i **	Input voltage	-0.3 to +7	V
I_o	Output current (at any pin)	3	mA
V_{OH}	Output voltage	12	V
T_{stg}	Storage temperature range	-65 to +125	°C
T_{op}	Operating temperature range	0 to 50	°C

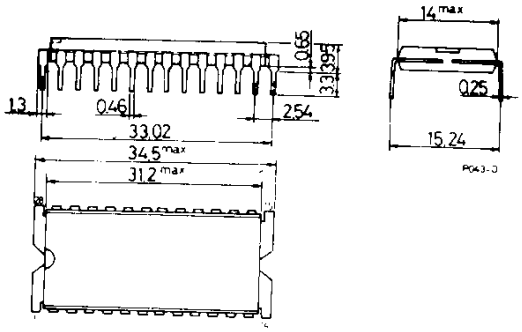
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

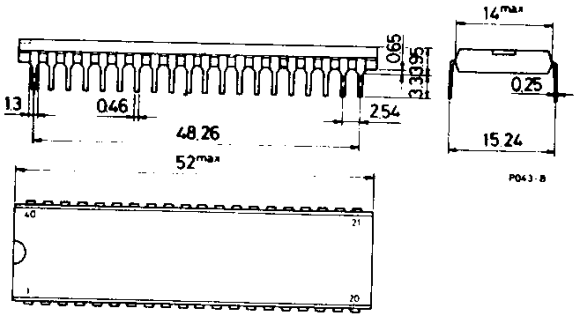
ORDERING NUMBERS: M258 B1/EB1 for dual in-line plastic package
M259 B1/EB1 for dual in-line plastic package

MECHANICAL DATA (dimensions in mm)

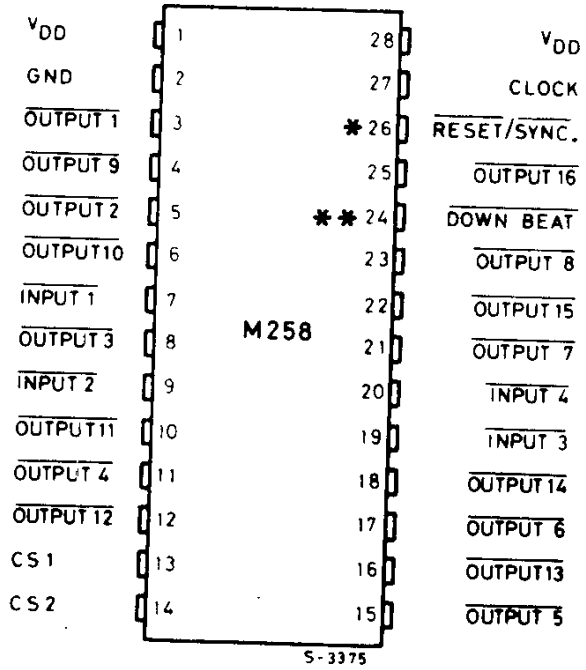
Dual in-line plastic package (28 lead)



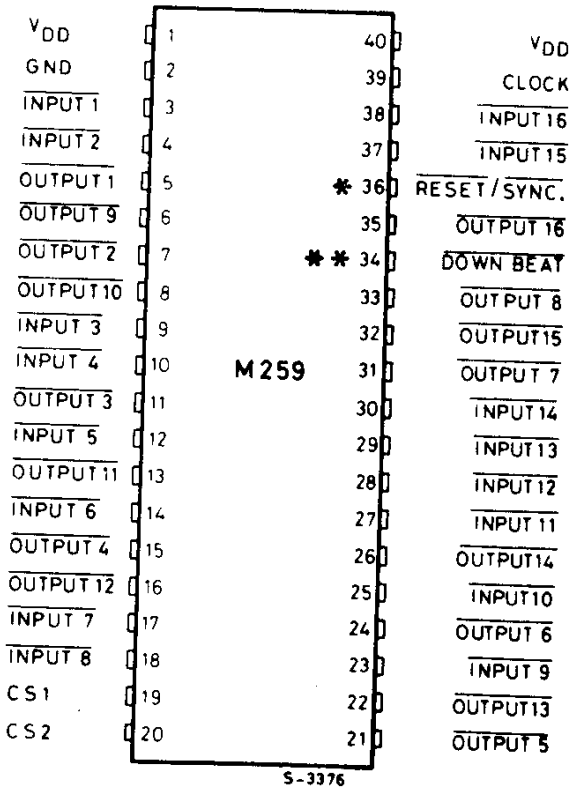
Dual in-line plastic package (40 lead)



PIN CONNECTIONS



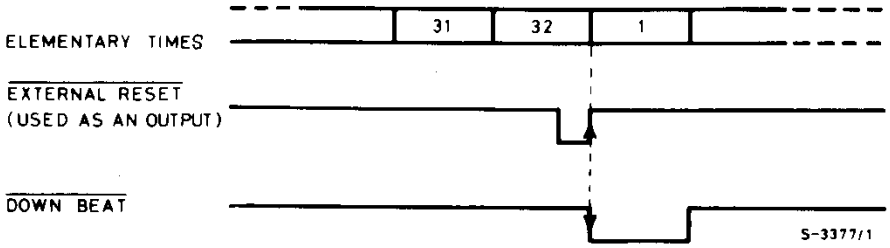
CS1 enables the outputs 01 to 08
CS2 enables the outputs 09 to 16



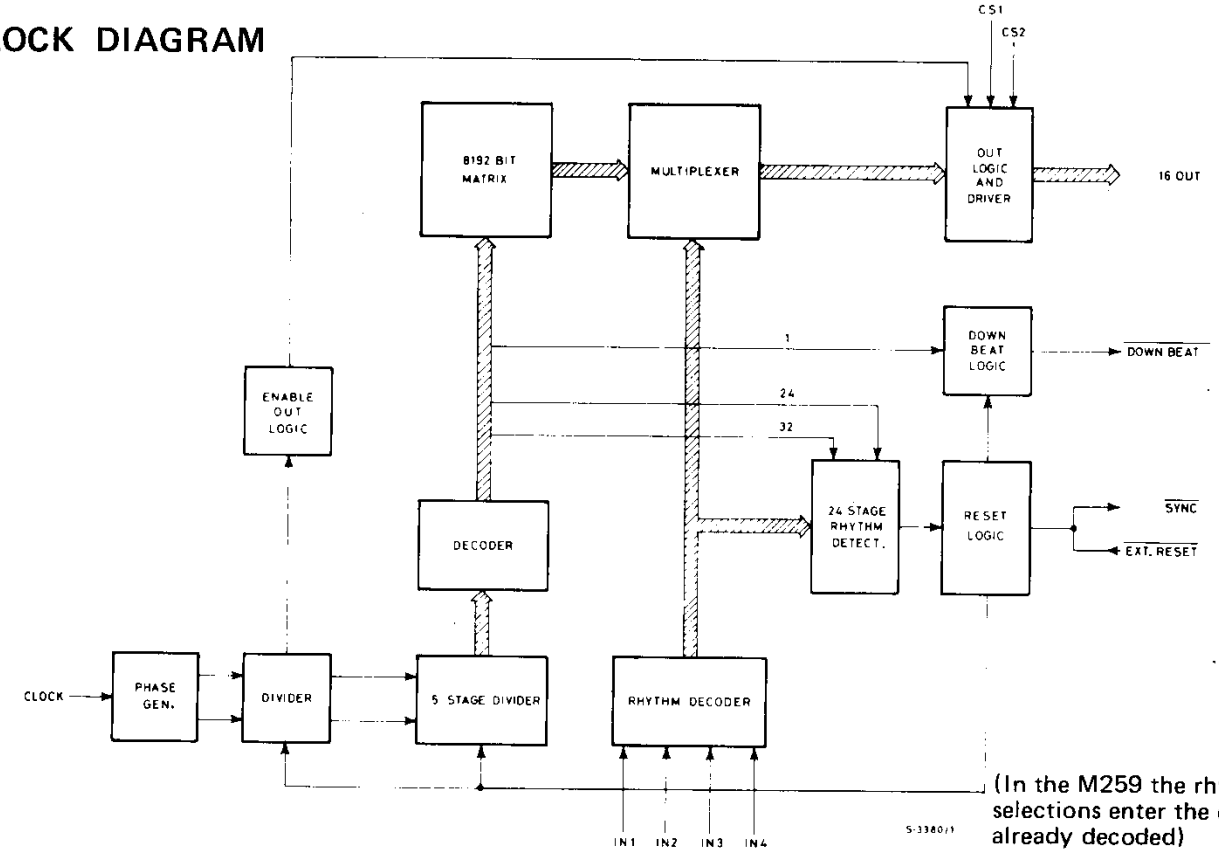
* This is a bidirectional pin. Used as an input it allows the chip reset; used as an output it can reset other devices.

** This pin generates a down beat trigger which can be used to drive an external lamp to indicate the first beat of the first bar of each rhythm.

RESET AND DOWN BEAT TIMING WAVEFORMS (POSITIVE LOGIC)



BLOCK DIAGRAM



(In the M259 the rhythm selections enter the chip already decoded)

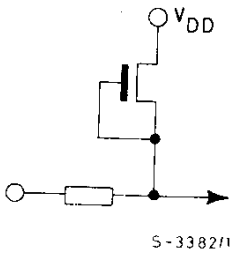
RHYTHM, SELECTION (for M258 only)

Rhythm	$\overline{IN4}$	$\overline{IN3}$	$\overline{IN2}$	$\overline{IN1}$
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

STATIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD} = 4.75 to 5.25V, T_{amb} = 0 to 50°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
CLOCK INPUT							
V_{IH}	Clock high voltage			2.4		V_{DD}	V
V_{IL}	Clock low voltage			0		0.4	V
DATA INPUTS							
V_{IH}	Input high voltage			2.4		V_{DD}	V
V_{IL}	Input low voltage			0		0.4	V
R_{IN}	Internal resistance to V_{DD}	V_I = 0V	V_{DD}= 5V	100	180		KΩ
I_{OL}(*)	Input load current	$V_I = V_{IL}$			-50		μA
EXT. RESET							
V_{IH}	Input high voltage			4.5		V_{DD}	V
V_{IL}	Input low voltage			0		1.5	V
R_{OFF}	Internal resistance to V_{DD} (inactive sync)	V_O= 0	V_{DD}= 5V	100	180		KΩ
R_{ON}	Internal resistance to V_{DD} (active sync)	V_O= 1V	V_{DD}= 4.75V		260	300	Ω
OUTPUTS (O_i, Down beat)							
R_{ON}		V_O= 1V			260	300	Ω
V_{OL}		Source current = 1 mA			0.26	0.3	V
I_{LO}		V_O= 12V	T_{amb}= 25°C			10	μA
POWER DISSIPATION							
I	Supply current	T_{amb}= 25°C			30		mA

(*) The "High Level" is clamped by the internal pull-up.



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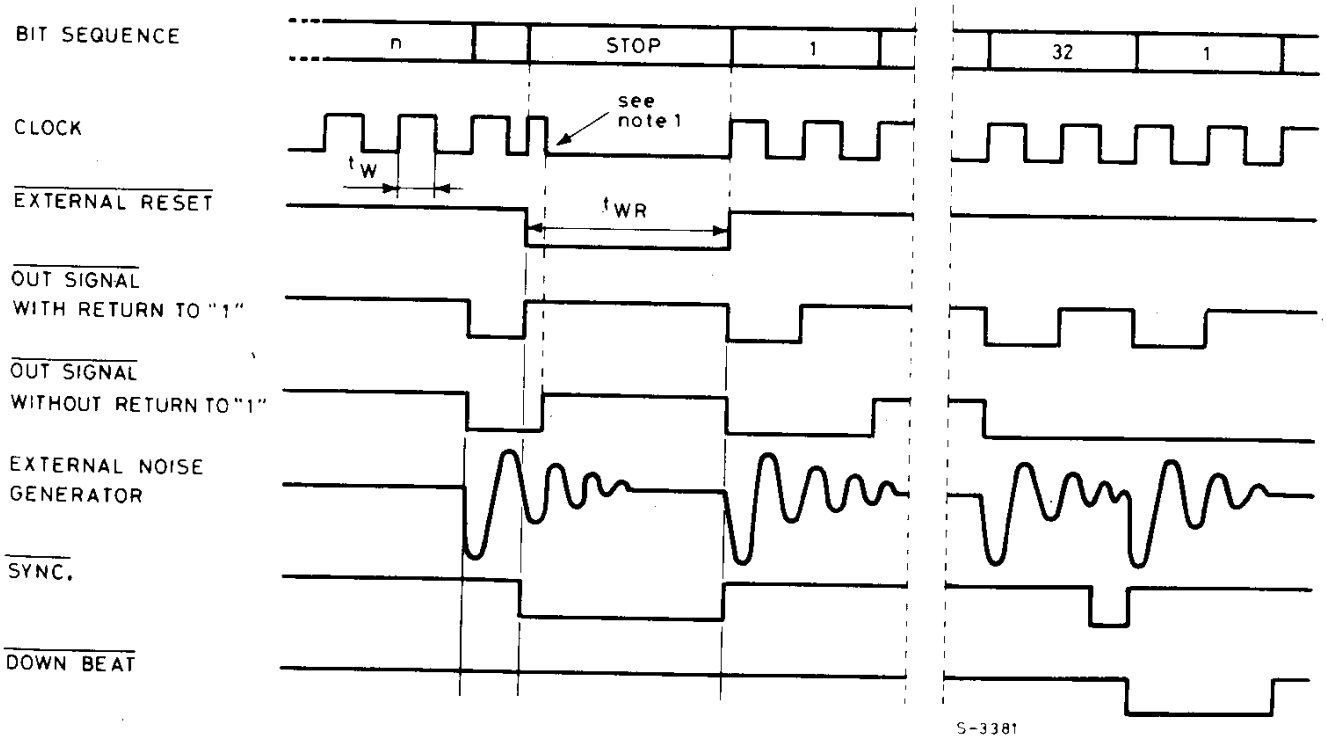
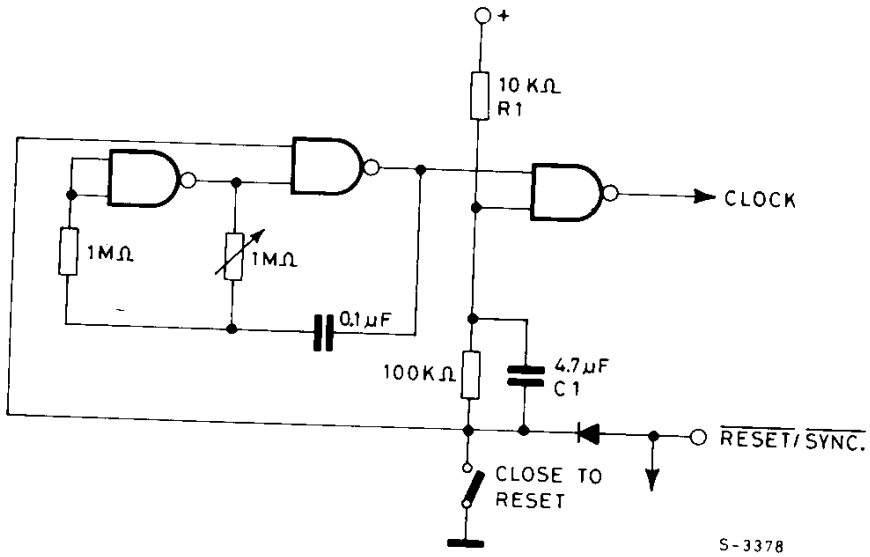
DYNAMIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD}= 4.75 to 5.25V, T_{amb} = 0 to 50°C unless otherwise specified)

Parameter		Test condistions	Values			Unit
			Min.	Typ.	Max.	
CLOCK INPUT						
f	Clock repetition rate		DC		100	KHz
t_w	Pulse width	Measured at 50% of the swing	5			μs
t_r	Rise time	Measured between 10% and 90% of the swing			100	μs
t_f	Fall time	Measured between 10% and 90% of the swing			100	μs
EXT. RESET						
t_{WR}	Pulse width		100			μs
t_{CR}	Clock delay with respect to reset		0			μs

TIMING WAVEFORMS

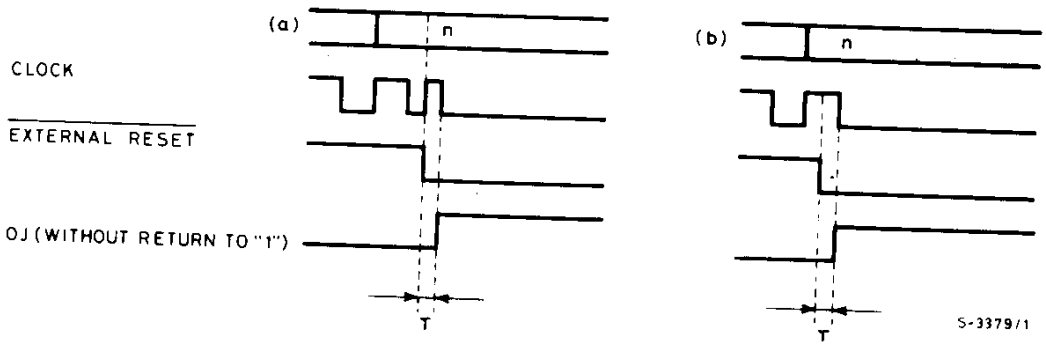


Note 1: This additional pulse, to reset the outputs without return to "1", can be obtained by using a clock generator as shown in the following diagram:



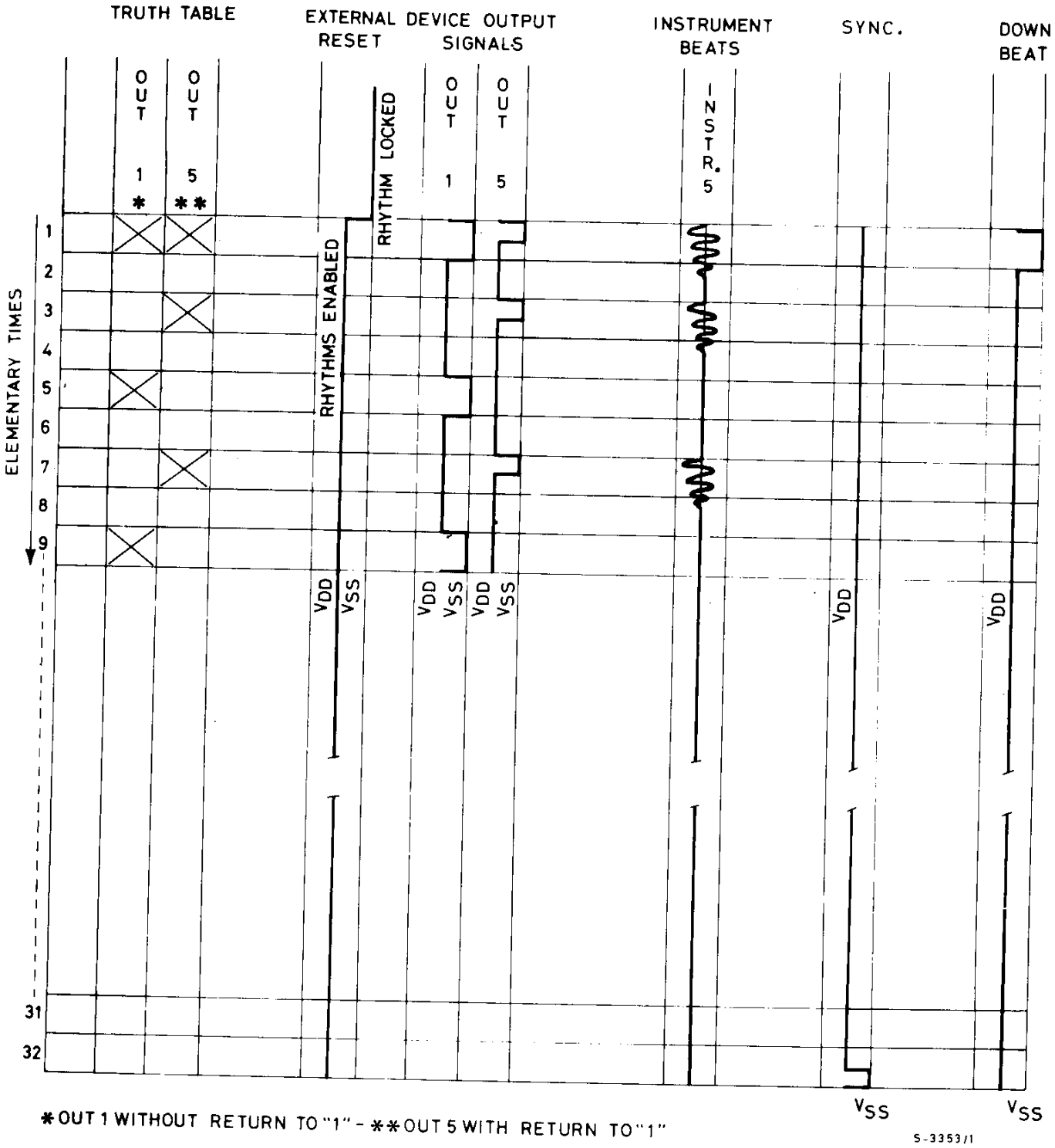
Ext. Reset/Sync. is a bidirectional pin. Used as an input it can reset the circuit as shown in the timing diagram and used as an output it can drive the reset of other devices.

Using the clock generator shown in the above figure, when the switch is closed asynchronous with respect to the clock, it is possible to have to two cases (see the following diagrams); in both the cases the output reset can be obtained by CS1 and CS2.



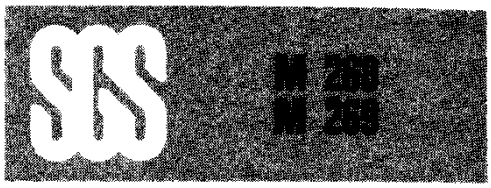
In both the cases the delay τ (in the outputs without return to "1") is defined through the constant R1 C1 $\geqslant$ 10 μsec.

INSTRUMENT BEATS VERSUS RHYTHM PROGRAM



Note: The outputs 01 to 08 are enabled by CS1; the outputs 09 to 16 are enabled by CS2. The outputs 01 to 04 and 09 to 12 are programmable separately without return to "1".

MOS INTEGRATED CIRCUITS



PRELIMINARY DATA

RHYTHM GENERATORS

- 16 CODED PROGRAMMABLE RHYTHMS FOR THE M268
- 8 PROGRAMMABLE RHYTHMS (ALSO AVAILABLE IN COMBINATION) FOR THE M269
- 12 OUTPUTS (2 SECTIONS 8 + 4)
- MASK PROGRAMMABLE RESET COUNTS (24 or 32)
- EPROM TECHNOLOGY PIN-TO-PIN COMPATIBLE DEVICE AVAILABLE FOR THE M268
- DOWN BEAT OUT
- SYNC OUT
- EXTERNAL RESET
- TWO CHIP SELECTS (CS1, CS2) FOR SEPARATE TRISTATE CONDITION OF THE TWO OUT. PUT SECTIONS
- INTERNAL PULL-UP ON THE INPUTS
- OPEN DRAIN OUTPUTS WITH RETURN TO "1" STATUS
- CHOICE BETWEEN RETURN TO "1" OR NOT ON 8 OUTPUTS (OUT 1, 2, 3, 4, 9, 10, 11, 12) SEPARATELY
- ONLY ONE POWER SUPPLY (+5V)
- VERY LOW POWER CONSUMPTION (150 mW TYP.)

The M268, M269 are monolithic rhythm generators specifically designed for electronic organs and other musical instruments.
Constructed on a single chip using MOS N-channel silicon gate technology, they are supplied in a 24 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Source supply voltage	-0.3 to +7	V
V_i **	Input voltage	-0.3 to +7	V
I_o	Output current (at any pin)	3	mA
V_{OH}	Output voltage	12	V
T_{stg}	Storage temperature range	-65 to +125	°C
T_{op}	Operating temperature range	0 to 50	°C

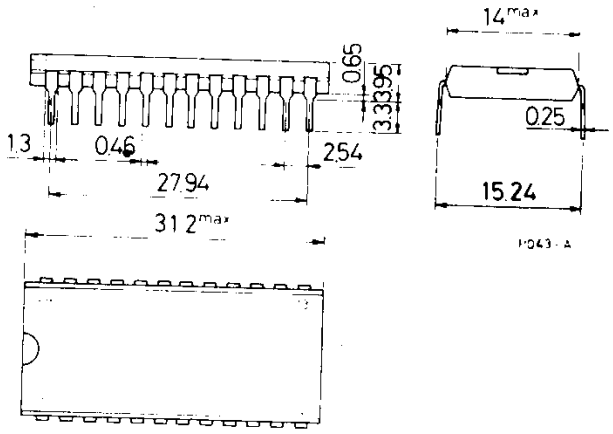
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

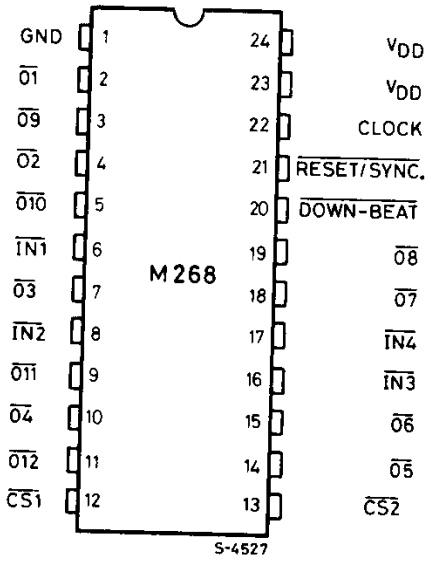
ORDERING NUMBERS: M268 B1/EB1 for dual in-line plastic package
M269 B1 for dual in-line plastic package

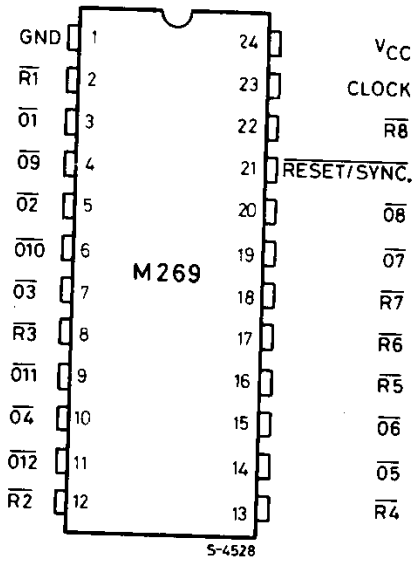
MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package (24 lead)



PIN CONNECTIONS



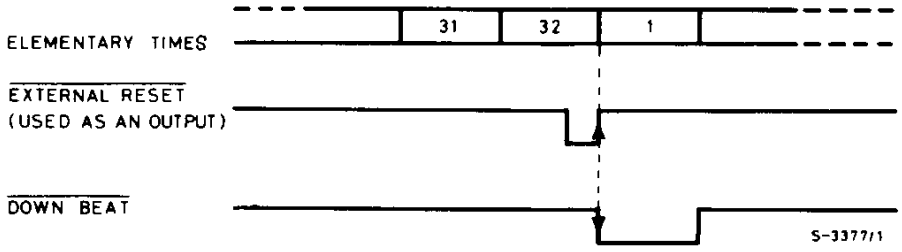


CS1 enables the outputs 01 to 08
CS2 enables the outputs 09 to 12

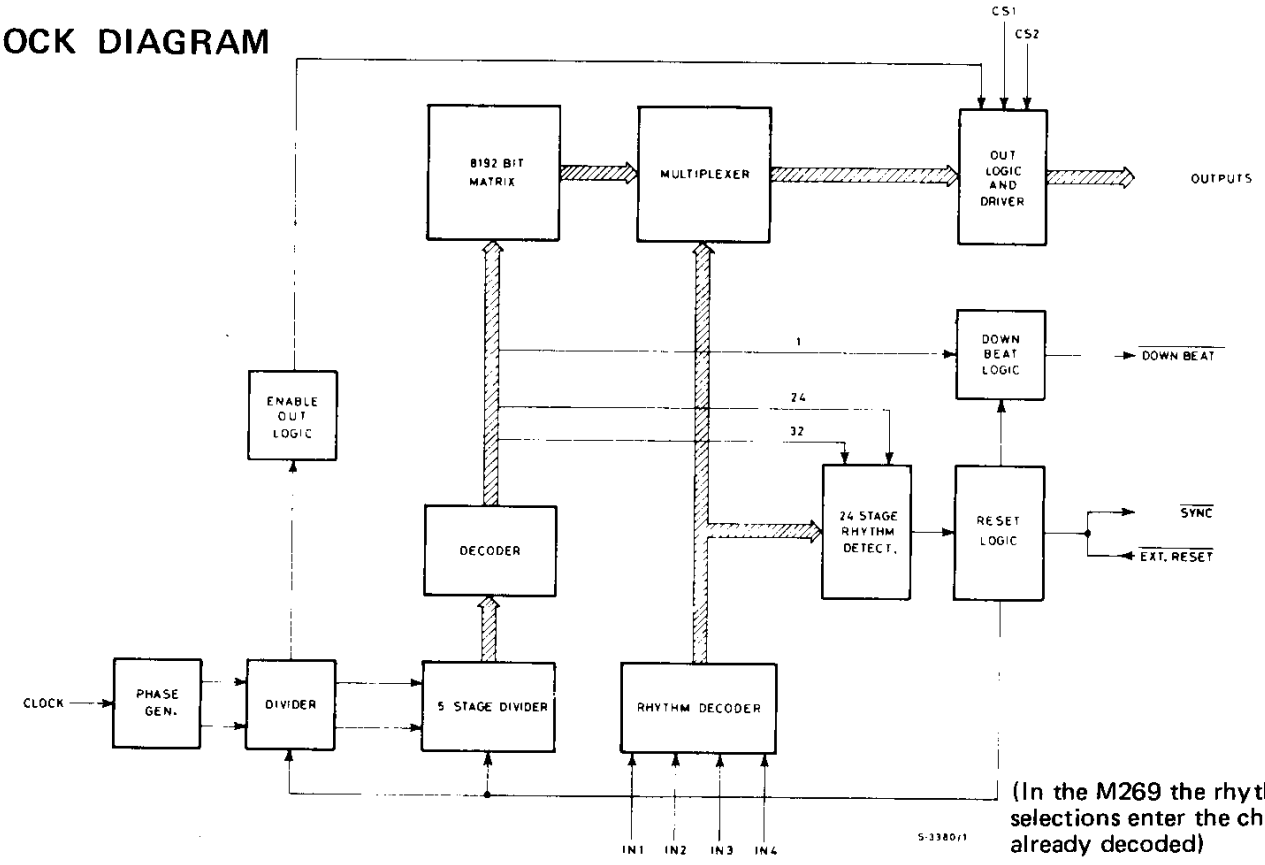
* This is a bidirectional pin. Used as an input it allows the chip reset; used as an output it can reset other devices.

** This pin generates a down beat trigger which can be used to drive an external lamp to indicate the first beat of the first bar of each rhythm.

RESET AND DOWN BEAT TIMING WAVEFORMS (POSITIVE LOGIC)



BLOCK DIAGRAM



(In the M269 the rhythm selections enter the chip already decoded)

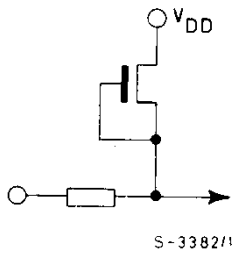
RHYTHM, SELECTION (for M268 only)

Rhythm	$\overline{IN4}$	$\overline{IN3}$	$\overline{IN2}$	$\overline{IN1}$
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

STATIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD} = 4.75 to 5.25V, T_{amb} = 0 to 50°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
CLOCK INPUT							
V_{IH}	Clock high voltage			2.4		V_{DD}	V
V_{IL}	Clock low voltage			0		0.4	V
DATA INPUTS							
V_{IH}	Input high voltage			2.4		V_{DD}	V
V_{IL}	Input low voltage			0		0.4	V
R_{IN}	Internal resistance to V_{DD}	V_I = 0V	V_{DD}= 5V	100	180		KΩ
I_{OL}(*)	Input load current	$V_I = V_{IL}$			-50		μA
EXT. RESET							
V_{IH}	Input high voltage			4.5		V_{DD}	V
V_{IL}	Input low voltage			0		1.5	V
R_{OFF}	Internal resistance to V_{DD} (inactive sync)	V_O= 0	V_{DD}= 5V	100	180		KΩ
R_{ON}	Internal resistance to V_{DD} (active sync)	V_O= 1V	V_{DD}= 4.75V		260	300	Ω
OUTPUTS (O_i, Down beat)							
R_{ON}		V_O= 1V			260	300	Ω
V_{OL}		Source current = 1 mA			0.26	0.3	V
I_{LO}		V_O= 12V	T_{amb}= 25°C			10	μA
POWER DISSIPATION							
I	Supply current	T_{amb}= 25°C			30		mA

(*) The "High Level" is clamped by the internal pull-up.



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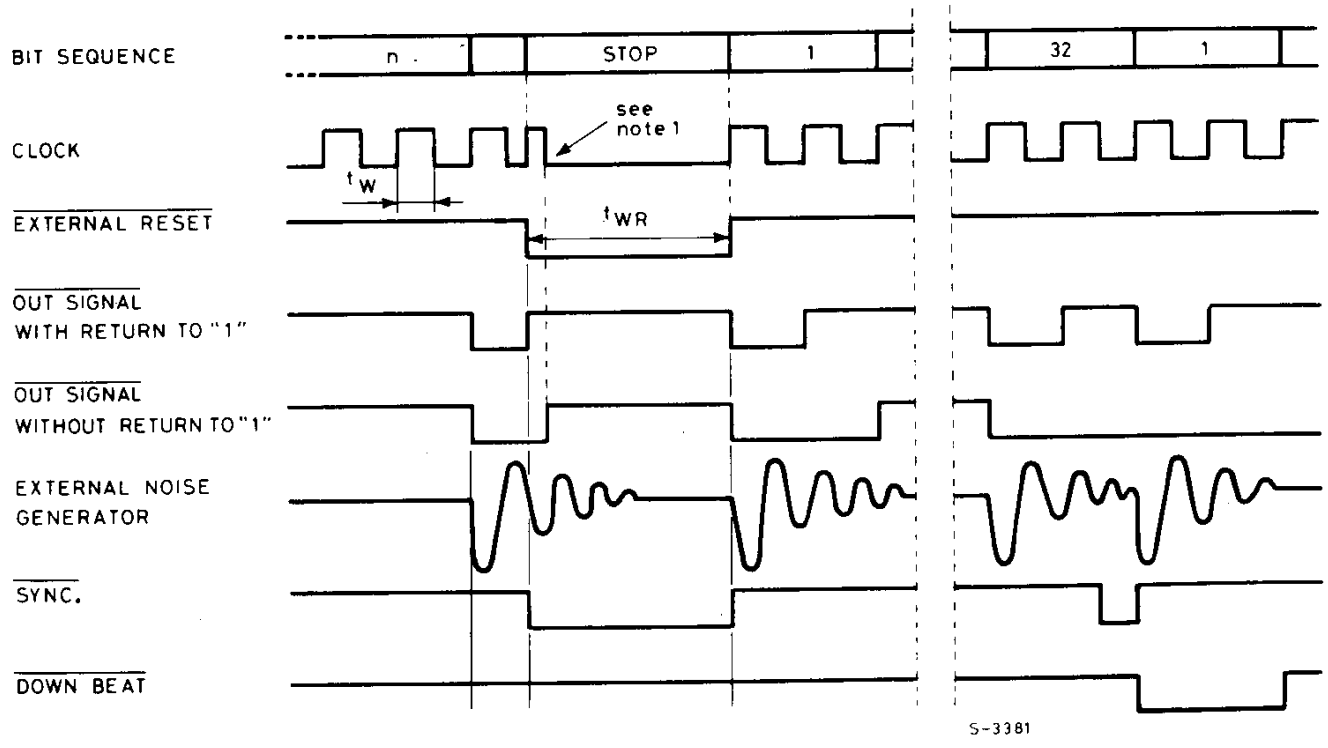
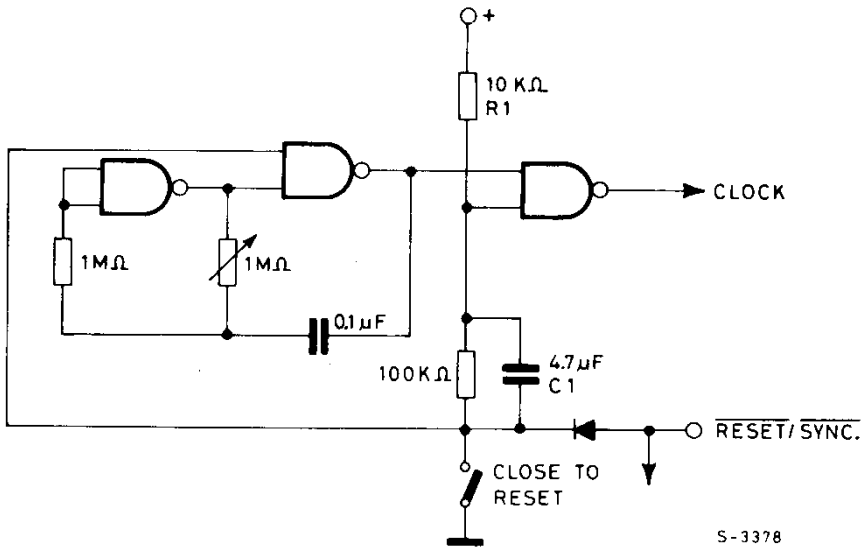
DYNAMIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD}= 4.75 to 5.25V, T_{amb} = 0 to 50°C unless otherwise specified)

Parameter		Test condistions	Values			Unit
			Min.	Typ.	Max.	
CLOCK INPUT						
f	Clock repetition rate		DC		100	KHz
t_w	Pulse width	Measured at 50% of the swing	5			µs
t_r	Rise time	Measured between 10% and 90% of the swing			100	µs
t_f	Fall time	Measured between 10% and 90% of the swing			100	µs
EXT. RESET						
t_{wR}	Pulse width		100			µs
t_{CR}	Clock delay with respect to reset		0			µs

TIMING WAVEFORMS

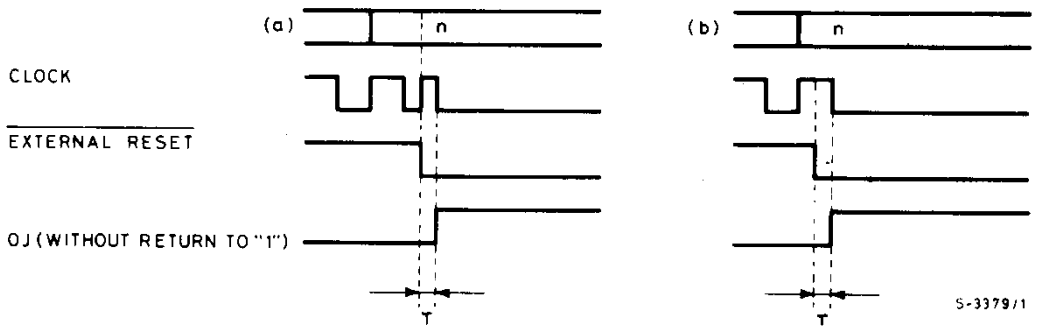


Note 1: This additional pulse, to reset the outputs without return to "1", can be obtained by using a clock generator as shown in the following diagram:



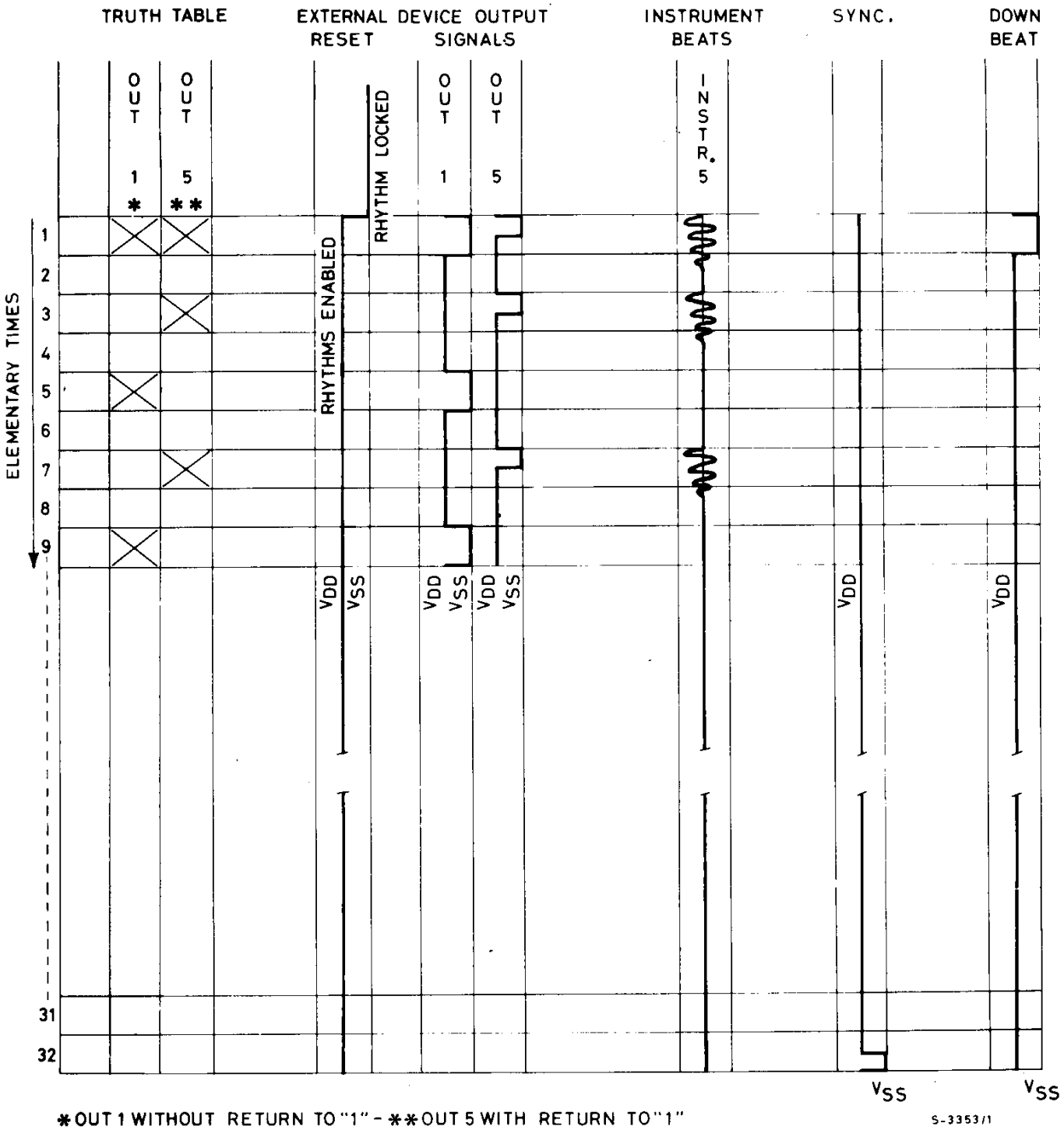
Ext. Reset/Sync. is a bidirectional pin. Used as an input it can reset the circuit as shown in the timing diagram and used as an output it can drive the reset of other devices.

Using the clock generator shown in the above figure, when the switch is closed asynchronous with respect to the clock, it is possible to have to two cases (see the following diagrams); in both the cases the output reset can be obtained by CS1 and CS2.



In both the cases the delay τ (in the outputs without return to "1") is defined through the constant R1 C1 $\geqslant$ 10 μsec.

INSTRUMENT BEATS VERSUS RHYTHM PROGRAM



Note: The output 01 to 08 are enabled by CS1; the outputs 09 to 12 are enabled by CS2. The outputs 01 to 04 and 09 to 12 are programmable separately without return to "1".

COS/MOS INTEGRATED CIRCUITS

M 738/M 740
M 741/M 747

PRELIMINARY DATA

7-STAGE DIVIDER

- LOW POWER DISSIPATION
- LOW OUTPUT IMPEDANCE ON BOTH HIGH AND LOW STATE
- WIDE SUPPLY VOLTAGE RANGE: 5 to 15V
- HIGH NOISE IMMUNITY
- INPUTS FULLY PROTECTED

The M738/M740/M741/M747 are integrated circuits constructed in COS/MOS technology for use as frequency dividers in electronic organs. All the devices consist of 7 stages of binary division connected to give five divider blocks for the M741/M747 and four divider blocks for the M738/M740. The information transfer occurs on the positive going edge of the clock, for M740 and M747, and the negative going edge of the clock for M738/M741, and each output features a symmetrical impedance buffer (300Ω typ. at V_{DD}= 10V). They are available in 14 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to	15	V
V_I	Input voltage (at any pin)	-0.5 to V_{DD}	+0.5	V
P_{tot}	Total power dissipation (per package)		200	mW
T_{stg}	Storage temperature	-65 to	150	°C
T_{op}	Operating temperature	-40 to	85	°C

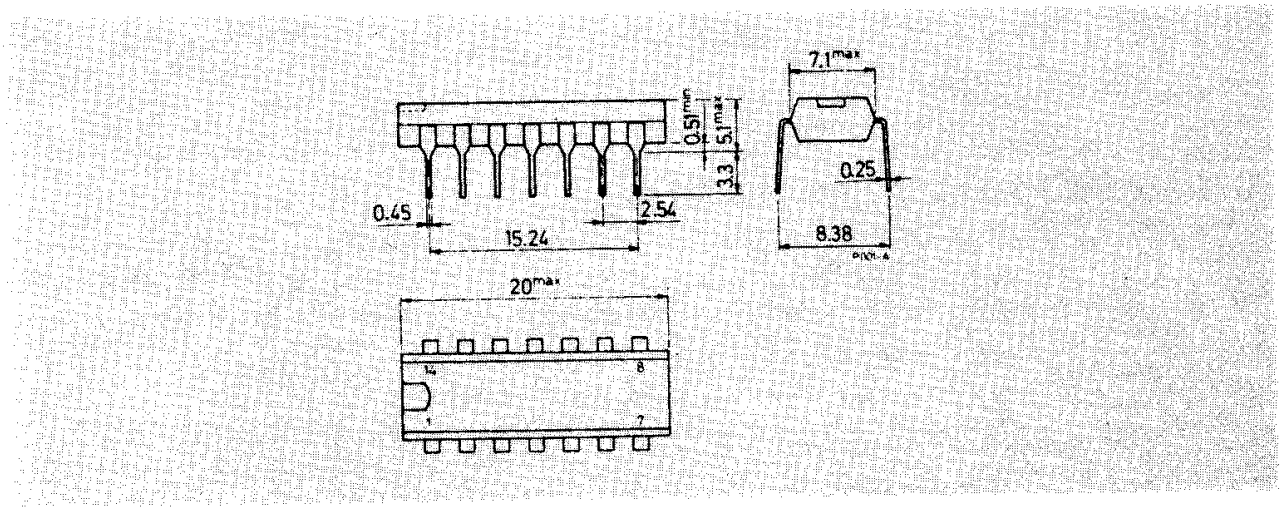
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages values are refered to V_{SS} pin voltage.

ORDERING NUMBERS: M 7XX B1 for dual in-line plastic package

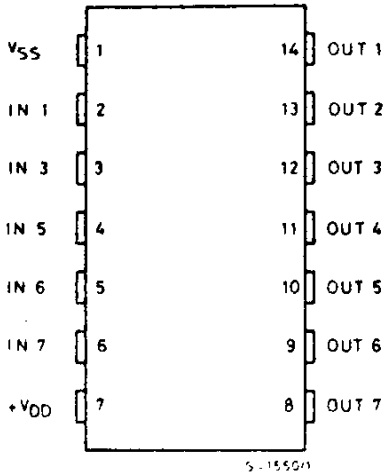
MECHANICAL DATA

Dimensions in mm



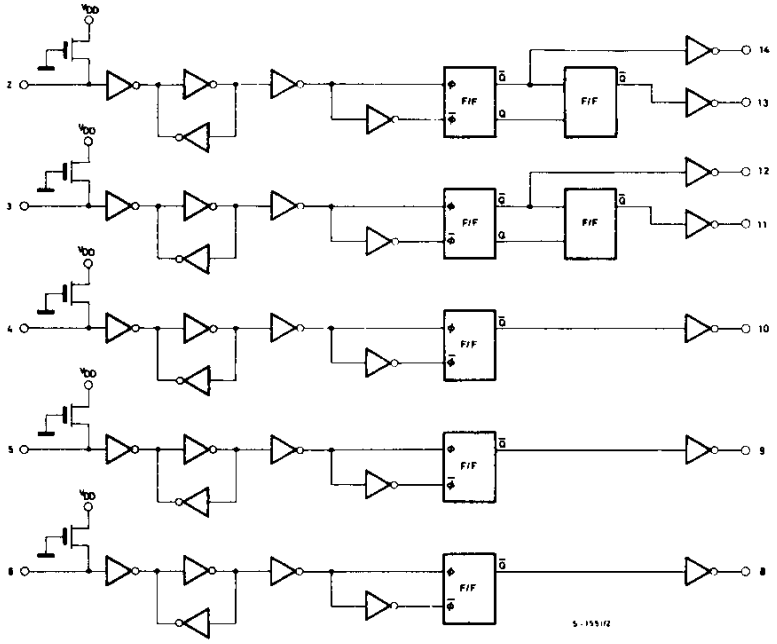
CONNECTION DIAGRAMS

For M741/M747

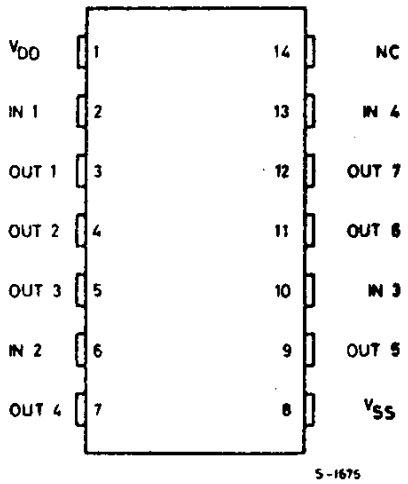


FUNCTIONAL DIAGRAMS

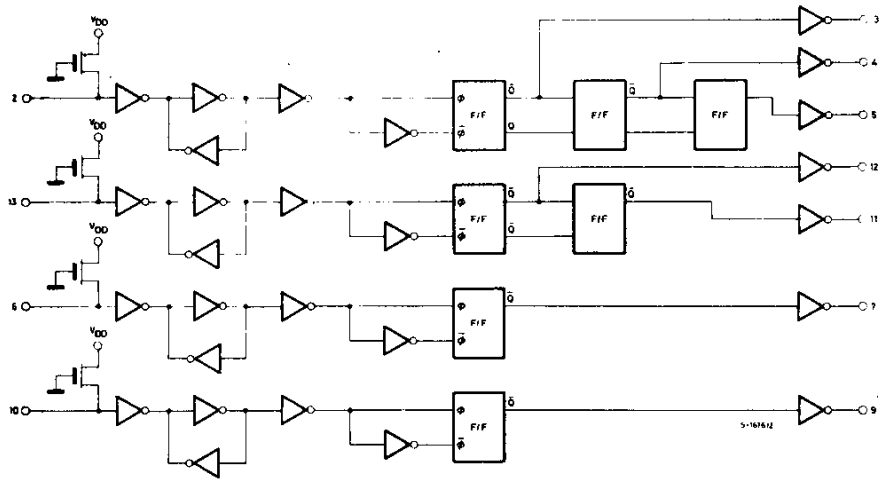
For M741/M747



For M738/M740



For M738/M740



RECOMMENDED OPERATING CONDITIONS

Parameter		V_{DD}(V)	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		5		15	V
V_I	Input voltage		-0.5		V_{DD}+0.5	V
T_{op}	Operating temperature		-40		85	°C
t_w	Width of clock pulse (high or low)	5		200		ns
		10		100		

STATIC ELECTRICAL CHARACTERISTICS (over recomended operating conditions)

Typical values are at T_{amb} = 25°C

Parameter	Test conditions			Values									Unit
		V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CCL} Quiescent supply current	V_i=V_{DD}		5			5			5			300	μA
			10			10			10			600	
			15			50			50			2000	
V_{OH} High level output voltage	I_o= 0		5	4.99			4.99			4.95			V
			10	9.99			9.99			9.95			
			15	14.99			14.99			14.95			
V_{OL} Low level output voltage	I_o= 0		5			0.01			0.01			0.05	V
			10			0.01			0.01			0.05	
			15			0.01			0.01			0.05	
I_{OL} Output drive current N-channel		0.5	5	0.5			0.5	0.8		0.45			mA
		0.5	10	1			1	1.6		0.95			
		0.5	15	1.6			1.6	2.5		1.55			
I_{OH} Output drive current P-channel		4.5	5	-0.5			-0.5	-0.8		-0.45			mA
		9.5	10	-1			-1	-1.6		-0.95			
		14.5	15	-1.6			-1.6	-2.5		-1.55			
I_{IL} Input current	V_i= 0		15				3	30	100				μA
I_{IH} Input current	V_i=V_{DD}		15			1			1			1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C)

Parameter		Test conditions		Values			Unit
			V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time from inputs to:	1 division stage outputs	C_L = 15 pF on all outputs see timing diagram	5			500	ns
			10			250	
	2 division stage outputs		5			1000	ns
			10			500	
	3 division stage outputs		5			1500	ns
			10			750	
t_{TLH}, t_{THL} Output transition time			5			500	ns
			10			250	
f_{max} Maximum toggle frequency		C_L= 15 pF on all outputs	5	0.6	2.5		MHz
			10	2	5		
* Cross talk immunity level					70		dB
C_I Input capacitance					5		pF

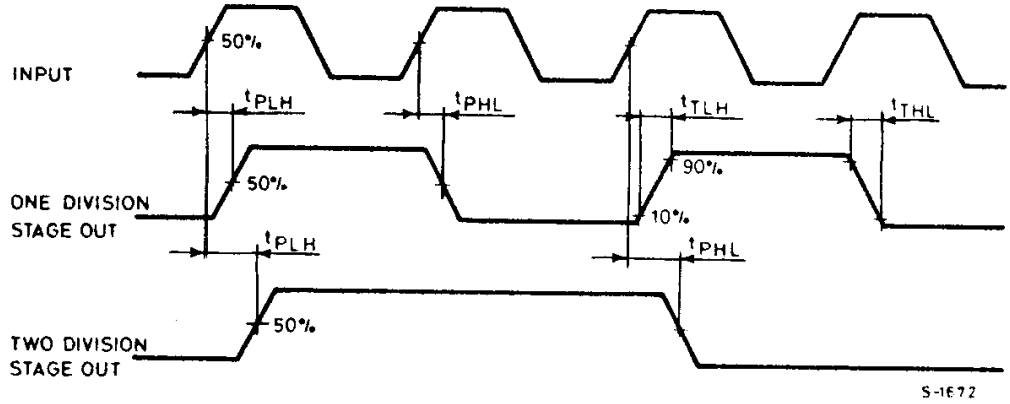
* Send a frequency of 20 kHz to input V_{I1} charge output V_{O1} with 5 kΩ and 15 pF, measure the level of the 10 kHz frequency present at all outputs.

Cross talk level = $20 \log \frac{V_{O1}\ (10\ kHz)}{V_{OX}\ (10\ kHz)}$.

With the exception of V_{O1}, the output where the 10 kHz signal is greatest is V_{OX}.
This operation is repeated for all the inputs.

TIMING DIAGRAM

For M740/M747



For M738/M741