Precision Low-Side, 125 kSps Simultaneous Sampling, Current Sensor and Voltage Monitor with SPI

Check for Samples: LMP92064

FEATURES

- **Two Simultaneous Sampling 12-bit ADCs**
  - **Conversion Rate: 125 kSps (Min)**
- **12-bit Current Sense Channel**
  - **Input-referred Offset: ±15 µV**
  - **Common-mode Voltage Range: –0.2V to 2V**
  - **Maximum Differential Input Voltage: +75 mV**
  - **Fixed Gain: 25 V/V**
  - **Gain Error: ±0.75 % (Max)**
  - **Bandwidth (–3dB): 70 kHz**
  - **DC PSRR: 100 dB**
  - **DC CMRR: 110 dB**
- **12-bit Voltage Channel**
  - **INL: ±1LSB**
  - **Offset Error: ±2 mV (Max)**
  - **Gain Error: ±0.75% (Max)**
  - **Maximum Input Voltage: +2.048V**
  - **Bandwidth: 100 kHz**
- **Internal Reference**
- **SPI Frequency: Up to 20 MHz**
- **Temperature Range: –40°C to +105°C**
- **WSON-16 Package**

APPLICATIONS

- **Enterprise Servers**
- **Telecommunications**
- **Power Management**

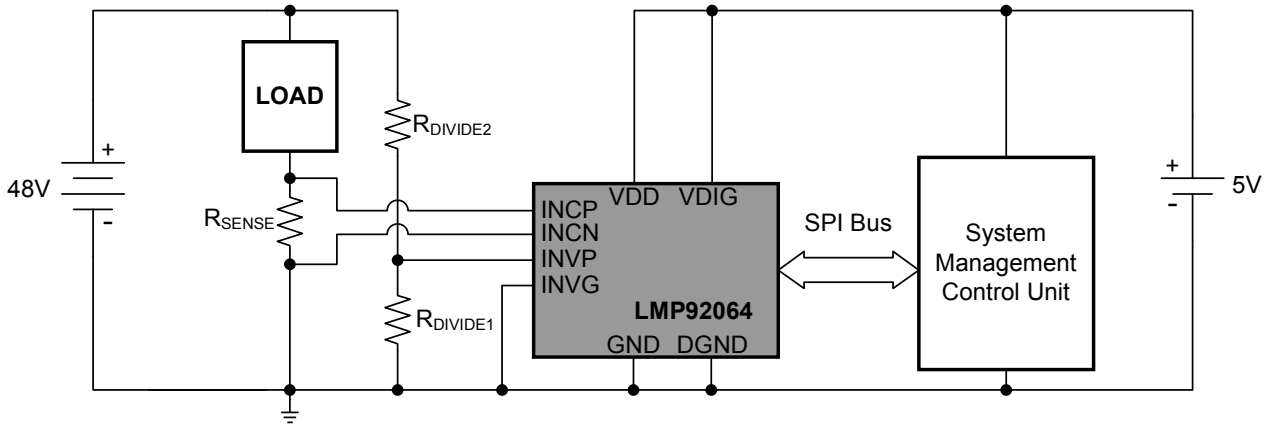
DESCRIPTION

The LMP92064 is a precision low-side digital current sensor and voltage monitor with a digital SPI interface. This analog front-end (AFE) includes a precision current sense amplifier to measure a load current across a shunt resistor and a buffered voltage channel to measure the voltage supply of the load. The current and voltage channels are sampled simultaneously by independent 125 kSps 12-bit ADC converters, allowing for very accurate power calculations in unidirectional sensing applications.

The LMP92064 includes an internal 2.048V reference for the ADCs, eliminating the need of an external reference and reducing component count and board space.

A host can communicate with the LMP92064 using a four-wire SPI interface running at speeds of up to 20 MHz. The fast SPI interface allows the user to take advantage of the higher bandwidth ADC to capture fast varying signals. The four-wire interface with dedicated unidirectional input and output lines also allows for an easy interface to digital isolators in applications where isolation is required.

The LMP92064 operates from a single 4.5V to 5.5V supply and includes a separate digital supply pin. The LMP92064 is specified over a temperature range of –40°C to 105°C, and is available in a 5mm x 4mm WSON-16 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM

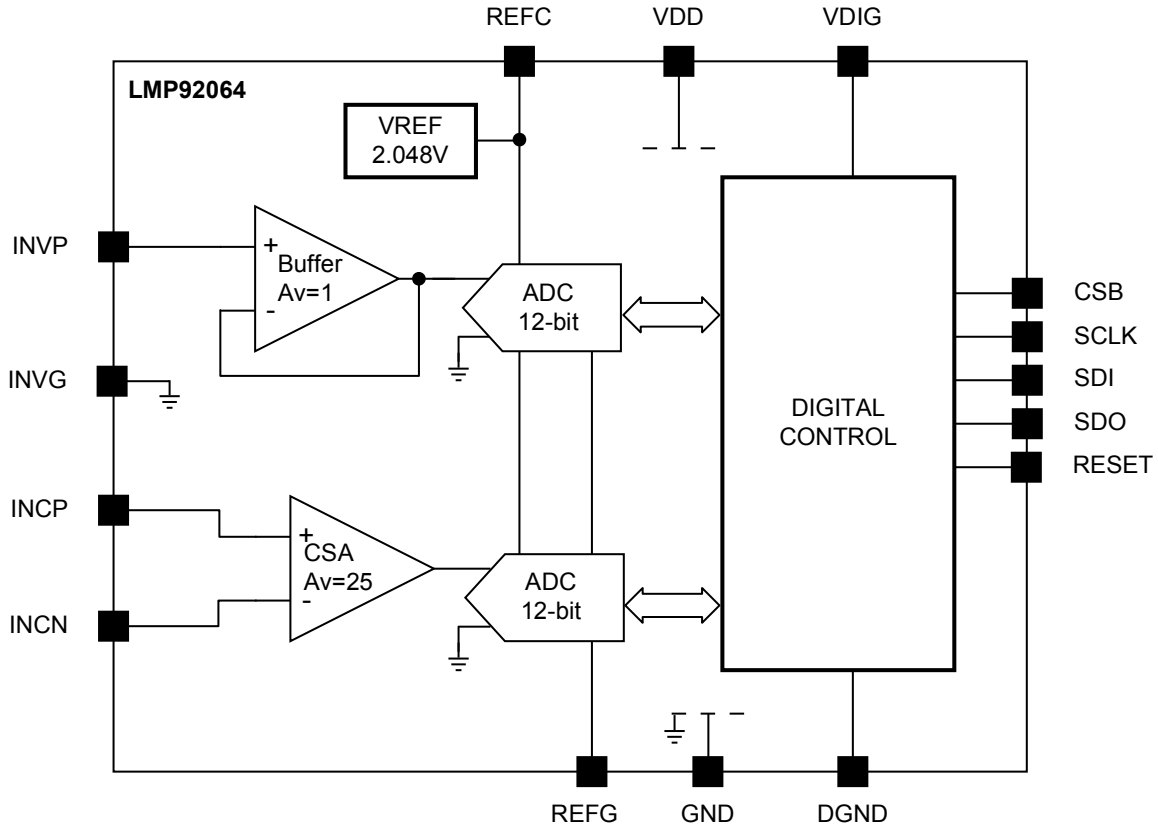


Figure 1.

CONNECTION DIAGRAM

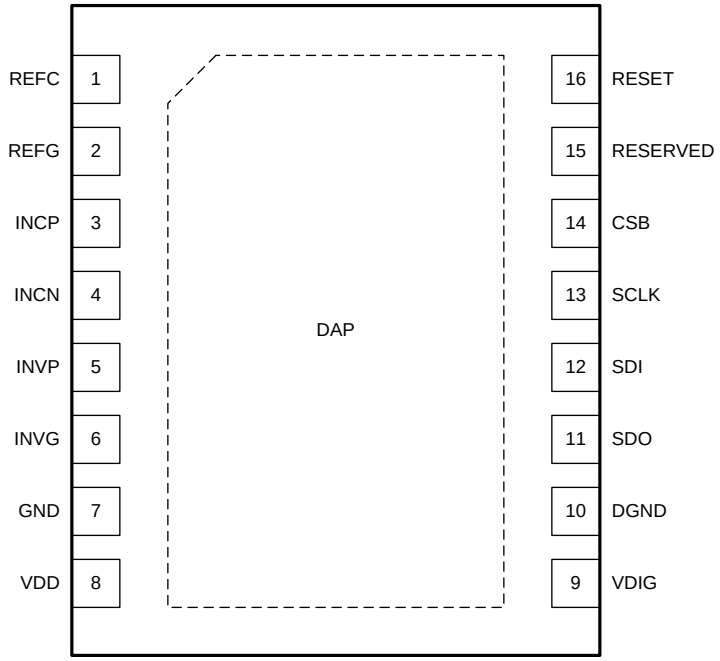


Figure 2. Top View
WSON-16 Package

Table 1. Pin Descriptions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
1	REFC	n/a	Internal reference bypass capacitor pin
2	REFG	G	Internal reference ground
3	INCP	I	Positive current channel input
4	INCN	I	Negative current channel input
5	INVP	I	Positive voltage channel input
6	INVG	G	Ground reference for the negative voltage channel input
7	GND	G	Analog ground
8	VDD	P	Analog power supply
9	VDIG	P	Digital power supply
10	DGND	G	Digital ground
11	SDO	O	SPI Bus push-pull serial data digital output
12	SDI	I	SPI Bus serial data digital input
13	SCLK	I	SPI Bus clock digital input
14	CSB	I	SPI Bus chip select bar digital input
15	RESERVED	n/a	Reserved (Do not connect)
16	RESET	I	Reset (high-active)
n/a	DAP	n/a	No connection (Do not connect)

(1) G = Ground, I = Input, O = Output, P = Power

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Analog Supply Voltage (VDD)		–0.3	6.0	V
Digital Supply Voltage (VDIG)		VDD-0.3	VDD+0.3	
Voltage at Input Pins(3)		–0.3	VDD+0.3	V
Storage Temperature Range		–65	150	°C
Junction Temperature			150	°C
Mounting temperature	Infrared or convection (20 sec)		260	°C
ESD Tolerance	Human Body Model		2000	V
	Charged Device Model		1000	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = DGND = 0V, unless otherwise specified.
(3) When the input voltage (VIN), at any pin exceeds power supplies (VIN < GND or VIN > VDD), the current at that pin must not exceed 5mA, and the voltage (VIN) at that pin must not exceed 6.0V. See *Pin Description* for additional details of input circuitry.

THERMAL CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted)

				UNIT
θ_{JA}	Package thermal resistance(1)	WSON-16	44	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7. The maximum power dissipation must be de-rated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

RECOMMENDED OPERATING CONDITIONS(1)(2)

	MIN	MAX	UNIT
Analog Supply Voltage (VDD)	4.5	5.5	V
Digital Supply Voltage (VDIG)	VDD		V
Temperature Range	–40	105	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = DGND = 0V, unless otherwise specified.

ELECTRICAL CHARACTERISTICS

Typical specifications are at 25ºC. All specifications are at 4.5V ≤ VDD ≤ 5.5V, VDIG = VDD and –0.2V ≤ VCM ≤ 2V, unless otherwise specified. **Boldface limits apply at temperature extremes.**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE INPUT CHANNEL						
V_{OS}	Input-referred Offset Voltage			±15	**±60**	µV
TCV_{OS}	Input-referred Offset Voltage Drift			±280		nV/ºC
	Long-term Stability			0.3		µV/mo
	Resolution			12 20		Bits µV
INL	Integral Non-Linearity Error			±1 ±0.025		LSB %
DNL	Differential Non-Linearity Error			±0.5		LSB
DC CMRR	Common-Mode Rejection Ratio	–0.2V ≤ VCM ≤ 2V		110		dB
DC PSRR	Power Supply Rejection Ratio	4.5V ≤ VDD ≤ 5.5V		100		dB
CMVR	Common-Mode Voltage Range	Low VCM		–0.2		V
		High VCM		2		
$V_{DIFF(MAX)}$	Maximum Differential Input Voltage Range			75		mV
A_V	Current Shunt Amplifier Gain			25		V/V
	Current Sense Channel Gain			50		kCode/V
GE	Gain Error (CSA, VREF and ADC)				**±0.75**	%
GD	Gain Drift			±25		ppm/°C
RIN	Input Impedance			100		GΩ
BW	–3dB Bandwidth			70		kHz
VOLTAGE INPUT CHANNEL						
	Offset Error (Buffer and ADC)		**–2**		**2**	mV
	Resolution			12		Bits
INL	Integral Non-Linearity Error			±1 ±0.025		LSB %
DC PSRR	Power Supply Rejection Ratio			70		dB
V_{CHVP}	Full-Scale Input Voltage			2.048		V
A_V	Buffer Amplifier Gain			1		V/V
	Voltage Sense Channel Gain			2		kCode/V
GE	Gain Error (Buffer, VREF and ADC)				**±0.75**	%
RIN	Input Impedance			100		GΩ
BW	Bandwidth (1)			100		kHz
DIGITAL INPUT/OUTPUT CHARACTERISTICS						
V_{IH}	Logical “1” Input Voltage		**0.7*VDIG**			V
V_{IL}	Logical “0” Input Voltage				**0.3*VDIG**	V
V_{OH}	Logical “1” Output Voltage	I_{SOURCE} = 300µA	**VDIG –0.15**			V
V_{OL}	Logical “0” Output Voltage	I_{SINK} = 300µA			**DGND +0.15**	V
SUPPLY CHARACTERISTICS						
I_{VDD}	Analog Supply Current			11		mA
I_{VDIG}	Digital Supply Current			2		mA

(1) No analog filter; limited by sampling rate.

TIMING CHARACTERISTICS

Typical specifications are at 25ºC. All specifications are at 4.5V ≤ VDD ≤ 5.5V, VDIG = VDD and a 20 pF capacitive load on SDO, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DS}	SDI to SCLK rising edge setup time		10			ns
t_{DH}	SCLK rising edge to SDI hold time		10			ns
f_{CLK}	Frequency of SCLK		100			Hz
					20	MHz
t_{HIGH}	High width of SPI clock		25			ns
t_{LOW}	Low width of SPI clock		25			ns
t_S	CSB falling edge to SCLK rising edge setup time		10			ns
t_C	SCLK rising edge to CSB rising edge hold time		30			ns
t_{DV}	SCLK falling edge to valid SDO readback data				20	ns
t_{RST}	Reset pin pulse width		3.5			ns
t_{CONV}	Conversion rate of all channels		125			kSps

TIMING DIAGRAMS

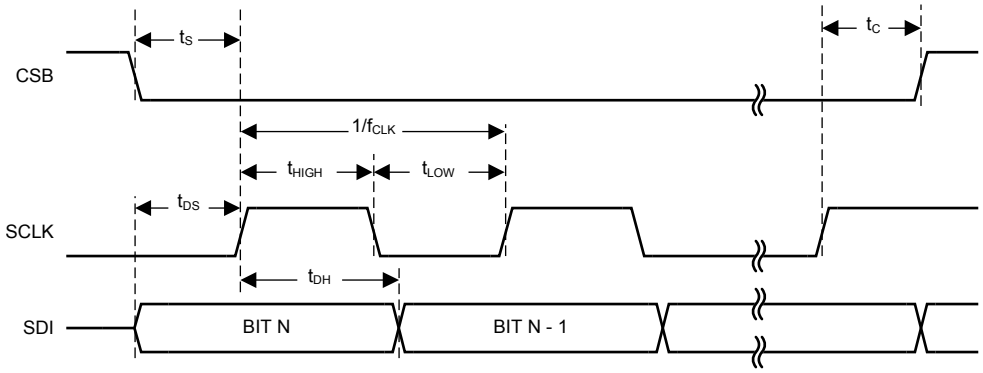


Figure 3. Serial Control Port Timing – Write

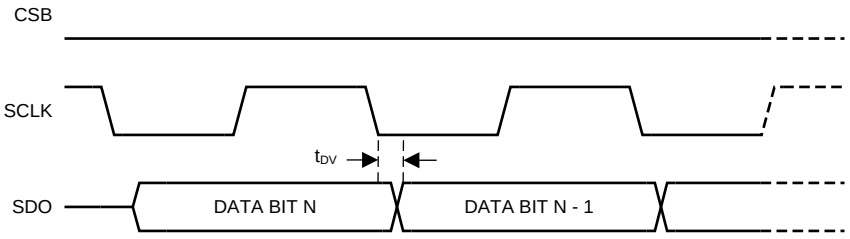


Figure 4. Serial Control Port Timing – Read

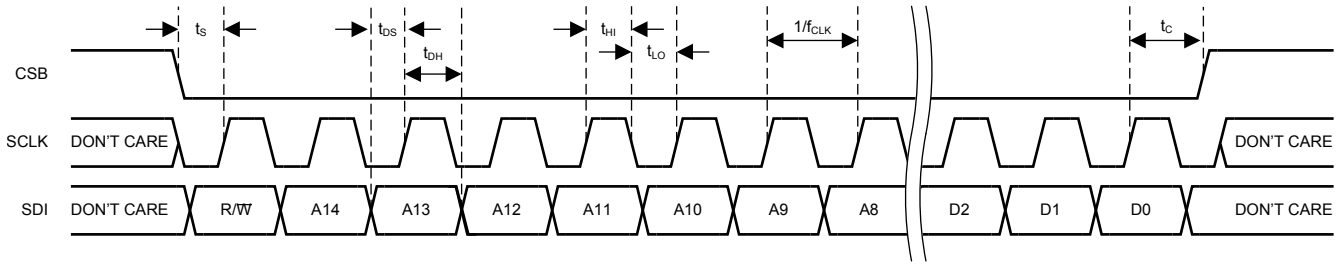


Figure 5. Serial Control Port Write – MSB First, 16-bit Instruction, Timing Measurements

TYPICAL CHARACTERISTICS

All plots at T_A = 25ºC, VDD = 5.0V, VDIG = 5.0V, VCM = 0V and GND = DGND = 0V, unless otherwise specified.

ANALOG SUPPLY CURRENT vs SUPPLY VOLTAGE

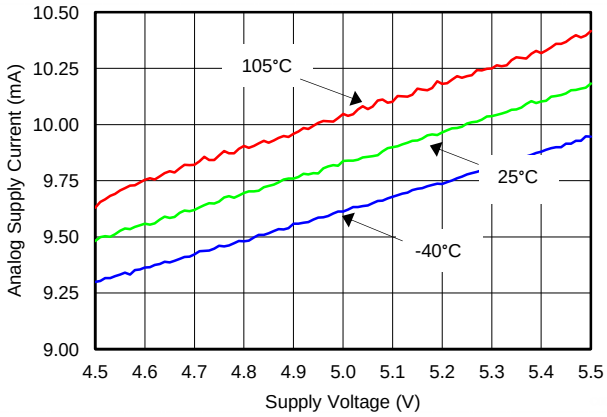


Figure 6.

INPUT-REFERRED OFFSET vs SUPPLY VOLTAGE (Current Channel)

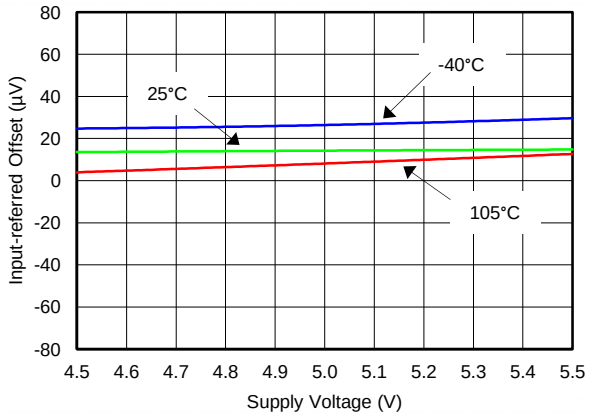


Figure 7.

INPUT-REFERRED OFFSET vs COMMON-MODE VOLTAGE (Current Channel)

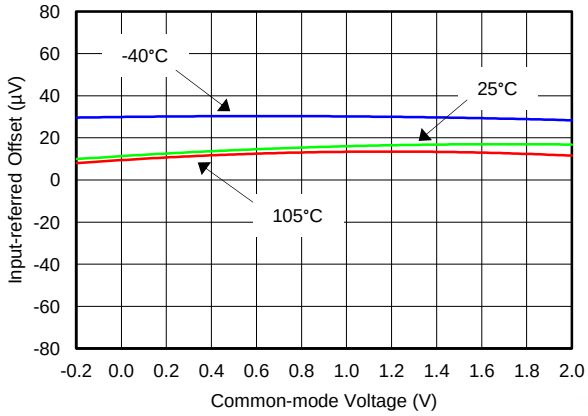


Figure 8.

GAIN ERROR vs SUPPLY VOLTAGE (Current Channel)

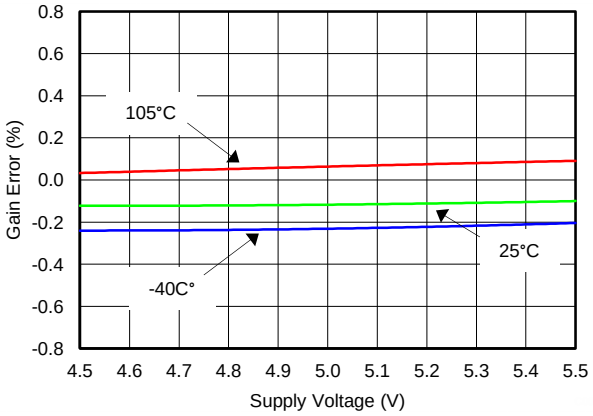


Figure 9.

GAIN ERROR vs COMMON-MODE VOLTAGE (Current Channel)

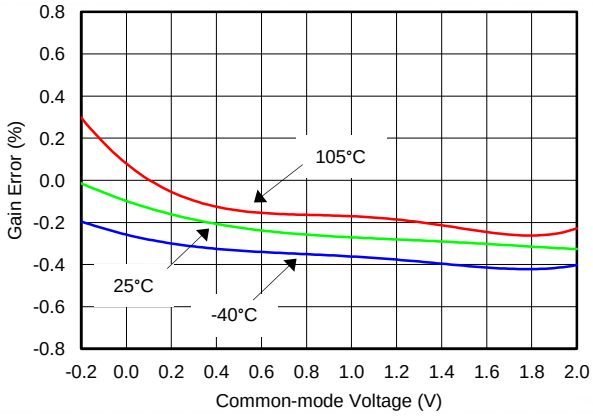


Figure 10.

GAIN vs FREQUENCY (Current Channel)

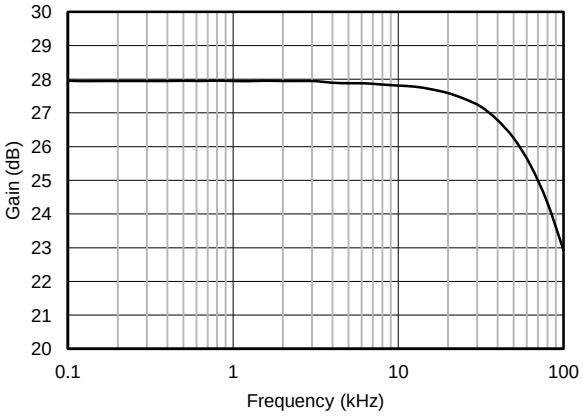


Figure 11.

TYPICAL CHARACTERISTICS (continued)

All plots at T_A = 25ºC, VDD = 5.0V, VDIG = 5.0V, VCM = 0V and GND = DGND = 0V, unless otherwise specified.

DIFFERENTIAL NONLINEARITY (Current Channel)

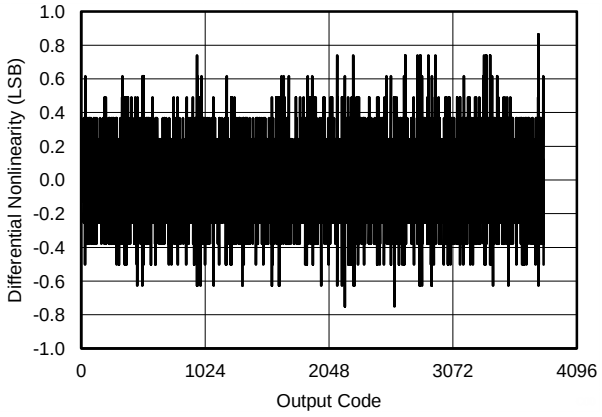


Figure 12.

INTEGRAL NONLINEARITY (Current Channel)

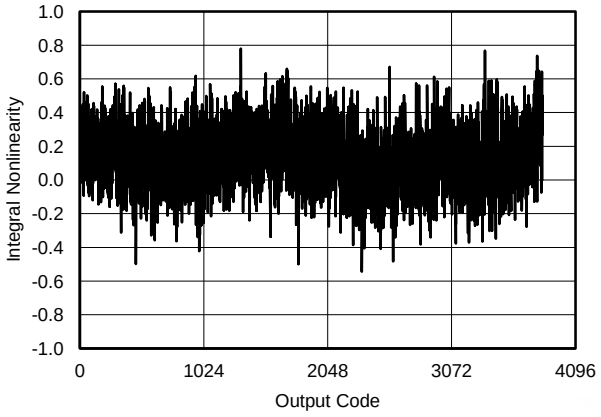


Figure 13.

COMMON-MODE REJECTION RATIO DISTRIBUTION (Current Channel)

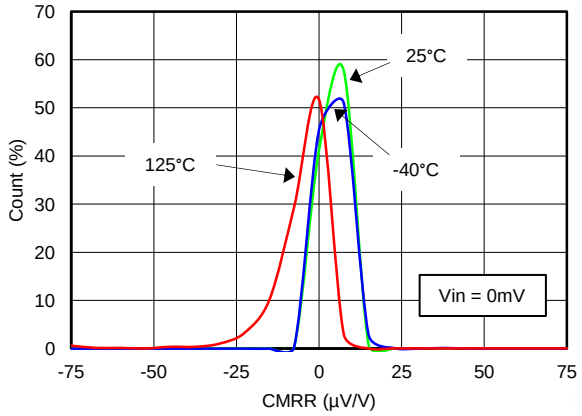


Figure 14.

POWER SUPPLY REJECTION RATIO DISTRIBUTION VCM = -0.2V (Current Channel)

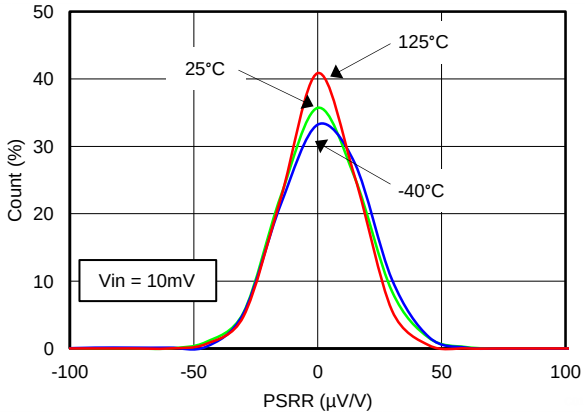


Figure 15.

INPUT-REFERRED OFFSET VS SUPPLY VOLTAGE (Voltage Channel)

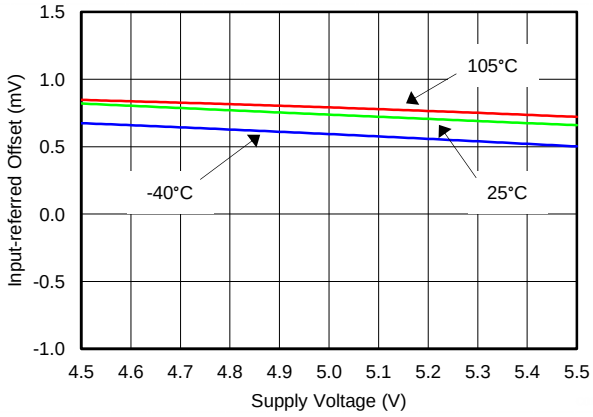


Figure 16.

GAIN ERROR VS SUPPLY VOLTAGE (Voltage Channel)

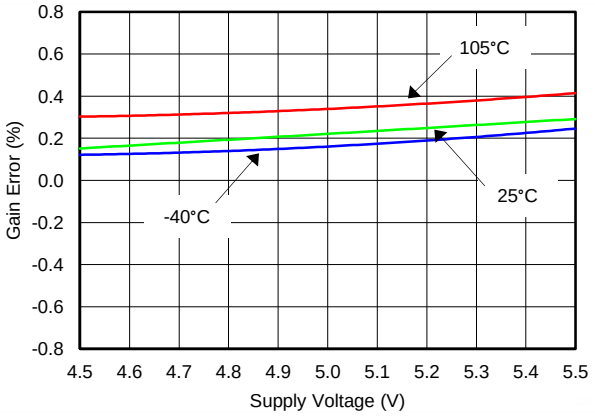


Figure 17.

TYPICAL CHARACTERISTICS (continued)

All plots at T_A = 25ºC, VDD = 5.0V, VDIG = 5.0V, VCM = 0V and GND = DGND = 0V, unless otherwise specified.

DIFFERENTIAL NONLINEARITY (Voltage Channel)

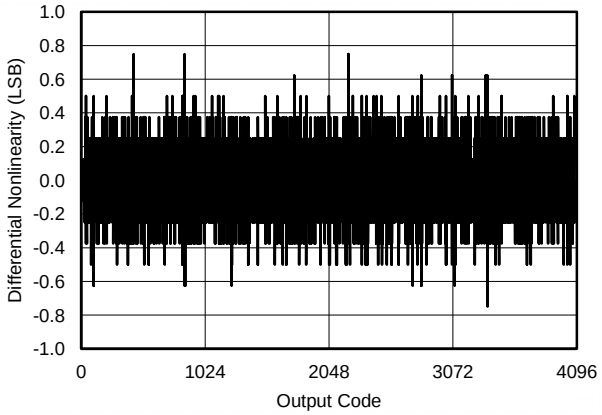


Figure 18.

INTEGRAL NONLINEARITY (Voltage Channel)

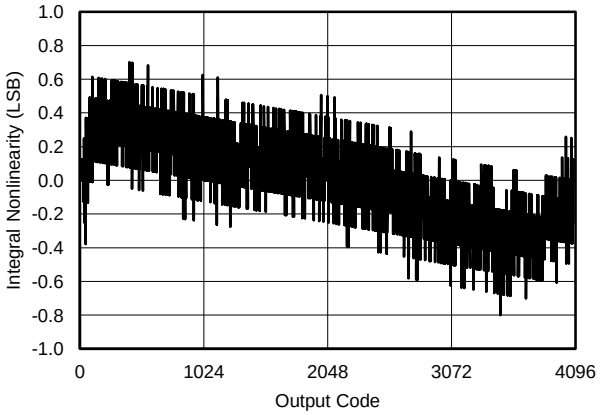


Figure 19.

POWER SUPPLY REJECTION RATIO DISTRIBUTION (Voltage Channel)

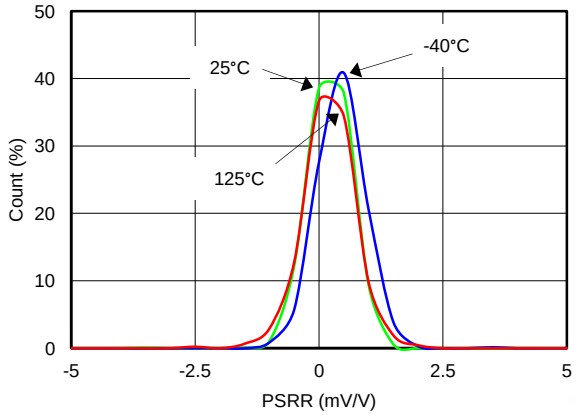


Figure 20.

GAIN VS FREQUENCY (Voltage Channel)

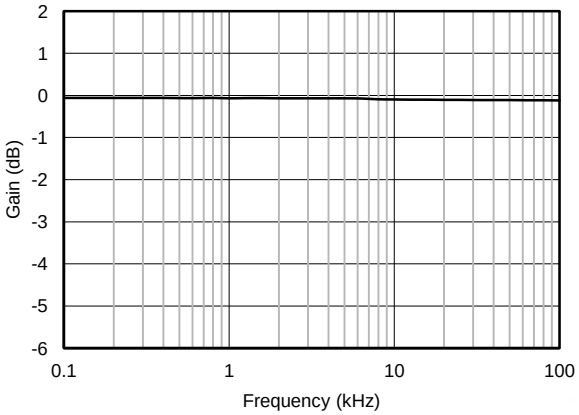


Figure 21.

APPLICATION INFORMATION

Current Sense Input Channel

The current sensing channel of the LMP92064 has a high impedance differential amplifier followed by a 12-bit analog-to-digital converter. The binary code result of a conversion is stored as a right-justified 16-bit number as shown in Table 2, where the 4 most significant bits are always 0. Due to an offset auto-calibration feature of the current sense channel path, the top 256 codes are clipped at code 3840, denoted by the trailing zeros found in the equivalent binary code of the maximum positive input voltage.

The output data of the current sense channel is accessible on registers 0x0203 and 0x0202.

Table 2. Ideal Current Channel Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT	
Full scale range	**V_{FS}= 81.92 mV**		
Least significant bit (LSB)	**V_{FS} / 4096**	**BINARY CODE [B15:B0]**	**HEX CODE**
Maximum Positive Input Voltage	V_{FS} – 256 LSB	0000 1111 0000 0000	0x0F00
Zero	0V	0000 0000 0000 0000	0x0000

Selection of the Current Sense Resistor

The accuracy of the current measurement depends heavily on the accuracy of the shunt resistor R_{SENSE}. Its value depends on the application and it is a compromise between signal accuracy, maximum permissible voltage loss and power dissipation in the shunt resistor. High values of R_{SENSE} provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_{SENSE} minimize voltage loss in the supply section, but at the expense of low-end accuracy.

The use of a “4-terminal” or “Kelvin” sense resistor is highly recommended. See the CURRENT INPUT ERROR SOURCES AND LAYOUT CONSIDERATIONS section for more information.

Current Sense Input Channel Common-Mode and Differential Voltage Range (Dynamic Range Considerations)

The input voltage should be in the range of –0.2V to 2V. The input can withstand voltage up to VDD+0.3V absolute maximum but the operational range is limited to 2V. Operation below –0.2V or above 2V on either input pin will introduce severe gain errors and non-linearity.

The maximum differential voltage (defined as the voltage difference between INCP and INCN) for which the part is designed to work is 75 mV. Larger differential or common mode input voltages will not damage the part (as long as the input pins remain between GND-0.3V and VDD+0.3V), however, exposure for extended periods may affect device reliability. The ADC output code will not roll over and will clip at min or max scale when the maximum differential voltage is exceeded.

Current Input Error Sources and Layout Considerations

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors (<100 mΩ), trace resistance shared with the load can cause significant errors. It is recommended to connect the sense resistor pads directly to the LMP92064's INCP and INCN inputs using “Kelvin” or “4-wire” connection techniques. An example is shown in Figure 22.

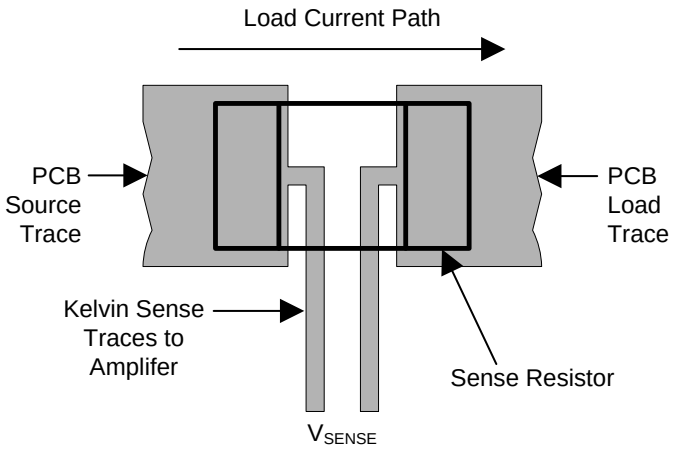


Figure 22. 4-Wire "Kelvin" Sensing Technique

Since the sense traces only carry the amplifier bias current, the connecting input traces can be thinner, signal level traces. The traces should be one continuous piece of copper from the sense resistor pad to the LMP92064 input pin pad, and ideally on the same layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat. To minimize noise pickup and thermal errors, the input traces should be treated as a signal pair and routed tightly together with a direct path to the input pins. The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines.

Voltage Sense Input Channel

The voltage sensing channel of the LMP92064 has a high impedance buffer amplifier followed by a 12-bit analog-to-digital converter. The binary code result of a conversion is also stored as a right-justified 16-bit number as shown in Table 3, where the 4 most significant bits are always 0.

The output data of the voltage sense channel is accessible on registers 0x0201 and 0x0200.

Table 3. Ideal Voltage Channel Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT	
Full scale range	**V_{FS}= 2.048V**		
Least significant bit (LSB)	**V_{FS} / 4096**	**BINARY CODE [B15:B0]**	**HEX CODE**
Maximum Positive Input Voltage	V_{FS} – 1 LSB	0000 1111 1111 1111	0x0FFF
Zero Code Voltage	0V	0000 0000 0000 0000	0x0000

Selection of the Voltage Input Resistor Divider

The input buffer amplifier of the voltage channel can tolerate high source impedances, which enables scaling the input voltage with the use of an external resistor divider. The accuracy of the voltage measurements depends on the accuracy of the components used for the resistor divider as well as the impedance of the divider.

Power Supply Decoupling

In order to decouple the LMP92064 from AC noise on the power supply, it is recommended to use a 0.1 µF bypass capacitor between the VDD and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases an additional 10 µF bypass capacitor may further reduce the supply noise. In addition the VDIG power pin should also be decoupled to DGND with a 0.1 µF bypass capacitor. Do not forget that these capacitors must be rated for the full supply voltage (2x the maximum voltage is recommended for the capacitor working voltage rating).

ADC Operation

The LMP92064 includes two 12-bit ADCs that are continuously running in the background. The device is configured, and data is read, using a four-wire SPI interface: CSB, SCLK, SDO and SDI. The device outputs its data on SDO, and the data for both channels is synchronized such that all data read would be from the same instant in time. New conversion data for both channels will only be made available after all registers are read in descending sequential order (addresses 0x0203-0x0200). All registers must be read otherwise new conversion data will not be available. Three different output data formats are available as detailed in Figure 23, Figure 24 and Figure 25.

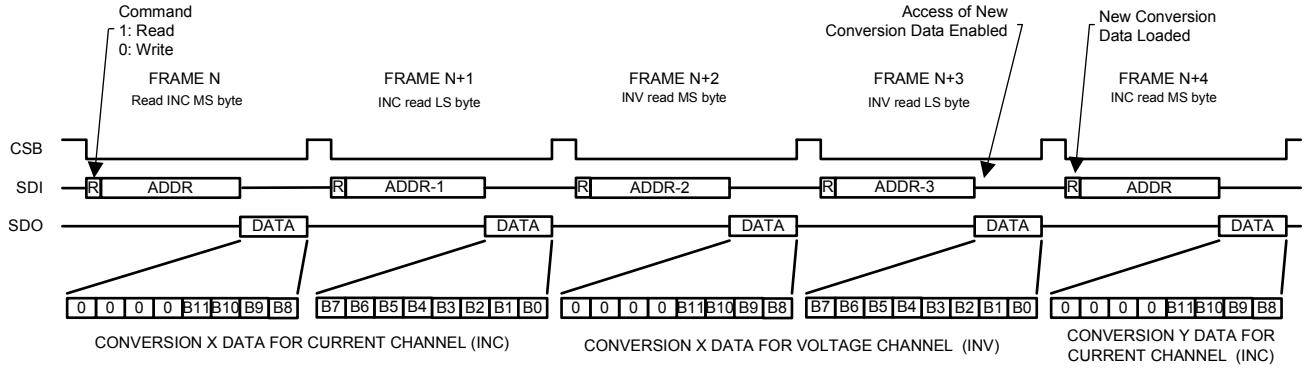


Figure 23. Timing Diagram with Byte Read Frames

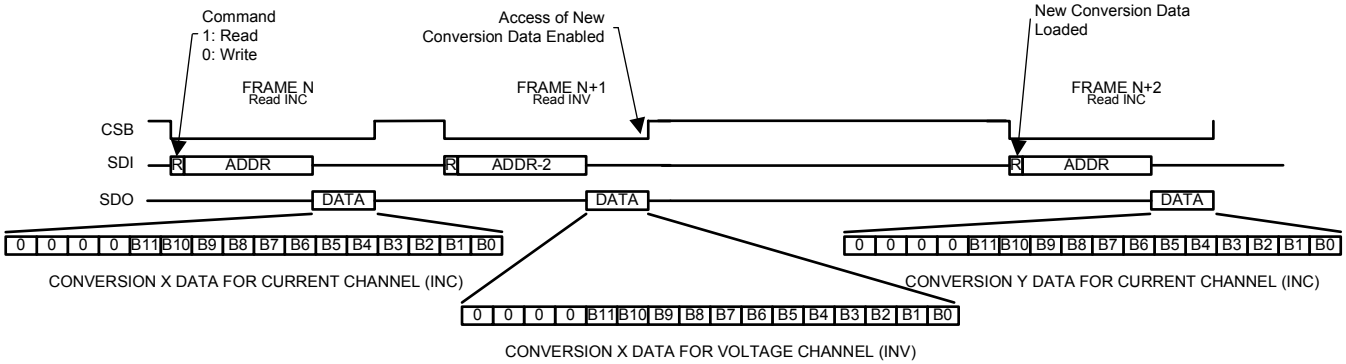


Figure 24. Timing Diagram with Word Read Frames

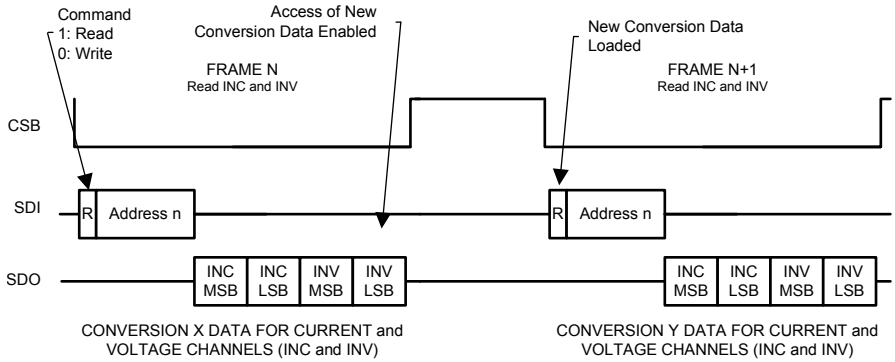


Figure 25. Timing Diagram with All Data Read Frames

The register address to read can automatically decrement if the CSB line is kept low longer. For example, to read all the conversion data, keep the CSB line low for 48 SPI clock cycles (16 clocks for command/address, 8 clocks for MSB of current channel, 8 clocks for LSB of current channel, 8 clocks for MSB of voltage channel and 8 clocks for LSB of voltage channel). The read command should start from address 0x0203.

Device Power-Up Sequence

The sources providing power to the analog and digital supply pins of the LMP92064, VDD and VDIG, must ramp up at the same time to have a proper power-on reset (POR) event. The easiest way to achieve it is to tie VDD and VDIG to the same power source using a star configuration.

Reference

The LMP92064 includes an internal 2.048V band-gap reference for the ADCs, which eliminates the need of an external reference and reduces component count and board space. The REFC pin is provided to allow bypassing this internal reference for low noise operation. A 1 µF ceramic decoupling capacitor is required between the REFC and REFG pins of the converter. The capacitor should be placed as close as possible to the pins of the device.

Reset

There are two methods to reset the LMP92064. A soft reset is done by setting bit7=1 in the CONFIG_A register. In a soft reset, the SPI state machine and the contents of registers 0x0000 and 0x0001 are unnafected.

A hardware reset is done by connecting the RESET pin of the LMP92064 to VDIG. If the pin is driven by a switch or a GPIO, it is recommended to add an external RC filter to prevent reset glitches.

Applications Diagram

A typical application of the LMP92064 is shown in Figure 26. The LMP92064 is monitoring the voltage drop across R_{SENSE} and the voltage across R1. The voltage across R_{SENSE} can be used to calculate the circuitry load current. The voltage across R1 can be used to calculate the -48V supply voltage. To prevent aliasing errors external analog differential filters are shown for each channel.

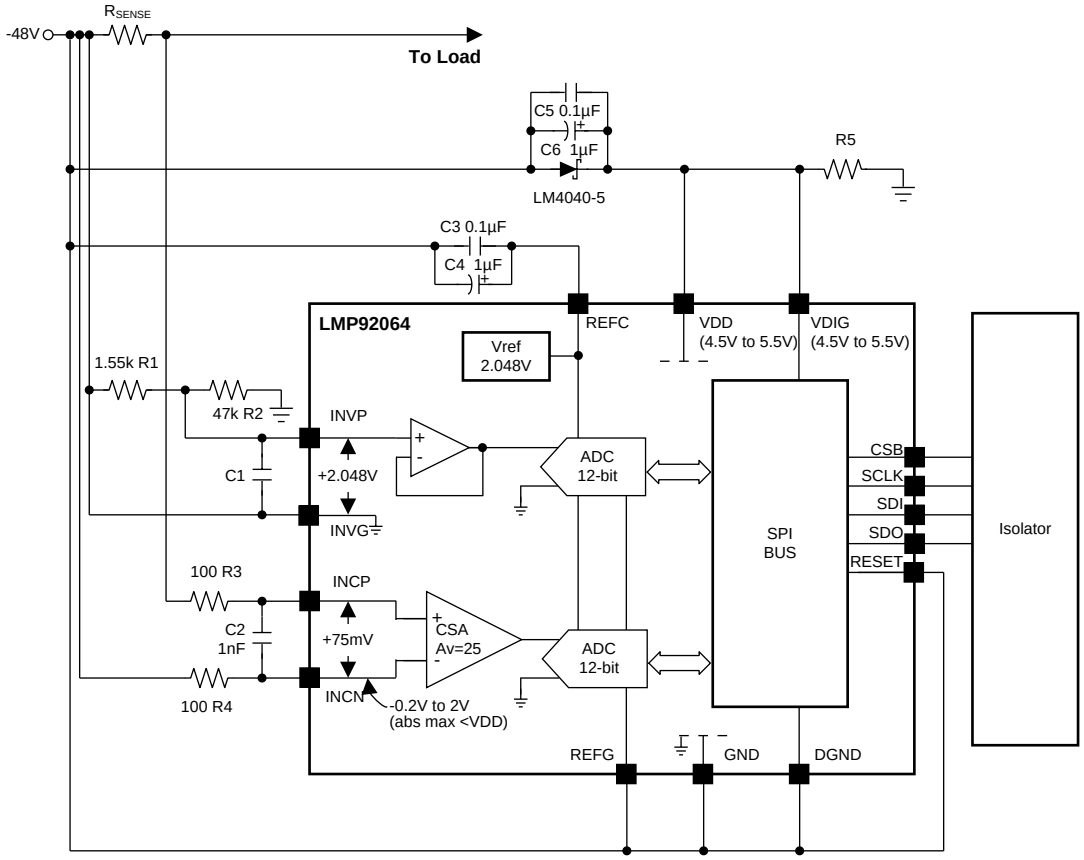


Figure 26. Typical Applications Circuit

Registers

1. If written to, Reserved bits must be written to 0 unless otherwise indicated.
2. Read back value of Reserved bits and registers is unspecified and should be discarded.
3. Recommended values must be programmed and forbidden values must not be programmed where they are indicated in order to avoid unexpected results.
4. If written to, registers indicated as Reserved must have the indicated default value as shown in the register map. Any other value can cause unexpected results.

Table 4. Register Map

REGISTER NAME	REGISTER DESCRIPTION	ADDRESS	ACCESS	DEFAULT
CONFIG_A	Interface Configuration A	0x0000	R/W	0x18
CONFIG_B	Interface Configuration B	0x0001	R/W	0x00
Reserved	Reserved	0x0002	R/W	0x00
CHIP_TYPE	Chip Type	0x0003	RO	0x07
CHIP_ID	Chip ID	0x0004 0x0005	RO	0x00 0x04
CHIP_REV	Chip Revision	0x0006	RO	0x01
MFR_ID	Manufacturer ID	0x000C 0x000D	RO	0x51 0x04
REG_UPDATE	Register Update	0x000F	R/W	0x00
CONFIG_REG	LMP92064 Specific Configuration Register	0x0100	R/W	0x00
STATUS	Status Register	0x0103	RO	N/A
DATA_VOUT	Voltage Channel Output Data	0x0200 0x0201	RO	N/A
DATA_COUT	Current Channel Output Data	0x0202 0x0203	RO	N/A

Table 5. CONFIG_A: Interface Configuration A

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0000	RESET	DDIR	ADDRDIR	SDDIR				

[7] RESET — **Soft reset (self-clearing)** — R/W

0: Normal (default)

1: Reset

Note: Contents of register 0x0000 and 0x0001 and SPI state machine are unaffected

[6] DDIR — **Data direction** — RO

0: Data is transmitted MSB first (default)

[5] ADDRDIR — **Multiple-read auto-address direction** — RO

0: Address auto-decrements (default)

Note: Address 0x0000 will wrap to 0x7FFF

[4] SSDIR — **Serial data direction** — RO

1: Unidirectional; SDI is used for write and SDO is used for read (default)

[3:0] — **Bits [3:0] should always mirror [7:4] as follows:** — R/W

[3] = [4]

[2] = [5]

[1] = [6]

[0] = [7]

Table 6. CONFIG_B: Interface Configuration B

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0001	STREAM	Reserved	BUFREG_RD	Reserved		Reserved		Reserved

[7] STREAM — **Stream** — RO

0: Streaming is on (default)

[6] Reserved — **Reserved** — RO

0 (default)

[5] BUFREG_RD — **Active/buffered register read-back** — R/W

0: Read back from active register (default)

1: Read back from buffered register

Note: Only double-buffered register affected: 0x0100

[4:3] Reserved — **Reserved** — RO

00 (default)

[2:1] Reserved — **Reserved** — RO

00 (default)

[0] Reserved — **Reserved** — RO

0 (default)

Table 7. CHIP_TYPE: Chip Type

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0003	CHIP_TYPE							

[7:0] CHIP_TYPE **Chip type** RO

0x07: Precision ADC

Table 8. CHIP_ID: Chip ID

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0004	CHIP_ID_LSB							

[7:0] CHIP_ID_LSB **Chip ID LSB** RO

0x00 (Manufacturer defined)

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0005	CHIP_ID_MSB							

[7:0] CHIP_ID_MSB **Chip ID MSB** RO

0x04 (Manufacturer defined)

Table 9. CHIP_REV: Chip Revision

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0006	CHIP_REV							

[7:0] CHIP_REV **Chip REV** RO

0x01

Table 10. MFR_ID: Manufacturer ID

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x000C	MFR_ID_LSB							

[7:0] MFR_ID_LSB **Manufacturer ID LSB** RO

0x51

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x000D	MFR_ID_MSB							

[7:0] MFR_ID_MSB **Manufacturer ID MSB** RO

0x04

Table 11. REG_UPDATE: Register Update

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x000F								BUFREG_ UPDATE

[7:1] Reserved **Reserved** RO

0 (default)

[0] BUFREG_ UPDATE **Buffered register update (self clearing)** R/W

0: No action (default)

1: Transfer buffered register contents to active register

Note: Register 0x0100 is buffered.

Table 12. CONFIG_REG: LMP92064 Specific Configuration Register

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0100	Reserved							

[7:0] Reserved **Reserved for future use** R/W

0x00 (default)

Note: This register is double-buffered; register 0x000F must be set to 1 to transfer the contents from the buffer to the active register.

Table 13. STATUS: Status Register

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0103	0	0	0	0	0	0	0	STATUS

[7:1] Unused **Unused** RO

Always read 7'b0

[0] STATUS **Status** RO

0: Device is not ready for conversion

1: Device is ready for conversion

Table 14. DATA_VOUT: Voltage Channel Output Data

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0200	VOUT_DATA_LSB							

[7:0] VOUT_DATA_LSB **Voltage output data least significant byte** RO

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0201	0	0	0	0	VOUT_DATA_MSB			

[7:4] Unused **Unused** RO

0000 (default)

[3:0] VOUT_DATA_MSB **Voltage output data most significant byte** RO

Table 15. DATA_COUT: Current Channel Output Data

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0202	COUT_DATA_LSB							

[7:0] COUT_DATA_LSB **Current output data least significant byte** RO

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0203	0	0	0	0	COUT_DATA_MSB			

[7:4] Unused **Unused** RO

0000 (default)

[3:0] COUT_DATA_MSB **Current output data most significant byte** RO

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP92064SD/NOPB	ACTIVE	WSON	NHR	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	L92064	Samples
LMP92064SDE/NOPB	ACTIVE	WSON	NHR	16	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	L92064	Samples
LMP92064SDX/NOPB	ACTIVE	WSON	NHR	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	L92064	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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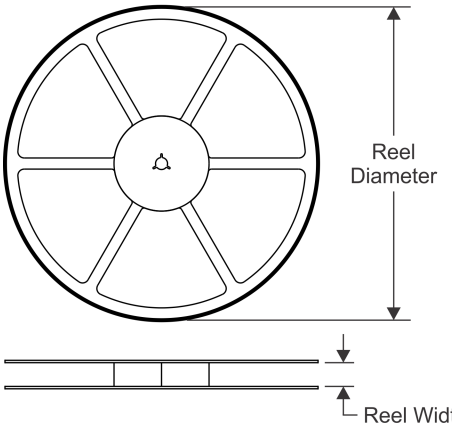
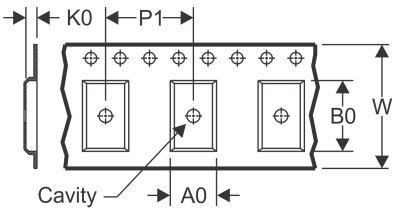
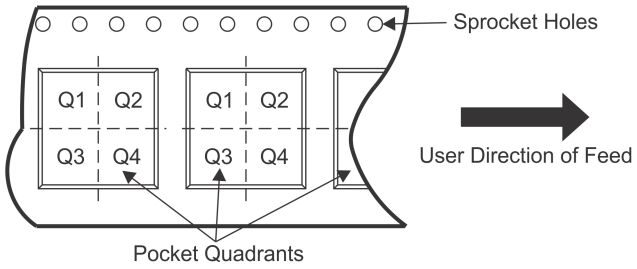


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

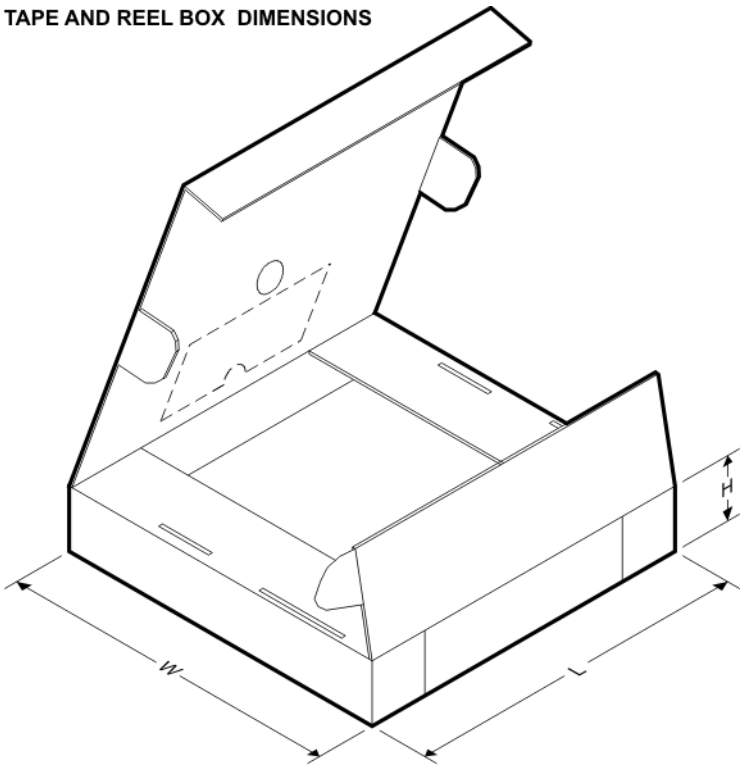
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP92064SD/NOPB	WSON	NHR	16	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LMP92064SDE/NOPB	WSON	NHR	16	250	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LMP92064SDX/NOPB	WSON	NHR	16	4500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

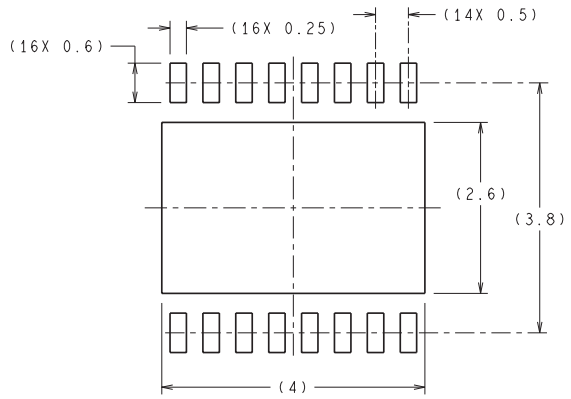
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP92064SD/NOPB	WSON	NHR	16	1000	213.0	191.0	55.0
LMP92064SDE/NOPB	WSON	NHR	16	250	213.0	191.0	55.0
LMP92064SDX/NOPB	WSON	NHR	16	4500	367.0	367.0	35.0

NHR0016B



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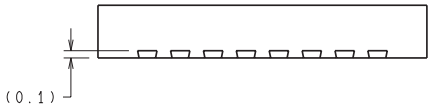
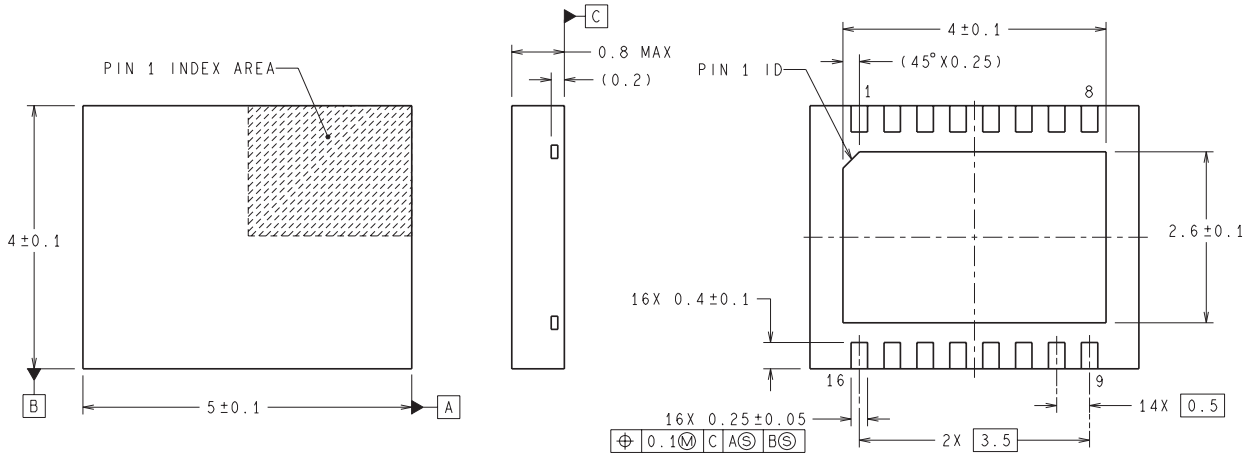
DIMENSIONS IN ( ) FOR REFERENCE ONLY





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