Xilinx® Virtex™ -5 LX50 Evaluation Kit

User Manual

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1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the Virtex-5 LX Evaluation Kit from Avnet Electronics Marketing. This document includes instructions for operating the board, descriptions of the hardware features and explanations of the test code programmed in the on-board PROM. For reference design documentation, see the PDF file included with the project files of the design.

1.1 Description

The Virtex-5 LX50 Evaluation Kit provides a complete hardware environment for designers to accelerate their time to market. The kit delivers a stable platform to develop and test designs targeted to the advanced Xilinx FPGA family. The installed Virtex-5 LX device offers a prototyping environment to effectively demonstrate the enhanced benefits of leading edge Xilinx FPGA solutions. Reference designs are included with the kit to exercise standard peripherals on the evaluation board for a quick start to device familiarization.

1.2 Board Features

FPGA
- Xilinx Virtex-5 XC5VLX50-FF676 FPGA

I/O Connectors
- Two EXP™ general-purpose I/O expansion connectors
- One 0.1" USB Debug Header
- One 50-pin 0.1" Header supports Avnet SystemACE Module (SAM)
- 80 pin LVDS connector supports 10-bit plus Frame and Clock TX and RX data.

Memory
- 64 MB DDR2 SDRAM
- 16 MB FLASH

Communication
- RS-232 serial port
- USB 2.0
- 10/100/1000 Ethernet

Power
- Regulated 3.3V, 2.5V, 1.8V, and 0.9V supply voltages derived from an external 5V supply
- SSTL2 Termination Regulator

Configuration
- XCF32P 32Mbit configuration PROM
- Xilinx Parallel Cable IV or Platform USB Cable support for JTAG Programming/Configuration

Display
- 2x16 character LCD display

1.3 Test Files

The configuration PROM on the Virtex-5 LX50 Evaluation Board comes programmed with test designs that can be used as base tests for the peripherals on the board. The test designs listed below are discussed in Section 3.0.

- USB/LCD Test
- Factory Test
- Ethernet Test

1.4 Reference Designs

Reference designs that demonstrate some of the potential applications of the Virtex-5 LX50 Evaluation board can be downloaded from the Avnet Design Resource Center (www.em.avnet.com/drc). The reference designs include all of the source code and project files necessary to implement the designs. See the PDF document included with each reference design for a complete description of the design and detailed instructions for running a demonstration on the Evaluation board. Check the DRC periodically for updates and new designs.

- V5LX50 Evaluation Boot Loader Example Design
- V5LX50 Evaluation Interrupt Example Design
- V5LX50 Evaluation Xilinx Micro Kernel (XMK) Example Design
- V5LX50 Evaluation lwIP Web Server Example Design
- V5LX50 Evaluation SystemACE Module Example Design

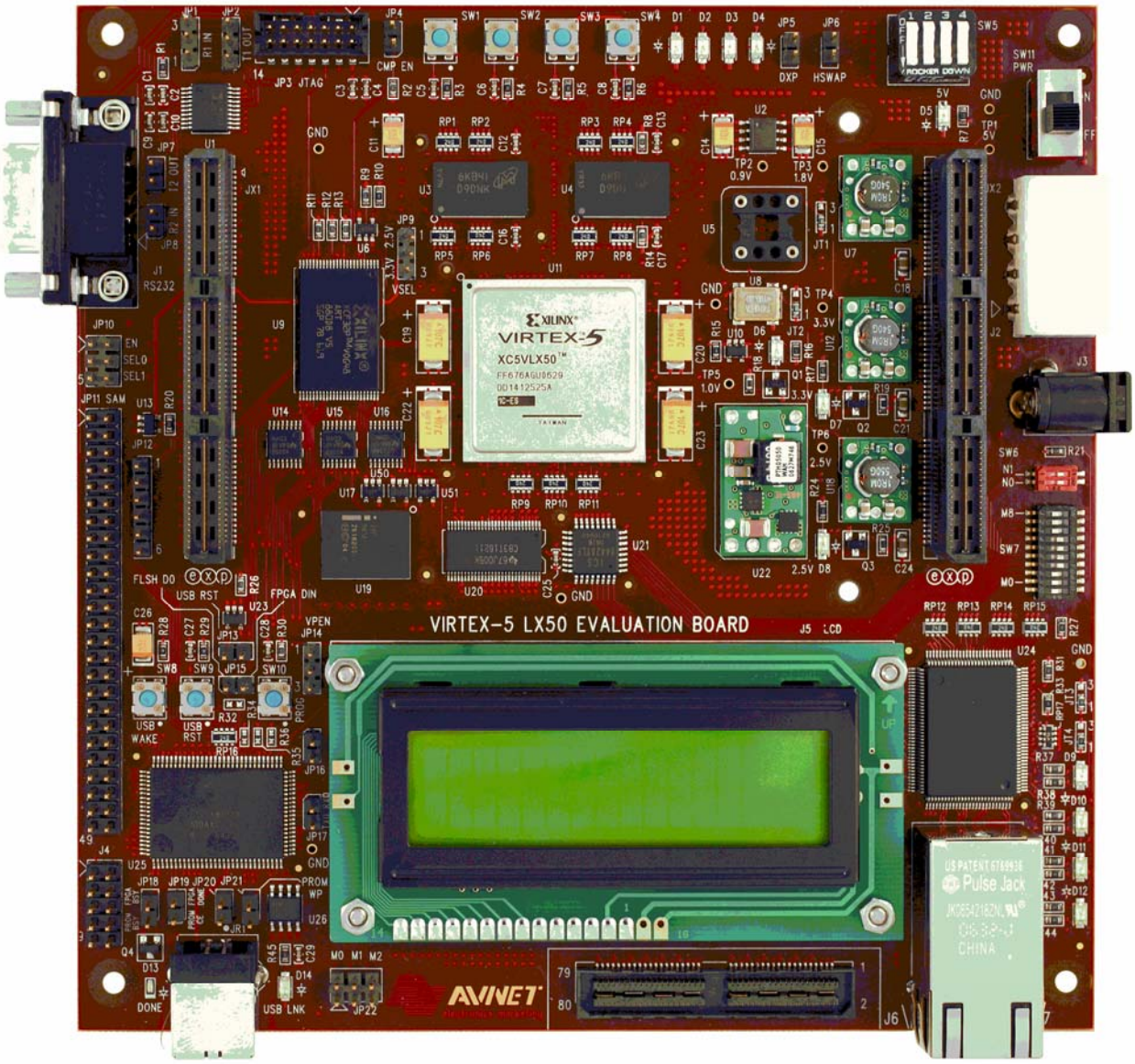


Figure 1 - Virtex-5 LX Evaluation Board Picture

1.5 Ordering Information

The following table lists the evaluation kit part numbers and available software options.
Internet link at http://www.em.avnet.com/drc

Part Number	Hardware
AES-XLX-V5LX-EVL50-G	Xilinx Virtex-5 LX50 Evaluation Kit populated with an XC5VLX50 -1 speed grade device

Table 1 - Ordering Information

2.0 Functional Description

A high-level block diagram of the Virtex-5 LX50 Evaluation board is shown below followed by a brief description of each sub-section.

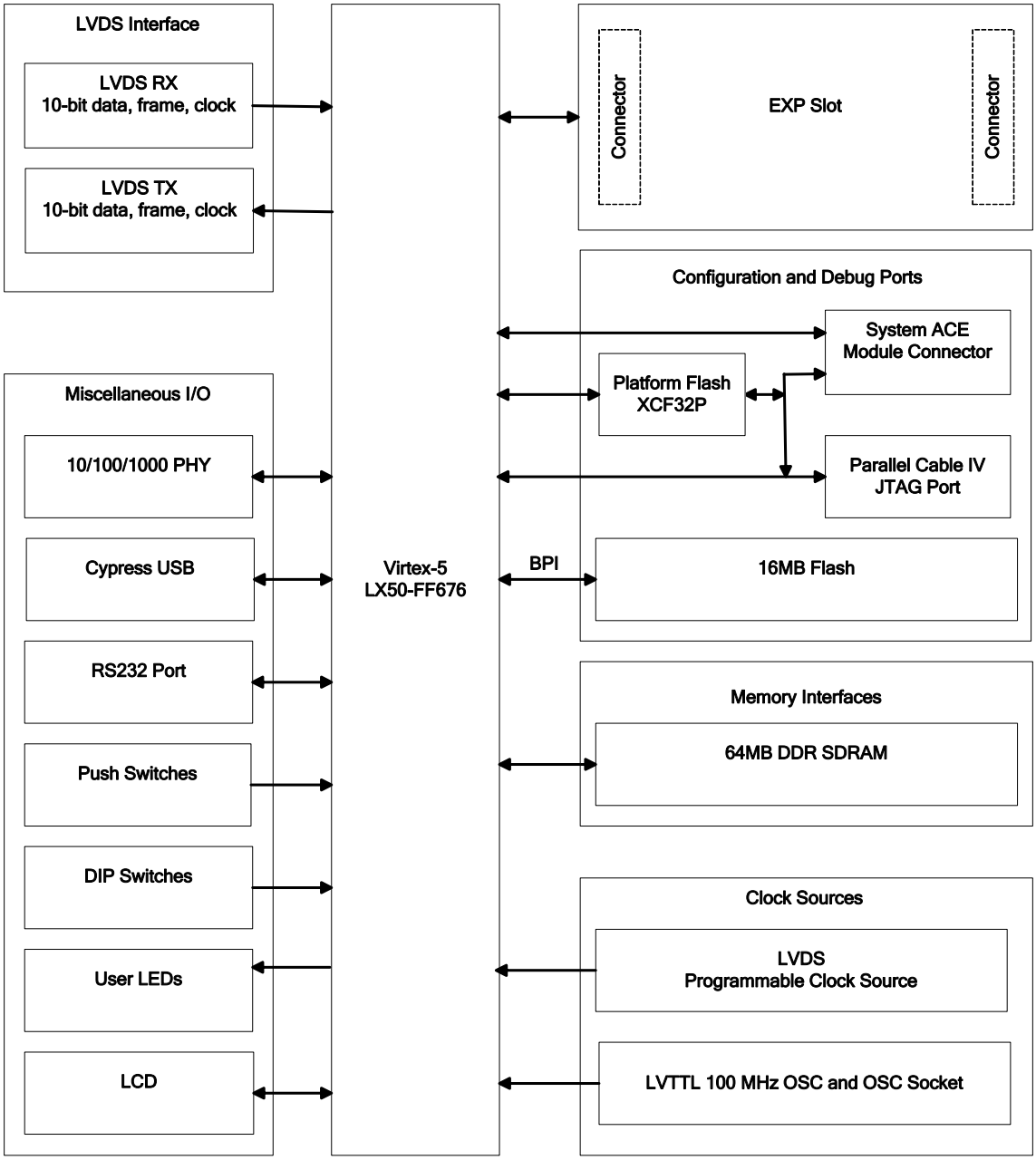


Figure 2 - Virtex-5 LX50 Evaluation Board Block Diagram

2.1 Xilinx Virtex-5 LX50 FPGA

The Virtex-5 LX50 FPGA feature 12 DCMs, 6 PLLs, and 1.25Gbps LVDS I/O. The following table shows some other main features of the FF676 package.

Device	Number of Slices	BlockRAM (Kb)	Xtreme DSP Slices	DSP48E Slices
XC5VLX50	7,200	1,728	128	48

Table 2 - 5VLX50 Features

Please refer to the Virtex-5 LX50 Data sheet for a complete detailed summary of all device features.

All of the 440 available I/O on the Virtex-5 LX50 device are used in the design.

Depending on the availability of production silicon, the Virtex-5 LX50 Evaluation board may use engineering sample devices (CES1 or later). Please see the device errata on the Xilinx web page (www.xilinx.com) for any potential limitations these devices may have.

2.2 LVDS Interface

The LVDS interface (J6 connector) is designed to support 10-bit TX and RX data transfers. 4 additional pairs are provided to be used as Frame and Clock if desired.

2.5V power is supplied through 8 pins of the LVDS connector.

The connector used for the LVDS interface is manufactured by Samtec, PN: QSE-040-01-F-D-A. See figure 3 for a picture of the connector.

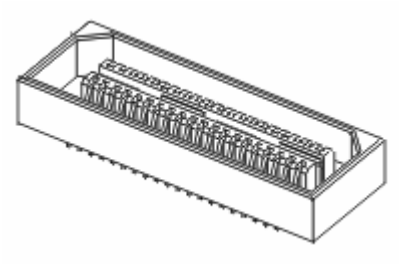


Figure 3 - LVDS connector – 80 pin

This connecter mates with a variety of other connector profiles. See the Samtec website (www.samtec.com) for details on mating connectors.

See Table 3, on the next page, for the LVDS pin assignments.

Signal Name	Virtex-5 Pin		Signal Name	Virtex-5 Pin
TX_CLK_P	R21		RX_CLK_P	AB24
TX_CLK_N	R20		RX_CLK_N	AC24
TX_FRAME_P	U19		RX_FRAME_P	AD24
TX_FRAME_N	U20		RX_FRAME_N	AD23
TX_DATA0_P	T20		RX_DATA0_P	AE26
TX_DATA0_N	T19		RX_DATA0_N	AD26
TX_DATA1_P	AA20		RX_DATA1_P	AC21
TX_DATA1_N	AA19		RX_DATA1_N	AB21
TX_DATA2_P	AD19		RX_DATA2_P	AE25
TX_DATA2_N	AC19		RX_DATA2_N	AD25
TX_DATA3_P	AB20		RX_DATA3_P	W24
TX_DATA3_N	AB19		RX_DATA3_N	W23
TX_DATA4_P	V19		RX_DATA4_P	AA23
TX_DATA4_N	W19		RX_DATA4_N	AA24
TX_DATA5_P	AF23		RX_DATA5_P	AB22
TX_DATA5_N	AE23		RX_DATA5_N	AA22
TX_DATA6_P	Y21		RX_DATA6_P	V24
TX_DATA6_N	Y20		RX_DATA6_N	V23
TX_DATA7_P	V21		RX_DATA7_P	V21
TX_DATA7_N	V22		RX_DATA7_N	V22
TX_DATA8_P	Y23		RX_DATA8_P	U22
TX_DATA8_N	Y22		RX_DATA8_N	U21
TX_DATA9_P	W21		RX_DATA9_P	T23
TX_DATA9_N	W20		RX_DATA9_N	T22

Table 3 - Virtex-5 LVDS Pin Assignments

2.3 Memory

The Virtex-5 LX Evaluation board is populated with both high-speed RAM and non-volatile Flash to support various types of applications. The board has 64 Megabytes (MB) of DDR2 SDRAM and 16 MB of Flash. The following figure shows a high-level block diagram of the memory interfaces on the Evaluation board. If additional memory is necessary for development, check the Avnet Design Resource Center (DRC) for the availability of EXP compliant daughter cards with expansion memory (sold separately). Here is the link to the DRC web page: www.em.avnet.com/drc.

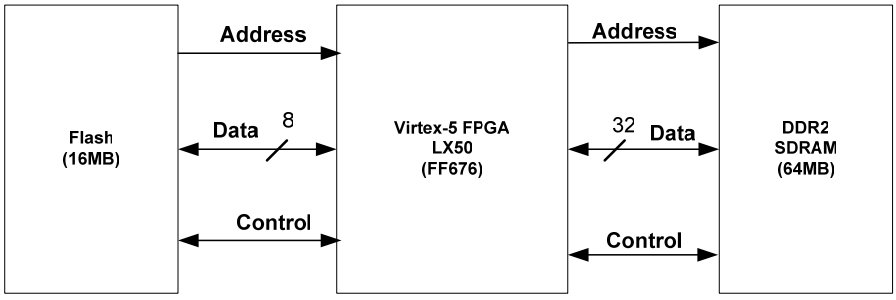


Figure 4 - Virtex-5 LX50 Evaluation Board Memory Interfaces

2.3.1 DDR2 SDRAM Interface

Two Micron DDR2 SDRAM devices, part number MT47H16M16BG-5E, make up the 32-bit data bus. Each device provides 32MB of memory on a single IC and is organized as 4 Megabits x 16 x 4 banks (256 Megabit). The device has an operating voltage of 1.8V and the interface is JEDEC Standard SSTL_2 (Class I for unidirectional signals, Class II for bidirectional signals). The -5E speed grade supports 5 ns cycle times with a 3 clock read latency (DDR2-400). DDR2 On-Die-Termination (ODT) is also supported. The following figure shows a high-level block diagram of the DDR SDRAM interface on the V5LX50 Evaluation board.

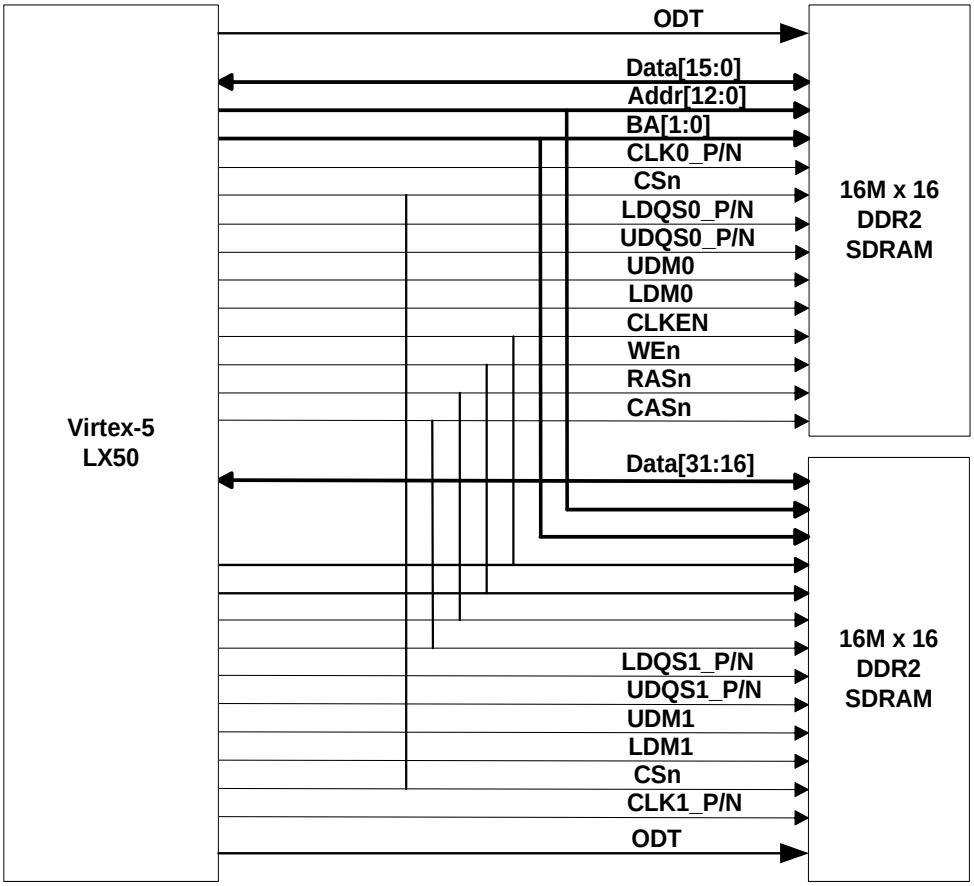


Figure 5 - DDR2 SDRAM Interface

The following table provides timing and other information about the Micron device necessary to implement a DDR2 memory controller.

MT47H16M16BG-5E: Timing Parameters	Time (ps) or Number
Load Mode Register time (TMRD)	25000
Write Recovery time (TWR)	15000
Write-to-Read Command Delay (TWTR)	1
Delay between ACT and PRE Commands (TRAS)	90000
Delay after ACT before another ACT (TRC)	65000
Delay after AUTOREFRESH Command (TRFC)	115000
Delay after ACT before READ/WRITE (TRCD)	25000
Delay after ACT before another row ACT (TRRD)	15000
Delay after PRECHARGE Command (TRP)	20000
Refresh Command Interval (TREFC)	115000
Avg. Refresh Period (TREFI)	7800000
Memory Data Width (DWIDTH) (x2 devices)	32
Row Address Width (AWIDTH)	13
Column Address Width (COL_AWIDTH)	9
Bank Address Width (BANK_AWIDTH)	2
Memory Range (64 MB total)	0x3FFFFFF

Table 4 - DDR2 SDRAM Timing Parameters

The following guidelines were used in the design of the DDR2 interface to the Virtex-4 FX FPGA. These guidelines are based on Micron recommendations and board level simulation.

- Dedicated bus with matched trace lengths (+/- 100 mils)
- Memory clocks routed differentially
- 50 ohm* controlled trace impedance
- Series termination on bidirectional signals at the memory device
- Parallel termination following the memory device connection on all signals
- 100 ohm* pull-up resistor to the termination supply on each branch of shared signals (control, address)
- Termination supply that can both source and sink current
- Feedback clock routed with twice the length to simulate the total flight time

* Ideal impedance values. Actual may vary.

Some of the design considerations were specific to the Virtex-4 architecture. For example, the data strobe signals (DQS) were placed on Clock Capable I/O pins in order to support data capture techniques utilizing the SERDES function of the Virtex-5 I/O blocks. The appropriate DDR2 memory signals were placed in the clock regions that correspond to these particular Clock Capable I/O pins.

The DDR2 signals are connected to I/O Banks 15 and 16 of the Virtex-5 LX FPGA. The output supply pins (VCCO) for Banks 15 and 16 are connected to 1.8 Volts. This supply rail can be measured at test point TP3, which can be found in the area between the power modules and the can clock oscillator socket labeled “U5”. The reference voltage pins (VREF) for Banks 15 and 16 are connected to the reference output of the National LP2997 DDR2 Termination Linear Regulator. This rail provides the voltage reference necessary for the SSTL_2 I/O standard. The LP2997 regulator also provides the termination supply rail. The termination voltage is 0.9 Volts and can be measured at test point TP2, which can be found just above the can clock oscillator socket labeled “U5”.

The following table contains the FPGA pin numbers for the DDR2 SDRAM interface.

Signal Name	Virtex-4 pin		Signal Name	Virtex-4 pin
DDR_A0	B11		DDR_D0	B24
DDR_A1	A14		DDR_D1	D24
DDR_A2	C11		DDR_D2	B25
DDR_A3	A12		DDR_D3	C24
DDR_A4	C12		DDR_D4	C23
DDR_A5	B12		DDR_D5	A25
DDR_A6	B16		DDR_D6	D23
DDR_A7	C14		DDR_D7	A23
DDR_A8	B15		DDR_D8	C21
DDR_A9	B14		DDR_D9	B19
DDR_A10	A13		DDR_D10	D21
DDR_A11	A15		DDR_D11	C18
DDR_A12	C16		DDR_D12	D18
			DDR_D13	C22
			DDR_D14	D20
DDR_BA0	C13		DDR_D15	B21
DDR_BA1	D16			
			DDR_D16	B5
DDR_CS#	D10		DDR_D17	D5
ODT	C9		DDR_D18	A5
			DDR_D19	C6
DDR_WE#	B17		DDR_D20	C7
DDR_RAS#	A10		DDR_D21	B6
DDR_CAS#	D11		DDR_D22	D6
DDR_CLKEN	A17		DDR_D23	A4
DDR_LDM0	A22		DDR_D24	A3
DDR_UDM0	A23		DDR_D25	C2
DDR_LDM1	A8		DDR_D26	C1
DDR_UDM1	A9		DDR_D27	D1
			DDR_D28	C1
DDR_LDQS0 P,N	A20, B20		DDR_D29	C4
DDR_UDQS0 P,N	C19, D19		DDR_D30	C3
DDR_LDQS1 P,N	D8, C8		DDR_D31	A2
DDR_UDQS1 P,N	B7, A7			
			DDR_CLK_FB_O	D3
			DDR_CLK_FB_I	AD18

Table 5 - Virtex-5 DDR2 FPGA Pinouts

2.4 Clock Sources

The Virtex-5 LX Evaluation board includes all of the necessary clocks on the board to implement designs as well as providing the flexibility for the user to supply their own application specific clocks. The clock sources described in this section are used to derive the required clocks for the memory and communications devices, and the general system clocks for the logic design. This section also provides information on how to supply external user clocks to the FPGA via the on-board connectors and oscillator socket.

The following figure shows the clock nets connected to the I/O banks containing the global clock input pins on the Virtex-5 LX50 FPGA. Fifteen out of the twenty global clock inputs of the Virtex-5 FPGA are utilized on the board as clock resources. The other global clock inputs are used for user I/O. It should be noted that single-ended clock inputs must be connected to the P-side of the pin pair because a direct connection to the global clock tree only exists on this pin. The I/O voltages (VCCO) for Bank 3 are jumper selectable to either 2.5V or 3.3V. Bank 4 is fixed at 2.5V due the non-clock I/O that is connected to it being fixed at 2.5V. In order to use the differential clock inputs as LVDS inputs, the VCCO voltage for the corresponding bank must be set for 2.5V since the Virtex-5 FPGA does not support 3.3V differential signaling. Single-ended clock inputs do not have this restriction and may be either 2.5V or 3.3V. The interface clocks coming from 3.3V devices on the board are level-shifted to the appropriate VCCO voltage by CB3T standard logic devices prior to the Virtex-5 input pins.

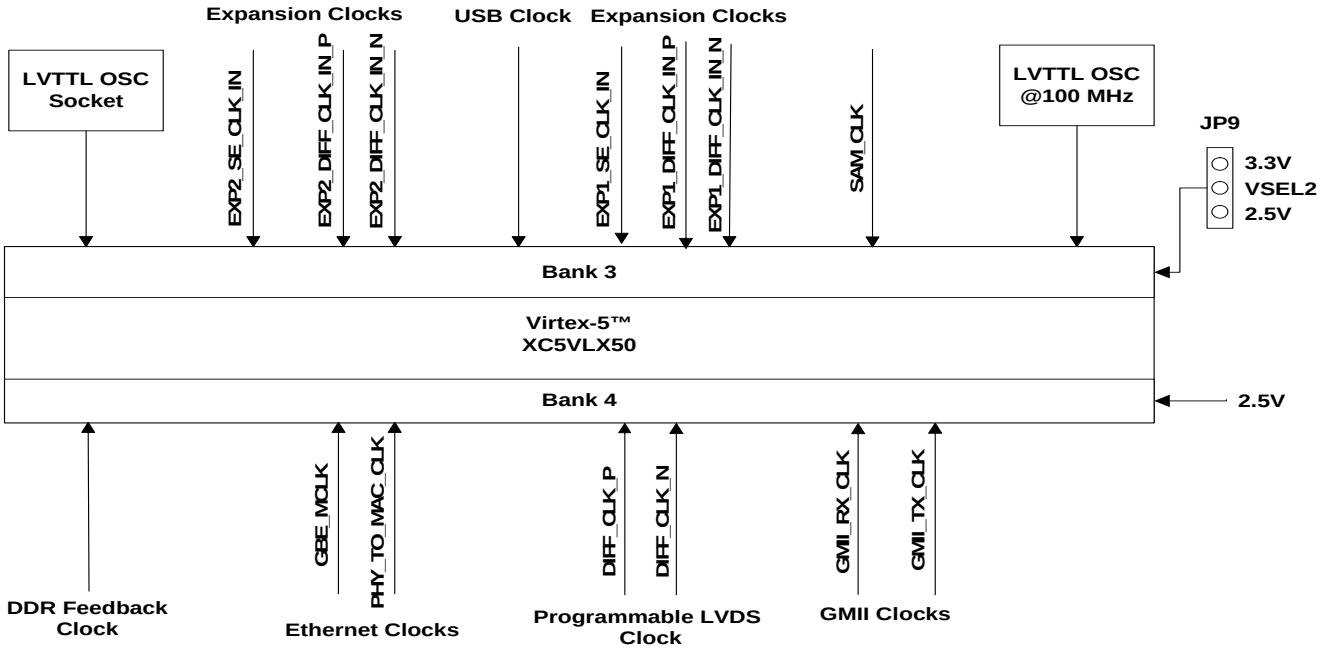


Figure 6 - Clock Nets Connected to Global Clock Inputs

The on-board 100MHz oscillator provides the system clock input to the global clock tree. This single-ended, 100MHz clock can be used in conjunction with the Virtex-5 LX Digital Clock Managers (DCMs) to generate the various processor clocks and the clocks forwarded to the DDR SDRAM devices. The interface clocks supplied by the communications devices are derived from dedicated crystal oscillators.

Reference#	Frequency	Derived Interface Clock	Derived Frequency	Virtex-4 pin#
U8	100 MHz	CLK_100MHZ	100 MHz	E18
Y3	24 MHz	USB_IFCLK	30, 48 MHz	E10
Y1	25 MHz	CLK_SYNTH0_P/N	25 – 700 MHz	AB10, AB9
Y1	25 MHz	CLK_SYNTH1_P/N	25 – 700 MHz	AC23, AC22
Y2	25 MHz	GMII_RX_CLK	2.5, 25 MHz	AC8
		GMII_TX_CLK		AC17
		GBE_MCLK	125 MHz	AD8

Table 6 - On-Board Clock Sources

In addition to the 100MHz oscillator, an 8-pin DIP clock socket is provided on the board so the user can supply their own oscillator of choice. The socket is a single-ended, LVTTL or LVCMOS compatible clock input to the FPGA that can be used as an alternate source for the system clock.

Signal Name	Socket pin#
Enable	1
GND	4
Output	5
VDD	8

Table 7 - Clock Socket "U5" Pin-out

Net Name	Input Type	Connector.pin#	Virtex-4 pin#
CLK_SOCKET	Global clock	U16.5	E16

Table 8 - User Clock Input

2.4.1 ICS8442 Programmable LVDS Clock Synthesizer

The Virtex-4 FX PCI Express Evaluation board design uses the ICS8442 LVDS frequency synthesizer for generating various clock frequencies. A list of features included in the ICS8442 device is shown below.

- Output frequency range: 25MHz to 700MHz
- RMS period jitter: 2.7ps (typical)
- Cycle-to-cycle jitter: 27ps (typical)
- Output rise and fall time: 650ps (maximum)
- Output duty cycle: 48/52

The following figure shows a high-level block diagram of the ICS8442 programmable LVDS clock synthesizer.

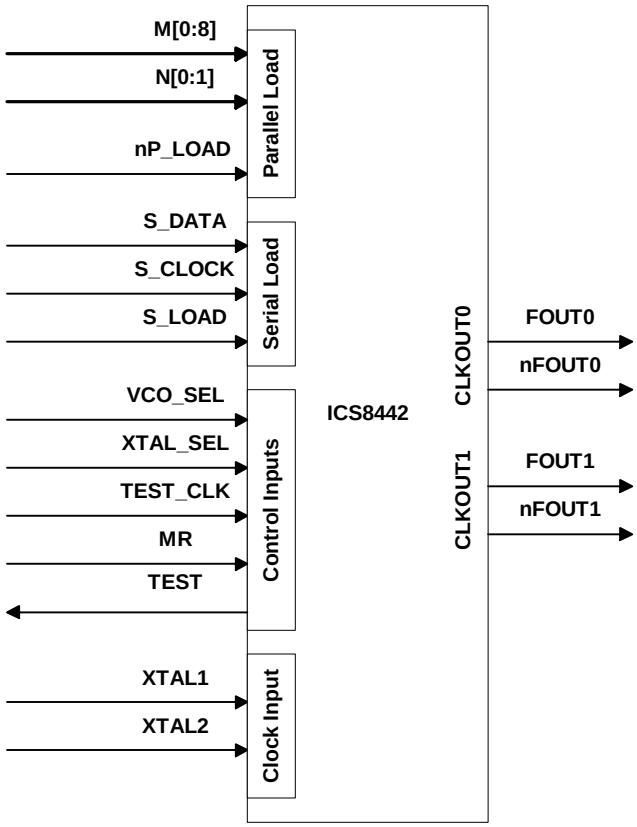


Figure 7 - ICS8442 Clock Synthesizer

Signal Name	Direction	Pull up/Pull down	Description
M[0:4], M[6:8]	Input	Pull down	The M divider inputs, latched on the rising edge of the nP_LOAD signal.
M[5]	Input	Pull up	
N[0:1]	Input	Pull down	The N divider inputs, latched on the rising edge of the nP_LOAD signal.
TEST	Output		The TEST output is active during the serial mode of operations. Please refer to the datasheet for more information.
MR	Input	Pull down	Active high reset signal.
S_CLOCK	Input	Pull down	Serial interface clock input. Data is shifted into the device on the rising edge of this clock.
S_DATA	Input	Pull down	Serial interface data input.
S_LOAD	Input	Pull down	Serial interface load signal. The contents of the serial data shift register is loaded into the internal dividers on the rising edge of this signal.
TEST_CLK	Input	Pull down	Test clock input.
nP_LOAD	Input	Pull down	The rising edge of this signal is used to load the M and N divider inputs into the device.
XTAL1, XTAL2	Input		Crystal clock input/output
XTAL_SEL	Input	Pull up	This signal is used to select between the crystal and the TEST_CLK input to the device. When this high, crystal is selected.
VCO_SEL	Input	Pull up	This signal is used to place the internal PLL in the bypass mode. When this signal is set to low, the PLL is placed in the bypass mode. For normal operations, this signal must be set to high.
FOUT0, FOUT1	Output		Positive LVDS clock outputs
nFOUT0, nFOUT1	Output		Negative LVDS clock outputs

Table 9 - ICS8442 Clock Synthesizer Pin Description

The Input Clock Select signals of the ICS8442, “VCO_SEL” and “XTAL_SEL”, are not used on the Virtex-5 LX Evaluation board. The internal pull-ups of these pins put the ICS8842 in normal operation mode where the 25MHz crystal is used as the reference clock to generate the output clocks. None of the serial input control signals are connected on the board. Programming the ICS8442 device is only possible using the M/N DIP switches on the board.

2.4.1.1 ICS8442 Clock Generation

The ICS8442 output clocks are generated based on the following formula (assuming the crystal clock input is set to 25MHz):

FOUT[0:1] = 25 x M/N

Where 8 < M < 28 and N can take a value of 1, 2, 4, or 8. The variable M is determined by setting the binary number M[0:8] while N is set according to the following table:

N[1:0]	N	Output Clock Frequency Range (MHz)	
		Minimum	Maximum
00	1	200	700
01	2	100	350
10	4	50	175
11	8	25	87.5

Table 10 - ICS8442 N Settings

For example, to generate a 62.5MHz clock, N[1:0] will be set to “10” (it can also be set to “11” since either one will be the correct frequency range for the 62.5MHz clock) and M will be set to “000001010” (decimal 10). So, from the above formula:

FOUT[0:1] = 25 x 10/4 = 62.5Mhz

The following table shows how the M and N values can be set to generate a clock source for a few common applications. All the values for M and N are based on the 25MHz crystal clock input to the ICS8442 device. A complete list of frequencies generated by the ICS8442 (based on a 25MHz input clock) is provided in the following sections.

Interconnect Technology	FOUT0 and FOUT1 (MHz)	ICS8442 M and N Settings										
		M8	M7	M6	M5	M4	M3	M2	M1	M0	N1	N0
Gigabit Ethernet	125	0	0	0	0	0	1	0	1	0	0	1

Table 11 - Example of the ICS8442 M and N Settings

2.4.1.2 ICS8442 Programming Mode

The Virtex-5 LX Evaluation board allows programming of the M and N values in parallel mode. In parallel mode, M and N values are programmed into the device when the nP_LOAD signal pulses low. Please refer to the ICS8442 datasheet for more information on programming modes of loading the M and N values into the device.

2.4.1.3 ICS8442 M and N Settings

The following figure shows how the ICS8442 programmable LVDS clock synthesizer is used on the Virtex-5 LX Evaluation board. To limit the number of required Virtex-5 I/O pins, only Parallel Mode is supported. DIP switches are provided on the board for the manual setting of the M and N values for the ICS8442.

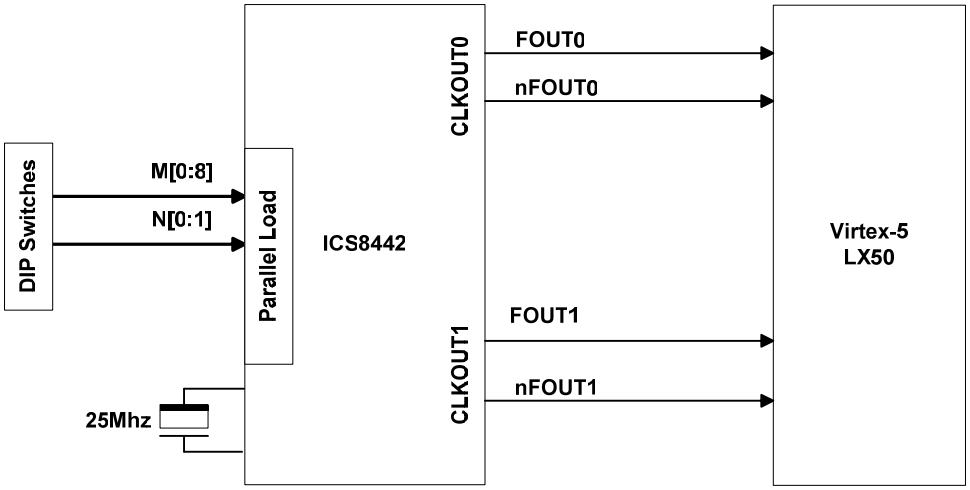


Figure 8 - ICS8442 Clock Synthesizer Interface to the FPGA

As shown in the above figure, the ICS8442 device outputs two identical LVDS clock sources. One of these clock sources (CLKOUT0) is routed to a global clock pin on Bank 4 of the Virtex-5. The other is routed to Bank 17 and is connected to a clock capable pin. These types of clock pins are not global, but "regional". Unlike global clocks, the span of a regional clock signal is limited to three clock regions. These networks are especially useful for source-synchronous interface designs. The Virtex-5 I/O banks are the same size as a clock region. Refer to the Virtex-5 User Guide for a detailed explanation of how regional clocking works and how it is implemented.

The following tables show the DIP switch settings for M and N selections. Please refer to Table 9 for the information on pull-up and pull-down resistors provided internal to the ICS8442 device for the M and N input signals.

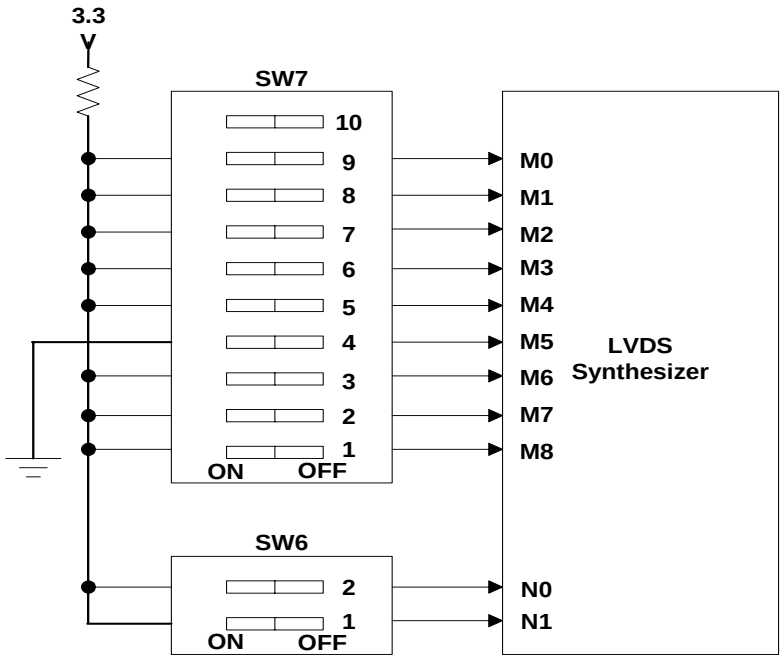


Figure 9 - M and N DIP Switches for the LVDS Synthesizer

SW7 and SW9	M[8:0]	Switch Position	
		OFF	ON
DIP1	M8	0	1
DIP2	M7	0	1
DIP3	M6	0	1
DIP4	M5	1	0 Note (1)
DIP5	M4	0	1
DIP6	M3	0	1
DIP7	M2	0	1
DIP8	M1	0	1
DIP9	M0	0	1
DIP10	Unused	NA	NA

Table 12 - DIP Switch Setting for M[8:0]

Note(1) – The polarity of M5 (DIP4) is the opposite of all other DIP switch positions.

SW8 and SW10	N[1:0]	Switch Position	
		OFF	ON
DIP1	N1	0	1
DIP2	N0	0	1

Table 13 - DIP Switch Setting for N[1:0]

The following table shows a complete list of frequencies generated by the ICS8442 device based on a 25MHz crystal reference clock input.

M[8:0]	N[1:0]	FOUT[1:0] (MHz)	M[8:0]	N[1:0]	FOUT[1:0] (MHz)
000001000	11	25 (Min)	000011000	10	150
000001001	11	28.125	000011001	10	156.25
000001010	11	31.25	000001101	01	162.5
000001011	11	34.375	000011010	10	162.5
000001100	11	37.5	000011011	10	168.75
000001101	11	40.625	000001110	01	175
000001110	11	43.75	000011100	10	175
000001111	11	46.875	000001111	01	187.5
000001000	10	50	000001000	00	200
000010000	11	50	000010000	01	200
000010001	11	53.125	000010001	01	212.5
000001001	10	56.25	000001001	00	225
000010010	11	56.25	000010010	01	225
000010011	11	59.375	000010011	01	237.5
000001010	10	62.5	000001010	00	250
000010100	11	62.5	000010100	01	250
000010101	11	65.625	000010101	01	262.5
000001011	10	68.75	000001011	00	275
000010110	11	68.75	000010110	01	275
000010111	11	71.875	000010111	01	287.5
000001100	10	75	000001100	00	300
000011000	11	75	000011000	01	300
000011001	11	78.125	000011001	01	312.5
000001101	10	81.25	000001101	00	325
000011010	11	81.25	000011010	01	325
000011011	11	84.375	000011011	01	337.5
000001110	10	87.5	000001110	00	350
000011100	11	87.5	000011100	01	350
000001111	10	93.75	000001111	00	375
000001000	01	100	000010000	00	400
000010000	10	100	000010001	00	425
000010001	10	106.25	000010010	00	450
000001001	01	112.5	000010011	00	475
000010010	10	112.5	000010100	00	500
000010011	10	118.75	000010101	00	525
000001010	01	125	000010110	00	550
000010100	10	125	000010111	00	575
000010101	10	131.25	000011000	00	600
000001011	01	137.5	000011001	00	625
000010110	10	137.5	000011010	00	650
000010111	10	143.75	000011011	00	675
000001100	01	150	000011100	00	700 (Max)

Table 14 - Synthesizer Clock Outputs for M and N Values

The following table shows the Virtex-5 pin connections for the two differential clock outputs of the synthesizer.

Net Name	I/O Type	Virtex-5 pin
DIFF_CLK_0_P	FPGA input	AB10
DIFF_CLK_0_N		AB9
DIFF_CLK_1_P	FPGA input	AC23
DIFF_CLK_1_N		AC22

Table 15 - ICS8442 Pin Assignments

2.5 Communication

The Virtex-5 LX FPGA has access to Ethernet, USB and RS232 physical layer transceivers for communication purposes. Network access is provided by a 10/100/1000 Mb/s Ethernet PHY, which is connected to the Virtex-5 via a standard GMII interface. The PHY connects to the outside world with a standard RJ45 connector (J7) and is located in the lower right corner of the board. General-purpose I/O transfers are supported by way of the USB 2.0 port. The USB Type B peripheral connector (JR1) is mounted on the board in the lower left corner of the board. Serial port communication to the embedded processor or FPGA fabric is provided through a dual-channel RS232 transceiver.

2.5.1 10/100/1000 Ethernet PHY

The PHY is a National DP83865DVH Gig PHYTER® V. The DP83865 is a low power version of National's Gig PHYTER V with a 1.8V core voltage and 2.5V I/O voltage. The PHY also supports 3.3V I/O, but the 2.5V option is used on the board. The PHY is connected to a Tyco RJ-45 jack with integrated magnetics (part number: 1-6605833-1). The jack also integrates two LEDs and their corresponding resistors as well as several other passive components. External logic is used to logically OR the three link indicators for 10, 100 and 1000 Mb/s to drive a Link LED on the RJ-45 jack. The external logic is for the default strap options and may not work if the strap options are changed. Four more LEDs are provided on the board for status indication. These LEDs indicate Link at 10 Mb/s, Link at 100 Mb/s, link at 1000 Mb/s and Full Duplex operation. The PHY clock is generated from its own 25 MHz crystal. The following figure shows a high-level block diagram of the interface to the DP83865 Tri-mode Ethernet PHY.

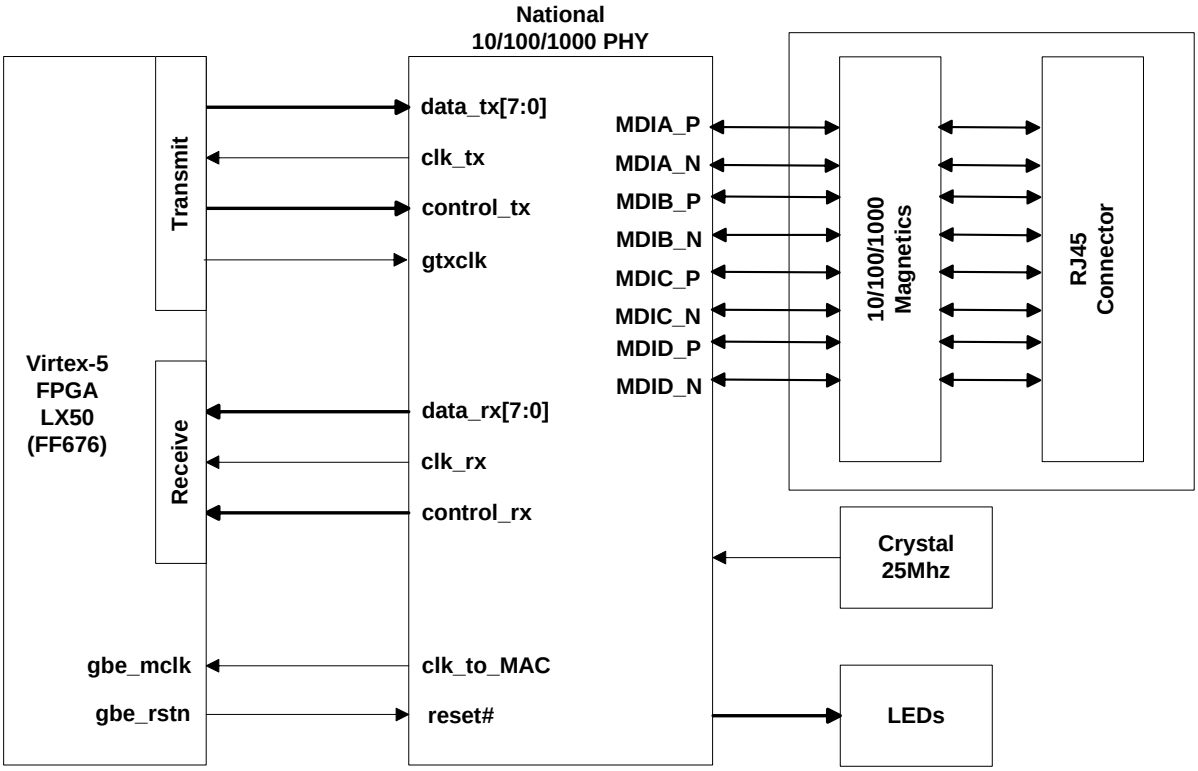


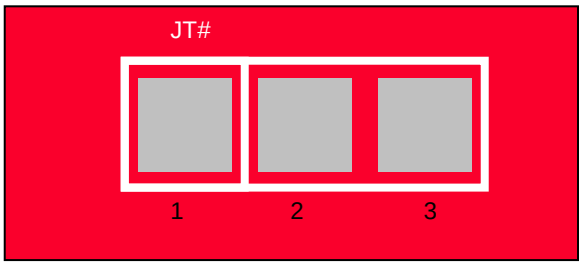
Figure 10 - 10/100/1000 Mb/s Ethernet Interface

The PHY address is set to 0b00001 by default. PHY address 0b00000 is reserved for a test mode and should not be used. Three-pad resistor jumpers are used to set the strapping options. These jumper pads provide the user with the ability to change the settings by moving the resistors. The strapping options are shown in the following table. The dual-function pins that are used for both a strapping option and to drive an LED, have a set of two jumpers per pin. The dual-function pins are indicated by an asterisk in the table.

Function	Jumper Installation	Resistor	Mode Enabled
Auto-Negotiation*	JT13: pins 1-2 JT14: pins 1-2	0 ohm 0 ohm	Auto-negotiation enabled (default)
	JT13: pins 2-3 JT14: pins 2-3	0 ohm 0 ohm	Auto-negotiation disabled
Full/Half Duplex*	JT15: pins 1-2 JT16: pins 1-2	0 ohm 0 ohm	Full Duplex (default)
	JT15: pins 2-3 JT16: pins 2-3	0 ohm 0 ohm	Half Duplex
Speed 1*	JT17: pins 1-2 JT18: pins 1-2 (Speed1 – 0)	0 ohm 0 ohm	Speed Selection: (Auto-Neg enabled) Speed1 Speed0 Speed Advertised 1 1 1000BASE-T, 10BASE-T 1 0 1000BASE-T 0 1 1000BASE-T, 100BASE-TX 0 0 1000BASE-T, 100BASE-TX, 10BASE-T Default: 1000BASE-T, 100BASE-TX, 10BASE-T
Speed 0*	JT11: pins 1-2 JT12: pins 1-2 (Speed0 – 0)	0 ohm 0 ohm	
PHY address 0*	JT9: pins 1-2 JT10: pins 1-2	0 ohm 0 ohm	PHY Address 0b00001 (default)
	JT9: pins 2-3 JT10: pins 2-3	0 ohm 0 ohm	PHY Address 0b00000
Non-IEEE Compliant Mode	JT3: pins 1-2	1 K	Compliant and Non-comp. Operation (default)
	JT3: pins 2-3	1 K	Inhibits Non-compliant operation
Manual MDIX Setting	JT4: pins 1-2	1 K	Straight Mode (default)
	JT4 pins 2-3	1 K	Cross-over Mode
Auto MDIX Enable	JT7: pins 1-2	1 K	Automatic Pair Swap – MDIX (default)
	JT7: pins 2-3	1 K	Set to manual preset – Manual MDIX Setting (JT12)
Multiple Node Enable	JT6: pins 1-2	1 K	Single node – NIC (default)
	JT6: pins 2-3	1 K	Multiple node priority – switch/hub
Clock to MAC Enable	JT8: pins 1-2	1 K	CLK_TO_MAC output enabled (default)
	JT8: pins 2-3	1 K	CLK_TO_MAC output disabled

Table 16 - Ethernet PHY Hardware Strapping Options

The default options as indicated in Table 23 are Auto-Negotiation enabled, Full Duplex mode, Speed advertised as 10/100/1000 Mb/s, PHY address 0b00001, IEEE Compliant and Non-compliant support, straight cable in non-MDIX mode, auto-MDIX mode enabled, Single node (NIC) and CLK_TO_MAC enabled. The pin-out for a jumper pad is shown below.



The auto-MDIX mode provides automatic swapping of the differential pairs. This allows the PHY to work with either a straight-through cable or crossover cable. Use a CAT-5e or CAT-6 Ethernet cable when operating at 1000 Mb/s (Gigabit Ethernet). The boundary-scan Test Access Port (TAP) controller of the DP83865 must be in reset for normal operation. This active low reset pin of the TAP (TRST) is pulled low through a 1K resistor on the board. The following table provides the Virtex-5 pin assignments for the Ethernet PHY interface.

Net Name	Virtex-5 pin		Net Name	Virtex-5 pin
GBE_MDC	AE7		GBE_INT#	AF8
GBE_MDIO	AF7		GBE_RST#	AC14
GBE_MCLK	AD15		GMII_CRS	AE13
GMII_GTC_CLK	AD8		GMII_COL	AC13
GMII_TXD0	AD16		GMII_RXD0	AE8
GMII_TXD1	AE16		GMII_RXD1	AF9
GMII_TXD2	AE15		GMII_RXD2	AD9
GMII_TXD3	AF15		GMII_RXD3	AF10
GMII_TXD4	AF13		GMII_RXD4	AE10
GMII_TXD5	AF14		GMII_RXD5	AE11
GMII_TXD6	AD13		GMII_RXD6	AC11
GMII_TXD7	AC7		GMII_RXD7	AF12
GMII_TX_EN	AF17		GMII_RX_DV	AE12
GMII_TX_ER	AE17		GMII_RX_ER	AB12
GMII_TX_CLK	AC17		GMII_RX_CLK	AC8

Table 17 - Ethernet PHY Pin Assignments

2.5.1.1 Universal Serial Bus (USB)

The Virtex-5 LX Evaluation Board includes a Cypress EZ-USB FX2™ USB Microcontroller, part number CY7C68013A-100AC. The EZ-USB FX2 device is a single-chip integrated USB 2.0 transceiver, Serial Interface Engine (SIE) and 8051 microcontroller. This device supports full-speed (12 Mbps) and high-speed (480 Mbps) modes, but does not support low-speed mode (1.5 Mbps). The FX2 interface to the Virtex-5 FPGA is a programmable state machine that supports 8- or 16-bit parallel data transfers. This interface is called the General Programmable Interface (GPIF). The GPIF is controlled by Waveform Descriptors that are created with the Cypress "GPIFTool" utility and downloaded to the FX2 over the USB cable. The GPIF descriptors are stored in internal RAM and are loaded by the firmware during initialization. The GPIF interface is made up of the signals in the following table, which are connected to Virtex-5 FPGA. The USB FX2 device can also be used in a slave mode where the FPGA accesses the FX2 like a FIFO. For more information about the FX2 modes of operation, see the "EZ-USB FX2 Technical Reference Manual" and the FX2 datasheet available on Cypress Semiconductor's web site (http://www.cypress.com).

Some of the additional GPIF pins are connected to the SelectMAP configuration port on the Virtex-5 FPGA. Avnet has designed a Windows utility program that can utilize this connection to the SelectMAP port to update the FPGA configuration over the USB port. The additional pins used for the SelectMAP interface are shaded in the table. The Virtex-5 LX Evaluation board should be used with version 3.3 or later of the "ADS USB Utility". This program can be downloaded from the Design Resource Center (www.em.avnet.com/drc). To use the USB Utility to configure the Virtex-5 LX50 device, remove all three of the jumpers on JP22 (Mode jumpers). Then place a jumper on JP16 "FPGA_CFG_OE" . The USB Utility only supports bit files generated with CCLK as the start-up clock.

It is important to note that the lower 8 bits of the USB data bus tied to the SelectMap data port of the Virtex-5 FPGA are shared with the on-board FLASH. The data is controlled via two 4-bit muxes. The OE of the muxes is controlled by some external decode logic (U16, U17, U50, and U51). The decode logic detects when the proper configuration mode for USB is selected and enables the mux's outputs. The USB device drives the mode pins during USB configuration, so it is important to remove all mode jumper pins if configuring the Virtex-5 FPGA via the USB utility. JP16 ("FPGA_CFG_OE") enables the switch on the muxes to allow USB data to pass to the Virtex-5 FPGA. This jumper must be installed to allow FPGA configuration via USB.

FX2 Signal	Net Name	Virtex-5 pin	Description
CTL[0]	USB_CTL0	AF18	Control output or Slave-FIFO Flag A (Level#)
CTL[1]	USB_CTL1	AC9	Control output or Slave-FIFO Flag B (Full#)
CTL[2]	USB_CTL2	AC16	Control output or Slave-FIFO Flag C (Empty#)
CTL[3]	CTL3_PROG#	-	Output enable for FPGA_PROG# driver
CTL[4]	CTL4_CS#	-	SelectMAP chip select when JP13 installed
CTL[5]	CTL5_RDWR#	-	SelectMAP write enable when JP13 installed
RDY[0]	USB_RDY0	AF19	Sample-able ready inputs
RDY[1]	USB_RDY1	AC18	
RDY[2]	FPGA_BUSY	-	SelectMAP port busy indication
RDY[3]	FPGA_DONE	-	FPGA configuration DONE pin
RDY[4]	FPGA_INIT#	-	FPGA initialization pin
FD[0]	USB_FD0 (D0)	-	Bidirectional FIFO data bus (also SMAP data) ********************IMPORTANT!!!******************** **These Data pins are muxed through U14 and U15. All Mode jumpers (JP22) must be removed and JP16 installed to allow data to pass through to the FPGA. This is true for both configuration and normal operation.**
FD[1]	USB_FD1 (D1)	-	
FD[2]	USB_FD2 (D2)	-	
FD[3]	USB_FD3 (D3)	-	
FD[4]	USB_FD4 (D4)	-	
FD[5]	USB_FD5 (D5)	-	
FD[6]	USB_FD6 (D6)	-	
FD[7]	USB_FD7 (D7)	-	
FD[8]	USB_FD8	AE22	Bidirectional FIFO data bus
FD[9]	USB_FD9	AD21	
FD[10]	USB_FD10	AF22	
FD[11]	USB_FD11	AD20	
FD[12]	USB_FD12	AE21	
FD[13]	USB_FD13	AE20	
FD[14]	USB_FD14	AF20	
FD[15]	USB_FD15	AE18	
GPIFADR[0]	USB_PC0	-	Optional FPGA_CCLK out – see JT6 selection
GPIFADR[1]	FPGA_M2	-	SelectMAP port mode - M2
GPIFADR[2]	FPGA_M1	-	SelectMAP port mode - M1
GPIFADR[3]	FPGA_M0	-	SelectMAP port mode - M0
GPIFADR[4]	JTAG_TDI	-	Optional JTAG interface – TDI (install RP1)
GPIFADR[5]	JTAG_TDO	-	Optional JTAG interface – TDO (install RP1)
GPIFADR[6]	JTAG_TMS	-	Optional JTAG interface – TMS (install RP1)
GPIFADR[7]	JTAG_TCK	-	Optional JTAG interface – TCK (install RP1)
IFCLK	USB_IFCLK	E10	Interface clock, optional FPGA_CCLK (JT6)
PA0/INT0#	USB_INT0#	AD11	Port A I/O or active-low interrupt 0
PA1/INT1#	USB_INT1#	AD10	Port A I/O or active-low interrupt 1
PA2/SLOE	USB_SLOE	Y8	Port A I/O or slave-FIFO output enable
PA3/WU2	USB_WU2	AB16	Port A I/O or alternate wake-up pin
PA4/FIFOADR0	USB_FA0	AA18	Port A I/O or slave-FIFO address select 0
PA5/FIFOADR1	USB_FA1	Y18	Port A I/O or slave-FIFO address select 1
PA6/PKTEND	USB_PEND	AD14	Port A I/O or slave-FIFO packet end
PA7/SLCS#	USB_SLCS#	AC12	Port A I/O or slave-FIFO enable
RESET#	USB_RST#	AC14	USB device active-low reset

Table 18 - USB Interface FPGA Pin-out

2.5.1.2 RS232

The RS232 transceiver is a 3222 available from Harris/Intersil (ICL3222CA) and Analog Devices (ADM3222). This transceiver operates at 3.3V with an internal charge pump to create the RS232 compatible output levels. This level converter supports two channels. The primary channel is used for transmit and receive data (TXD and RXD). The secondary channel may be connected to the FPGA by installing jumpers on “JP7” and “JP8” for use as CTS and RTS signals. The RS232 console interface is brought out on the DB9 connector labeled “J1”. The Virtex-5 LX Evaluation board supports both straight-through and null-modem serial cables by selecting the DB9 pin-out with the 3-pin jumper headers labeled “JP1” and “JP2” as shown in the following figure.

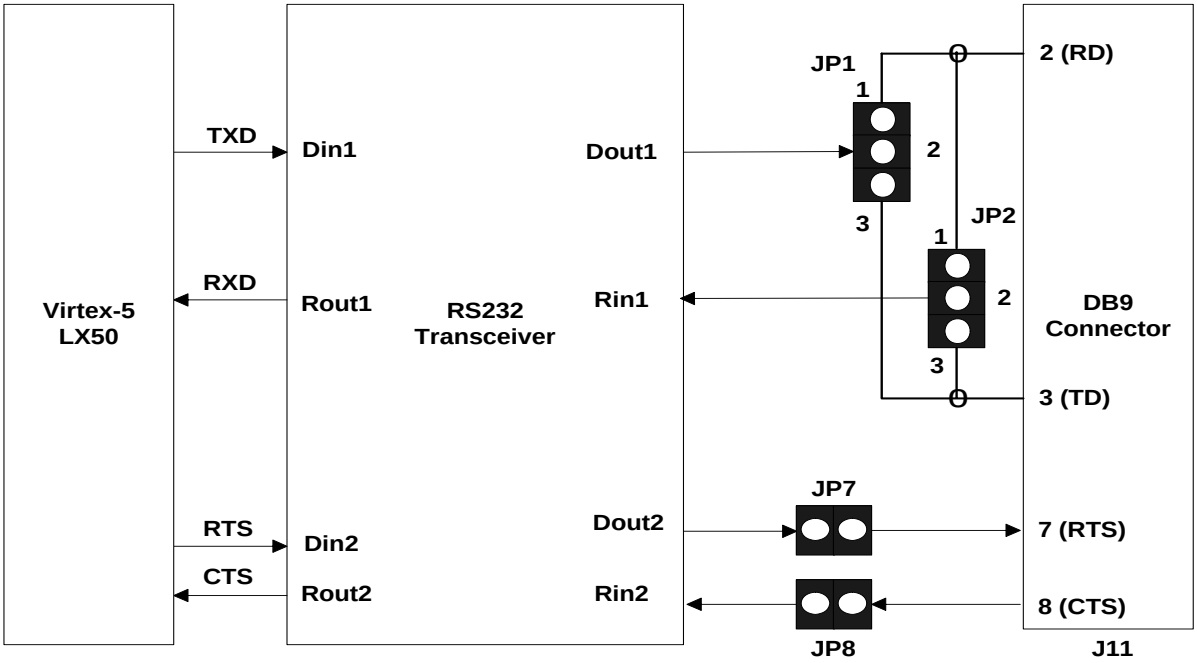


Figure 11 - RS232 Interface

A male-to-female serial cable should be used to plug "J1" into a standard PC serial port (male DB9). The following tables show the FPGA pin-out and jumper settings for the RS232 interface.

Net Name	Description	Virtex-5 Pin
RS232_RXD	Received Data, RD	AB7
RS232_TXD	Transmit Data, TD	AC6
RS232_RTS	Request To Send, RTS	AD5
RS232_CTS	Clear To Send, CTS	AB5

Table 19 - RS232 Signals

Mode of Operation	JP1	JP2	Cable
DCE (default)	Install a jumper on pins 2-3	Install a jumper on pins 1-2	Straight-thru
DTE	Install a jumper on pins 1-2	Install a jumper on pins 2-3	Null-modem

Table 20 - RS232 Port Jumper Settings

2.6 User Switches

Four momentary closure push buttons have been installed on the board and attached to the FPGA. These buttons can be programmed by the user and are ideal for logic reset and similar functions. Pull down resistors hold the signals low until the switch closure pulls it high (active high signals).

Net Name	Reference	Virtex-5 Pin
SWITCH_PB1	SW1	B1
SWITCH_PB2	SW2	B2
SWITCH_PB3	SW3	E8
SWITCH_PB4	SW4	F17

Table 21 - Push Button Pin Assignments

A FOUR-position dipswitch (SPST) has been installed on the board and attached to the FPGA. These switches provide digital inputs to user logic as needed. The signals are pulled low by 1K ohm resistors when the switch is open and tied high to 1.8V when flipped to the ON position.

Net Name	Reference	Virtex-5 Pin
SWITCH0	SW4 – 1	B26
SWITCH1	SW4 – 2	C26
SWITCH2	SW4 – 3	D26
SWITCH3	SW4 – 4	D25

Table 22 - DIP Switch Pin Assignments

2.7 User LEDs

Four discrete LEDs are installed on the board and can be used to display the status of the internal logic. These LEDs are attached as shown below and are lit by forcing the associated FPGA I/O pin to a logic '1' and are off when the pin is either low (0) or not driven.

Net Name	Reference	Virtex-5 Pin#
LED0	D1	E11
LED1	D2	E17
LED2	D3	F10
LED3	D4	F19

Table 23 - LED Pin Assignments

2.8 Configuration Port

The Virtex-5 LX Evaluation Board supports several methods of configuring the FPGA. The possible configuration sources include Boundary-scan (JTAG cable), the Platform Flash PROM, the Cypress USB device or the System ACE Module (SAM) header. The Virtex-5 device also supports configuration from BPI Flash. The blue LED labeled "DONE" on the board illuminates to indicate when the FPGA has been successfully configured.
The following sections provide brief descriptions of each of these interfaces.

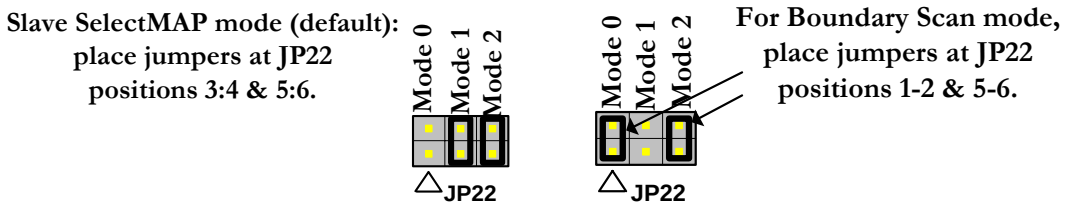
2.8.1 Configuration Modes

Upon power-up the FPGA will be enabled in a configuration mode defined by jumper header "JP22". The default configuration mode is "Slave SelectMAP" mode, which will allow the FPGA to be programmed from the Configuration PROM. The Configuration PROM has been programmed with basic test application code to test the on-board peripherals. Section 3.0 describes the various tests included with the Configuration PROM. The following table describes the various configuration modes.

Configuration Mode	M2 JP22 (5-6)	M1 JP22 (3-4)	M0 JP22 (1-2)
Master serial	Not Supported.		
Slave serial	JUMPERED	JUMPERED	JUMPERED
Master SelectMAP	JUMPERED	OPEN	OPEN
* Slave SelectMAP	JUMPERED	JUMPERED	OPEN
Boundary-scan	JUMPERED	OPEN	JUMPERED
Master SPI	OPEN	OPEN	JUMPERED
Master BPI-Up	OPEN	JUMPERED	OPEN
Master BPI-Down	OPEN	JUMPERED	JUMPERED

*Default assembled state

Table 24 - FPGA Configuration Modes



2.8.2 JTAG Chain

The Virtex-5 LX Evaluation Board has two devices in its JTAG chain: a Virtex-5 LX FPGA and a XCF32P configuration PROM. The following figure shows a high-level block diagram of the JTAG Chain on the Evaluation board.

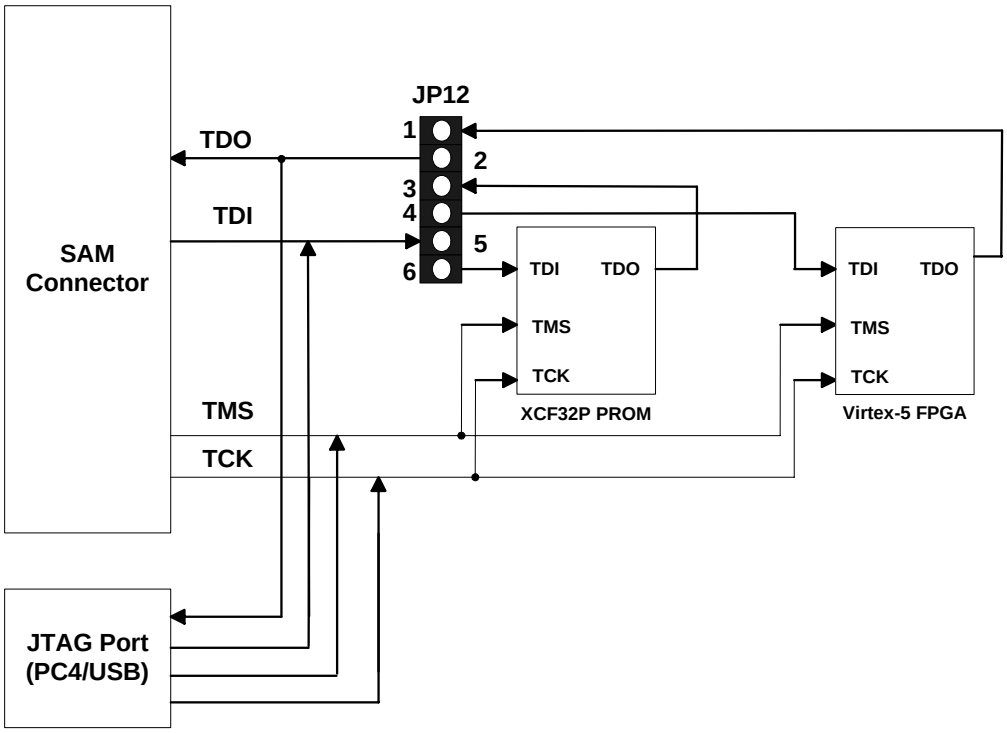


Figure 12 - JTAG Chain on the Virtex-5 LX Evaluation Board

The 6-pin header "JP23" provides the ability to isolate either device in the chain using the following jumper selections detailed in the following table.

JP12 Pins	JTAG Chain Selection
1-2 & 4-5	FPGA only
2-3 & 5-6	PROM only
1-2, 3-4 & 5-6	Both FPGA and PROM

Table 25 - JTAG Jumper Configurations

As delivered, JP12 is configured to include both the FPGA and the Configuration PROM in the JTAG chain.

Programming the Virtex-5 FPGA via Boundary-scan mode requires a JTAG download cable (not included in the kit).

If the Parallel Cable IV or Platform Cable USB is used, the ribbon cable connector mates with keyed connector "JP3".

2.8.2.1 Configuration PROM

The PROM can be re-programmed with new configuration data using a JTAG download cable and the iMPACT software that comes with the Xilinx ISE tools. The iMPACT software puts the PROM in either serial or parallel mode during programming based on a user-selectable programming option (the default in iMPACT is serial). After the PROM has been re-programmed, remove power and set the FPGA configuration mode that corresponds with the programming option that was selected in iMPACT. The jumper settings for Master SelectMAP (Parallel) mode is shown in the following figure. A jumper must be installed on JP14 (labeled "PROM EN") and JP18 (to enable configuration from the PROM. When power is re-applied, the FPGA will clock the configuration data from the PROM.

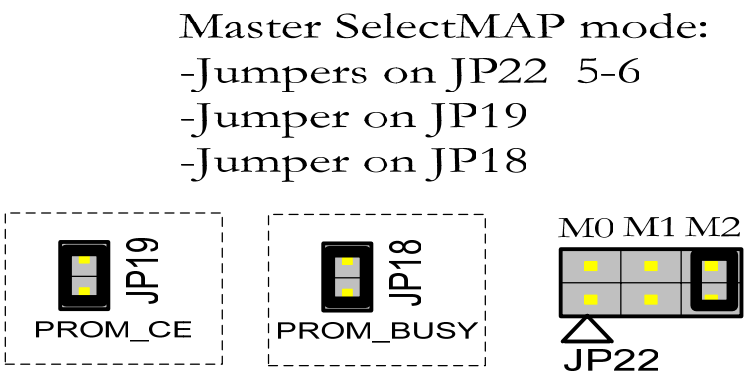


Figure 13 - Jumper Settings for Master SelectMAP mode

The Virtex-4 FX PCI Express Board is designed to support the advanced features of the parallel Platform Flash PROM including support for multiple design revisions and compressed configuration files. When using multiple revisions it is necessary to use compression in order to fit more than one design in the 32Mbit PROM. Slave SelectMAP mode must be used when using compressed configuration files. In slave modes the Platform Flash PROM drives the configuration clock to FPGA. A jumper must be installed on JP4 "CMP_EN" to connect the clock out pin on the PROM to the CCLK net of the FPGA. This jumper should be removed for master modes or if using the USB Utility to configure the FPGA.

2.8.2.2 System ACE Module Connector

The Virtex-5 LX Evaluation board provides support for the Avnet/Memec SystemACE Module (SAM) via the 50-pin connector labeled "JP11" on the board. The SAM can be used to configure the FPGA or to provide bulk Flash to the processor. This interface gives software designers the ability to run real-time operating systems (RTOS) from removable CompactFlash cards. The Avnet/Memec System ACE module (DS-KIT-SYSTEMACE) is sold separately. The figure below shows the System ACE Module connected to the header on the Virtex-5 LX Evaluation board.

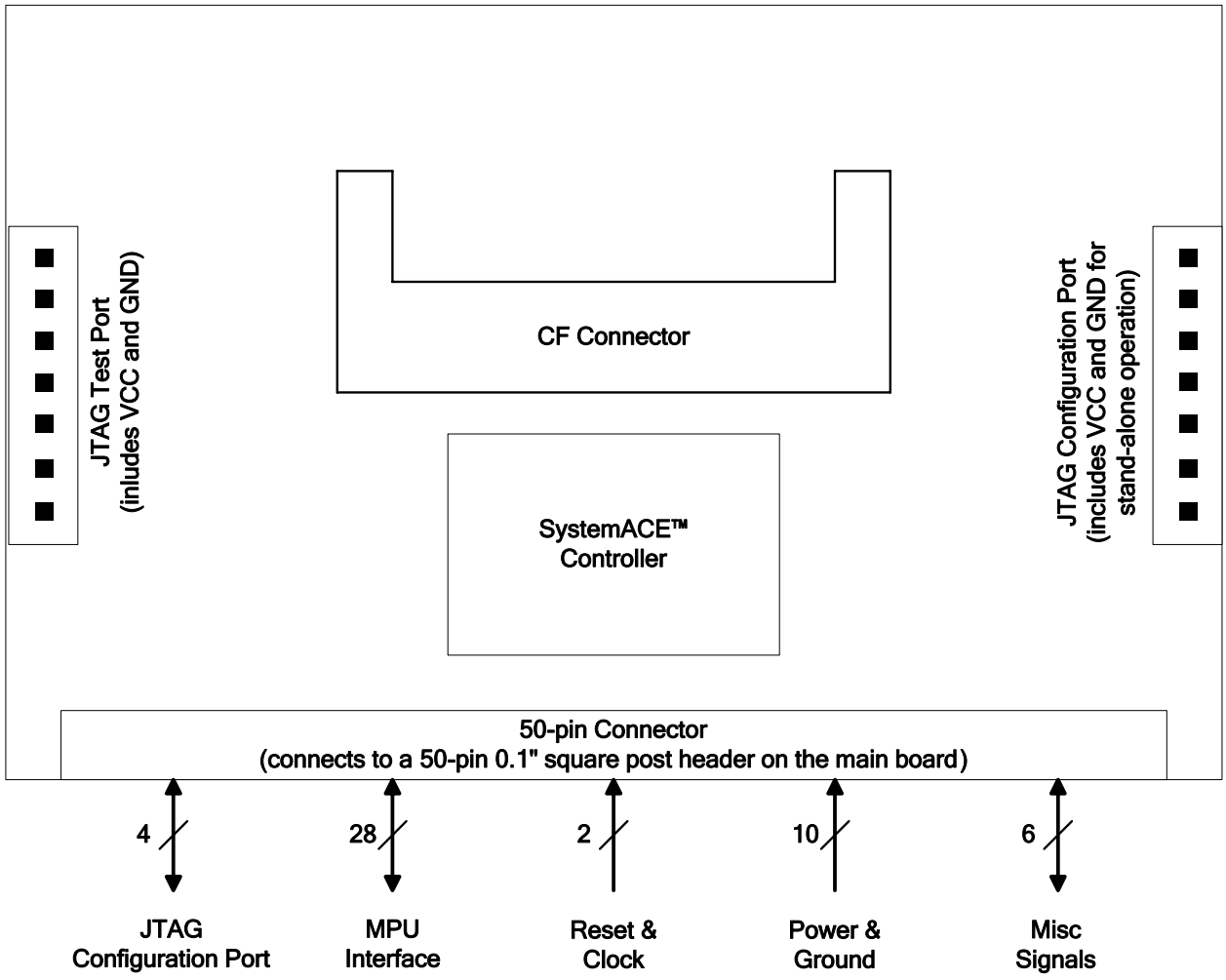


Figure 14 - SAM Interface (50-pin header)

The following table shows the System ACE ports that are accessible over the SAM header. The majority of the pins on this header may be used as general-purpose I/O when not using a System ACE Module. The Virtex-5 pin numbers are provided for these general-purpose pins.

Virtex-5 Pin	System ACE Signal Name	SAM Connector Pin # (JP11)		System ACE Signal Name	Virtex-5 Pin
-	**3.3V**	1	2	**3.3V**	**-**
-	TDO	3	4	**GND**	**-**
-	TMS	5	6	CLOCK	F8
-	TDI	7	8	**GND**	**-**
-	PROGRAMn	9	10	TCK	-
-	**GND**	11	12	**GND**	**-**
T4	OEn	13	14	INITn	-
T5	MPA0	15	16	WEn	U4
T7	MPA2	17	18	MPA1	U5
-	**2.5V**	19	20	MPA3	V3
U6	MPD00	21	22	**2.5V**	**-**
Y3	MPD02	23	24	MPD01	V4
W3	MPD04	25	26	MPD03	AA3
AC3	MPD06	27	28	MPD05	W4
AC4	MPD08	29	30	MPD07	AB4
W5	MPD10	31	32	MPD09	AA4
Y5	MPD12	33	34	MPD11	AD3
U7	MPD14	35	36	MPD13	AD4
V7	MPA4	37	38	MPD15	AA5
W6	MPA6	39	40	MPA5	V6
Y7	IRQ	41	42	**GND**	**-**
AA7	RESETn	43	44	CEn	AB6
-	DONE	45	46	BRDY	Y6
-	CCLK	47	48	BITSTREAM	-
-	**GND**	49	50	**NC**	**-**

Table 26 - SAM Interface Signals

2.8.2.3 JTAG Port (PC4)

The Virtex-5 LX Evaluation board provides a JTAG port (PC4 type) connector for configuration of the FPGA and programming of the on-board ISP PROM. The following figure shows the pin assignments for the PC4 header on this development board.

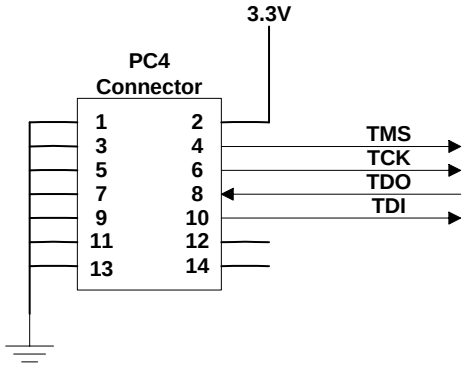


Figure 15 - PC4 JTAG Port Connector

2.9 Power

The Virtex-5 LX Evaluation Board power is developed from a +5V input provided by the external 5V 2.5A wall outlet transformer. The transformer cable plugs into the board at the barrel connector labeled “J3”. The +3.3V, +2.5V, +1.8V, power rails are developed by a TI PTH04070 power module. The +1.0V FPGA core power rail is developed by a single TI PTH5050W power module. The PTH5050W power module is capable of furnishing up to 6A. The TI PTH04070 power modules are capable of delivering 3A each. The +0.9V DDR2 reference/termination voltage is by a linear regulator from the +1.8V rail. The current requirements for the board are application specific. The following figure shows a high-level block diagram of the main power supply on the development board. Optionally, the Virtex-5 LX Evaluation Board can be powered from a standard 4 pin PC power supply plug by plugging the power connector into J2. Only the 5V pin is used of the PC supply plug will be used.

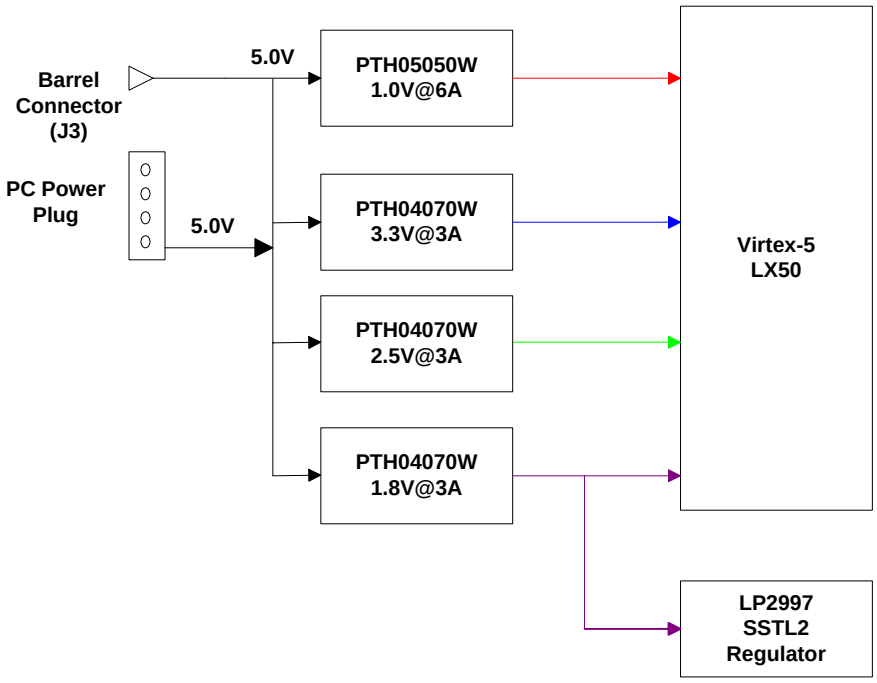


Figure 16 - Main Power Supply

2.9.1 FPGA I/O Voltage (Vcco)

FPGA banks 0, 1, 2, and 18 are powered at VCCO = 3.3V. Banks 4, 17, and 21 are powered at VCCO = 2.5V. There are four banks that have a selectable VCCO equal to either 2.5V or 3.3V. These four banks are banks 11, 12, 13 and 14, and are the banks for both of the EXP connectors. All four EXP banks are configured as a group depending n the position of JP9 . Banks 15 and 16 are powered at VCCO = 1.8V and are used for the DDR2 memory interface.

Bank #	1.8V	2.5V	3.3V	Selectable Rail
0			X	-
1			X	-
2			X	-
3		X	X	Vcco_exp
4		X		-
11		X	X	Vcco_exp
12		X	X	Vcco_exp
13		X	X	Vcco_exp
14		X	X	Vcco_exp
15	X			-
16	X			-
17		X		-
18			X	-
21		X		-

Table 27- I/O Bank Voltages

2.9.2 FPGA Reference Voltage (Vref)

The Virtex-5 LX Evaluation Board provides the reference voltage of +0.9V to FPGA banks 15 and 16, both of which are connected to the DDR2 memory interface.

2.10 Expansion Connectors

The Virtex-5 LX Evaluation board provides expansion capabilities for customized user application daughter cards and interfaces over two EXP expansion connectors. The EXP expansion connectors on the board can support two half-card EXP modules, or a single dual slot EXP module. Both off-the-shelf EXP modules and user-developed modules can easily be plugged onto the Virtex-5 LX Evaluation board to add features and functions to the backend application of the main board. For more information, view the EXP specification at www.em.avnet.com/exp.

2.10.1 EXP Interface

The EXP specification defines a 132-pin connector, with 24 power, 24 grounds, and 84 user I/Os. The standard EXP configuration implemented on the Virtex-5 LX Evaluation board uses two connectors (Samtec part number QTE-060-09-F-D-A) in a dual slot EXP configuration, for a total of 168 user I/Os. Using a jumper, you can set the voltage levels for the EXP user I/O to either 2.5V or 3.3V. As shown in the following figure, "JP9" sets the I/O voltage for the EXP connectors labeled "JX1" and "JX2" , by setting the VCCO voltage for the banks of the FPGA that connect to the EXP I/O.

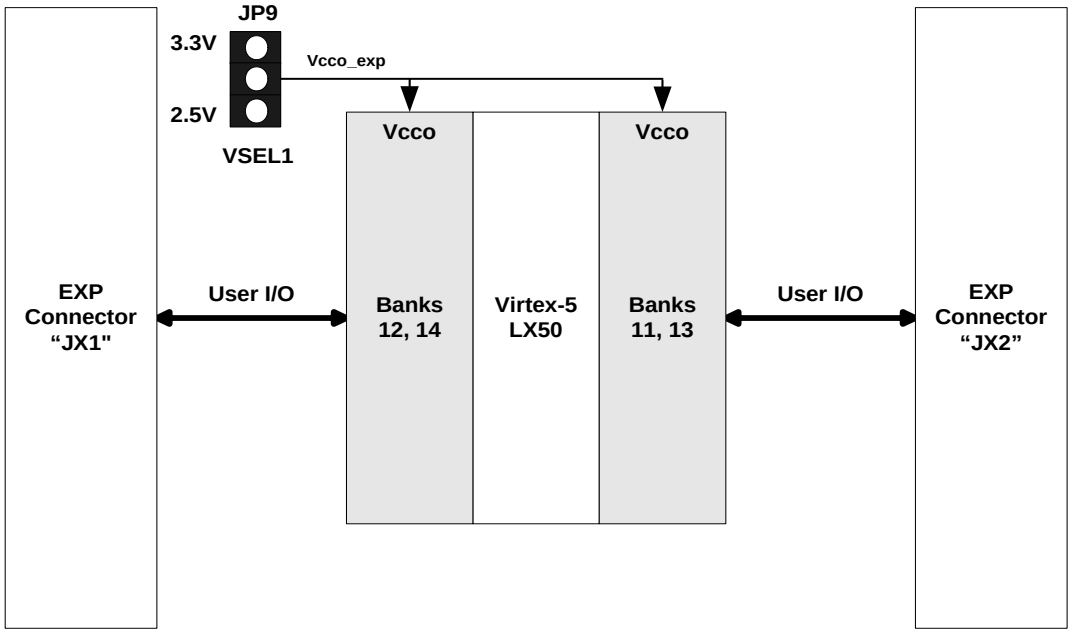


Figure 17 - EXP I/O Voltage Settings

The EXP specification defines four user signal types: Single Ended I/O, Differential I/O, Differential and Single Ended Clock Inputs, and Differential and Single Ended Clock Outputs. Because the FPGA I/Os can be configured for either single-ended or differential use, the differential I/Os defined in the EXP specification can serve a dual role. All the differential I/O signals can be configured as either differential pairs or single-ended signals, as required by the end application. In providing differential signaling, higher performance LVDS interfaces can be implemented between the baseboard and EXP module. Connection to high speed A/Ds, D/As, and flat panel displays are possible with this signaling configuration. Applications that require single-ended signals only can use each differential pair as two single-ended signals, for a total of 84 single-ended I/O per connector (168 total in the dual slot configuration).

Net Names	Signal Description	Pins per Connector	Pins per Dual Slot
EXPx_SE_IO	Single-ended I/O	34	68
EXPx_SE_CLK_IN	Single-ended clock inputs	2	4
EXPx_DIFF_p/n	Differential I/O pairs	20*	40*
EXPx_DIFF_CLK_IN_p/n	Differential clock input pair, global	1	2
EXPx_DIFF_CLK_OUT_p/n	Differential clock output pairs	1	2
EXPx_RCLK_DIFF_p/n10	Differential clock input pair, regional	1*	2*
EXPx_RCLK_DIFF_p/n*	Additional Regional clock input pair	1*	2*
Total		84	168

Table 28 - EXP Connector Signals

* Since the Virtex-5 FPGA supports regional clocking, the optional RCLK pair defined in version 1.2 of the EXP specification is utilized reducing the number of output-capable differential pairs from 22 down to 21. The Virtex-5 LX Evaluation board also implements an additional regional clock pair to support applications requiring more than one clock-capable pairs per EXP connector. For example, a SPI-4.2 interface could use the “EXPx__DIFF_p/n10” for the interface clock and the extra regional clock pair for the status clock. This reduces the number of output-capable differential pairs to 20.

The Virtex-5 FPGA user I/O pins that connect to the two EXP connectors are shown in the following table. The Samtec QTE connector plugs on the Virtex-5 LX Evaluation board (part number: QTE-060-09-F-D-A) mate with the Samtec QSE high-performance receptacles (part number: QSE-060-01-F-D-A), located on the daughter card. Samtec also provides several high-performance ribbon cables that will mate to the “JX1” and “JX2” connectors.

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Virtex-5 Pin	Net Name	EXP Connector Pin # (JX1)		Net Name	Virtex-5 Pin
G4	EXP1_SE_IO_0	2	1	EXP1_SE_IO_1	D14
H7	EXP1_SE_IO_2	4	3	EXP1_SE_IO_3	G5
-	**2.5V**	6	5	**2.5V**	-
H6	EXP1_SE_IO_4	8	7	EXP1_SE_IO_5	H4
J4	EXP1_SE_IO_6	10	9	EXP1_SE_IO_7	J5
-	**2.5V**	12	11	**2.5V**	-
K7	EXP1_SE_IO_8	14	13	EXP1_SE_IO_9	J6
L4	EXP1_SE_IO_10	16	15	EXP1_SE_IO_11	K6
-	**2.5V**	18	17	**2.5V**	-
L7	EXP1_SE_IO_12	20	19	EXP1_SE_IO_13	L3
M5	EXP1_SE_IO_14	22	21	EXP1_SE_IO_15	M6
-	**2.5V**	24	23	**2.5V**	-
M2	EXP1_SE_IO_16	26	25	EXP1_SE_IO_17	M1
M7	EXP1_SE_IO_18	28	27	EXP1_SE_IO_19	M4
-	**2.5V**	30	29	**2.5V**	-
N4	EXP1_SE_IO_20	32	31	EXP1_SE_IO_21	N7
N6	EXP1_SE_IO_22	34	33	EXP1_SE_IO_23	N1
-	**2.5V**	36	35	**2.5V**	-
P5	EXP1_SE_IO_24	38	37	EXP1_SE_IO_25	N2
P1	EXP1_SE_IO_26	40	39	EXP1_SE_IO_27	N3
E12	EXP1_DIFF_CLK_IN_p	42	41	EXP1_SE_IO_28	P3
F12	EXP1_DIFF_CLK_IN_n	44	43	EXP1_SE_CLK_IN	D13
-	**GND**	46	45	**GND**	-
R3	EXP1_SE_IO_30	48	47	EXP1_SE_IO_29	R1
R2	EXP1_SE_IO_31	50	49	EXP1_SE_CLK_OUT	P4
-	**GND**	52	51	**GND**	-
E2	EXP1_DIFF_p20	54	53	EXP1_DIFF_p21	E6
E1	EXP1_DIFF_n20	56	55	EXP1_DIFF_n21	E5
-	**GND**	58	57	**GND**	-
F5	EXP1_DIFF_p18	60	59	EXP1_SE_IO_32	T2
F4	EXP1_DIFF_n18	62	61	EXP1_SE_IO_33	T3
-	**GND**	64	63	**GND**	-
F3	EXP1_DIFF_p16	66	65	EXP1_DIFF_p19	E7
E3	EXP1_DIFF_n16	68	67	EXP1_DIFF_n19	F7
-	**GND**	70	69	**GND**	-
Y1	EXP1_DIFF_CLK_OUT_p	72	71	EXP1_DIFF_p17	F2
W1	EXP1_DIFF_CLK_OUT_n	74	73	EXP1_DIFF_n17	G2
-	**GND**	76	75	**GND**	-
G1	EXP1_DIFF_p14	78	77	EXP1_DIFF_p15	K3
H1	EXP1_DIFF_n14	80	79	EXP1_DIFF_n15	K2
H3	EXP1_DIFF_p12	82	81	EXP1_DIFF_p13	J1
J3	EXP1_DIFF_n12	84	83	EXP1_DIFF_n13	H2
-	**3.3V**	86	85	**3.3V**	-
K5	EXP1_RCLK_DIFF_p10	88	87	EXP1_DIFF_p11	L2
L5	EXP1_RCLK_DIFF_n10	90	89	EXP1_DIFF_n11	K1
-	**3.3V**	92	91	**3.3V**	-
P6	EXP1_DIFF_p8	94	93	EXP1_DIFF_p9	G6
R7	EXP1_DIFF_n8	96	95	EXP1_DIFF_n9	G7
-	**3.3V**	98	97	**3.3V**	-
U2	EXP1_DIFF_p6	100	99	EXP1_DIFF_p7	R6
U1	EXP1_DIFF_n6	102	101	EXP1_DIFF_n7	R5
-	**3.3V**	104	103	**3.3V**	-
V2	EXP1_DIFF_p4	106	105	EXP1_DIFF_p5	AA2
V1	EXP1_DIFF_n4	108	107	EXP1_DIFF_n5	Y2
-	**3.3V**	110	109	**3.3V**	-
AB2	EXP1_DIFF_p2	112	111	EXP1_DIFF_p3	AC2
AB1	EXP1_DIFF_n2	114	113	EXP1_DIFF_n3	AC1
-	**3.3V**	116	115	**3.3V**	-
AF2	EXP1_DIFF_p0	118	117	EXP1_DIFF_p1	AE1
AE2	EXP1_DIFF_n0	120	119	EXP1_DIFF_n1	AD1
-	**GND**	122	121	**GND**	-
-	**GND**	124	123	**GND**	-
-	**GND**	126	125	**GND**	-
-	**GND**	128	127	**GND**	-
-	**GND**	130	129	**GND**	-
-	**GND**	132	131	**GND**	-

Table 29 - EXP Connector "JX1" Pin-out

Virtex-4 Pin#	Net Name	EXP Connector Pin # (JX2)		Net Name	Virtex-4 Pin#
H19	EXP2_SE_IO_0	2	1	EXP2_SE_IO_1	E15
H21	EXP2_SE_IO_2	4	3	EXP2_SE_IO_3	G21
-	**2.5V**	6	5	**2.5V**	-
H22	EXP2_SE_IO_4	8	7	EXP2_SE_IO_5	G22
J21	EXP2_SE_IO_6	10	9	EXP2_SE_IO_7	H23
-	**2.5V**	12	11	**2.5V**	-
J19	EXP2_SE_IO_8	14	13	EXP2_SE_IO_9	J20
K21	EXP2_SE_IO_10	16	15	EXP2_SE_IO_11	J23
-	**2.5V**	18	17	**2.5V**	-
L20	EXP2_SE_IO_12	20	19	EXP2_SE_IO_13	K20
L23	EXP2_SE_IO_14	22	21	EXP2_SE_IO_15	L19
-	**2.5V**	24	23	**2.5V**	-
M21	EXP2_SE_IO_16	26	25	EXP2_SE_IO_17	L22
M25	EXP2_SE_IO_18	28	27	EXP2_SE_IO_19	M22
-	**2.5V**	30	29	**2.5V**	-
M20	EXP2_SE_IO_20	32	31	EXP2_SE_IO_21	M24
N22	EXP2_SE_IO_22	34	33	EXP2_SE_IO_23	M26
-	**2.5V**	36	35	**2.5V**	-
N21	EXP2_SE_IO_24	38	37	EXP2_SE_IO_25	N23
N19	EXP2_SE_IO_26	40	39	EXP2_SE_IO_27	N24
F14	EXP2_DIFF_CLK_IN_p	42	41	EXP2_SE_IO_28	N26
E13	EXP2_DIFF_CLK_IN_n	44	43	EXP2_SE_CLK_IN	D15
-	**GND**	46	45	**GND**	-
P19	EXP2_SE_IO_30	48	47	EXP2_SE_IO_29	P24
P23	EXP2_SE_IO_31	50	49	EXP2_SE_CLK_OUT	M19
-	**GND**	52	51	**GND**	-
E22	EXP2_DIFF_p20	54	53	EXP2_DIFF_p21	E25
E23	EXP2_DIFF_n20	56	55	EXP2_DIFF_n21	E26
-	**GND**	58	57	**GND**	-
E21	EXP2_DIFF_p18	60	59	EXP2_SE_IO_32	P25
E20	EXP2_DIFF_n18	62	61	EXP2_SE_IO_33	P26
-	**GND**	64	63	**GND**	-
G24	EXP2_DIFF_p16	66	65	EXP2_DIFF_p19	F24
G25	EXP2_DIFF_n16	68	67	EXP2_DIFF_n19	F25
-	**GND**	70	69	**GND**	-
V26	EXP2_DIFF_CLK_OUT_p	72	71	EXP2_DIFF_p17	F22
U26	EXP2_DIFF_CLK_OUT_n	74	73	EXP2_DIFF_n17	F23
-	**GND**	76	75	**GND**	-
G26	EXP2_DIFF_p14	78	77	EXP2_DIFF_p15	H24
H26	EXP2_DIFF_n14	80	79	EXP2_DIFF_n15	J24
G20	EXP2_DIFF_p12	82	81	EXP2_DIFF_p13	J25
F20	EXP2_DIFF_n12	84	83	EXP2_DIFF_n13	J26
-	**3.3V**	86	85	**3.3V**	-
K23	EXP2_RCLK_DIFF_p10	88	87	EXP2_DIFF_p11	K25
K22	EXP2_RCLK_DIFF_n10	90	89	EXP2_DIFF_n11	K26
-	**3.3V**	92	91	**3.3V**	-
P21	EXP2_DIFF_p8	94	93	EXP2_DIFF_p9	L24
P20	EXP2_DIFF_n8	96	95	EXP2_DIFF_n9	L25
-	**3.3V**	98	97	**3.3V**	-
R25	EXP2_DIFF_p6	100	99	EXP2_DIFF_p7	R22
R26	EXP2_DIFF_n6	102	101	EXP2_DIFF_n7	R23
-	**3.3V**	104	103	**3.3V**	-
T24	EXP2_DIFF_p4	106	105	EXP2_DIFF_p5	U24
T25	EXP2_DIFF_n4	108	107	EXP2_DIFF_n5	U25
-	**3.3V**	110	109	**3.3V**	-
W25	EXP2_DIFF_p2	112	111	EXP2_DIFF_p3	Y25
W26	EXP2_DIFF_n2	114	113	EXP2_DIFF_n3	Y26
-	**3.3V**	116	115	**3.3V**	-
AB25	EXP2_DIFF_p0	118	117	EXP2_DIFF_p1	AC26
AA25	EXP2_DIFF_n0	120	119	EXP2_DIFF_n1	AB26
-	**GND**	122	121	**GND**	-
-	**GND**	124	123	**GND**	-
-	**GND**	126	125	**GND**	-
-	**GND**	128	127	**GND**	-
-	**GND**	130	129	**GND**	-
-	**GND**	132	131	**GND**	-

Table 30 - EXP Connector "JX2" Pin-out

2.11 LCD Display

The Virtex-5 LX Evaluation board comes equipped with a 2X16 character LCD display. The LCD is manufactured by Mytech and the part number is MOC-16216B-B. The LCD is operated in 4-bit mode by using only the upper 4 four data bits of the LCD data bus. There is no read operation implemented for the LCD, it is write only. A total of six signals are required to use the LCD. The LCD is powered from the 5V rail. The LCD is attached to the board via 4 standoffs with screws, and interfaced to the PCB by connecting to a 14 pin header (J5). The table below shows the connections to the header and the Virtex-5 FPGA.

Signal Name	J5 connector Pin	Virtex-5 pin
GND	1	-
VDD (5V)	2	-
VL	3	-
LCD_RS	4	AE3
R/W#	5	Connected to GND on the board
LCD_E	6	AF3
NC	7	-
NC	8	-
NC	9	-
NC	10	-
LCD_DB4	11	AF4
LCD_DB5	12	AF5
LCD_DB6	13	AE6
LCD_DB7	14	AD6

Table 31 - LCD Interface Pin-out

3.0 Test Designs

This section describes the three test designs that are pre-programmed into the XCF32P Configuration PROM. These designs are used to verify some of the functionality of the board and may require additional test apparatus. The remaining production tests are not included with the kit because they require custom-designed test fixtures.

If the Configuration PROM has been erased, the MCS file containing the test designs is available on the Design Resource Center web site: www.em.avnet.com/drc. To load, assign the MCS file to first device in the chain (xcf32p) and select the first three revisions for programming, erase and verify. Use parallel mode and program in Configuration Master Mode using the internal clock (40 MHz). The following jumper settings put the FPGA in Slave SelectMAP mode and enable the PROM to drive CCLK; this is necessary to use the compressed designs. Jumpers are set as follows:

Jumper Settings:

```
JP22 (3-4) - Installed
JP22 (5-6) - Installed
JP19       - Installed
JP4        - Installed
```

The Ethernet and Factory test designs use a terminal session as the user interface. Using a straight-through serial cable, connect the Virtex-5 LX Evaluation Board to a PC. Open a terminal session and configure it for 19200 baud, 8 data bits, no parity, 1 stop bit and no flow control (19200-8-N-1-N). First select the desired test design by installing jumpers on “JP12” according to the following table and then press the “SW10” push button on the board to load the design.

Jumper JP12:			Test File Selected:
1-2	3-4	5-6	
ON/OFF	OFF	OFF	Factory Test
OFF	ON	OFF	Ethernet Test
OFF	OFF	ON	-----

Table 32 - Test Designs (in Configuration PROM)

3.1 Factory Test

The Factory Test verifies the electrical connectivity of the DDR SDRAM and Flash memory, the user LEDs and switches, and the EXP expansion connectors (requires a Samtec loopback cable). The user can initiate the tests by typing 'test <enter>' in a terminal session configured as shown in Section 3.0 (19200-8-N-1-N). Some of the tests require user inputs and observation (watching the LEDs and pressing the switches). The cumulative results are displayed at the completion of test processes. The EXP loopback test requires a Samtec cable, part number: EQCD-060-12.00-SED-SEU-1 or similar. Check the following catalog page for more information: http://www.samtec.com/ftppub/pdf/EQCD.PDF.

3.2 Ethernet Test

The Ethernet Test design provides the user with the ability to ping the Virtex-5 LX Evaluation board to verify network connectivity via the on-board National 10/100/1000 Mbps Ethernet PHY. The National PHY supports auto-MDIX mode, which allows either a straight-through or a cross-over Ethernet cable to be used. The default IP address of the board is 172.16.158.147. To ping the board, plug an Ethernet cable into the RJ45 connector labeled "J12". Then change the IP address of the board to match the subnet of the PC or network it's connected to using a terminal program configured as shown in Section 3.0 (19200-8-N-1-N). At the prompt, type 'i' and then enter the new IP address for the board (first three fields must match the IP address of the PC: MMM.MMM.MMM.xxx; the last field must be different). Use periods '.' between fields and hit the <enter> key when finished. Then open a command shell on the PC (Start Menu -> Run, cmd) and type 'ping MMM.MMM.MMM.xxx'. You should see four replies to the ping request.

4.0 Revisions

V1.0	Initial release for production board (AES-XLX-V5-EVL-PCB-B)	November 11, 2006

Appendix A

This section provides a description of the jumper settings for the Virtex-5 LX Evaluation board. The board is ready to use out of the box with the default jumper settings. The following figure depicts a map of the component side of the board with Jumper/Header/Connector locations detailed. The jumper sites are colored yellow below.

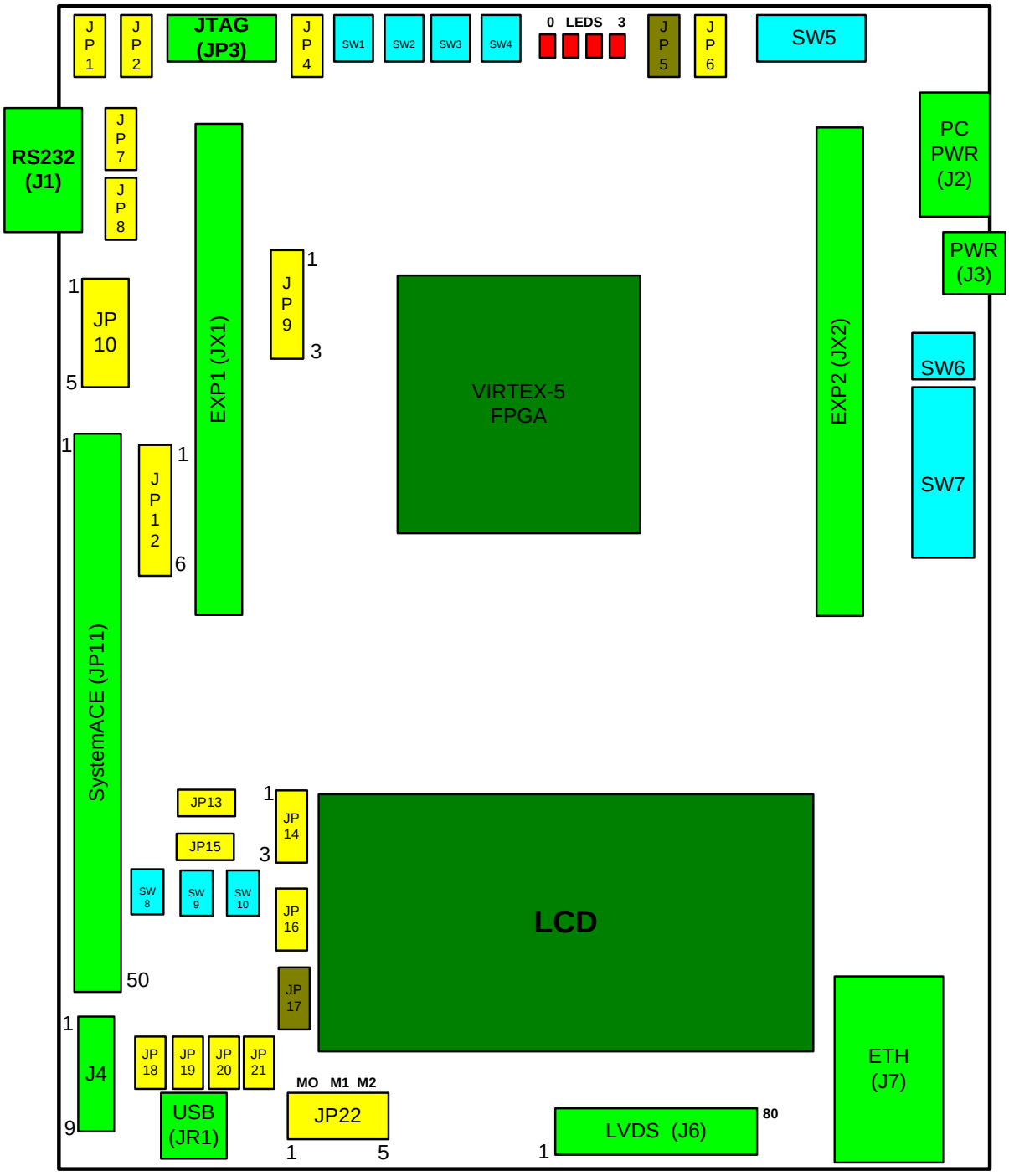


Figure 18 - Board Jumpers/Headers/etc.

JP1 “R1IN” - Connects the “R1IN” signal of the RS232 transceiver to either pin 2 or pin 3 of the DB9 connector. Install a shunt across pins 1-2 for DTE mode or pins 2-3 for DCE mode. Default: JP1 2-3.

JP2 “T1OUT” - Connects the “T1OUT” signal of the RS232 transceiver to either pin 2 or pin 3 of the DB9 connector. Install a shunt across pins 1-2 for DCE mode or pins 2-3 for DTE mode. Default: JP2 1-2.

JP4 “CMP EN” – Compression Enable, when installed enables the parallel PROM to drive the configuration clock of the FPGA. The PROM must supply CCLK when a compressed configuration file is used. If using the PROM device as the clock source, make sure the jumper on JP16 is not installed and that the jumper settings on JP22 put the FPGA in a Slave configuration mode. Default: Installed, the PROM provides the configuration clock.

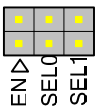
JP6 – HSWAP_EN, Enables pull-ups on the Virtex-5 I/O pins during configuration. Install a jumper to enable the configuration pull-ups. Default: Open; pull-ups disabled.

JP7 “T2OUT” – Install a shunt to connect the second TX port of the RS232 transceiver to the DB9 connector for hardware handshaking. This can be used to implement the clear to send (CTS) signal. Default: Open.

JP8 “R2IN” – Install a shunt to connect the second RX port of the RS232 transceiver to the DB9 connector for hardware handshaking. This can be used to implement the ready to send (RTS) signal. Default: Open.

JP9 – Vcco selectable voltage for Banks 11, 12, 13 and 14 on the Virtex-5 LX Evaluation Board. JP9 in its default configuration (VCCO_exp = +2.5V) is JP9 (1-2). JP9(2-3) will set the EXP voltage banks to 3.3V.

JP10 “REV SEL” – Design Revision Select, selects the configuration design when the PROM is programmed with multiple revisions. When no jumpers are installed, the PROM is set for external selection mode with revision 0 selected. Installing jumpers on JP10 will pull the corresponding select pin high, as indicated in the following figure. Default: JP10 1-2 (Enable Rev 0).



JP10 Revision Select	1-2	3-4	5-6
External disabled	1	x	x
Enabled - Rev. 0	0	0	0
Enabled - Rev. 1	0	1	0
Enabled - Rev. 2	0	0	1
Enabled - Rev. 3	0	1	1

Figure 19 - PROM Revision Selection

JP12 JTAG Chain configuration - Selects the configuration of the JTAG chain. Install jumpers across pins 1-2, 3-4 and 5-6 to put both devices in the chain (XCF32P PROM and Virtex-5 FPGA). Default: Installed across pins 1-2, 3-4 & 5-6.

JP13 “USB DIS” – USB Disable, install a shunt to hold the Cypress EZ-USB device in reset. When open, the USB reset line is controlled by either an I/O pin of the FPGA or the push-button labeled “SW2”. Default: Open, the FPGA or push-button controls the USB reset.

JP14 “VPEN” – Flash Write-protect Enable, install a shunt to protect programmed data in the Flash memory. Default: JP14 1:2, read/write enabled (unprotected).

JP15 “FLASH_D0/FPGA_DIN” – Serial Mode Enable, connects the D0 pin of the parallel PROM to the DIN pin of the FPGA. The Virtex-5 FPGA has a separate pin, DIN, for serial configuration data. When using the parallel PROM in a serial configuration mode, install a shunt on JP15. Default: Open, serial mode is not used.

JP16 “FPGA_CFG OE” – CCLK Enable; when installed enables the USB device to drive the configuration clock of the FPGA. If using the USB device as the clock source, disable the PROM by removing the jumper on JP19 and make sure the jumper s on JP22 are all removed. The USB device will drive the mode pins to put the FPGA in a Slave configuration mode. Default: Open, the FPGA or PROM provides the configuration clock.

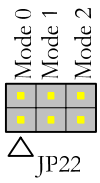
JP18 “PROM_BSY/FPGA_BUSY” – Parallel Mode Enable, connects the BUSY pin of the parallel PROM to the BUSY pin of the FPGA. The parallel configuration mode uses the BUSY signal of the FPGA for flow-control purposes. Default: Installed, a parallel configuration mode is used to load the demo design on power-up.

JP19 “PROM EN” – PROM Enable, connects the DONE pin on the FPGA to the chip enable pin of the PROM. The PROM is disabled by a pull-up resistor when a jumper is not installed. Default: Installed, the PROM is enabled when the FPGA is not configured.

JP20 – USB Serial EEPROM address select, Default: Open.

JP21 – USB Serial EEPROM write protect, install a shunt to protect programmed data. Default: Open, read/write enabled.

JP22 “Configuration mode selection” – Use to select the configuration mode for the FPGA. By default, these pins are pulled low enabling Master Serial mode. Installing jumpers on JP22 will pull the corresponding mode pin high, as indicated in Figure 19. See section 2.8.2.1 for more information.



JP22	1-2	3-4	5-6
Config Mode	M0	M1	M2
Slave Serial	1	1	1
Master SelectMAP	0	0	1
Slave SelectMAP	0	1	1
Boundary Scan	1	0	1
Master BPI-UP	0	1	0
Master BPI-Down	0	1	1

Figure 20 - Configuration Mode Jumpers