THE CDG2000 HF TRANSCEIVER

Part five, by Colin Horrabin, G3SBI, Dave Roberts, G8KBB, and George Fare, G3OGQ *

THIS MONTH, we begin a close look at the synthesiser. It is critical to the operation and performance of the transceiver, and provides the local oscillator on transmit and on receive.

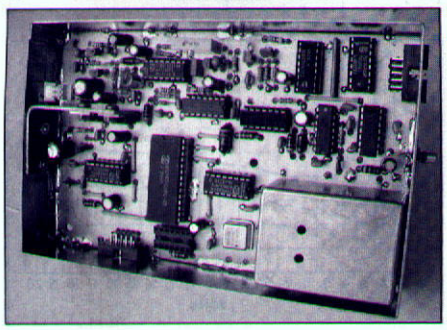
It is required to provide an output signal that can drive the 74AC series logic divider in the H-mode mixer [13]. This signal must have as little phase noise as possible and must be crystal-derived for stability and accuracy. It is controlled by the main CPU and must be capable of being set to any frequency in the range 46 to 78MHz. Whilst this may appear to have a 32MHz range and therefore capable of covering the whole of the HF spectrum, remember that there is a divide-by-2 process in the mixer – so for a 30MHz range we would require a VCO swing of 60MHz. This is avoided by using a programmable divider in the VCO output circuit. This can be seen in **Fig 26**, which shows a block diagram of the synthesiser.

By using low- as well as high-side local oscillator injection, an even narrower VCO range is possible, but is not used here. The controller software does, however, support this if you wish to experiment with it.

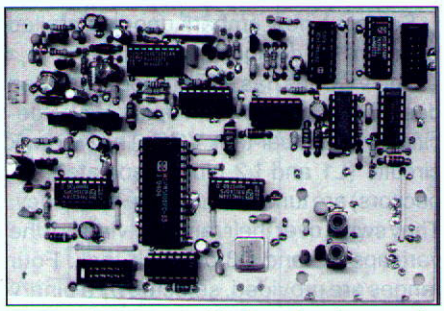
The heart of the synthesiser is the VCO. This has four ranges controlled by the two control lines from the I²C bus interface which give overlapped coverage from 46 to 78MHz. The output of the VCO takes three paths, two of which lead to the output. The signal can either be passed to the output via a multiplexer or it can first be divided by 2, 3, 4 or 5. This ratio can be changed to any value up to 15 if the design is used for other purposes, but this is unnecessary for CDG2000. The other path taken by the VCO signal is into the phase-locked loop. Before this, however, it is divided by 512 using a divide-by-4 and a divide-by-128. This gives a frequency in the range 90 to 152kHz which is phase-locked to a signal from a Direct Digital Synthesiser (DDS) at the same frequency. The control signal from the Phase Comparator is filtered and amplified by the loop filter before being passed to the VCO varicaps through a final low-pass filter.

The completed unit is, like other CDG2000 modules, constructed on a 160 x 100mm Eurocard which may be fitted into a tinplate box as shown in the photograph (bottom left). If the unit is otherwise screened, for example by being fitted into a rig that offers screening by other means such as a 'bookcase' style of construction, then this is unnecessary. What is essential, however, is the extra screening around the VCO, provided by a small diecast box. This can be seen in the same photograph. Also visible in the photograph is a small heatsink connecting the two voltage regulators to the side of the box. The photograph above shows the partially-constructed unit without screening or heatsink. The VCO coils can be seen at the bottom right hand corner of the board and the reader will notice the lack of components in the vicinity of the VCO – that is because the majority of the VCO is constructed of surface-mount components which are situated on the track side of the PCB as shown in the third photograph – a close-up of the VCO.

* *1 Old Hall Close, Higher Walton, Warrington WA4 6SZ.*



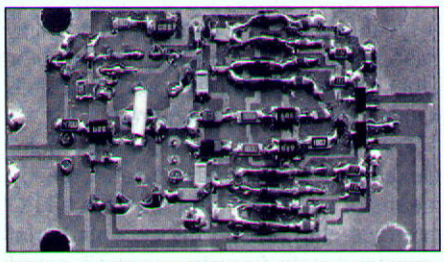
The completed synthesiser.



The partially-assembled synthesiser card - no screening or heatsink.

THE CIRCUIT

THE FULL CIRCUIT diagram of the synthesiser is shown in **Fig 27**. Before we embark on a detailed description though, a few points need to be made, to give credit where it is due. Colin Horrabin, G3SBI, sent notes on a novel tank VCO design to Pat Hawker, G3VA, who published them in *RadCom* [14]. Learning from earlier designs of VCOs [15], Colin produced an inherently low-noise design capable of excellent performance where a second coil acted as a Q-multiplier giving a 30dB per decade noise reduction. Remember from the overview to CDG2000 [16], that there is no point trying to use the PLL to 'clean up' a noisy VCO as this will inevitably let through the DDS spurii to the VCO. This has been well covered in the literature [17]. Even exceptional DDS designs such as the newest Analog Devices products with spurious products of -97dBc are inadequate for the performance levels we seek [18]. This VCO design was picked up by John Thorpe (the man behind the excellent AOR AR7030 receiver), who developed it into a reproducible design. He also moved away from the PCB inductors used by Colin in his prototype. It is this VCO that we used and are indebted to John for the permission to repeat his circuit here. The excellent performance of the VCO is easy to see from the phase noise in the reviews of the AR7030 [19].



Close-up of the VCO (on the track side of the board).

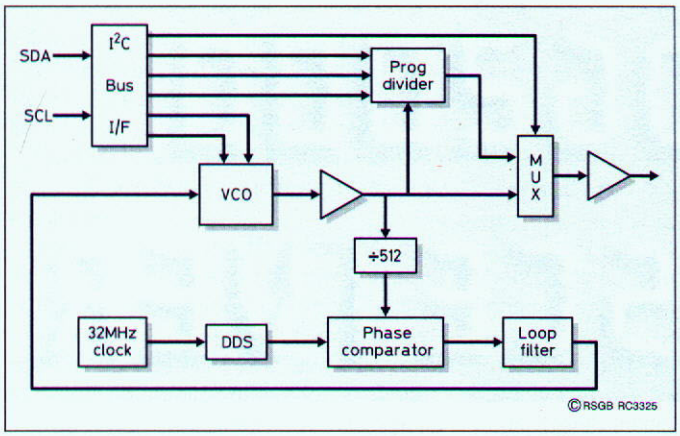


Fig 26: Block diagram.

So, let us now embark upon a detailed review of the design.

The VCO, as has been noted, has been described in 'Technical Topics' [14]. Specifically it is a dual-tank VCO. The two tank circuits (L1 and L2 plus associated capacitors) are tuned to the same frequency. They swing over their range by virtue of the varicaps D2 and D3 on each tank. Four ranges are provided, selected by a binary code on the two switch inputs to the VCO. These cause transistors TR8 and TR9 to switch in additional capacitance. The switching is effected by a parallel pair of diodes D8/D9 and D10/11, to reduce losses and maintain operational Q.

The VCO tuning ranges are shown in **Fig 28**.

The output of the VCO is buffered by IC6 and converted to a logic level signal. The reader will notice that the device used to do this has an individually-decoupled and filtered supply line. The same is true for many of the other logic devices used. This is because an AC logic gate, as used here, is not just a logic gate – it is a very effective non-linear mixer/modulator, and stray noise on either a logic input tied high or on the power rail will manifest itself as phase noise on the output signal. Care also needs to be exercised over the supply to the loop filter / amplifier. Very clean 20V and 8V rails are needed. This is achieved by heavy filtering of the voltages delivered by monolithic regulators Reg1 and Reg3.

The buffered signal is either passed directly to the output via IC11 or it is divided first by IC10. This allows the output to be either the basic VCO frequency, or this frequency divided by 2 to 5. The divider is a synchronous device (essential to minimise phase noise) and may be used for other ratios by tying the programmable divider 'load' inputs as required.

The selection of the divide ratio, multiplexer and VCO control is effected by means of a parallel interface from an I²C interface chip (IC9). This accepts serial command data from the controller and outputs the appropriate signals. It also detects the phase-lock signal from the PLL so that it may be read by the controller. A bit map showing the function of the output bits (0 to 7) from the PCF8574 is shown in **Table 4**. The operation of I²C is not addressed here, but in précis it comprises a two-wire interface (clock and data) that allows a master device, in this case the controller, to address a number of parallel-connected slave devices and read from or write to them. For further information, refer to the PCF8574 datasheet [20]. In the case of the synthesiser, the controller writes to the PCF8574 which allows it to set the states of six control lines and to read the state of the PLL lock signal. Each I²C device has a unique address and, for the synthesiser, this is 0x4A if a PCF8574 is used or 0x7A if a PCF8574A is used.

The VCO frequency is divided by 512 in IC7 and IC8. The resultant signal is passed to one comparator input of IC5, a 74HCT9046 [21]. This is an enhanced version of the familiar 4046 PLL chip. The reference frequency for the PLL is generated by a DDS – more of that later. The output of the phase comparator drives the loop amplifier and filter which gives the loop a bandwidth of around 1kHz. The output of the amplifier is further low-pass filtered by a passive RC filter which then drives the VCO. The loop filter amplifier is also attributable to John Thorpe.

The DDS is hardly the latest technology, being formed by the venerable HSP45102 DDS [22] chip, IC2, clocked at 32MHz by X1. The DAC is external to the DDS chip with an R - 2R ladder driven by two 6-bit latches (IC3 and 4) giving a 12-bit DAC. While more modern devices may be as good (or better), this combination has been found by a number of designers to offer excellent performance. The signal is low-pass filtered and passed to the phase comparator.

The Digital to Analogue converter used by the DDS warrants closer attention. It has been found that the structure shown performs well, with a noise floor about -90dBc/Hz. As was pointed out by one of the article's reviewers, this should not be the case - with 1% resistors an effective resolution of about 6 bits only ought to be obtained. It is believed that the measured performance is due to operation far below the Nyquist limit, but this remains an area of interesting investigation and one that will probably draw much comment. It would therefore be prudent to use 0.1% resistors such as the Meggitt RN series from Farnell, even though the performance presented here was obtained using 1% devices.

Bit(s)	Function
0, 1	Set 74AC163 divide ratio from 2 (both high) to 5 (both low)
2	If low, hold 74AC163 reset when not being used
3	Select direct output of VCO (if high) or divided by 74AC163 (if low)
4, 5	VCO range selection
6	PLL lock detect
7	Unused

Table 4: I²C control.

The lock output of the phase comparator is made available to the controller via the I²C bus.

NEXT MONTH

THE SYNTHESISER description continues next month with the construction, measurements, programming and alignment sections, and the components list.

REFERENCES

[13] H-mode mixer, 'Technical Topics', *RadCom* Sept 1998, p58.

[14] VCO design, 'Technical Topics', *RadCom* Feb 1996, Jan 1995, July 1994.

[15] Peter Martinez, G3PLX, p4.53, *Radio Communication Handbook*, 5th Ed RSGB.

[16] CDG2000 Part 1, *RadCom* June 2002.

[17] Use of PLL and DDS to reduce noise and avoid spurs, 'Technical Topics', *RadCom* Feb 1996, April 1996.

[18] AD9857 datasheet available from **www.analog.com**

[19] AR7030 review by Peter Hart, G3SJX, *RadCom* p44, July 1996.

[20] Datasheet for PCF8574 from **www.semiconductors.philips.com**

[21] Datasheet for 74HCT9046 from **www.semiconductors.philips.com**

[22] HSP45102 datasheet. ♦

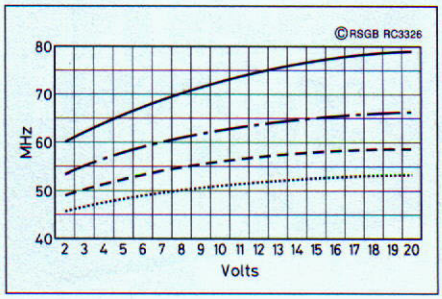


Fig 28: VCO tuning.

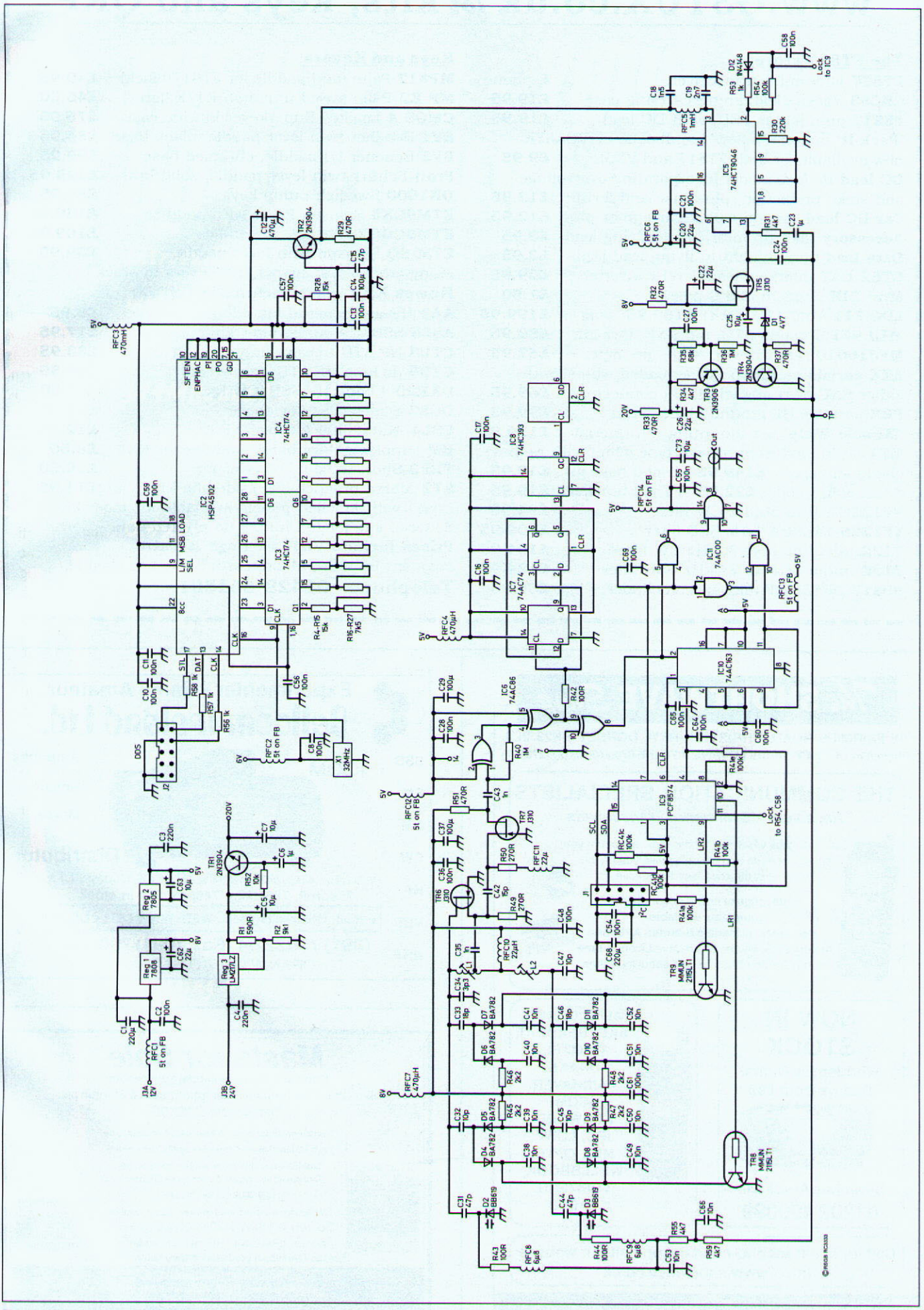


Fig 27: Full circuit diagram of the synthesiser.

THE CDG2000 HF TRANSCEIVER

Part six, by Colin Horrabin, G3SBI, Dave Roberts, G8KBB, and George Fare, G3OGQ *

CONSTRUCTION of the synthesiser is straightforward if a tad fiddly. The VCO is built mainly from surface-mount components on a section of the board with very fine tracking as can be seen in the photograph at the bottom right of p21 last month. The DAC R-2R ladder is also formed of surface mount components mounted closely together underneath IC3 and IC4.

The PCB is a single-sided board with a ground plane. The tracking is shown in **Fig 29** and the component layout in **Fig 30** (opposite). Drill the board and ensure that the diecast box can be fitted correctly. The idea is to drill four holes in the PCB corresponding to the four screw holes in the corners of the box. File off the lip on the edge of the box so that the screws are long enough to bolt the lid under the board, through the board, to the box on the top. Do not remove the lip of the lid, because the space it forms between the lid and the bottom of the board will contain the surface-mount components of the VCO. You will notice that there are several tracks that pass under the edge of the lid, and the lip of the lid may short these to ground. File a slot in the lip to clear these.

If you are mounting the board in a tin box, seam-solder it in – *but not until you have sorted out the apertures for the I²C and DDS buses, power and output signals.*

The board has been designed so that right-angle 10-way IDC connectors may be fitted such that they protrude slightly into the tinplate box. If you use a right-angle 10-way box header, check the orientation, as it may differ from the board layout shown. The best way of attaching the output signal is to drill a hole in the box above the output pad, take a small connector such as a PCB-mounting SMC, snip off the four ground pins and solder the connector flush to the surface of the box with the signal pin protruding into the enclosure through a hole. This can be seen on the right hand side in the first photograph last month. A short wire can later be used to connect it to the PCB. The power can be run either through two feedthrough capacitors into the box, or via a right-angled 3-way PCB connector. Referring again to last month's first photograph, a small heatsink can also be seen running from the two voltage regulators to the edge of the box. If a tinplate box is not used, an alternative means of heat removal must be employed.

All ICs may be mounted on turned-pin sockets with ground pins soldered direct to the ground plane or with standard sockets with pins to ground bent out at 90° and soldered to the ground plane.

Now assemble the VCO. Before assembling the rest of the circuitry, it is worth checking the VCO operation and putting it approximately on frequency. Make sure that the diodes are mounted the right way round. The two coils, two FETs and the 100µF capacitor are the only components mounted on the ground-plane side of the VCO.

The DDS, its clock and DAC should be assembled and tested next. To do this, you will need the controller or a test program that can configure the DDS chip. A clean sine wave between 90 and 150kHz should be obtained at the output of the low-pass filter (pin 3 of IC5) and the signal from the DAC itself should show no discontinuities that might indicate a fault in the R-2R ladder. In order to program the DDS, a 32-bit serial bit stream is clocked into the device and, when all 32 bits have been loaded, it is transferred to the accumulator latch using a single pulse on the load signal. This is shown in **Fig 31**.

Now assemble the remaining components. Check that all supply voltages are clean. Check that the VCO signal is being correctly buffered. In the absence of I²C, check that grounding the control lines from the PCF8574 (if used) correctly selects the VCO output or the VCO output divided by 2, 3, 4 or 5, and that the VCO control lines select the correct range. You can safely ground the output lines of the PCF8574 if fitted, as the output lines have high impedance pull-ups. In adjusting the VCO coils, keep the cores at about the same position in the formers as each other.

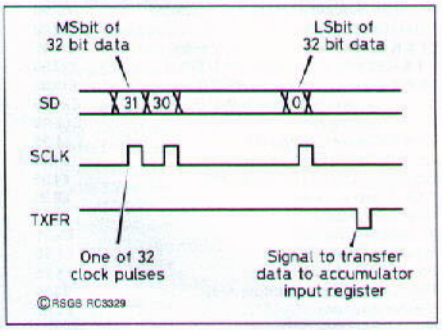


Fig 31: DDS programming.

In operation, the VCO tuning range should be from 3 to 18V (approx) according to band and frequency. Check all supply voltages with an oscilloscope. Apart from low levels of signal from the VCO (it gets everywhere), no signs of noise or instability should be found on any supply voltage or the VCO control line.

An indication of lock is found when small further adjustment of L1 and L2 shows no frequency change, even though the control voltage may continue to change.

MEASUREMENTS

UNLESS YOU POSSESS some really good test gear, measuring the VCO phase noise is best done using the completed receiver. A good way to do it is as follows (see **Fig 32**).

Two signal generators are used. One is a

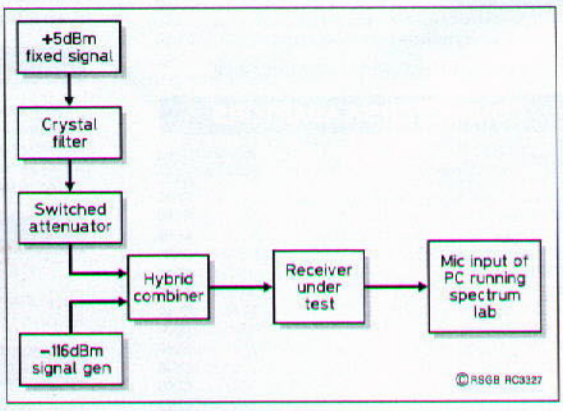


Fig 32: Phase noise measurement.

* *1 Old Hall Close, Higher Walton, Warrington WA4 6SZ.*

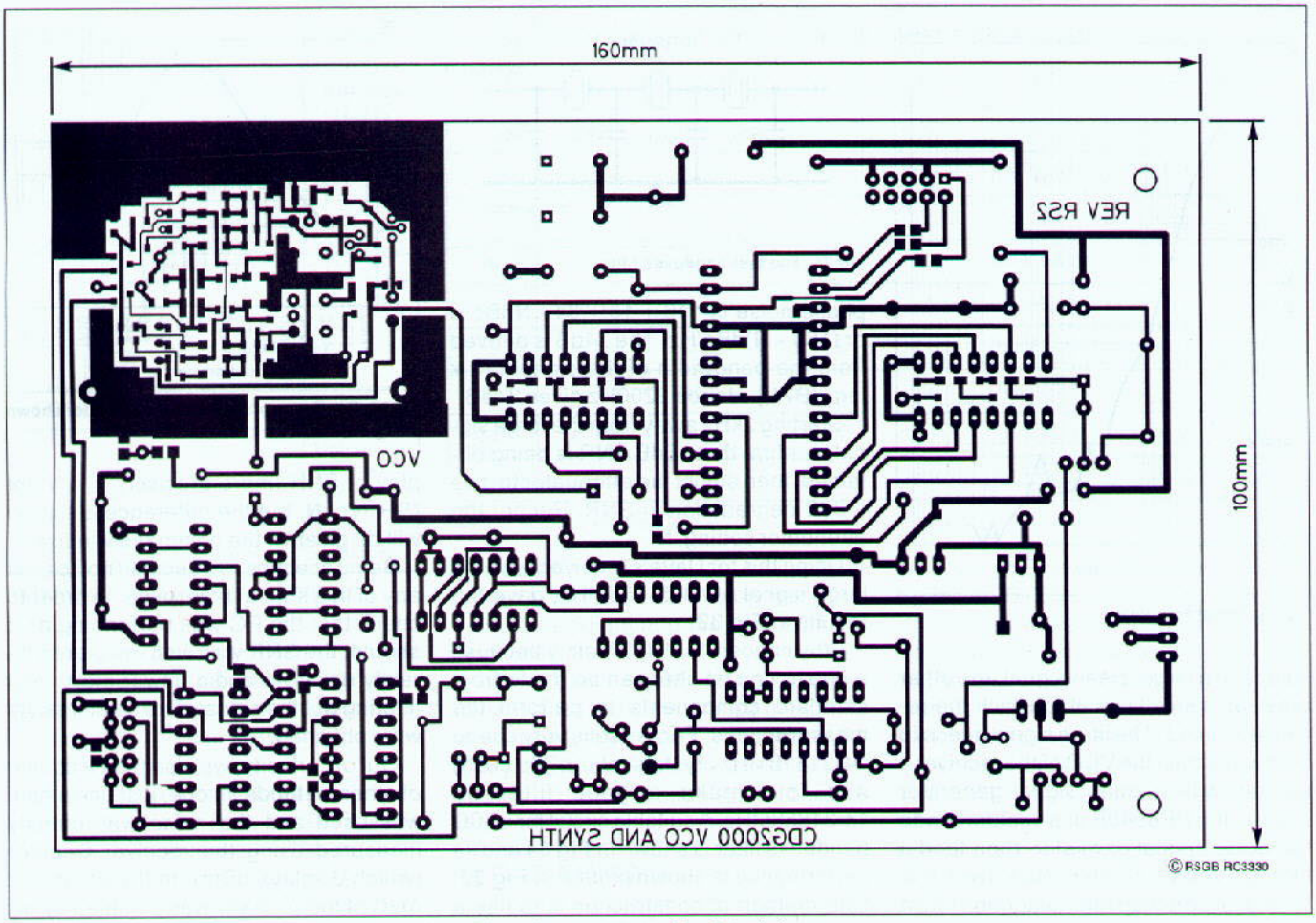


Fig 29: PCB tracking for the synthesiser board, viewed from the component side. Actual size.

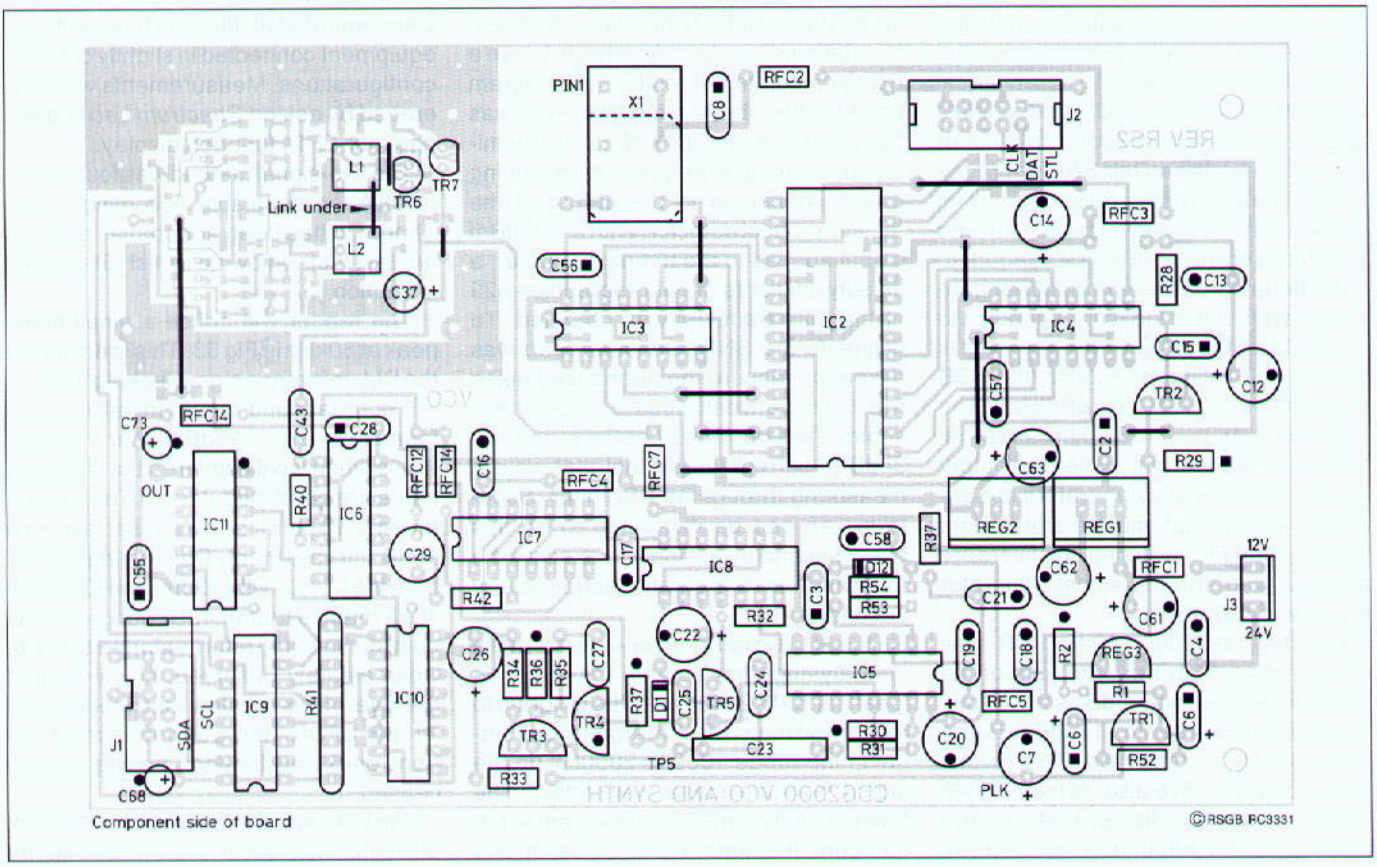


Fig 30: Component placement. Actual size.

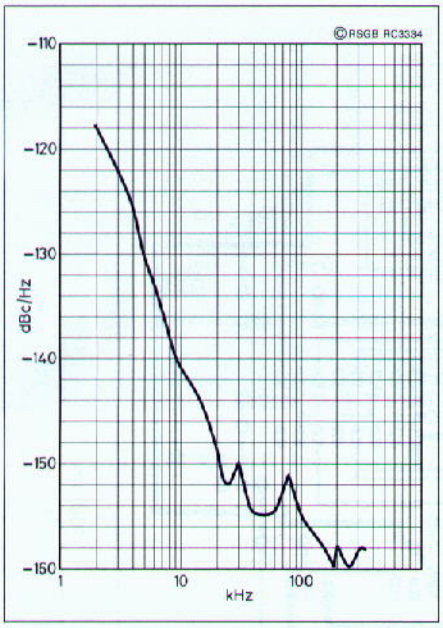


Fig 33: The phase noise.

source of a large, clean signal, the other provides a small signal to which the receiver is tuned. The large signal needs to be cleaner than the VCO of the receiver – so start with a clean signal generator such as the HP8640B or a custom-made low noise crystal oscillator, then feed it through a crystal filter. Now feed this through a switched attenuator and into a hybrid combiner. The other input to the combiner comes from the second signal generator. This configuration allows a small signal to be applied, such that a 10dB SNR can be created. When the 'large' signal is applied, it will cause the noise floor to be raised by reciprocal mixing between the VCO's phase noise and its own – hence it needs to be cleaner than the VCO. When the SNR degrades by 3dB, the noise due to reciprocal mixing equals that of the receiver noise floor and the phase noise (in dB) will be equal to the difference between the signal generator levels plus 10dB, corresponding to the 10dB of the SNR. If the receiver is using an SSB filter of 2.2kHz, the SSB phase noise of the VCO in dBc/Hz will be this value plus 34dB. The external attenuator is important – when the output levels of most signal generators are adjusted, it is not just passive attenuators that are changed; switched amplifiers are also involved and the signal generator noise level will change.

For the CDG2000, 10dB SNR was measured at -121dBm. The loss of the hybrid combiner was 5dB, so the low-level signal was set to -116dBm and a 10dB SNR was observed. The crystal filter had a loss of 5dB also, so the HP8640 output was set to +5dBm so that the large signal into the attenuator was 0dBm. Hence, for NdB of attenuation, the SSB

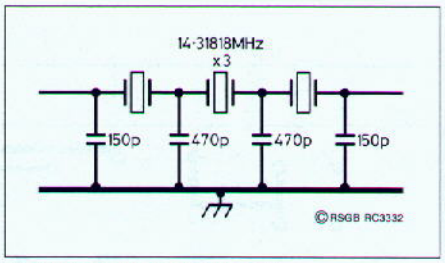


Fig 34: The test bandpass filter.

phase noise is 116 + 10 + 34 - NdBc/H or (160 - N)dBc/Hz. The 34dB is derived from the bandwidth of the signal (10 x $\log_{10}$(BW)). Hence 2200Hz gives 34dB.

Starting 2kHz away from the large signal, confirm that 10dB SNR is being obtained, then adjust the attenuator to give a 3dB degradation in SNR. Record the attenuator setting, N.

Doing this for Dave's receiver, with the large signal at 14.31858MHz, gave the results in **Fig 33**.

Why choose 14MHz? Mainly because a cheap crystal filter can be made from standard components to perform the measurements. Farnell sells very cheap 14.31818MHz crystals (about 70p each) and four make a good filter on 14.31858MHz. A suitable circuit for a 50Ω bandpass filter is shown in **Fig 34** and its performance is shown plotted in **Fig 35**. One method of construction is to use a small diecast box with BNC connectors at each end.

This begs the question of how to measure SNR. One way is to use an audio 'true' power meter to measure the noise from the audio output. Another is to use a PC to calculate it directly. The program used for the above measurements was *Spectrum Lab* by DL4YHF [23]. The microphone input of the sound card running it was connected to the output of the receive product detector. With a -116dBm signal applied to the hybrid combiner, a display similar to the photograph on p29 of the July *RadCom* was obtained. To calculate the SNR, *Spectrum Lab* was asked to measure the normalised noise (dB / Hz) between 1000 and 2000 Hz, subtract this from the signal level and add 34dB to correct for the fact that we are measuring through an SSB filter. *Spectrum Lab* can be instructed to do this every second by asking it to execute the following as a periodic action every second:

print(peak_a(1000,2000)-34-noise_n(1000,2000))

Analysing the above, the function 'peak_a(1000,2000)' asks the program to locate and measure the largest peak signal in the range 1000 to 2000Hz (ie the signal from the signal generator). The function 'noise_n(1000,2000)' asks it to measure the normalised noise in this range, ignoring the signal. A direct dis-

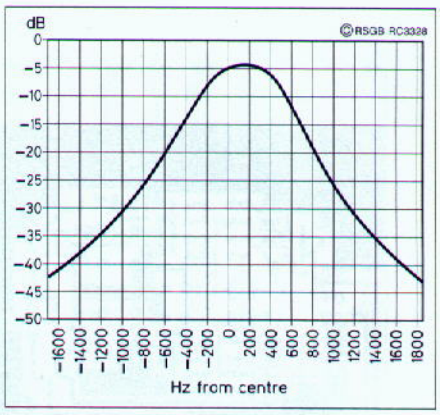


Fig 35: Response of the 14.31858MHz filter shown in Fig 34.

play of SNR (more precisely, S / N *not* (S + N) / N, but the difference is minor) will be given in the command window.

Being sceptics, we decided not to trust any of this stuff at face value. In order to check that the PC was performing as it should, the SNR was also measured directly using an audio power meter and filtering out the signal. The same results were obtained.

Out of curiosity, we also tried a couple of other methods. In one, just one signal was used and the noise was directly measured using the receiver S-meter (which displays dBm). In the other, the AGC of the receiver was disabled by removing the two CA3046 chips and the log output of the IF again used to measure the signal. In all cases, the results were within 3dB of each other. Measurements were repeated at different times with the equipment connected in slightly different configurations. Measurements were averaged by asking *Spectrum Lab* to average four FFTs for each display.

The two-signal method was found to be reliable and repeatable. According to John Thorpe, it has been adopted as a standard test method by the British Standards Institution.

The reader will notice a small noise peak at 80kHz in Fig 33. This is not due to the PLL reference signal leaking through – it is broadband noise. Initially, it was found to be some 15dB higher in level – this is when we discovered that AC logic gates are good modulators! The capacitor on IC10 pins 1 and 3 caused almost a 10dB improvement. Decoupling the 5V from the I²C bus with 220µF and IC11 with 10µF made a further 4dB change. At this point diminishing returns started to set in. Colin astutely observed, however, that the level of this is below that needed for a 113dB SFDR (the performance of the front end) and fruitless poking around ceased.

The PLL reference frequency does leak through, but its level is low (between -90 and -107dBc). Higher gain in the loop

Bit(s)	Function	Setting for 14MHz band
0, 1	Set 74AC163 divide ratio from 2 (both high) to 5 (both low)	N/A
2	If low, hold 74AC163 reset when not being used	Low
3	Select direct output of VCO (if high) or divided by 74AC163 (if low)	High
4, 5	VCO range selection	Both high
6	PLL lock detect	High so controller can read it
7	Unused	Not applicable

Table 6: VCO configuration for 14MHz.

Band (MHz)	VCO range (MHz)		Rx LO (MHz)		DDS setting (Hex)		Control word
	Min	Max	Min	Max	Min	Max	
1.8	64.800	66.000	10.800	11.000	01033333	01080000	C4
3.5	75.000	76.800	12.500	12.800	012C0000	01333334	C4
7	64.000	64.400	16.000	16.100	01000000	0101999A	C5
10	76.400	76.600	19.100	19.150	01319999	01326667	C5
14	46.000	46.700	23.000	23.350	00B80000	00BACCCD	F8
18	54.136	54.336	27.068	27.168	00D88B43	00D95811	D8
21	60.000	60.900	30.000	30.450	00F00000	00F3999A	E8
24	67.600	68.000	33.800	34.000	010E6666	01100000	C8
28	74.000	78.000	37.000	39.000	01280000	01380000	C8

Table 7: Settings by band.

amplifier, or changing the PLL divider ratio from 512 to 256 and doubling the DDS output frequencies might help, but it is low enough already not to be worrysome.

Some other remarks about noise need to be made. Noise from the DDS leaks out – there are several small spurii on all bands, some of which are obviously DDS-related, as they tune at different 'rates'. The series resistors in the input control lines to the DDS from the controller reduce leakage through that port. Noise from outside will leak in – for example, in Dave's model the LCD display was lit by a CCFL backlight and the inverter for it modulated the VCO.

One spurious signal that could annoy some is caused by the choice of 32MHz as the reference clock – it causes an S4 spur just above 14MHz – obvious with hindsight. It is just a couple of kHz above the band edge.

PROGRAMMING

PROGRAMMING THE SYNTHESISER is straightforward. For a given band such as 14MHz, the band edges are 14,000 and 14,350kHz. With the local oscillator on the high side, it needs to be 9MHz higher, or 23,000 to 23,350kHz. The mixer is driven at twice this frequency so the synthesiser needs to deliver 46,000 to 46,700kHz. From Fig 3, the VCO range needed will be the lowest one with both switched capacitors in circuit, so the two switching transistors must be on (bases driven high). No additional division of the VCO frequency is needed, so the AC163 needs to be held reset and the multiplexer needs to be set for direct output. Combining this data, the settings for the output of the PCF8574 need to be as shown in **Table 6**.

In binary, MSbit first, the required set-

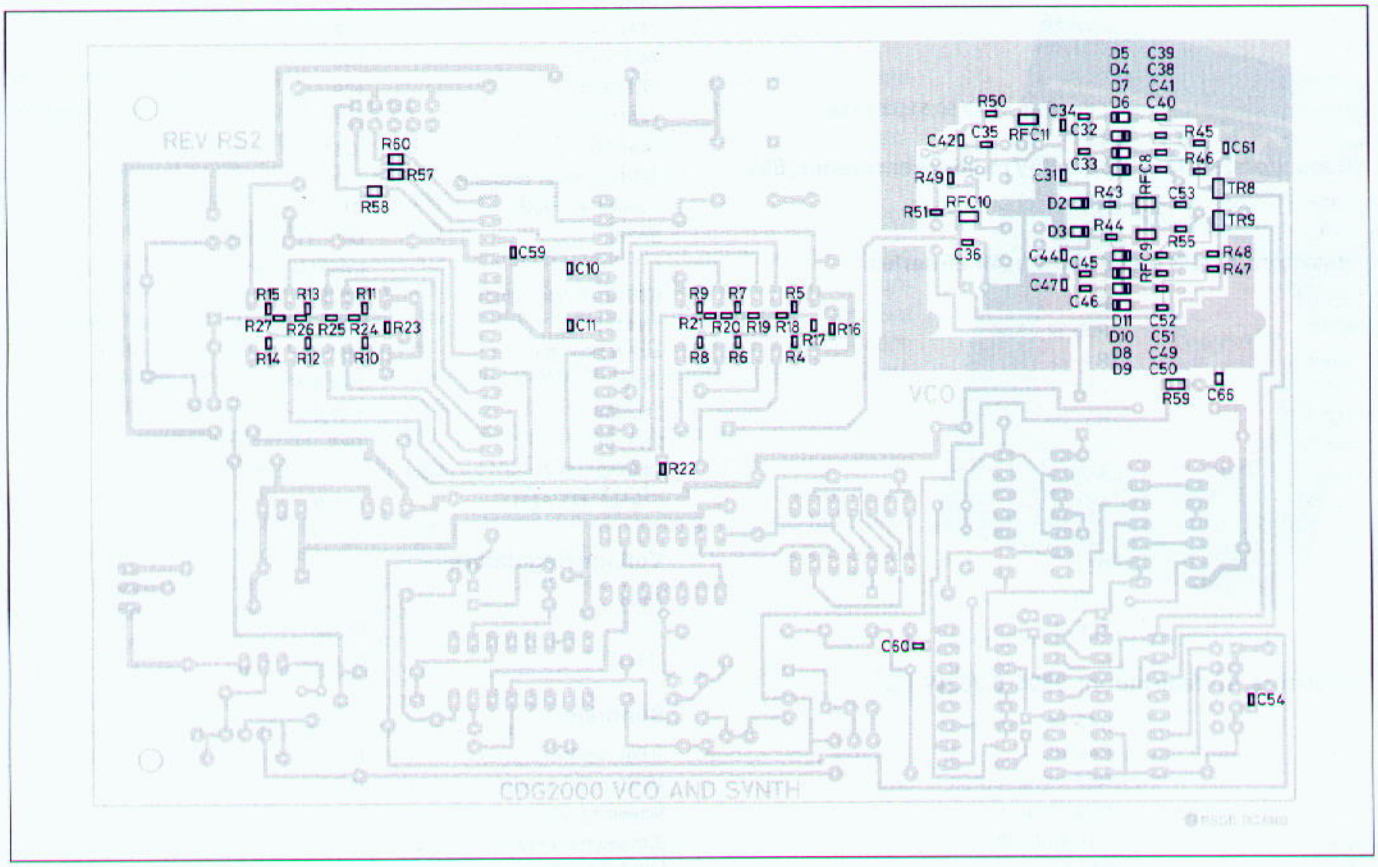


Fig 36: Component layout *on the track side*. See the third photograph on p21 last month.

ting would be x111 10xx where 'x' denotes any value. On the basis that the troublesome modulators called AC logic devices should have pins driven by a low impedance, and that the unused bit 7 might as well be high, the setting should be 1111 1000, or in hex notation, 0xF8.

The DDS needs to deliver an appropriate frequency for phase-locking and, as the PLL divisor is 512, the DDS needs to deliver 89.84375 to 91.2109375kHz.

The way that a DDS works is that, for a clock frequency of f_cHz, with a 32-bit accumulator, to deliver an output of f_0Hz, the DDS register should be set to

$$2^{32} \times \frac{f_0}{f_c}.$$

Hex notation is easiest here so, for the range stated above, with a 32MHz clock the DDS needs to be set to values in the range 0x00B80000 to 0x00BACCCD. Note also that, with a 32MHz clock, the smallest DDS step would be

$$\frac{32 \times 10^6}{2^{32}} \approx 0.00745\text{Hz}.$$

The divide-by-512 'multiplies' this into a smallest tuning step of 3.8 Hz. Fig 31 shows the way the data is sent to the DDS.

One thing to note. When the AC163

COMPONENTS LIST FOR THE SYNTHESISER

Capacitors

47p	ceramic plate	C15
1n	multi-layer ceramic	C43
1n5	polystyrene	C18
2n7	polystyrene	C19
100n	multi-layer ceramic	C2,8,13,16,17,21,27 28,55,56,57,58,64,65,69
100n	polyester	C24
220n	multi layer ceramic	C3,4
1µF	polyester	C23
1µF	16V tantalum	C6
10µF	16V tantalum	C5,7,25,63,73
22µF	16V tantalum	C20,22,26,62
100µF	16V tantalum	C14,29,37
220µF	16V tantalum	C1,68
470µF	16V tantalum	C12

Capacitors, surface mount 0805 NPO (COG)

3p3	C34
10p	C32,45,47
15p	C42
18p	C33,46
47p	C31,44
1n	C35
10n	C38,39,40,41,49,50,51,52,53,66

Capacitors, surface mount Y5V multi-layer ceramic, 50V

100n	C10,11,36,54,59,60,61

Resistors, 0.25W metal film 1%, MF25 series

100R	R42
470R	R29,32,33,37
590R	R1
1k	R53
4k7	R31,34
9k1	R2
10k	R52
15k	R28
68k	R35
100k	R54
220k	R30
1M	R36,40

Resistors, surface mount 0805 0.063W 1%

100R	R43,44
270R	R49,50
470R	R51
1k	R56,57,58
2k2	R45,46,47,48
4k7	R55,59

Resistors, surface mount 0805 0.1% 10ppm/°C

7k5 (Farnell 554 844)	R16 - 27
15k (Farnell 555 137)	R4 - 15

Resistors SIL pack

100k	R41A - E

Inductors

6µ8 SMC (Farnell 200 542)	RFC8,9
22µH SMC (Farnell 200 578)	RFC10,11
470µH axial (DC 4Ω max)	RFC3,4,7
1mH axial (DC 4Ω max)	RFC5
TOKO A700 9550W custom	L1,2 (limited supplies available from G3OGQ, £1.20each)
5 turns 30SWG enam on F bead	RFC1,2,6,12,13,14

Semiconductors

HSP45102	IC2
74HC174	IC3,4
74HCT9046 (Quarndon)	IC5
74AC86	IC6
74AC74	IC7
74HC393	IC8
PCF8574	IC9
74AC163	IC10
74AC00	IC11
32MHz crystal oscillator (Farnell 221 685)	X1
BA782	D4 - 11 (limited supplies available from G3OGQ, £1.10 each)
BB619 (Electrovalue)	D2,3
1N4148	D12
4V7 0.25W Zener	D1
J310	TR5,6,7
2N3904	TR1,2,4
2N3906	TR3
MMUN2115LT1 SOT23 digital (Farnell 473 625)	TR8,9

Voltage Regulators

7808	REG1
7805	REG2
LM217LZ	REG3

Sundries

3 Pin header	J3
10 Way IDC header	J1,2
Screening Box (Eddystone 11451P with M3.5 x 16 long screws)	1 off

divider is used, the tuning rate changes and the controller needs to take account of this to maintain the same tuning rate on each band.

For the amateur bands, the values are shown in **Table 7**, assuming a 32MHz clock.

The CDG2000 software needs to be configured for the DDS clock and band settings, hence no fine adjustment of its frequency is needed. Indeed, as all parameters are configurable, it will cope with any DDS clock and band settings without the need to modify the software.

ALIGNMENT

THERE'S NOT MUCH to say here. There are only two things to adjust – the VCO coils. Basically, ensure that the voltage swing across all bands keeps away from voltage rails. This can be monitored at TP. Calibration for the DDS clock frequency is achieved in software on the CDG2000 controller, as are the control latch settings, band edge limits and tuning rate. This is covered in the controller user guide.

COMPONENT AVAILABILITY

MOST OF THE components in the synthesiser are readily available from suppliers such as Farnell. Some, however, are harder to find. The DDS chip is stocked by RS Components. The 74HCT9046 is available from Quarndon [24]. The PIN diodes used are becoming hard to find - any similar type of VHF bandswitching diodes (R_{on} = 0.6Ω at 3 - 4mA) will do just fine. A limited quantity of the specified diodes is available from the authors. The only hard part to find is the coil in the VCO. Two identical coils are needed. The AR7030 used custom-made coils and the special part number is given. A limited quantity is available from the authors (see the Components List on p24).

One thing to be borne in mind. Where 74AC logic is used, we mean it - don't try to use 74HC logic as, quite simply, it ain't up to it. Similarly, where 74HC logic is specified, don't use 74AC logic.

ACKNOWLEDGEMENT

OUR THANKS must go to Mark Sumner of AOR UK and to John Thorpe for the VCO coils and their support for the project.

NEXT MONTH

THE CONTROLLER is the last unit of CDG2000 to be described at length in this series. It manages all aspects of the transceiver.

REFERENCES

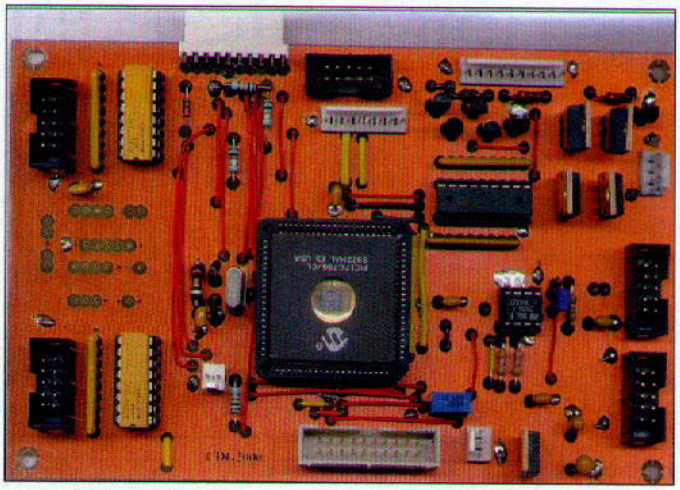
[23] Use of DL4YHF *Spectrum Lab* program also described in *RadCom* July 2002 pp24, 29.

[24] Quarndon, Slack Lane, Derby DE22 3ED. Tel: 01332 332 651. ♦

THE CQG2000 HF TRANSCEIVER

Final part, by Colin Horrabin, G3SBI, Dave Roberts, G8KBB, and George Fare, G3OGQ *

THE CONTROLLER is designed to manage all aspects of the transceiver. It provides two VFOs, manages the user interface and controls all functions of the rig. It handles transmit / receive switching and provides an automatic keyer. It can be seen in this photograph.



The controller PCB.

As you may remember from the first part of this series, the three transceivers built so far have differed widely in their interfaces. Dave wanted a minimalist design with 'soft' buttons and a single rotary control. This was anathema to George who wanted separate controls for each major function. Colin's design fell somewhere in between.

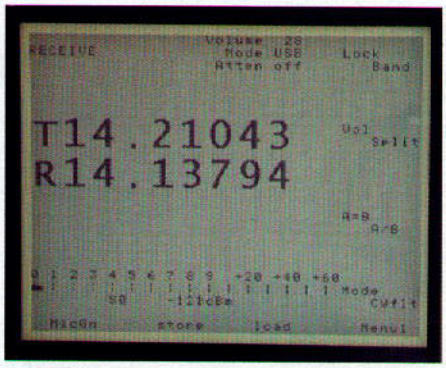
In consequence of these widely differing requirements, the controller needed to be highly configurable. It can support the following user interface options:

- up to 32 push-buttons in two scanned banks that can be soft-programmed;
- 1 or 2 rotary controls (shaft encoders);
- 20 x 2 or 40 x 4 alphanumeric displays or
- 320 x 240 graphics displays.

In addition it possesses:

- an I²C bus to control the transceiver;
- dual DDS control interface;
- a PTT input;
- a keyer input;
- analogue inputs for S-meter and power meter functions;
- switched 12V outputs for transmit / receive and mode control;
- an in-circuit programming interface;
- an RS232 interface.

All push-buttons are 'soft'-controlled. When first switched on, the buttons have no effect. Holding one down for more than five seconds, however, allows the button to be programmed to one of a large number of functions by means of the main tuning control. Releasing the button stores that button's function in non-volatile memory. It will retain that function when switched off. When the graphics display version is used, the function associated with a button is displayed in an on-screen menu close to the button, and



The display.

the functions may change with selectable menus. The photograph above shows this.

Almost all operational parameters are configurable - the DDS frequency, the band details, the VCO and relay control data, etc. Those that cannot be configured can be altered by rebuilding the software.

The software is written in PIC assembler, and the full source code is available for amateur use from the Internet [25] together with a User Guide and pre-built executables for our configurations. The PIC may be programmed in circuit in the controller by means of a small interface board plugged into the parallel port of a PC if a dedicated PIC programmer is not available.

THE CIRCUIT

THE CIRCUIT DIAGRAM of the controller is shown in **Figs 37, 38** and **39**. The heart of the controller is a PIC micro - the PIC17C766. This is a 'high end' processor in an 84-pin chip

Connector	Usage
P1	Future RS232 interface
JP1	IF log amp (S-meter) & power meter inputs and keyer input
JP2	DDS bus - drives 1 or 2 DDS devices
JP3	I²C bus.
JP4	Switched 12V
JP5	LCD connector
JP6	Opto switches
JP7	Switch matrix input 2
JP8	Switch matrix input 1
JP9	Power to the controller (+12V and whatever negative voltage the LCD & RS232 need)
JP10	In-circuit serial programming interface.
JP11	Write protect configuration data in EEPROM.
JP12	Unused and not fitted - future interrupt input from I²C
JP13	Incoming 12V to the FET switches
JP14	Push to talk. Ground for transmit

Table 8: Interfaces to the controller.

carrier with a rich set of interface devices [26].

Several interfaces to the controller are provided – these are summarised below in **Table 8**.

Close-up of the S-meter.

JP1 provides two analogue inputs and also carries the keyer lines. The analogue inputs are used for the on-screen S-meter and transmitter power meters. Each requires an analogue voltage in the range 0 to 4V and the software allows it to be converted into an accurate S-meter which will also display a text reading in S points and dBm. An example is shown in the photograph, above right. If the on-screen S-meter is not used, the controller can instead provide a DC voltage that is controllable by software and reflects the attenuator and band settings so that an analogue S-meter can be corrected automatically to read true values regardless of receiver configuration.

JP2 allows the controller to manage the Direct Digital Synthesiser that provides frequency control. In fact, support for 2 DDS chips is provided, but only one is used at present. There is a common serial data / clock interface and two separate load signals.

JP3 is the I²C bus that controls the transceiver. An overview of I²C will be given later but, in summary, it is a two-wire bus that allows the controller to read from and write to a number of devices that are all connected in parallel on the two-wire bus. The detailed circuit diagram shows it on a 10-way connector, with multiple ground and power lines. The keyer lines are also connected to the bus for convenience. The I²C bus also controls an EEPROM on the controller board that provides non-volatile storage for the rig.

JP4, 9 and 13 are concerned with power. JP9 provides power to the controller itself – a voltage sufficient for the 5V regulator plus a negative voltage for the LCD if required. JP13 provides a high current +12V feed to a set of FET switches. These are controlled by the processor and provide switched voltages on JP4, allowing the processor to switch on and off 12V supplies on transmit and receive, as well as controlling other functions as required. The two main outputs for transmit and receive power have active pull-downs to reduce leakage into the circuits when off.

The display is connected to JP5. A wide range of displays can be used provided that each employs an 8-bit parallel bus interface. In George's transceiver, this is a 4-line 40-character alphanumeric display based on the industry standard HD44780 controller. In Dave's it is a 320 x 240 pixel, ¼ VGA graphics panel with a CCFL backlight. Colin's uses the Hitachi HD61830.

JP6 connects to one or two shaft encoders. These are used to provide main tuning and other functions and are quadrature signal devices with two signals from each that allow the controller to read the speed, direction and amount of rotation of each.

Keyboard scanning is provided on JP7 and JP8. The software assumes a 4 x 4 matrix on each port as shown in **Fig 40** providing 32 switches. Not all have to be used. Every 1ms or 2ms (this is configurable), a scan line is pulled low and the state of the switches for the previous scan line low is stored. This means that, within each 10ms period, all 32 switches are scanned. The scan speed is low, so if the lines connecting keyboard to controller are long they can be heavily filtered. Note that series resistors and pull-ups are provided to facilitate this.

Apart from the LCD display updating (and the LCD itself), the controller is very quiet electrically. It has a 32MHz clock which is provided by a crystal connected directly to the PIC and no external bus on which digital signals are changing unless an update to a peripheral is requested.

I²C BUS OVERVIEW

A FULL DESCRIPTION of I²C bus is beyond the space available here. Detailed information is to be found from Philips who invented it [27] and a good description is presented in the PIC17C766 datasheet [26]. In summary, it is a two-wire bus where a master provides a clock for a number of slave devices and the master and slaves communicate by means of a single data line. It is possible to have multiple-bus masters in I²C, but that option is not used here – the controller is the master. The bus operates at 100kHz. Faster modes are possible, but not necessary. The slow speed also means that the I²C bus cable can be up to 6 feet long (but keep it as short as practicable). Each device on the bus has its own address, and **Table 9** shows the addresses in use at the moment for CDG2000. When the controller wishes to address a device, it sends a START signal by pulling low the data line whilst clock is high. When it has finished, it signals a STOP by raising data whilst clock is high. This is shown in **Fig 41**. Having sent a START, it sends the slave address of the device it wishes to communicate with, with the last bit denoting a read or a write. The slave then acknowledges the request by sending back an ACK (pulls data low whilst clock goes high then low). What happens next depends on the type of peripheral. For the simple PCF8574 [28] latches, data are then sent or received next. For more complex devices such as the EEPROM, a sub-address is sent first.

By the way, an I²C bus is used by the SDRAMs you probably have in your PC to communicate with the chipset – ever wondered how the motherboard magically knows the size and type of memory you

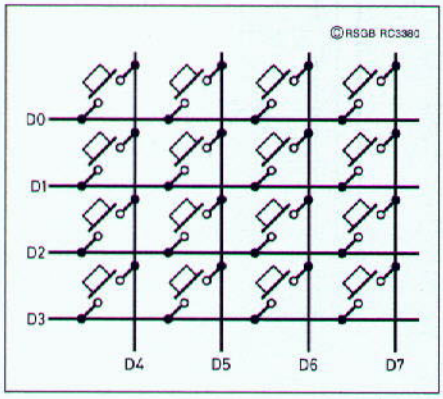


Fig 40: The switch scan circuit.

Address range	Device	Usage
A0-AF	ST24C16	EEPROM
54-55	MAX521	8 analogue outputs
5A-5B	DS1807	Ch A=mic gain Ch B=af gain
5C-5D	DS1807	Ch A=VOX gain Ch B=anti-VOX
4E-4F	PCF8574	Band switch for LPF
4A-4B	PCF8574	VCO control
48-49	PCF8574	Secondary band switch for LPF
46-47	PCF8574	DSP Control
44-45	PCF8574	First band switch on front-end board
42-43	PCF8574	Second band switch on front-end

Table 9: I²C device address map.

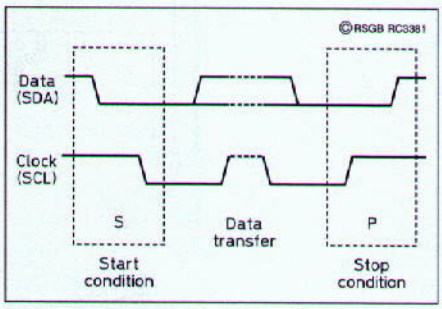


Fig 41: I²C start and stop.

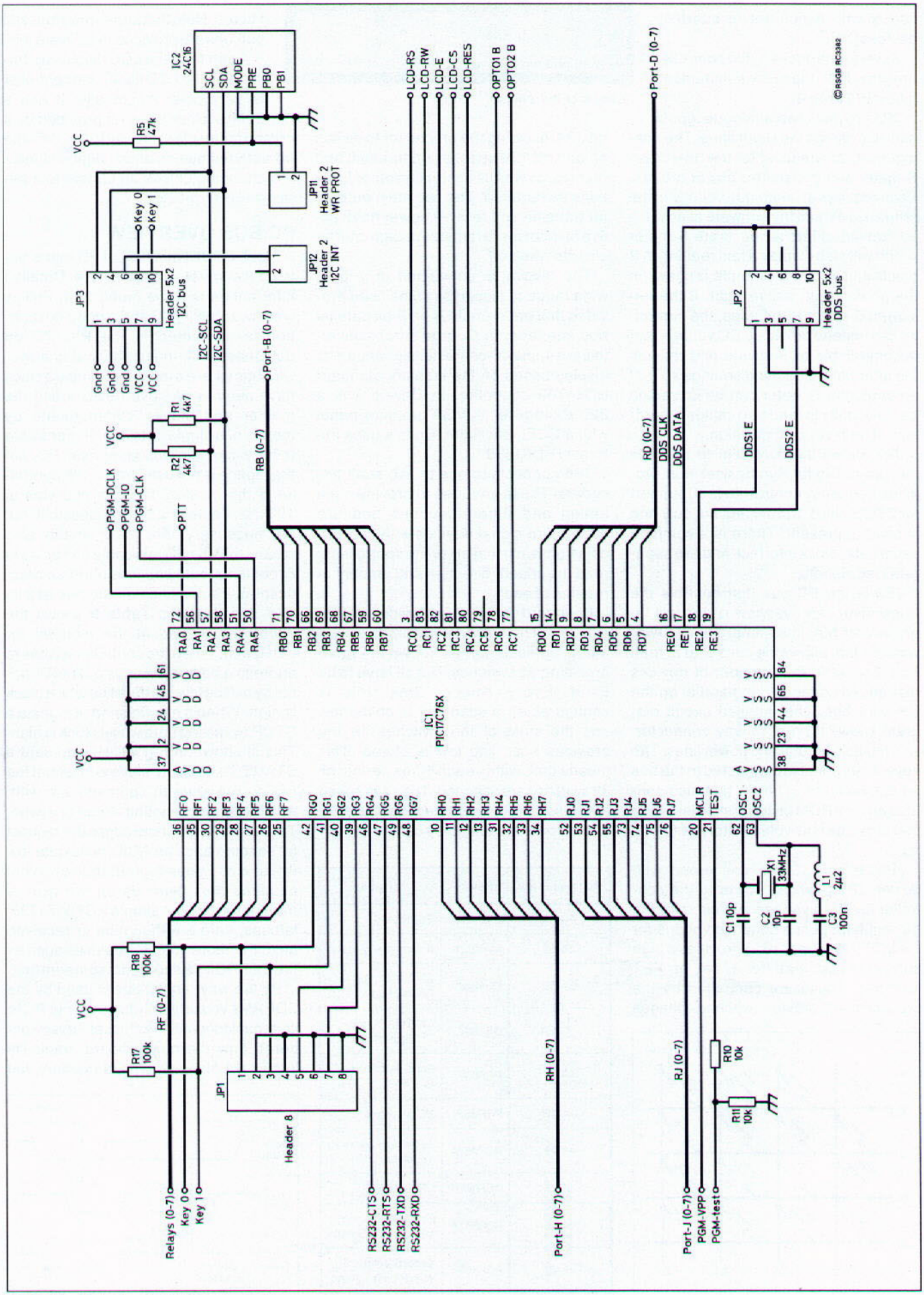


Fig 37: The Controller circuit diagram - part 1.

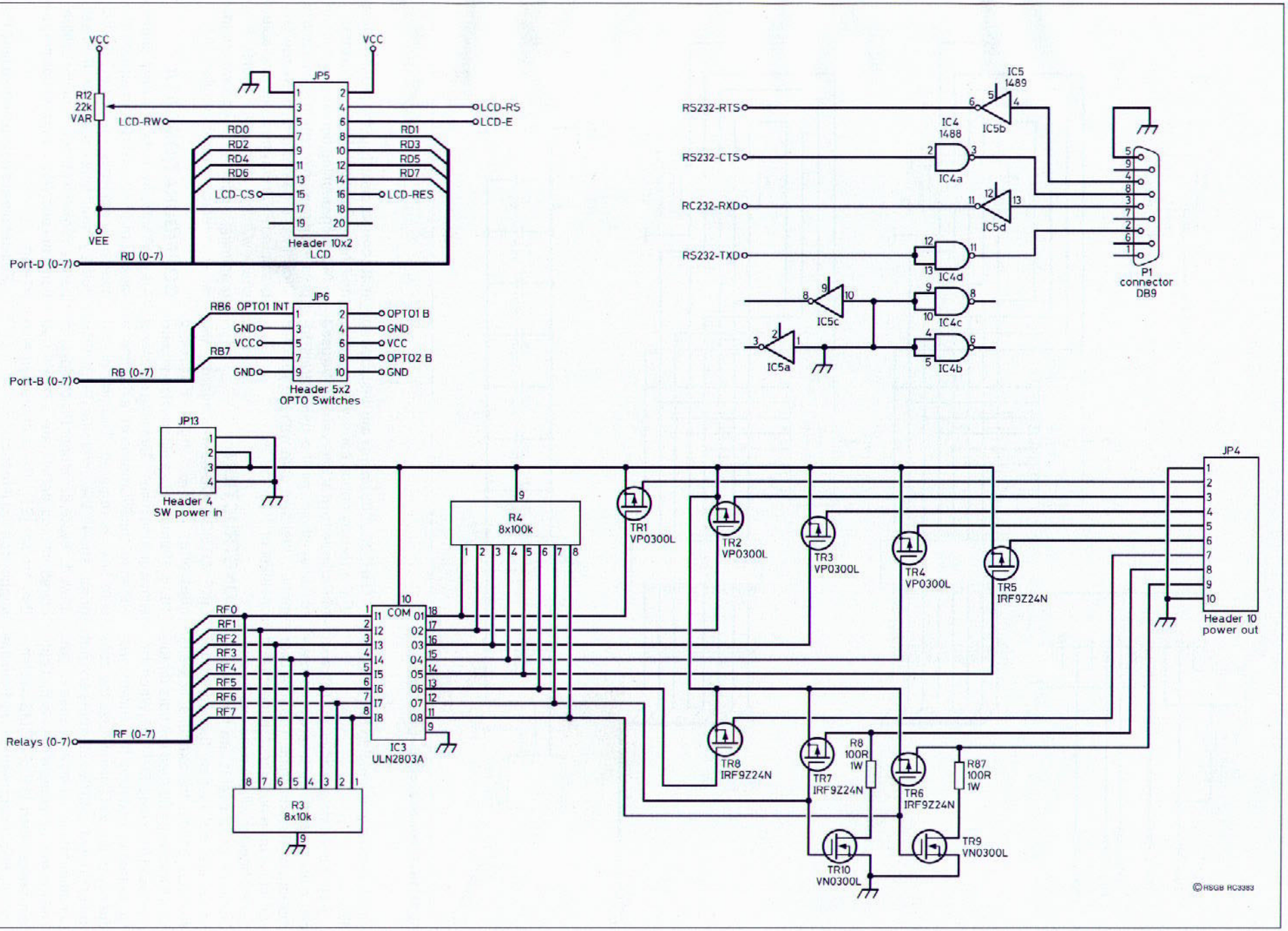


Fig 38: The Controller circuit diagram - part 2.

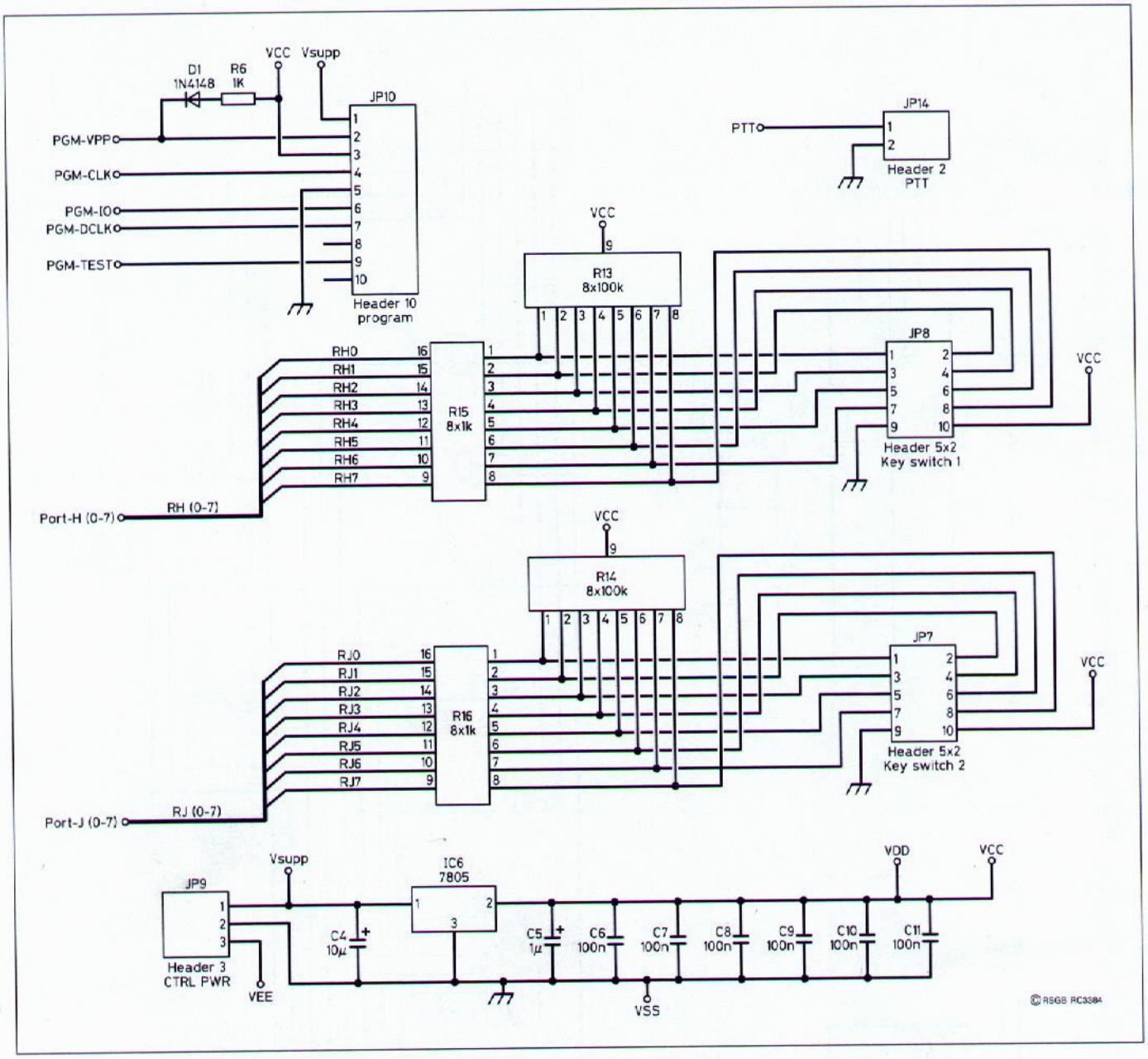


Fig 39: The Controller circuit diagram - part 3.

install without you needing to configure it?

As has been stated earlier, the I²C process in the controller software is an interrupt-driven state machine. The controller can 'stack up' a number of requests that the I²C handler will process one by one. Some of these events are time-critical some are not. When the controller switches bands, for example, it waits until it knows it has read the data for the new band from the EEPROM. When it is, for example, updating the current frequency of the VFO, it instructs the controller to have up to five attempts and not to bother telling it if it succeeded or not. The reason for multiple tries is that certain devices such as EEPROMS can temporarily disconnect themselves from the bus if they are busy writing to non-volatile storage.

The CDG2000 boards are designed so that a 10-way ribbon cable with connectors crimped to it at intervals can be used to 'daisy-chain' all the peripherals together. Just take care with the sockets' orientation!

CONSTRUCTION

LIKE OTHER CDG2000 boards, the controller is a single Eurocard 160 x 100mm. It is a single-sided board with a ground plane. Given the density of wiring for the PIC however, a number of wire links is required. The first photograph shows the controller PCB. PCB artwork, layout, component lists and other constructional details are available on the Internet [25]. The authors can also supply it on CD if required.

Construction is straightforward – the main things to take care with are the pins that connect directly to the ground plane and the orientation of the connectors.

Full programming details are also not presented here. A program is available to allow this to be performed. Ready-programmed PICs may be made available – check with the authors for details. Programming is effected using a small interface connected to the controller.

CONFIGURATION DATA

AS A MINIMUM of data is hard coded, most data items can be changed from the screen. Specifically, the actual DDS frequency, band limits, step rate, IF offset, per-band relay settings, S-meter calibration, data and VCO control words may be altered.

Full details are not presented here but are in the User Guide [25]. In order to facilitate setting the data, a spreadsheet

is available to calculate all the nasty hex values that must be entered for a specific clock frequency and band configuration.

SOFTWARE INTERNALS

INTERNALLY, THE CPU operates on 1ms, 10ms and 1s cycles. Every second millisecond, the push-button scan is advanced and the PTT line is debounced. Both are debounced digitally to avoid transient effects and the results are made available for the 10ms process. Every 10ms, the core events are processed in sequence; all push-button events are handled, the transmit / receive and keyer finite-state machines are executed, the display is updated and any required peripheral events are initiated. Every second, EEPROM data-writes occur if required and miscellaneous events such as controlling the LCD backlight are processed.

Interrupts are used for the following:

- PTT line changes;
- opto shaft encoder events;
- I²C event interrupts;
- 1ms core clock events.

I²C activity is controlled by a background-interrupt-driven finite-state machine. When the main processes want to request I²C activity, they locate a free buffer, define the required activity by setting the buffer, and then pass it to the event handler.

Concern has been raised over the responsiveness of PIC processors when used for tuning control and display-frequency update [29] and the use of dual PICs has been suggested. This is avoided here by virtue of the interrupt handling of opto events and the 10ms main event loop. If an alphanumeric display is used, frequency updates on the screen take under 7ms. When a graphics display is used it takes between 18 and 21ms, well over the 10ms loop time. This has no effect, however, on performance, as interrupt-collected tuning events are accumulated and handled within the main loop (in this case, every msec when the frequency is changed, 10ms otherwise) so that it remains responsive without losing pulses. No detrimental effect will be noticed in use.

All band data and related parameters are stored in the EEPROM. On first use, however, there is no need to pre-configure the EEPROM. Critical data is checksummed and, if the data read does not pass checking, it is rejected and data from the EPROM memory of the PIC is used instead. If a change is made to the data, the updated values are written back to EEPROM to be read next time they are needed. It is also possible to ask the controller to reinitialise the data from EPROM.

REFERENCES

[25] Warrington ARC www.warc.org.uk

[26] Microchip PIC17C766 datasheet, reference DS30289A from www. microchip.com

[27] Philips I²C bus information from www.semiconductors.philips.com/i2c

[28] PCF8574 datasheet from www.semiconductors.philips.com

[29] Use of PICs in DDS designs, 'Technical Topics', *RadCom* January 2001, p61.

AND FINALLY...

THIS IS THE END of the series, which has concentrated on the receiver. Transmit modules and expanded information on the controller and receiver are contained on a CD-ROM now available from G3OGQ at £3.50 inclusive. In response to many requests, a PCB for the front-end is also now available and further boards are in preparation. Watch the Warrington ARC website [25] for updates which will appear from time to time. ♦