

The *Star-10* Transceiver — Part 2

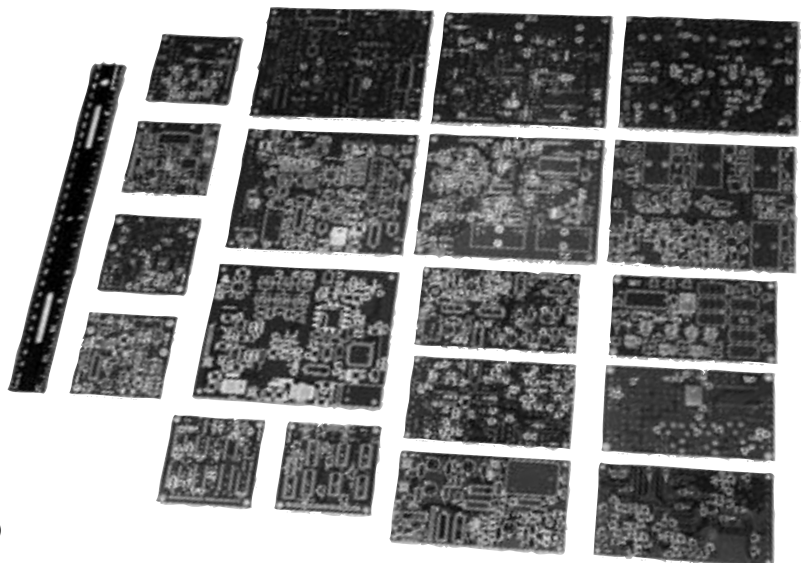
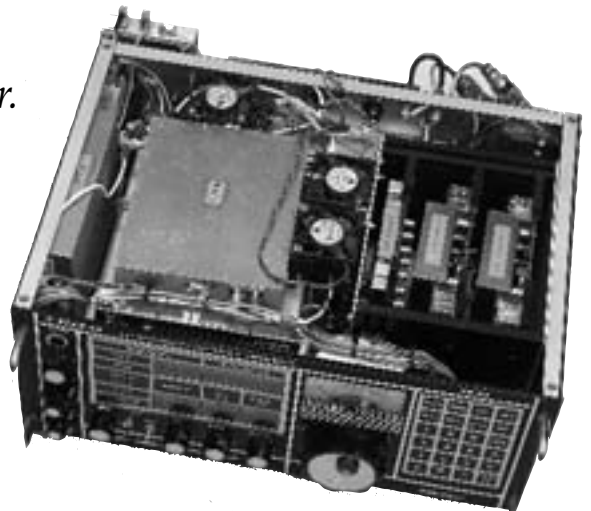
In Part 2 of this series we will look at some of the circuits used in this high-performance transceiver.

Mission — The *Star-10* transceiver has been a unique research experience into understanding what can be done from the laws-of-physics point of view in receiver and transceiver dynamic range performance. This research has been performed over a period of five years with parts, technologies and packaging means available to me at the time. The transceiver has been implemented with some unique parts that may no longer be available. The *Star-10* development has been a purely scientific endeavor intended primarily to understand what could be done to achieve ultimate receiver performance. Although the results have been outstanding, slightly better results may be possible using newer technologies and parts. The *Star-10* project was not intended as a commercial product. Its duplication is probably not economically feasible.

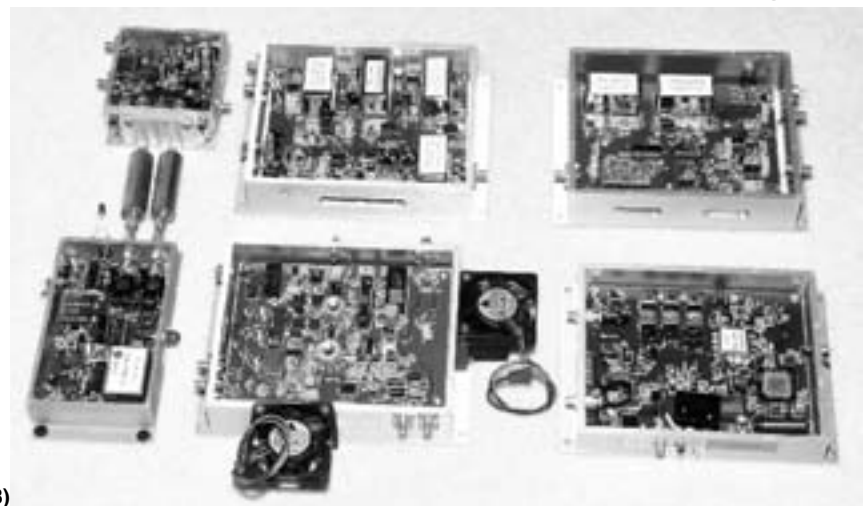
Introduction

In Part 1 of this series, I presented a system design criteria for a modern double conversion transceiver, namely the *Star-10*. The primary goal of this design was to produce a continuous HF coverage system with consistent high dynamic range receiver performance over the entire frequency range of 1.8 MHz to 30 MHz. I wanted to build a radio that rivals the performance of today's top-of-the-line equipment. The focus was how to design a no-compromise broadband radio, obtaining superior performance without resorting to a channelized, amateur-band-only design. The accent was put on good image and spurious rejection, using an up convert/down convert design, ample

Visible from the left are the FSYNTH assembly (left side panel), the IF75BC assembly (top left), the automatically switched half-octave receiver band-pass and transmitter high power, low-pass filter bank assembly, and the DFCB command and control assembly and keypad mounted on the back of the front panel. Front panel, side panels, top and bottom are removable allowing access to the assemblies.



(A)



(B)

Figure 6 — Part A shows the double-sided, plated-through-hole PC boards developed for the *Star-10* transceiver ready for assembly. Part B shows several of the completed assemblies for the *Star-10* transceiver. Starting from top left, PDAF (product detector/audio); IF9RX (receiver second IF); IF9TX (transmitter first IF); PLXO / MRU (phase locked crystal oscillator / master reference unit); IF75BC (bilateral front end converter), and FSYNTH / FRU (frequency synthesizer / frequency reference unit). For functionality of these blocks, refer to Figure 2 in Part 1 of the article, in the Nov/Dec 2007 issue of *QEX*.

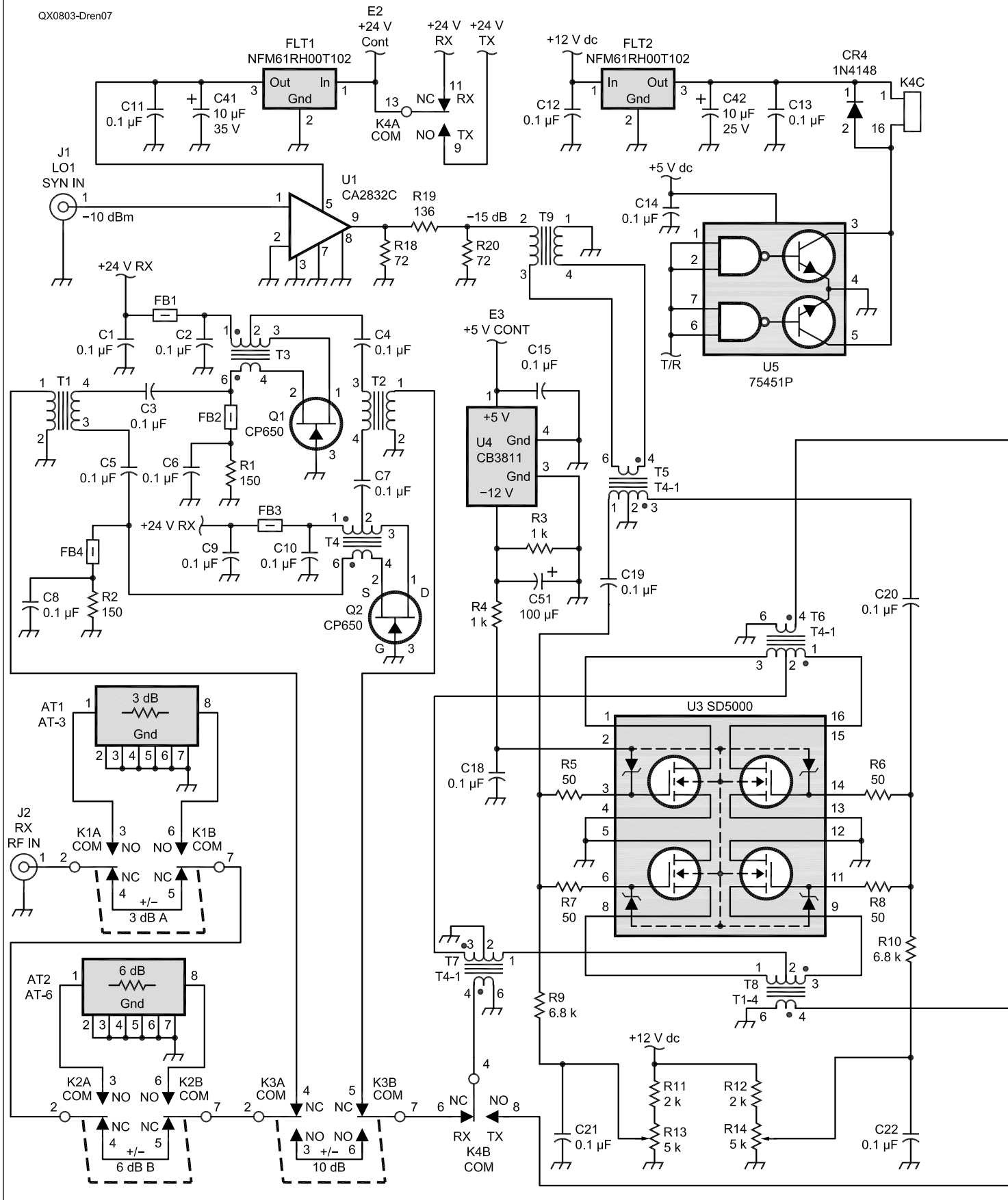
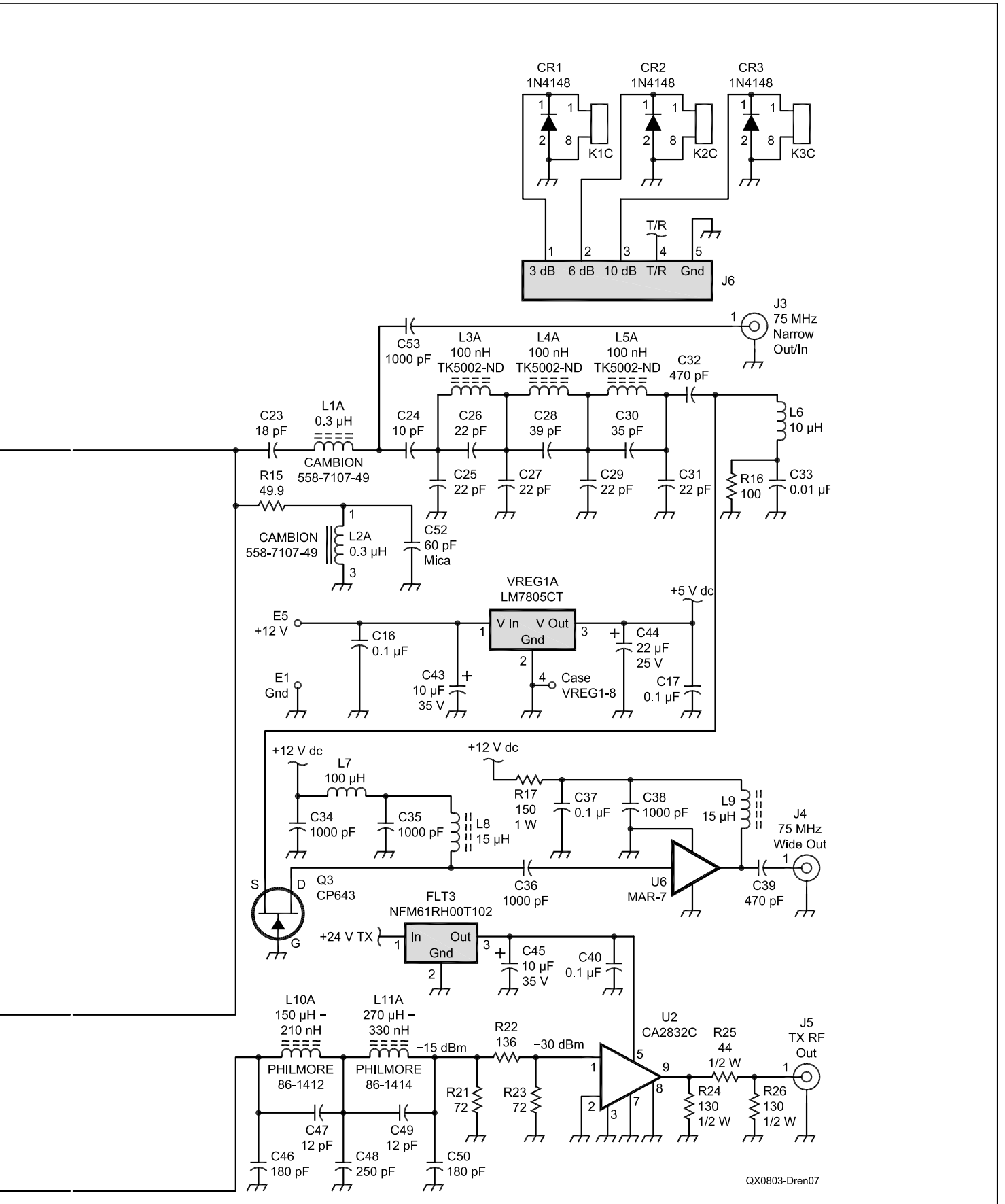


Figure 7 — Schematic diagram of the front end bilateral converter assembly, IF75BC.



automatically switched front end and IF filtering. The radio uses a DDS-Driven PLL synthesizer. Thus, the *Star-10* design resulted in a 75 MHz first IF and a 9 MHz second IF architecture, using a novel bilateral concept, a complex array of old and new technologies, circuits and packaging techniques. After ample system analysis, intense circuit design, multiple brass boarding and testing, PC board layouts were developed and four sets of boards were manufactured, populated and tested again and again before the final implementation. Two transceivers were developed using these boards, a work-in-progress prototype by KG6NK, and the featured *Star-10* model presented here.

The unpopulated double-sided, plated-through PC boards developed specifically for the *Star-10* transceiver are shown in Figure 6A. Some of the completed and tested assemblies are shown in Figure 6B. [To provide easy reference between the parts of this series, we have numbered the Figures consecutively throughout. — *Ed.*]

I will next discuss the major assemblies

and major design details of the *Star-10* transceiver. For clarity, you should first read Part 1 of this series in order to better understand the functionality of each of the assemblies. Part 1 is available on the ARRL *QEX* Web site at www.arrl.org/qex. You will be constantly directed to the transceiver's block diagram in Figure 2 from Part 1 to better understand where a specific assembly fits. To make the best use of printed space, only major blocks will be discussed in detail. As previously indicated, no circuit layouts, construction plans or software listings are offered in this article series.

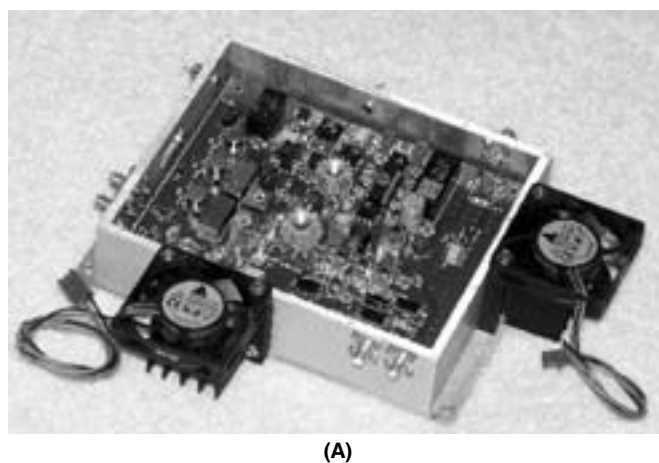
Front End (IF75BC)

As the name implies, this is the first IF (75 MHz) or the bilateral 75 MHz converter. This assembly is a key ingredient of the *Star-10* receiver design because it sets the entire system noise figure and intercept point. IF75BC operates in receive as well as transmit modes.

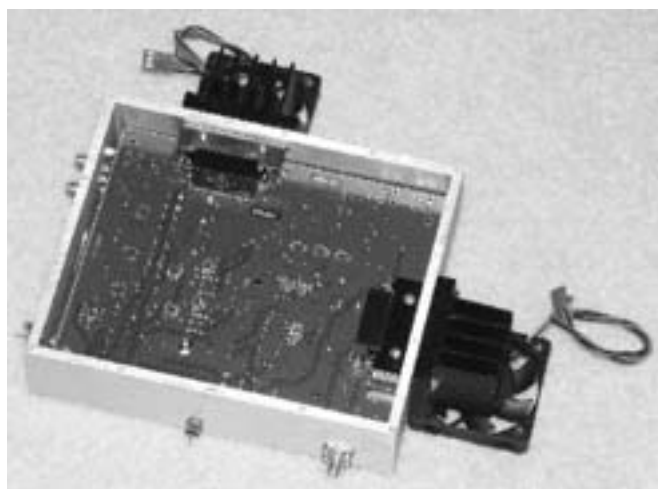
Referring to Figure 2 from Part 1, the

IF75BC assembly provides receiver up conversion for the entire HF range from 1.8 MHz to 30 MHz, to the 75 MHz IF, or down conversion from this IF to the same HF range of 1.8 MHz to 30 MHz in transmit. The IF75BC is preceded by a half-octave band-pass filter bank (composed of eight automatically selectable filters) in receive, the power linear amplifier and a similar half-octave low-pass, high power filter bank (composed of eight automatically selectable equivalent filters) in transmit. To keep intermodulation distortion under control, no PIN switching diodes are used to select filters. All filters in the *Star-10* are switched with either miniature Teledyne RF relays, or high power RF relays. These assemblies will be discussed in more detail later. A schematic diagram of IF 75BC is shown in Figure 7. The actual IF75BC board and assembly implementation are shown in Figure 8.

The 75 MHz first IF choice puts the receiver image away by 150 MHz at any frequency between 1.8 MHz and 30 MHz. This works in direct conjunction with the proper



(A)



(B)

Figure 8 — The IF75BC bilateral front-end converter assembly implementation is shown in Part A. This assembly provides crunch-proof receiver functions and doubles as the transmitter predriver. It uses class A push-pull amplifiers, a push-pull Norton amplifier equipped with very high dynamic range CP-650 FETs, and an H-mode class III mixer using the SD-5000. Two quiet, brushless fans extract the heat out of the CA2832 class A drive amplifiers located under the circuit board. IF75BC assembly dissipates approximately 30 W of dc power (at 24 V dc and 12 V dc) to insure superior dynamic range for the receiver. The unit doubles as a bilateral IF in transmit, providing RF drive signals for the follow-up power linear amplifier. Monolithic CA2832 class A amplifiers are used sparingly throughout the *Star-10* transceiver. Two CA2832 amplifiers are used in the IF75BC as shown in Part B. They are installed on the back of the circuit board. Heat is extracted through the assembly walls using two heat sinks and special brushless quiet (acoustic and electric) fans mounted on the sides of the aluminum assembly, and is further exhausted through the top of the transceiver cover. IF75BC dissipates approximately 30 W dc at 24 V dc and 12 V dc. In the *Star-10* transceiver package, the IF75BC assembly is located on the shelf shown in Part C, along with the IF9TX seen under the shelf. This shelf installs on the main shelf, which also supports the entire half octave filter bank, as can be seen in the photo at the beginning of this article.



(C)

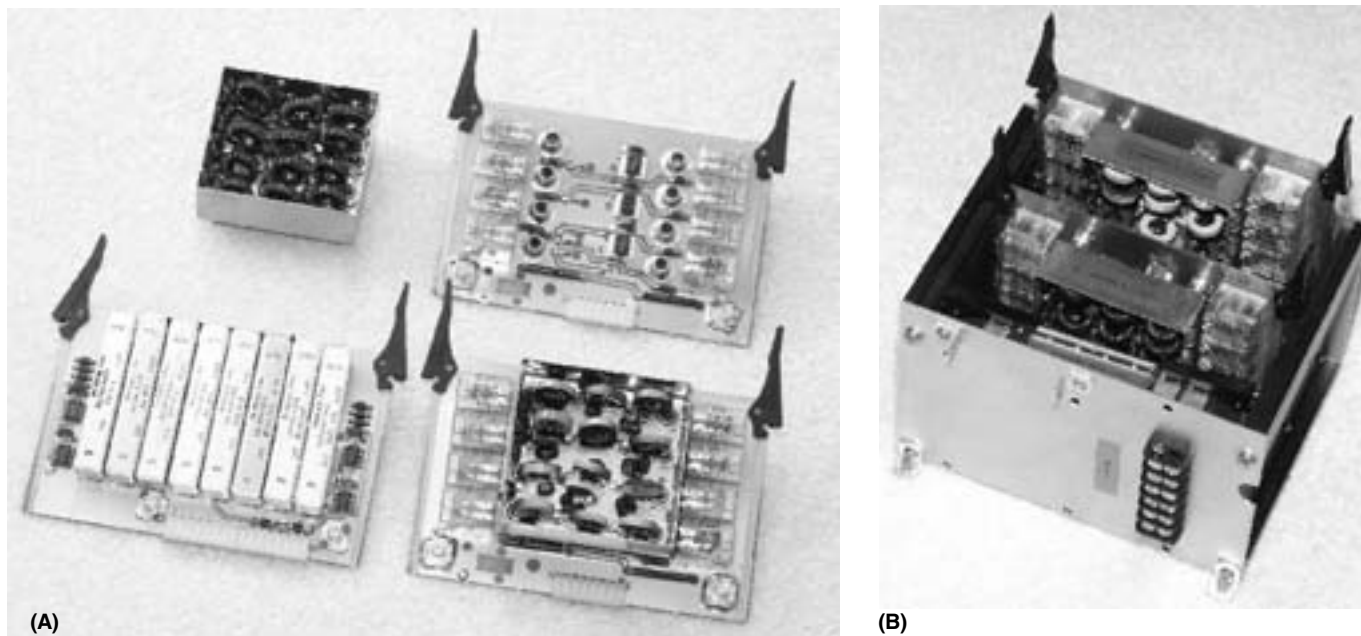


Figure 9 — Part A shows receiver and transmitter half-octave filters banks. Automatically switched half-octave filter banks are shown in Part B, where the motherboard/cage assembly holds the receiver front-end filter boards (eight filters) as well as the transmitter high-power, low-pass filter boards (eight filters). This assembly is located on a shelf shown on the right side of the transceiver, as shown in the lead photo. The DFCB command and control assembly automatically selects the filters.

half-octave filter being selected in the front-end banks. The amount of rejection provided is consequently uniform throughout the coverage due to the proper selection of the half-octave ranges. (See References 1, 2, 3, listed at the end of this article.) A high-pass receiver front end filter, which is sometimes used in general coverage designs, was found unnecessary due to the extremely good shape factor offered by the half-octave band-pass filters. Conversely, the proper half-octave low-pass filter selected in the transmit chain ensures equally good spurious and harmonic rejection throughout the entire frequency range.

Looking at the schematic diagram in Figure 7, the filtered received RF signals from the half-octave band-pass filter bank enter the receiver circuits of the IF75BC board assembly at J2 through the advanced intercept point attenuator (AIPA) and the +10 dB push-pull preamplifier located on this board. This combination allows for the programmable AIPA attenuators (part of the gain control system) to be inserted in the receiver front end if so desired. Because of the dynamic range capability of the *Star-10*, these functions have not been used extensively since good results were obtained with the preamplifier on and no attenuators.

Three front panel programmable attenuation steps are provided by AIPA: 3 dB, 6 dB and 10 dB. Commands for these selections enter the IF75BC through the J6 connector. The 3 dB and 6 dB positions are imple-

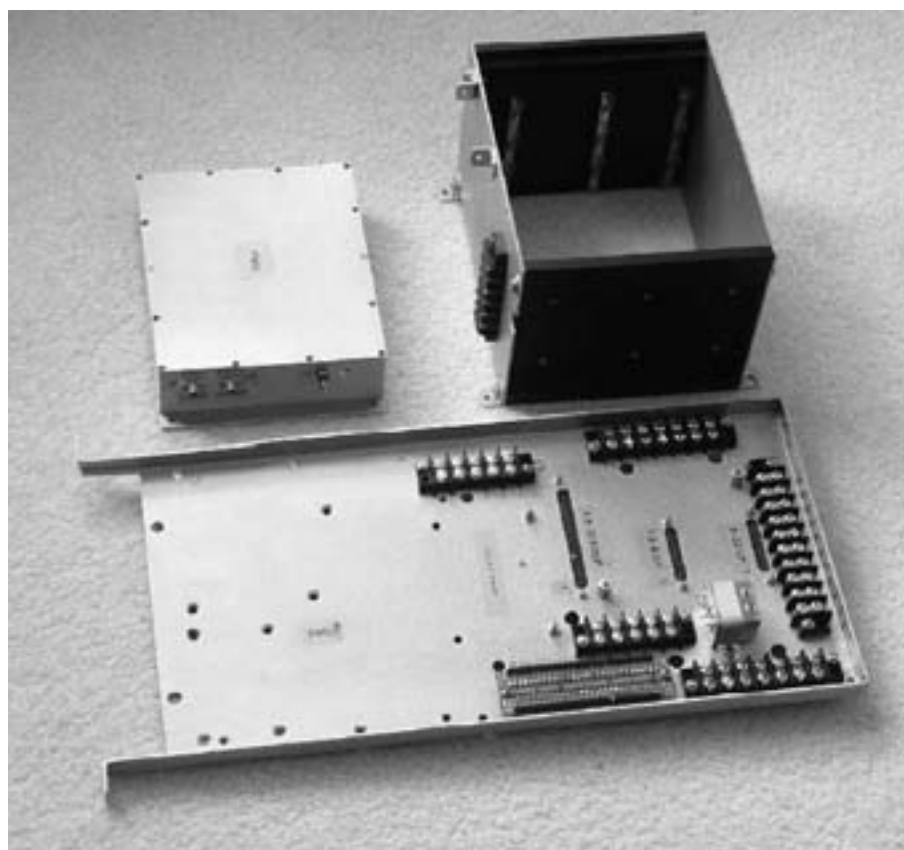


Figure 10 — View of the bottom shelf (motherboard), which holds the automatically switched half-octave filter banks and the motherboard cage (at the top right corner of the photo). Command and control lines have been wired to the connectors visible in the slots in the shelf.

mented by inserting a 3 dB or a 6 dB pad via corresponding relays (AT1, K1 and AT2, K2) in the circuit, while the 10 dB function is implemented through totally bypassing the push-pull amplifier, using K3 as shown. The preamp can always be on because of the dynamic range capability of the *Star-10*. The AIPA functions are remote controlled from the front panel via miniature RF relays located on the IF75BC board. The front panel switch (marked AIPA) that controls these attenuators also controls three LED indicators showing what is selected on the composite front panel display (dial) as shown in the lead photo.

To ensure the high dynamic range for the receiver, IF75BC uses an adaptation of a push-pull Norton amplifier, using very high dynamic range CP-650 FETs. This preamplifier, as well as other IF75BC functions, use 24 V dc in addition to 12 V dc and other voltages. The power consumption of the IF75BC front end board and assembly is around 30 W dc, requiring heat sinks as shown in Figure 8 A, B and C.

The Norton amplifier circuit was initially developed and patented by David Norton and Allen Podell in 1975 (reference 4, 5, 6). This circuit constitutes a novel development in the application of negative feedback techniques to active double-balanced mixers, in which the concept of single-transformer “loss less feedback” is employed to improve both, the intercept point and the noise figure. The Norton design uses transformer coupling to achieve “noiseless negative feedback” – a truly outstanding approach.

Loss less feedback amplifiers have been recognized as an outstanding means of providing high dynamic range, in terms of both linearity and noise figure. In the following years since its invention, various forms of the Norton amplifier have found wide usage in good communications receivers and radio astronomy applications.

A variation on the Norton amplifier was further described by Joe Reisert in *ham radio* magazine (reference 7). The circuit has been further improved by Jacob Makhinson and

was described in detail in references 8, 9, 10, 11, 12.

Looking at Figure 7, the conditioned RF signals from AIPA enter the first mixer U3 which is used in an H-mode (references 6, 7, 8, 9) biasing system. The variable high resolution LO signal from the synthesizer (FRU - FSYNTH) is presented to the mixer via J1 and U1, via a CA2832 class A monolithic amplifier (note: *Star-10* makes ample use of the Motorola CA2832 monolithic amplifiers) operating at 24 V. Thus, the LO level is built up from approximately -9 dBm to about +27 dBm. Mixer biasing is further provided through R13, R14 and U4. The H-mode mixer used is typical of the design described in the above references. However, most of these designs have been used in low IF configurations (e.g. 9 MHz) and with limited RF/LO bandwidths. They are usually fed by out of phase digital drivers which maintain tight LO jitter and phase coherence over relatively narrow frequency ranges. However, using such designs over very broad

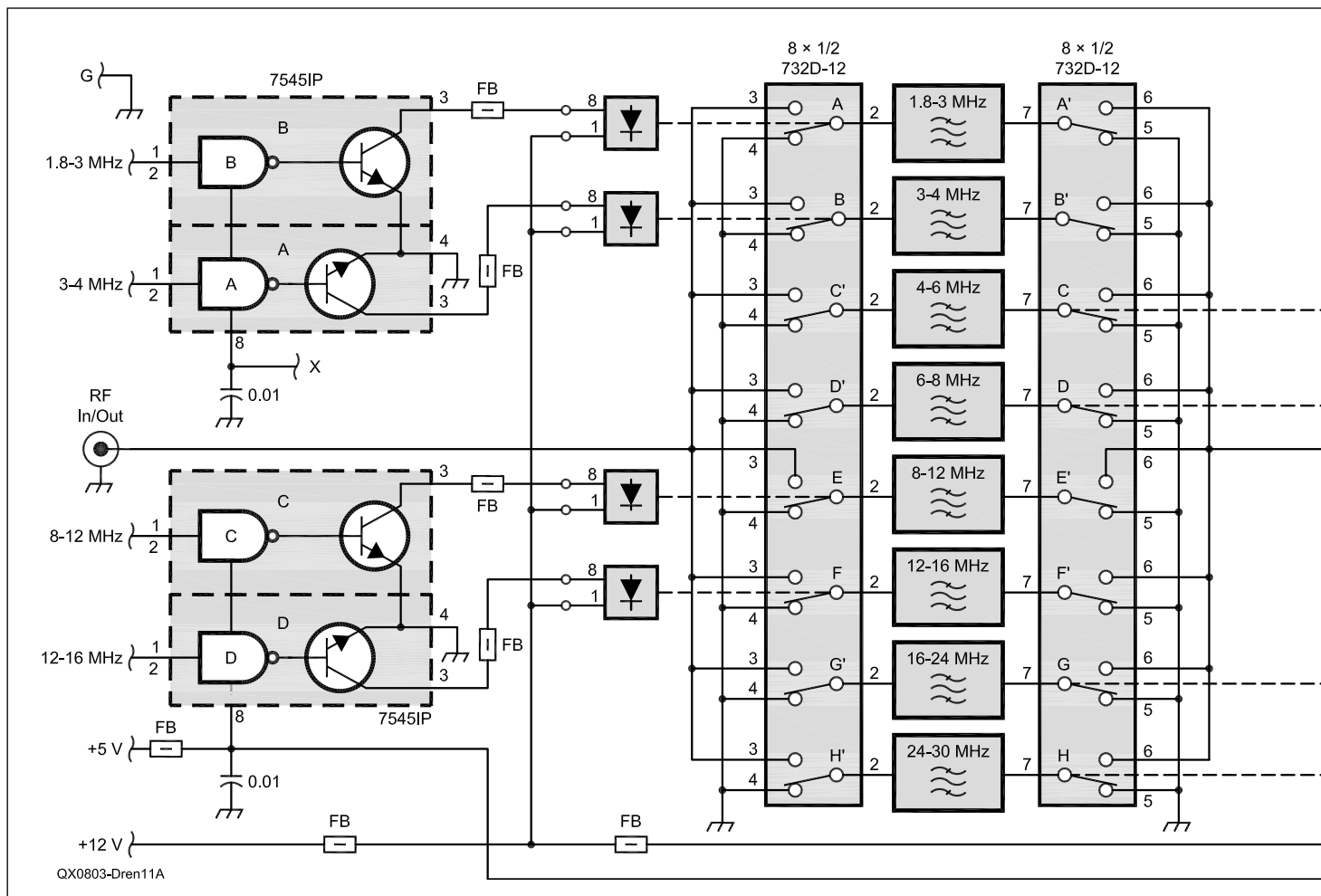


Figure 11A — The schematic diagram for the receiver band-pass filter bank.

frequency ranges such as the four octaves used in the *Star-10* would require sub - pico second rise time phase matching between the digital drivers. Because of the *Star-10* broadband nature, it was found impractical to provide LO drive via digital means. After long analysis and experimentation, it was found that using a transformer combination can provide the required phase balance over the entire frequency coverage with minor phase mismatching consequences. Following intense testing, this solution was found to be a practical compromise.

Making the preamplifier and the H-mode mixer work in the actual IF75BC board required ample circuit layout planning, where connecting paths in the double sided plated through PC board was implemented with short and balanced paths, which were trimmed equally to promote amplifier stability. Additional ferrite beads were used together with short leads to prevent oscillation. The negative biasing supply for the SD-5000 mixer was achieved using a dc-to-

dc converter at U4 as shown. Considerable care was taken in the entire board design to ensure proper ground distribution and avoid resonant features.

The transmit chain on IF75BC, when activated via the T/R relay K4, outputs RF signals to the power linear amplifier through the 30 MHz low-pass filter made of L10, L11, C46 through C50, and another class A - CA2832 monolithic amplifier, U2. Driver circuits for the RF relays on IF75BC as well as throughout the entire transceiver use high current open collector digital line drivers 75451 ICs (U5 on this board). The RF output at J5 goes further to the high power linear amplifier, and to the automatically switched half-octave low-pass filter banks, through the RF power transmitter gain control (TGC) circuits and further through the main T/R switch, to the antenna. The T/R relay on IF75BC which is facilitated through the on board K4, also provides proper switched 24 V dc to the bilateral amplifier (BILAT AMP) assembly located further down in the

75 MHz IF chain as shown in Figure 2, Part 1 of this article series.

There are two 75 MHz IF receiver outputs on the IF75BC; the first is diplexed via L2, C52, C53 and is further output at J3 to be input to the quartz crystal roofing filter assembly, FL75. This signal serves in receive as well as in transmit as the narrow 75 MHz IF output/input. The other output at J4 serves as the 75 MHz wide IF (500 kHz) intended for spectrum analysis and noise blanker functions to be achieved further in IF9NB. This wide band signal follows the path from C24 through the 500 kHz band pass filter made of L3 through L5 and C25 through C32 and further through Q3 and U6. This completes the IF75BC assembly description.

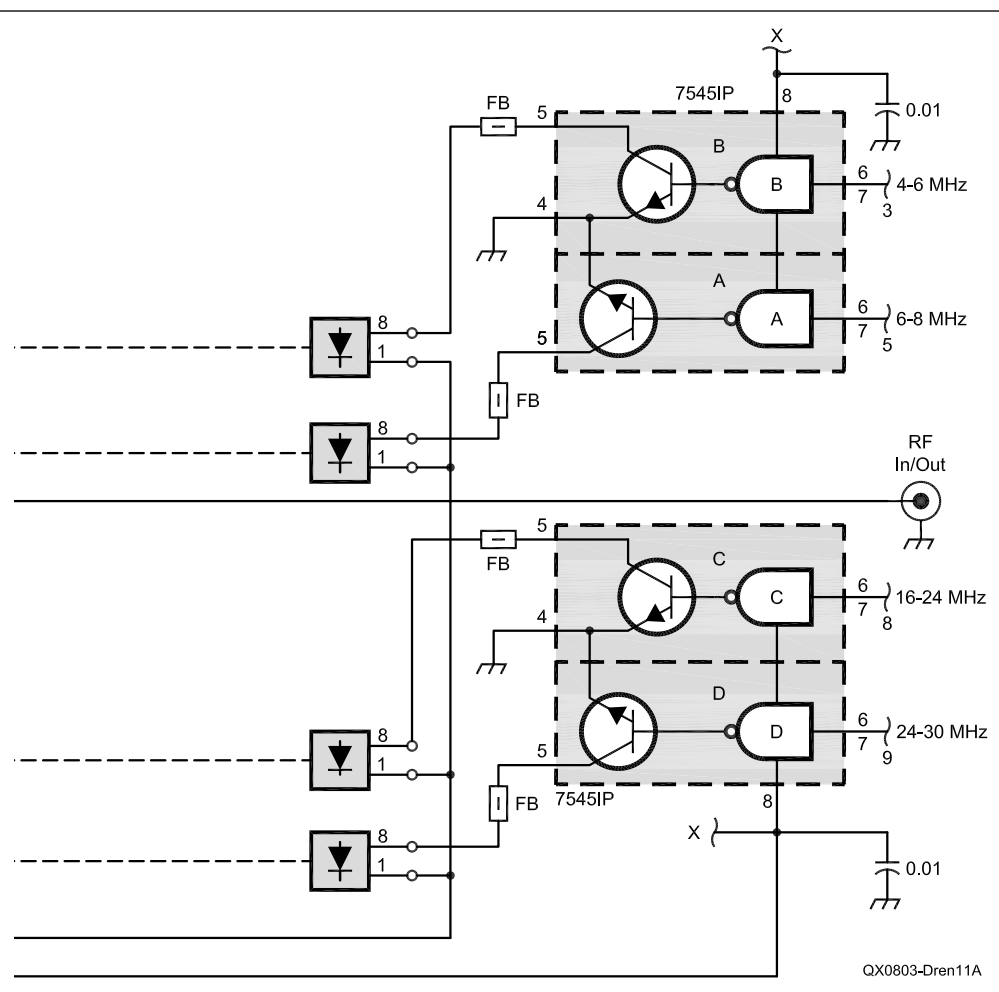
Receiver and Transmitter Half-Octave Filter Banks

Looking at the *Star-10* transceiver block diagram from Figure 2 of Part 1, the IF75BC assembly is preceded by the half-octave band-pass and low-pass filters banks as shown in Figure 9. The actual location of this assembly in the *Star-10* transceiver package can be seen on the right side of the leading photo at the beginning of this Part.

The design of these filters and their functionality in a general coverage HF transceiver or receiver has been previously described in great detail in references 1, 2 and 3. The *Star-10* transceiver uses this design in a new mechanical implementation specific to this transceiver package.

There are eight automatically selectable band-pass receiver filters (bottom left board of Figure 9 A) and eight high-power low-pass similar filters (the remaining assemblies shown in Figure 9 A). The filter banks are plug in shielded assemblies as shown. They insert into the PC boards that contain the control circuits utilizing 75451 line drivers to switch corresponding RF relays, which in turn use commands from the DFCB assembly microprocessor to select the proper receive and transmit combination. The boards equipped with the plug in filter banks (as shown) are in turn, plug-in assemblies themselves. They insert into a machined motherboard cage assembly as shown in Figure 9 B. Command signals coming from DFCB board and RF connectors are provided at the bottom of the assembly which is supported by the bottom shelf of the *Star-10* system as shown in Figure 10.

The schematic diagram for the receiver's band-pass filters - bank is shown in Figure 11 A. The schematic diagram for the high power low-pass filters banks (two assemblies) is shown in Figure 11 B. There are eight band-pass filters in the receiver assembly and four low-pass filters in each of the two low-pass assemblies, for a total of eight equivalent



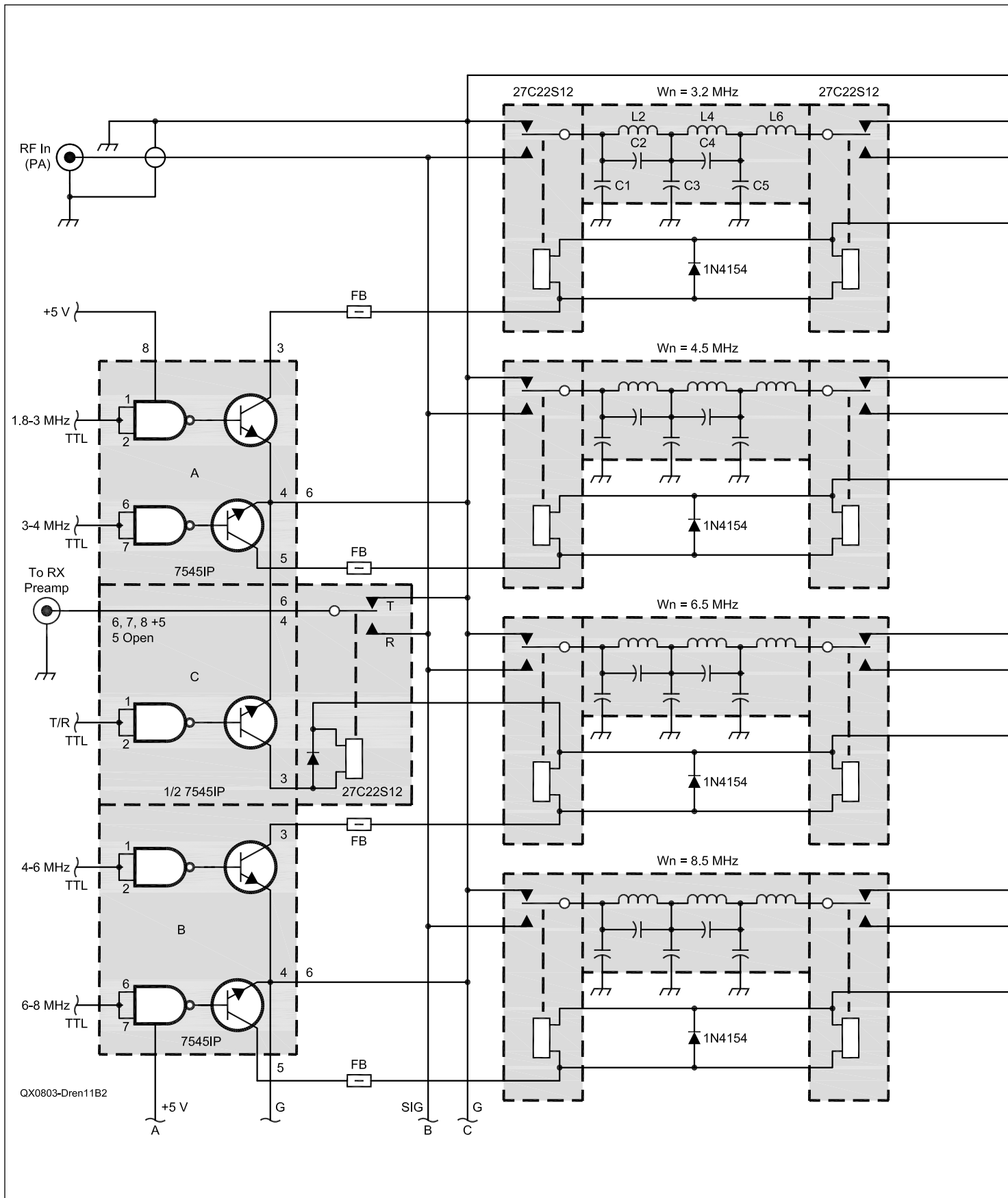
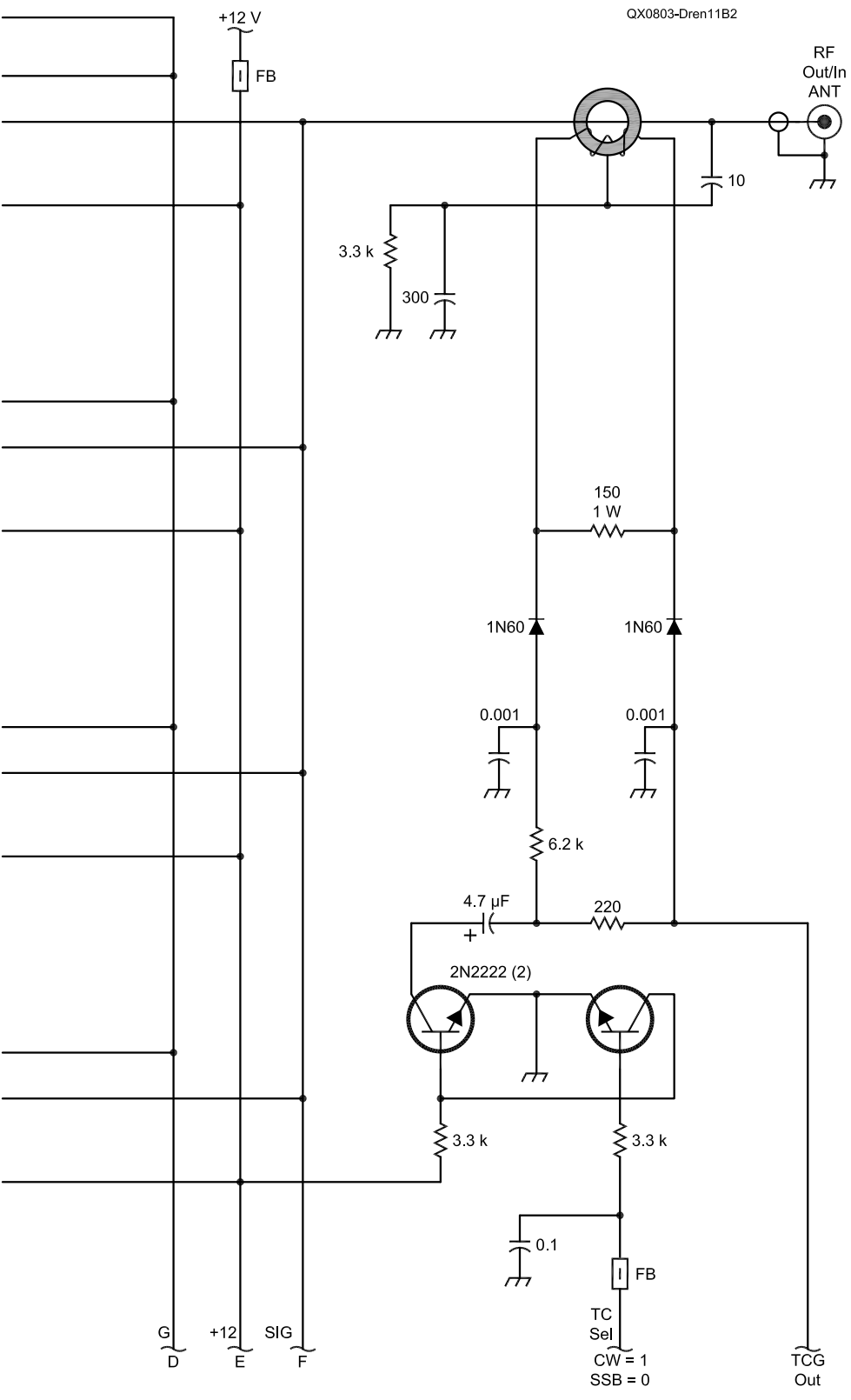


Figure 11B — The schematic diagram for the high-power, low-pass filter banks.



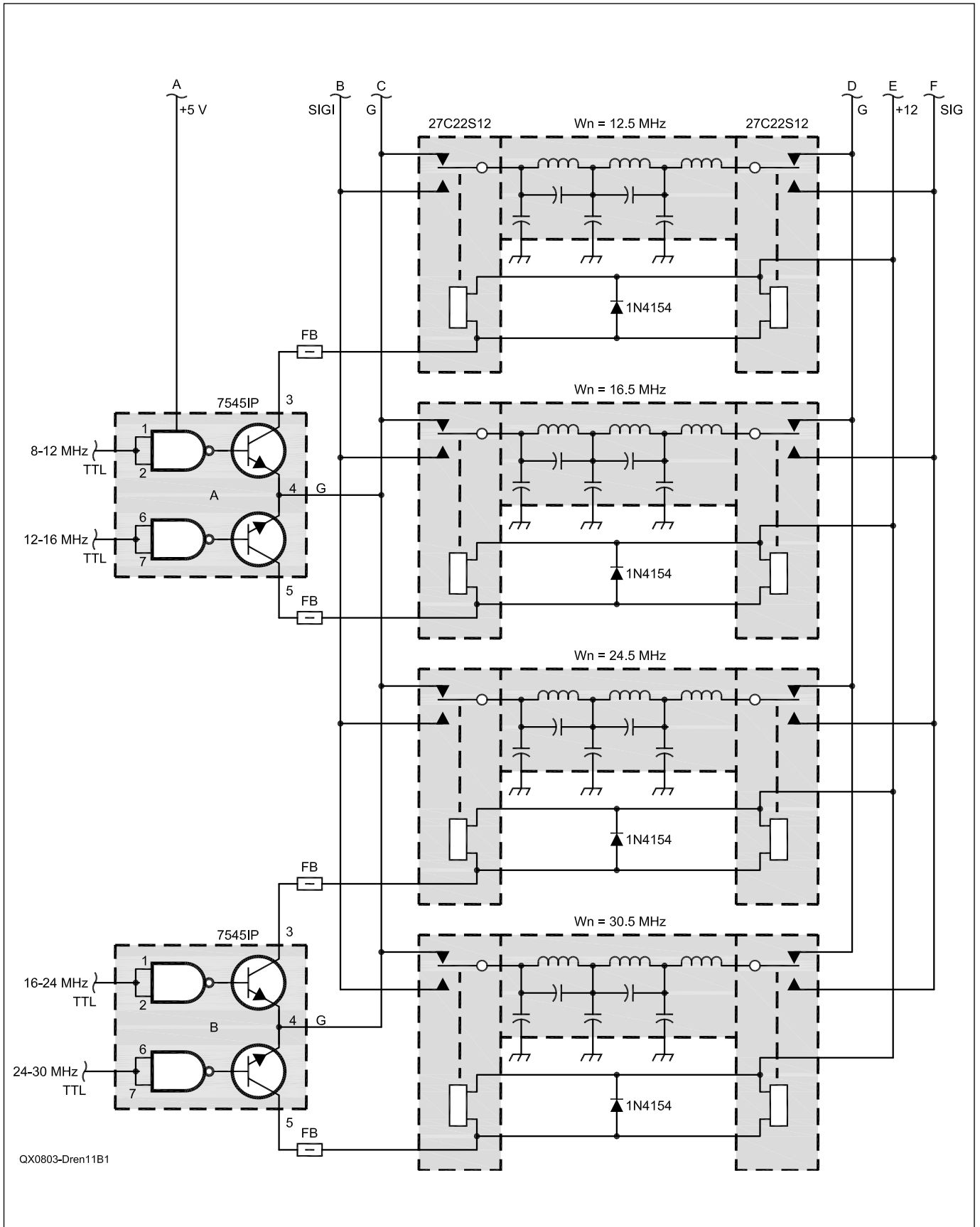
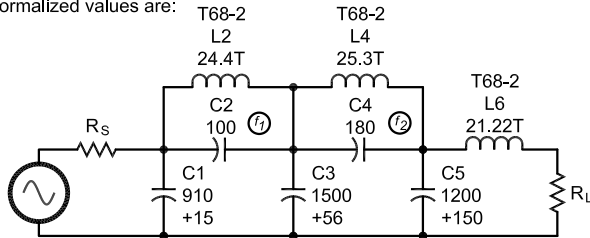


Figure 11B continued

#1

$f_c = 3.2$ MHz Band = 1.8 – 3 MHz
Reject 6 MHz by 60 dB
 f_c : Reject = 1.875:1

Use A C0615C $\theta = 35^\circ$ Filter
Minimum Attenuation At 6 MHz = 67.8 dB
Normalized values are:



$R_S = 1$	$R_L = 1$
$C_1 = 0.9316$	$C_2 = 0.1082$
$L_2 = 1.368$	$C_2 = 1.564$
$C_4 = 0.1880$	$L_4 = 0.1466$
$C_5 = 1.371$	$L_6 = 1.033$
$f_1 = 2.5989$	$f_2 = 1.9051$

the denormalized values are:

$R_S = 50$	$R_L = 50$
$C_1 = 926.7 \mu\text{F} (910 + 15)**$	$C_2 = 107.6 \text{ pF} (100)$
$L_2 = 3.40 \mu\text{H}$	$C_3 = 1556 \text{ pF} (1500 + 56)$
$C_4 = 187 \text{ pF} (180)$	$L_4 = 3.65 \mu\text{H}$
$C_5 = 13.64 \text{ pF} (1200 + 150)$	$L_6 = 2.568 \mu\text{H}$
$f_1 = 8.316$ MHz	$f_2 = 6.0963$ MHz

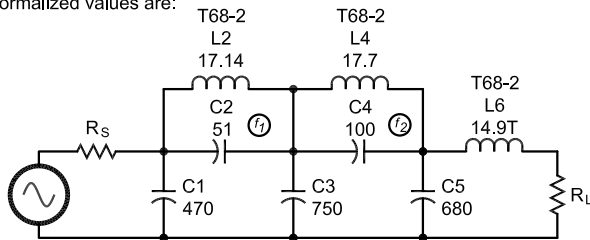
tune L_2, C_2 for an attenuation peak at f_1
tune L_4, C_4 for an attenuation peak at f_2

* Design value
** Actual value used

#3

$f_c = 6.5$ MHz Band = 4 – 6 MHz
Reject 12 MHz
 f_c : Reject = 1.846:1

Use A C0615C $\theta = 35^\circ$ Filter
Minimum Attenuation At 12 MHz = 67.8 dB
Normalized values are:



$R_S = 1$	$R_L = 1$
$C_1 = 0.9316$	$C_2 = 0.1082$
$L_2 = 1.368$	$C_2 = 1.564$
$C_4 = 0.1880$	$L_4 = 1.466$
$C_5 = 1.371$	$L_6 = 1.033$
$f_1 = 2.59897$	$f_2 = 1.9051$

the denormalized values are:

$R_S = 50$	$R_L = 50$
$C_1 = 456.2 \text{ pF} (470)$	$C_2 = 53 \text{ pF} (51)$
$L_2 = 1.675 \mu\text{H}$	$C_3 = 766 \text{ pF} (750)$
$C_4 = 92 \text{ pF} (100)$	$L_4 = 1.79 \mu\text{H}$
$C_5 = 671.4 \text{ pF} (680)$	$L_6 = 1.265 \mu\text{H}$
$f_1 = 16.893$ MHz	$f_2 = 12.383$ MHz

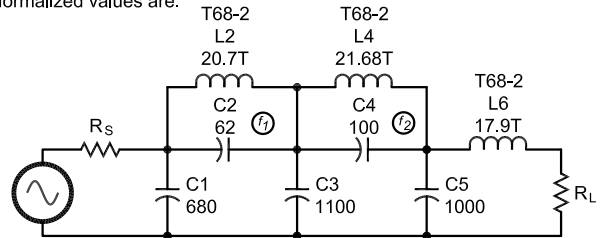
tune L_2, C_2 for an attenuation peak at f_1
tune L_4, C_4 for an attenuation peak at f_2

#2

QX0803-Dren11C

$f_c = 4.5$ MHz Band = 3 – 4 MHz
Reject 9 MHz
 f_c : Reject ratio = 2:1

Use A C0615C $\theta = 32^\circ$ Filter
Minimum Attenuation At 9 MHz = 72.8 dB
Normalized values are:



$R_S = 1$	$R_L = 1$
$C_1 = 0.9492$	$C_2 = 0.08912$
$L_2 = 1.393$	$C_3 = 1.601$
$C_4 = 0.1540$	$L_4 = 1.518$
$C_5 = 1.395$	$L_6 = 1.034$
$f_1 = 2.8385$	$f_2 = 2.06813$

the denormalized values are:

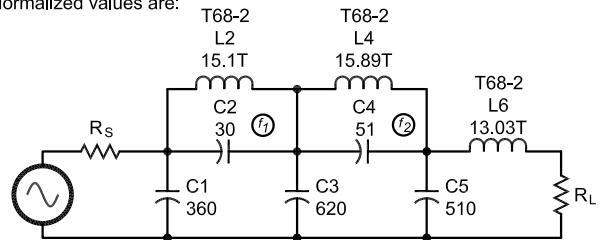
$R_S = 50$	$R_L = 50$
$C_1 = 671.4 \text{ pF} (680)$	$C_2 = 63 \text{ pF} (62)$
$L_2 = 2.46 \mu\text{H}$	$C_3 = 1132.4 \text{ pF} (1100)$
$C_4 = 108.9 \text{ pF} (100)$	$L_4 = 2.68 \mu\text{H}$
$C_5 = 986.7 \text{ pF} (1000)$	$L_6 = 1.83 \mu\text{H}$
$f_1 = 12.773$ MHz	$f_2 = 9.3066$ MHz

tune L_2, C_2 for an attenuation peak at f_1
tune L_4, C_4 for an attenuation peak at f_2

#4

$f_c = 8.5$ MHz Band = 6 – 8 MHz
Reject 18 MHz
 f_c : Reject = 2.11:1

Use A C0615C $\theta = 31^\circ$ Filter
Minimum Attenuation At 18 MHz = 74.5 dB
Normalized values are:



$R_S = 1$	$R_L = 1$
$C_1 = 0.9547$	$C_2 = 0.08325$
$L_2 = 1.400$	$C_2 = 1.612$
$C_4 = 0.1436$	$L_4 = 1.535$
$C_5 = 1.402$	$L_6 = 1.034$
$f_1 = 2.9287$	$f_2 = 2.1298$

the denormalized values are:

$R_S = 50$	$R_L = 50$
$C_1 = 357.5 \text{ pF} (360)$	$C_2 = 31.2 \text{ pF} (30)$
$L_2 = 1.31 \mu\text{H}$	$C_3 = 603.7 \text{ pF} (620)$
$C_4 = 53.8 \text{ pF} (50)$	$L_4 = 1.44 \mu\text{H}$
$C_5 = 525 \text{ pF} (510)$	$L_6 = 0.968 \mu\text{H}$
$f_1 = 24.894$ MHz	$f_2 = 18.1033$ MHz

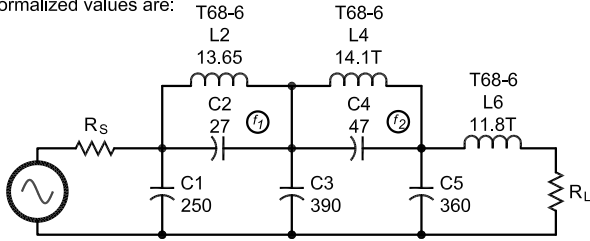
tune L_2, C_2 for an attenuation peak at f_1
tune L_4, C_4 for an attenuation peak at f_2

Figure 11C — Design values for the low-pass filter banks. The band-pass design is directly derived from the low-pass design.

#5

$f_c = 12.5$ MHz Band = 8 - 12 MHz
Reject 24 MHz
 f_c : Reject = 1.92:1

Use A C0615C $\theta = 34^\circ$ Filter
Minimum Attenuation At 24 MHz = 69.4 dB
Normalized values are:



$R_s = 1$	$R_L = 1$
$C_1 = 0.9377$	$C_2 = 0.101$
$L_2 = 1.376$	$C_3 = 1.577$
$C_4 = 0.1761$	$L_4 = 1.484$
$C_5 = 1.379$	$L_6 = 1.034$
$f_1 = 2.6741$	$f_2 = 1.9561$

the denormalized values are:

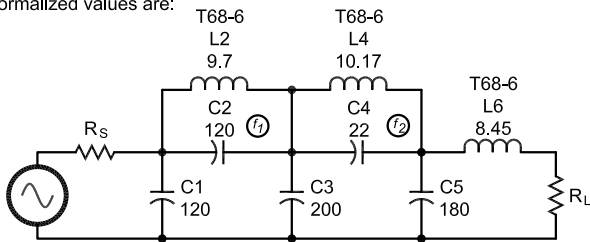
$R_s = 50$	$R_L = 50$
$C_1 = 238.8$ pF (250)	$C_2 = 25.9$ pF (27)
$L_2 = 0.876$ μ H	$C_3 = 401.6$ pF (390)
$C_4 = 44.8$ pF (47)	$L_4 = 0.945$ μ H
$C_5 = 351.1$ pF (360)	$L_6 = 0.658$ μ H
$f_1 = 33.426$ MHz	$f_2 = 24.451$ MHz

tune L_2, C_2 for an attenuation peak at f_1
tune L_4, C_4 for an attenuation peak at f_2

#7

$f_c = 24.5$ MHz Band = 16 - 24 MHz
Reject 48 MHz
 f_c : Reject = 1.96:1

Use A C0615C $\theta = 33^\circ$ Filter
Minimum Attenuation At 48 MHz = 71.1 dB
Normalized values are:



$R_s = 1$	$R_L = 1$
$C_1 = 0.9436$	$C_2 = 0.09523$
$L_2 = 1.385$	$C_3 = 1.589$
$C_4 = 0.1648$	$L_4 = 1.501$
$C_5 = 1.387$	$L_6 = 1.034$
$f_1 = 2.75377$	$f_2 = 2.0103$

the denormalized values are:

$R_s = 50$	$R_L = 50$
$C_1 = 122.6$ pF (120)	$C_2 = 12.37$ pF (12)
$L_2 = 0.449$ μ H	$C_3 = 206.4$ pF (200)
$C_4 = 21.4$ pF (22)	$L_4 = 0.487$ μ H
$C_5 = 180.2$ pF (180)	$L_6 = 0.336$ μ H
$f_1 = 67.467$ MHz	$f_2 = 49.292$ MHz

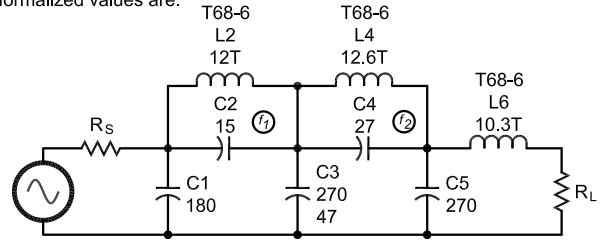
tune L_2, C_2 for an attenuation peak at f_1
tune L_4, C_4 for an attenuation peak at f_2

#6

QX0803-Dren11C

$f_c = 16.5$ MHz Band = 12 - 16 MHz
Reject 36 MHz
 f_c : Reject ratio = 2.18:1

Use A C0615C $\theta = 30^\circ$ Filter
Minimum Attenuation At 36 MHz = 76.3 dB
Normalized values are:



$R_s = 1$	$R_L = 1$
$C_1 = 0.96$	$C_2 = 0.0776$
$L_2 = 1.408$	$C_3 = 1.623$
$C_4 = 0.1337$	$L_4 = 1.551$
$C_5 = 1.410$	$L_6 = 1.034$
$f_1 = 3.02499$	$f_2 = 2.19586$

the denormalized values are:

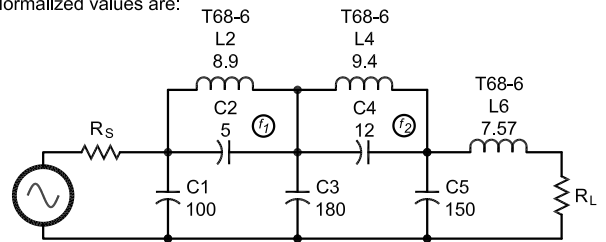
$R_s = 50$	$R_L = 50$
$C_1 = 185.19$ pF (180)	$C_2 = 14.9$ pF (15)
$L_2 = 0.679$ μ H	$C_3 = 313.1$ pF (270 + 47)
$C_4 = 25.8$ pF (27)	$L_4 = 0.748$ μ H
$C_5 = 272$ pF (270)	$L_6 = 0.4987$ μ H
$f_1 = 49.9123$ MHz	$f_2 = 36.2317$ MHz

tune L_2, C_2 for an attenuation peak at f_1
tune L_4, C_4 for an attenuation peak at f_2

#8

$f_c = 30.5$ MHz Band = 24 - 30 MHz
Reject 72 MHz
 f_c : Reject = 2.36:1

Use A C0615C $\theta = 27^\circ$ Filter
Minimum Attenuation At 72 MHz = 82 dB
Normalized values are:



$R_s = 1$	$R_L = 1$
$C_1 = 0.9747$	$C_2 = 0.06212$
$L_2 = 1.429$	$C_3 = 1.654$
$C_4 = 0.1066$	$L_4 = 1.595$
$C_5 = 1.430$	$L_6 = 1.035$
$f_1 = 3.3568$	$f_2 = 2.4244$

the denormalized values are:

$R_s = 50$	$R_L = 50$
$C_1 = 101.7$ pF (100)	$C_2 = 6.5$ pF (5)
$L_2 = 0.373$ μ H	$C_3 = 172.6$ pF (180)
$C_4 = 11.1$ pF (12)	$L_4 = 0.416$ μ H
$C_5 = 149.2$ pF (150)	$L_6 = 0.270$ μ H
$f_1 = 102.38$ MHz	$f_2 = 73.944$ MHz

tune L_2, C_2 for an attenuation peak at f_1
tune L_4, C_4 for an attenuation peak at f_2

half-octave filters (1.8 to 3, 3 to 4, 4 to 6, 6 to 8, 8 to 12, 12 to 16, 16 to 24, and 24 to 30 MHz). The chosen electrical design for all filters is the Cauer (elliptical) approach. This type of filter has an in-band characteristic similar to that of a Chebyshev filter; it also has a more abrupt transition band characteristic than the monotonically increasing attenuation of the Chebyshev approach. This design was chosen because of the superior rejection and the relatively easier execution and tuning procedures required. Shown in Figure 11 C are the electrical schematics and design values for all the low-pass filter banks. The band-pass design was directly derived from the low-pass implementation. For a much more in depth discussion on the actual design of these filters, you are directed to my article series from references 1 and 2, which is available on my Web site listed at the end of this article.

75 MHz Bilateral IF

The roofing filter assemblies (FL75), the 75 MHz Bilateral Amplifier (BILAT AMP), and the 75 MHz to 9 MHz Bilateral Converter (IF9BC) will be described together because they constitute the 75 MHz bilateral IF. Looking at the *Star-10* transceiver block diagram from Figure 2 of Part 1, these three assemblies follow the IF75BC providing further signal processing through the 75 MHz bilateral IF (BILAT AMP), and selective signal conditioning through the FL75 roofing filter assembly.

A second conversion to the 9 MHz IF stage (used in receive and transmit) is facilitated through the IF9BC assembly. Physically, the above assemblies are partly located on the left side of the transceiver under the shelf shown in Figure 8 C. The BILAT AMP assembly is located in the center area of the bottom side of the main shelf (for a view of the shelf, see Figure 10) as shown in Figure 12 (the smaller assembly in the center equipped with a fan).

The BILAT AMP and the FL75 roofing filter assemblies are shown in Figure 13. The schematic diagram for the BILAT AMP assembly is shown in Figure 14. The performance characteristics of the bilateral amplifier are shown in Table 1.

Looking at Figure 14, the 75 MHz BILAT AMP uses two back-to-back CA2832 monolithic amplifiers which were discussed earlier. As can be seen, only one of the amplifiers is on at the time, the default being the receiver chain at the top of Figure 14. Power is applied selectively to the respective circuit via the T/R function through the switched 24 V dc lines from IF75BC. In transmit, the power is switched on to the bottom circuit and the top circuit remains dormant for the duration of transmit. Natural isolation between the active

circuit and the dormant circuit is provided via the inherent isolation (>20 dB) allowed by the passive splitter/combiner arrangement shown.

One of the 75 MHz IF outputs from IF75BC enters the first section (A) of the roofing filter FL75 (see Figure 2 in Part 1) as shown. Again, all RF interconnects between assemblies in the *Star-10* are 50 ohms, making it easy to use miniature coaxial cables

equipped with SMA connectors. The output of the first FL75 filter section is then input to the BILAT AMP at J1, where it enters the first splitter/combiner PSC2-1 (A1) at pin 1 as shown. The receiver path continues at pin 5 of the PSC2-1 and is output to the BIPA circuit located on the IF9BC assembly. The BIPA circuit is a 30 dB –programmable – from the front panel – PIN diode attenuator circuit that will be discussed in more detail later. The return path from the BIPA circuit is input back into the receiver's 75 MHz IF and is further amplified in the BILAT AMP assembly by the CA2832 amplifier at U1, to be recombined with the isolated transmitter path through another PSC2-1 (A2). The output of the BILAT AMP assembly is then output at J2 and is further input to the second section (B) of the FL75 roofing filter assembly. This functionality is true in receive as well as transmit providing true bilateral functionality for the entire 75 MHz IF. It should be noted that the 75 MHz filter assembly has been split in two sections and is intentionally isolated by the amplifier in order to cope with the relatively high IF levels seen at these points in the circuits (see system analysis

Table 1
Bilateral Amplifier (BILAT AMP)
Specifications

Mode of operation: Bidirectional OR function (one way active at any given time)
Operating frequency: 75 MHz
Gain (max): +36 dB
NF: 5 dB
1 dB compression point (CP1): +35 dBm
IP3: +50 dBm
RF in (max): +5 dBm
RF out (max) +32 dBm
Vcc: +24 V dc
Ic: 450 mA (one-way active)
Amplification Class: AA

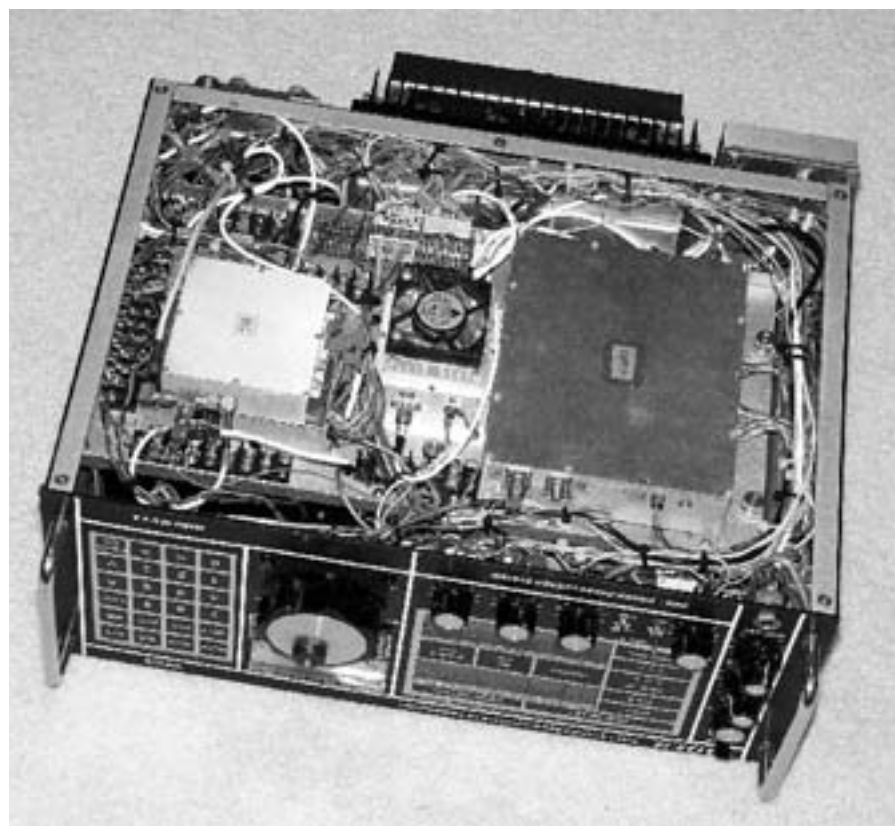


Figure 12 — Bottom view of the *Star-10* transceiver, with the back of the main shelf exposed. Shown in the center is the 75 MHz bilateral amplifier (BILAT AMP) using two back-to-back monolithic CA2832 class A amplifiers (one used in receive and the other in transmit), isolated from each other via splitters/combiners. These high dynamic range amplifiers are capable of 35 dB gain, a 5 dB noise figure and a +50 dBm IP3. Cooling is achieved via another brushless fan extracting the heat through the bottom panel.

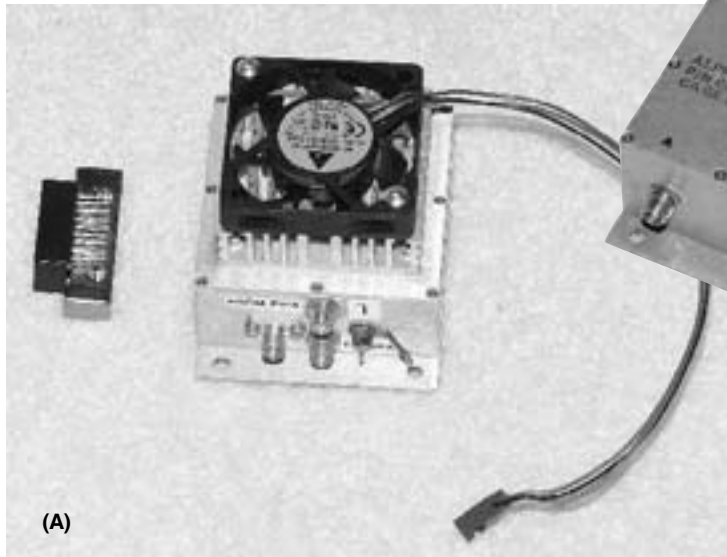


Figure 13 — The physical implementation of the BILAT AMP assembly is shown in Part A. Two back-to-back class A CA2832C amplifiers (one shown at left for size) are packaged together in this assembly. They are passively isolated from each other via a splitter/combiner assembly which provides 20 dB of natural isolation between receive and transmit functions. Switched 24 V dc is selectively provided to the amplifiers depending on the receive or transmit function selected by the T/R assembly via the IF75BC T/R relay. BIPA attenuation is inserted as shown in Figure 2 of Part 1 of the article. The schematic diagram of the BILAT AMP assembly is shown in Figure 14. Part B shows the roofing filter FL75 assembly. It contains two four-pole filters (eight poles) with a 3 dB bandwidth of approximately 10 kHz. These high intercept filters have been especially designed and manufactured for the *Star-10* by Temex Inc. Initially, a fifth overtone filter set was designed and tested. The initial concern was about the maximum amount of RF drive level these filters will see at this point in the system (approximately +5 dBm), at what duty cycle, and how their aging (calculated at 32 years) will suffer under these conditions, their insertion loss and their group delay properties. A second set was designed and manufactured by Alpha Components Inc., using a fundamental Gaussian design, which can provide better resistance to high drive levels.

from part 1 of the article). Thus, the first roofing filter is different in design than the second roofing filter.

The roofing filters assembly contains two four-pole filters (eight poles composite) with a 3 dB bandwidth of approximately 10 kHz. These high intercept filters have been especially designed and manufactured for the *Star-10* by Temex Inc. Initially, a fifth overtone filter set was designed and tested. The initial concern was about the maximum amount of RF drive level these filters will see at this point in the system (approximately +5 dBm maximum), at what duty cycle, and how their aging (calculated at 32 years) will suffer under these conditions, their insertion loss and their group delay properties. A second set was designed and manufactured by Alpha Components Inc., using a fundamental Gaussian design which can provide better resistance to high drive levels. Although a narrower bandwidth was desirable, at 75 MHz, a 10 kHz bandwidth was the best that could be done considering all other design criteria.

It should be noted that despite popular belief, narrowing bandwidth in roofing filters for up-convert transceivers, although very desirable, it is not by far as important as creating crunch proof front ends such as done in IF75BC. Roofing filters of 3 to 4 kHz bandwidth at 75 MHz that withstand high RF levels are hard to realize and manufacture consistently. High dynamic range 75 MHz roofing filters with a 3 dB bandwidth of 10 kHz and high intercept points are, however, possible. Reducing the first IF frequency to a lower frequency, can ease the design of these filters at the cost of more demanding front end filtering to cope with image and spurious rejection. Going to low first IFs of, say, 9 MHz

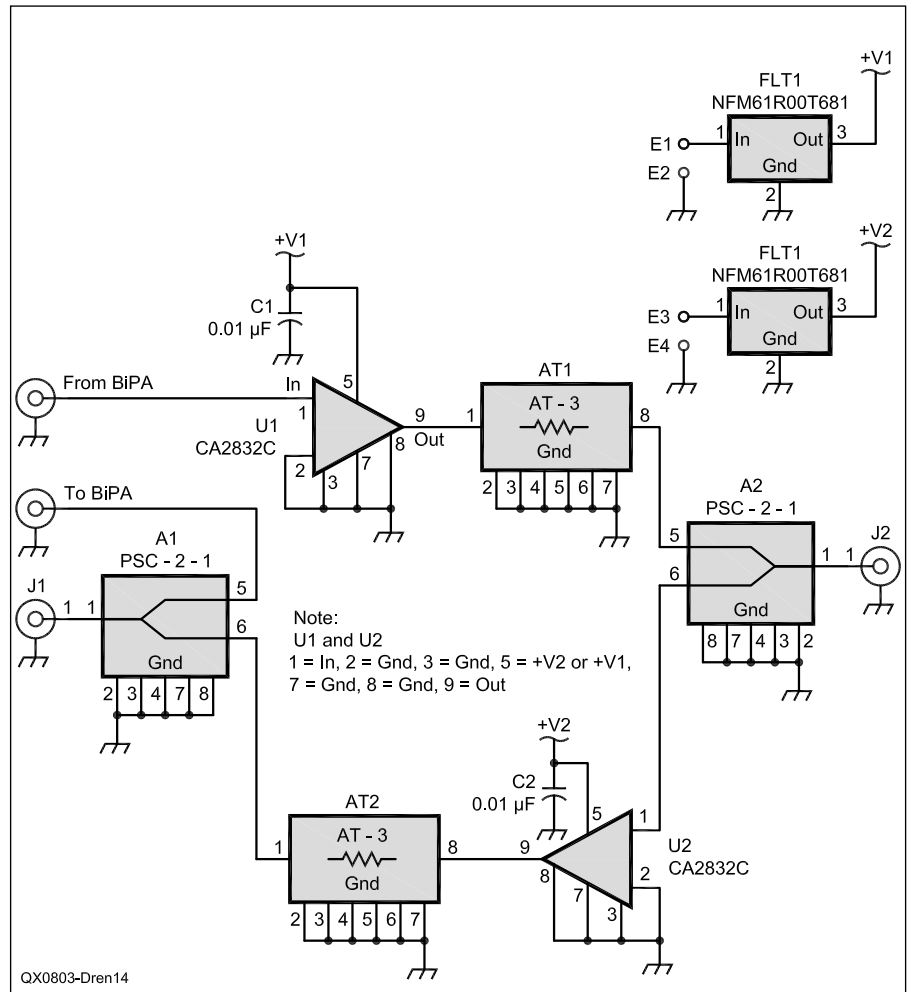


Figure 14 — This is the schematic diagram for the BILAT AMP assembly. This circuit provides high dynamic range selective amplification - bilateral functionality with automatic passive isolation (without using relays) between the active section and the off section, depending on whether the receive or transmit function is selected. The customary 3 dB impedance matching pads at the output of the amplifiers were later eliminated in the interest of gain and noise figure.

can allow for narrow roofing filters of 2 to 3 kHz (compatible with the ultimate bandwidth required of SSB signals); however, the entire idea of a high performance general continuous coverage transceiver can be thrown out the window, resulting in a compromise — channelized band-only, coverage.

Returning to the BILAT AMP assembly, the AT1 and AT2 pads seen in the BILAT AMP have been provided for amplifier matching. However, after long experimentation, they have been removed from the circuit in the interest of gain and noise figure improvements.

The output of the second section of FL75 is input to the IF9BC assembly along with the wide (500 kHz) 75 MHz IF signal intended for spectrum analysis (see Figure 2 in Part 1). The IF9BC assembly is the second bilateral converter which provides 9 MHz receiver IF signals to IF9RX and accepts 9 MHz transmitter IF signals from IF9TX. The wide band 9 MHz IF is further input to IF9NB, which in turn, provides oscilloscope, spectrum analyzer and noise blanker functions for the transceiver. Again, this is shown in the block diagram in Figure 2 of Part 1.

Looking at Figure 15, the two 75 MHz paths are input at J1 (wide) and J3 (narrow) to be converted to 9 MHz IFs separately via two independent high level mixers paths (Mix 1 and 2) in IF9BC using class II, TAK-3H mixers as shown.

Figure 15 shows the 84 MHz fixed frequency LO coming from the MRU (master reference unit) / PLXO, which is filtered and amplified by a class A amplifier and enters the IF9BC at J2. The signal is split by the A1 splitter (another PSC2-1) and is presented equally to the two TAK-3H mixers with a level of +17 dBm. The top mixer IF output is filtered through a wide bandwidth band-pass filter, and is finally amplified by AR1 (a MAR-8 device) to be output to the IF9NB assembly at J4. The narrow-band 9 MHz IF (with a bandwidth equal to the composite bandwidth of the two 75 MHz roofing filters at FL75) coming from MIX2 (the other TAK-3H mixer) is conditioned via the diplexer circuit of L10, C16, R5, L9 and C15, and is split by A2. The first half is output via a 1.5 dB pad through J5 to go to the narrow band receiver IF, IF9RX. The other half goes through another 1.5 dB pad and J6 to be connected with the narrow band transmitter IF when activated. I will explain more about this in Part 3.

I will now discuss the previously mentioned BIPA function using a Pi configuration PIN attenuator provided on IF9BC. This attenuator provides adjustable front panel and first IF/RF gain and noise blanking gating, coming from the IF9NB. It could also be used as a second AGC loop (not implemented yet).

In Figure 15, the 75 MHz input coming from the BILAT AMP is at J7. The attenuated output resulting from the BIPA circuit is available at J8. Control is provided via E2A and B. The BIPA attenuator function is packaged on a 24 pin PC board layout which follows a 24 pin IC module physical design approach. A picture of the BIPA assembly is shown in Figure 16. The schematic diagram of the assembly is shown in Figure 17.

Looking at Figure 17, BIPA uses four voltage controlled 5082-3080 PIN diodes in a Pi configuration. The design was inspired by Raymond Waugh's article in *Microwave Journal* (reference 13). This design approach provides very good impedance matching and flat attenuation over a wide frequency band and can be used in many applications. In fact, I used this circuit in the 9 MHz transmit IF as a CW drive controller as we will discuss later in Part 3.

This attenuator design is very good. After extensive testing at 75 MHz, it was found that with a 3.5 V bias at pin 24 and a control voltage of 0.3 V dc to 10.2 V dc at pins 10, 11, and 12, a range of 43 dB (-45 dB to -2 dB minimum insertion loss) of attenuation can be obtained. Less than 2 dB insertion losses can be obtained with higher control voltages according to reference 13. With the circuit operated at 0 dBm (a rather high level) the third order IMD was -65 dB; at +10 dBm, third order IMD was -50 dB. Additional tests were conducted using 20 kHz tones spacing at 9 MHz (for the IF9TX function) with better results (-70 dB). The BIPA control on *Star-10*, with improved attenuation characteristics can be used not only for manual gain control, but also for muting the IF chain as commanded by the noise blanker. It can also serve as the second AGC control loop in the middle of the receiver chain, for an improved AGC system.

It was found that the minimum insertion loss of the BIPA circuit as applied in the *Star-10* system is about 2 to 3 dB (depending on cables and connectors used). When plugging this into the dynamic range analysis from Part 1, it can be seen that the MDS can be improved if this minimum insertion loss number could be reduced further. If implementing this circuit, a special effort should be made to further reduce its minimum insertion loss through increasing the bias voltage to the rail. This proved helpful in improving the MDS performance. An MDS of -136 dBm (versus the initial -132 dBm) was obtained by improving the minimum insertion loss and/or shorting out the BIPA circuit. This circuit can use a shorting feature utilizing a miniature RF relay similar to the one implemented in the preamp from the IF75BC assembly. The BIPA circuit is a remarkable circuit with outstanding attenuation range and IMD performance.

Master Reference Unit (MRU) / PLL Oscillator (PLXO84)

Next, I will direct our discussion from the receiver and transmitter signal path to the coherent local oscillators (LO) system used in the transceiver. As I previously explained in Part 1, *Star-10* is a “fully coherent” or “fully synthesized” system. This means that all local oscillator frequency sources in the double conversion superheterodyne implementation are locked to a single high stability - high spectral purity source whose performance is reflected in the total long term stability and phase noise performance of the system and is directly translated into the receiver's and transmitter's performance. A high performance master oscillator is required to provide reference frequencies for the synthesizer and all LOs. This master frequency source is the MRU (master reference unit) which generates the 84 MHz reference frequency local oscillator to be used further by the synthesizer (FRU) - FSYNTH and also as a direct fixed LO for converting the 75 MHz bilateral IF to the 9 MHz bilateral IF in IF9BC. Thus, the 84 MHz - MRU LO serves as both, a high quality reference for the two DDSs in the FRU - FSYNTH, as well as a high quality fixed LO for the second conversion. A fully coherent system with equally good phase noise performance at all mixer ports results.

Before going into the circuit description of the MRU, it should be noted that in calculating the phase noise contributions of all LOs in a complex coherent RF system such as *Star-10*, a careful synthesizer analysis should be performed to insure that they are all fully compatible with each other and with the MDS - phase noise and spurious performance of the radio itself. This means that synthesizer performance at all receiver/transmitter LO ports should be equally good throughout as phase noise translates directly dB per dB (minus the mixer loss) into the MDS of the radio within the IF band-pass of interest. Many receiver and transceiver designers do not take this fact into consideration as witnessed by receiver MDS being sometimes obscured (phase noise limited) by the converted poor phase noise. This rule also applies to frequency doublers of lower reference frequencies (for example 32 MHz \times 2 for 64 MHz) being commonly used to obtain master reference frequencies, implementation that loses phase noise performance by 6 dB (20 log 2) through the doubling process by the time it gets to the synthesizer and reflects badly in the LO outputs.

Synthesizer design should start with the highest technologically feasible reference frequency and dividing it down from there if necessary (not multiplying up as some companies do) and partitioning the synthesis for

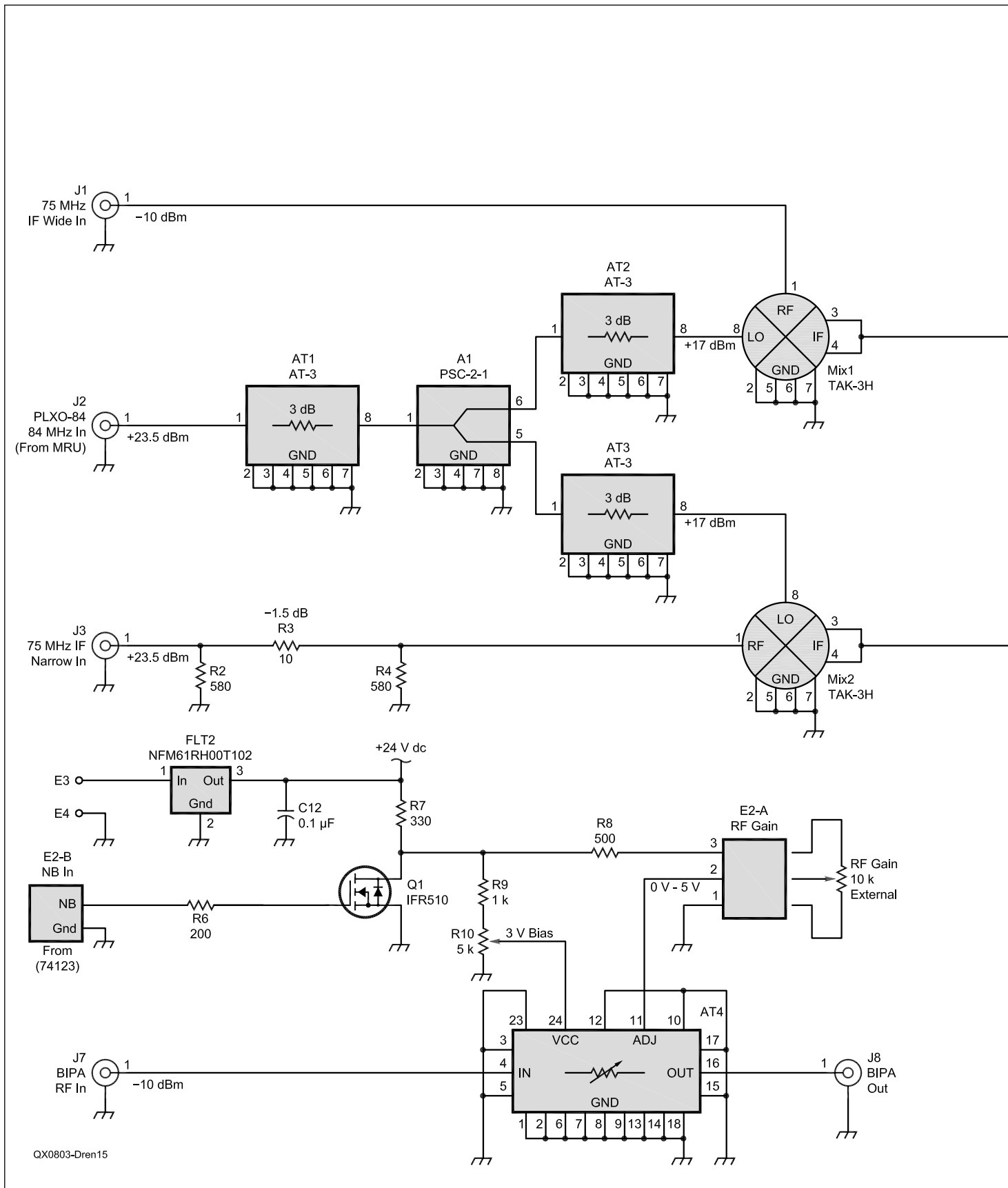
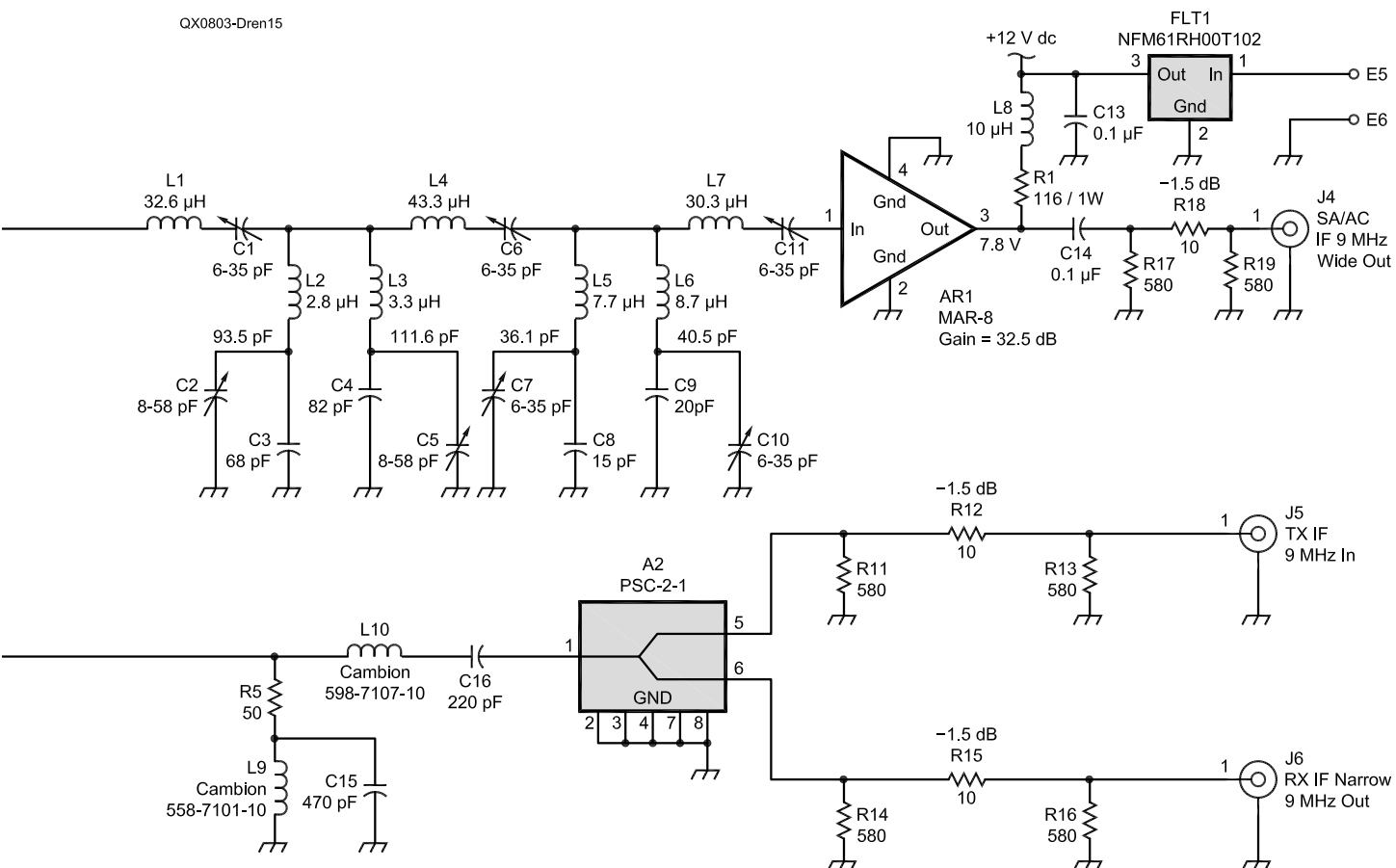


Figure 15 — This schematic diagram shows the circuit for IF9BC, the 9 MHz IF/bilateral converter.

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the various conversions such as to be fully comparable and balanced between all conversion stages. It does not do a system any good to have a good synthesizer as the first LO, while the second and third LOs in the multiple-conversion RF system are inferior in phase noise performance. The composite results will always reflect the worst LO performance.

The *Star-10* MRU schematic diagram is shown in Figure 18. The actual MRU assembly implementation is shown in Figure 19. Looking at Figure 2 of Part 1, it can be seen that the MRU consists of a 10 MHz OCXO providing the system's long-term stability of 1×10^{-8} after a 30 seconds warm-up, and an 84 MHz PLXO, locked to the stable 10 MHz OCXO for high Q – good phase noise performance of the 84 MHz master reference.

Looking at Figure 18, the *Star-10* MRU utilizes an 84 MHz - precision cut (0.001%) fifth overtone Quartz crystal (X1) with one side of the crystal grounded in a phase-locked series resonant Colpitts oscillator arrangement comprised of Q1 (2N5179), L2, L3, C3, C4, R2, R3 and R4. The Colpitts approach was chosen because of its well-known circuit stability while the 0.001% Quartz crystal cut was chosen to guarantee initial start-up almost on frequency before locking occurs. C3 and C4 are high Q, silver mica capacitors customary of the Colpitts implementation.

Looking at Figure 18, the 84 MHz Colpitts oscillator is initially tuned within its narrow resonance range via L2 and L3, which were calculated to resonate the Colpitts circuit on the fifth overtone of the crystal. Additional tweaking was required to bring the circuit into resonance due to board stray elements with L3 being the key-tuning element. This coil is wound using seven turns of #20 wire on a 1/4 inch molded plastic form and using a high-Q aluminium core as an initial frequency control element. L2 is wound in a similar fashion. More detail about this kind of circuit and its PLXO implementation can be found in reference 14, which is available on my Web site listed at the end of this article.

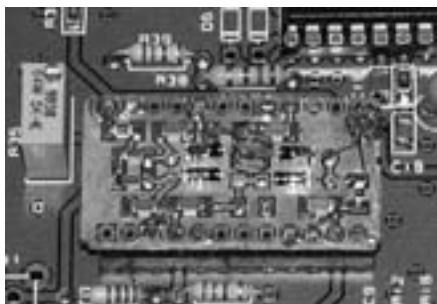


Figure 16 — Actual implementation of the BIPA Pi attenuator used in the IF9BC and the IF9TX assemblies.

The initial free running 84 MHz oscillator is digitally divided down by 84 for a 1 MHz square wave reference signal to be phase compared against a 1 MHz precision frequency signal obtained from the 10 MHz OCXO, as compared against the 10 MHz WWV signal. Upon power on of the *Star-10*, the default-received frequency is the 10 MHz WWV. An exclusive OR phase detector is used to obtain a dc correction signal which is fed back to the 84 MHz Colpitts oscillator via a simple loop filter and a varactor.

Here is how it works. Upon applying power to the MRU assembly, the high performance, low phase noise Colpitts Quartz oscillator starts up almost on frequency due to its 0.001% precision cut. The clean sine wave generated is further amplified by Q2, a 2N5109 transistor. The signal is then filtered using a similar 84 MHz Quartz crystal at X2 and is presented to the divide by two digital divider U1, a UPB1509. This high quality chip has analog to digital conditioning circuits, which allow for a clean 42 MHz signal to be produced. The 42 MHz analog signal is further conditioned/filtered in the IC for extremely low jitter, only to be filtered again via a 42 MHz tubular Quartz crystal filter at X3. The signal is finally presented to U2, a MAX999 low jitter comparator. The threshold of this chip is adjusted via a ten-turn potentiometer, R10. The MAX999 comparator is billed to guarantee a 4.5 ns propagation delay time at 100 MHz. This implies low jitter performance with rise times in the range of 2 ns or less, but experiments comparing

the 84 MHz directly through this device showed a relatively noisy signal. Thus, the divide by two conditioning resulted. Using a 42 MHz (less than half its frequency spec) signal into the comparator showed superior and stable (low jitter) results.

The clean 42 MHz square wave signal at U2 pin 1 is further presented to a digital divider string comprised of U3 and U4, two 74161 chips for a divide by 42 (7 and 6) function. A clean 1 MHz square wave results from the 84 MHz Colpitts oscillator, which is further presented to U9A, an exclusive OR phase detector. Further signal conditioning is achieved using U6, a high-speed 54S00 used as sequential gates. The other side of the phase detector is presented with a highly accurate 1 MHz comparison signal derived from the 10 MHz OCXO through another MAX999 comparator and a 50% duty cycle – divide by 10, IC at U8, a 74LS290 part.

It should be noted that the exclusive OR phase detector was chosen on purpose because of its narrow $\text{Pi}/4$ capture range which is exactly what is needed to lock a 0.001% deviation Quartz crystal over the operating temperature range of interest. Using a wider phase detector would result in more searching and additional jitter translating into inferior phase noise performance (something some engineers never learn). Exclusive OR phase detectors need 50% duty cycle digital signals, and locked condition is achieved when the two reference signals are out of phase by 90 degrees. These conditions are fully achieved in the *Star-10* MRU design

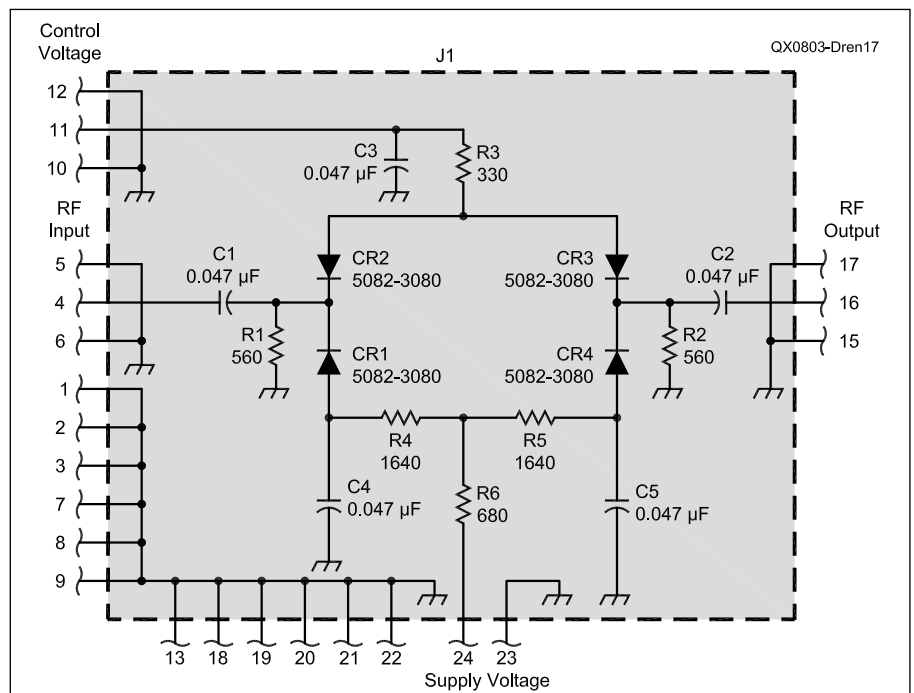


Figure 17 — This is the BIPA circuit diagram.

(note: A quieter mixer type phase detector was briefly considered, but found unnecessary since superior phase noise performance was already achieved with the simple exclusive OR design – see Specification table in Part 1).

The loop correction voltage is obtained at U9A pin 3. The signal is applied through the loop filter comprised of R11, R12 and C19 to the varactor CR1, a BB109. The loop correction signal (2.5 V dc when locked) is fed back to the 84 MHz Colpitts oscillator at the point between C3 and C5 which also serves as the output point of the locked 84 MHz oscillator to be amplified by Q3, Q4, Q6, and filtered by X4, X5, over two channels to provide +10 dBm to +13 dBm fixed reference signals to FSYNTH and serve as a second LO drive in IF9BC. Two additional fifth order tubular narrow band pass filters visible in Figure 19 help reducing further any harmonic spurious content.

It was initially feared that the 1 MHz reference square waves would generate multiple markers at every MHz throughout the HF range. Because of the comprehensive filtering, used, this has not been the case.

For more in depth information on the works of a PLXO MRU and its exclusive OR phase detector, please refer to references 14, 15 and 17.

Operation of the MRU is simple and automatic. Upon turning the power ON to the *Star-10* transceiver, the loop searches within the first 30 seconds for the 10 MHz OCXO signal, which is forced into a quick, warm up mode (the oven heats up). The 84MHz signal searches back and forth quickly at a decreasing frequency of approximately 10 Hz and down until the oven in the 10 MHz OCXO reaches its internal temperature (over 100 degrees F) and an exact 1 MHz reference signal is obtained and heard by the receiver beating against the 10 MHz WWV signal. A front panel yellow LED reports to the operator this lock-up process. At this point (MRU locked), the receiver can be redirected to the frequency of interest via the keypad, or via the optoencoder using the proper digit underscore marker on the main dial. All LOs in the *Star-10* are now coherent with the MRU and WWV within 1×10^{-8} and operation can begin. The radio is now guaranteed to be exactly on frequency in receive or transmit regardless of where it is tuned within the 1.8 MHz to 30 MHz range. No drift.

Frequency Reference Unit (FRU) Frequency Synthesizer - (FSYNTH)

The frequency synthesizer in the *Star-10* transceiver is a microwave DDS-Driven PLL running from 770 MHz to 1050 MHz. The idea of DD-Driven PLL is not new. I introduced this idea at RF Expo – 1988,

in Anaheim, California (see reference 15). Since then, the majority of transceivers on the market use this concept to generate high-resolution local oscillators frequencies. The synthesizer in *Star-10* goes a step further by generating the LO frequencies at ten times the required frequency range, or 770 MHz to 1050 MHz for improved phase noise performance after a division by 10, which facilitates a 6 dB improvement at the divided down 77 MHz to 105 MHz. This design takes advantage of the reduction in percentage bandwidth offered by the microwave design by using a single VCO (instead of four). The FSYNTH design has been discussed in detail in references 16 and 17. Additional information can be found in reference 18. The schematic for the FSYNTH assembly is shown in Figure 20 and its physical implementation is shown in Figure 21.

Looking at Figure 20, the FSYNTH assembly uses two DDSs, both AD 9850 to generate the variable PLL reference for the DDS-Driven PLL LO as well as the BFO LO. The 50-ohm 84 MHz reference signal coming from the MRU PLXO is input to the FSYNTH assembly at J1. From this point on, it is equally distributed between the two AD 9850 DDSs at pins 9 of U1 and U2. The word-clock commands information for both DDSs coming from the DFCB command and control assembly are input at J1. The command and control assembly will be discussed later. The resolution of the top DDS (U1) is 1 Hz and results in 10 Hz after it gets multiplied by 10 in the PLL loop of the DDS-Driven PLL part of FSYNTH. The highly filtered (to prevent spurious) BFO DDS has a resolution of 10 Hz. The ultimate resolution of FSYNTH as reflected in the transceiver's ultimate resolution from 1.8 MHz to 30 MHz is 10 Hz. For a much more in depth explanation of how the FSYNTH assembly works, please refer to reference 17, page 5. This reference is available on my Web site, which is listed at the end of this article.

Although new and improved DDS devices have evolved since the introduction of the AD9850, the fact remains that spurious performance is still the main challenge in DDS systems used as simplistic direct synthesizers, despite new and clever noise cancelling techniques that have been recently introduced. (See Analog Devices AD9959 Application Note: www.analog.com/UploadedFiles/Data_Sheets/AD9959.pdf, p 11.)

As such, the AD9850, if used properly, remains the workhorse of the Analog Devices family of DDS ICs even after all these years. An AD9850 DDS device used in a well-controlled, tight-loop, DDS-driven PLL can indeed exceed the spurious performance of simplistic DDS-only synthesizers

using even the most modern DDS devices.

The secret of this superior performance lays in a combination of design parameters, primarily in choosing a correct Nyquist reference frequency (References 15, 16, 17), and the proper interface of the DDS with the PLL phase detector, combined with a well designed loop filter in the PLL.

The FSYNTH performance has been improved since its original design through constant tweaking of the loop filter and a better selection of parts in the microwave divider section and the squaring circuits. This design is capable of -133 dBc/Hz performance from 2 kHz through 20 kHz offset at the divided down output. This performance has been tested and documented as shown in Figure 22. Further phase noise improvements will be discussed in Part 3.

Additional improvements in phase noise performance can be obtained by altering the loop bandwidth and other circuits at the cost of other parameters such as end-to-end synthesizer lock-up split operation and others.

Command and Control Assembly (DFCB)

The command and control assembly - DFCB is the heart of the *Star-10* transceiver. It provides the smarts and the friendly user interface for the system. The system control is achieved through the microprocessor board (part of DFCB) which houses the PIC-17C44 chip discussed in Part 1, its associated hardware, software, and the back-light LCD display assembly viewable through the front panel. This is packaged together on the DFCB, and is used together with the keypad data entry board and the optoencoder and all other user interfaces and controls located behind the front panel of the transceiver as shown in Figure 23.

The command and control system addresses all frequency and mode commands in the FRU — FSYNTH, as well as the various associated frequency selection commands to the half-octave front end filter banks, the ultimate bandwidth and mode selection commands for the receiver IF9RX and IF9TX, the T/R control commands, debouncing delayed Morse code key commands which work in conjunction with the synthesizer split lock-up functions and even display light intensity and multiple sound feed-back tones audible through the receiver's audio amplifier upon depressing keys on the key pad data entry shown on the right side of Figure 23.

The microprocessor code embedded into the command and control system is represented by what the *Star-10* transceiver really does, as commanded from the front panel of the radio. The command and control - DFCB system is primarily capable of addressing

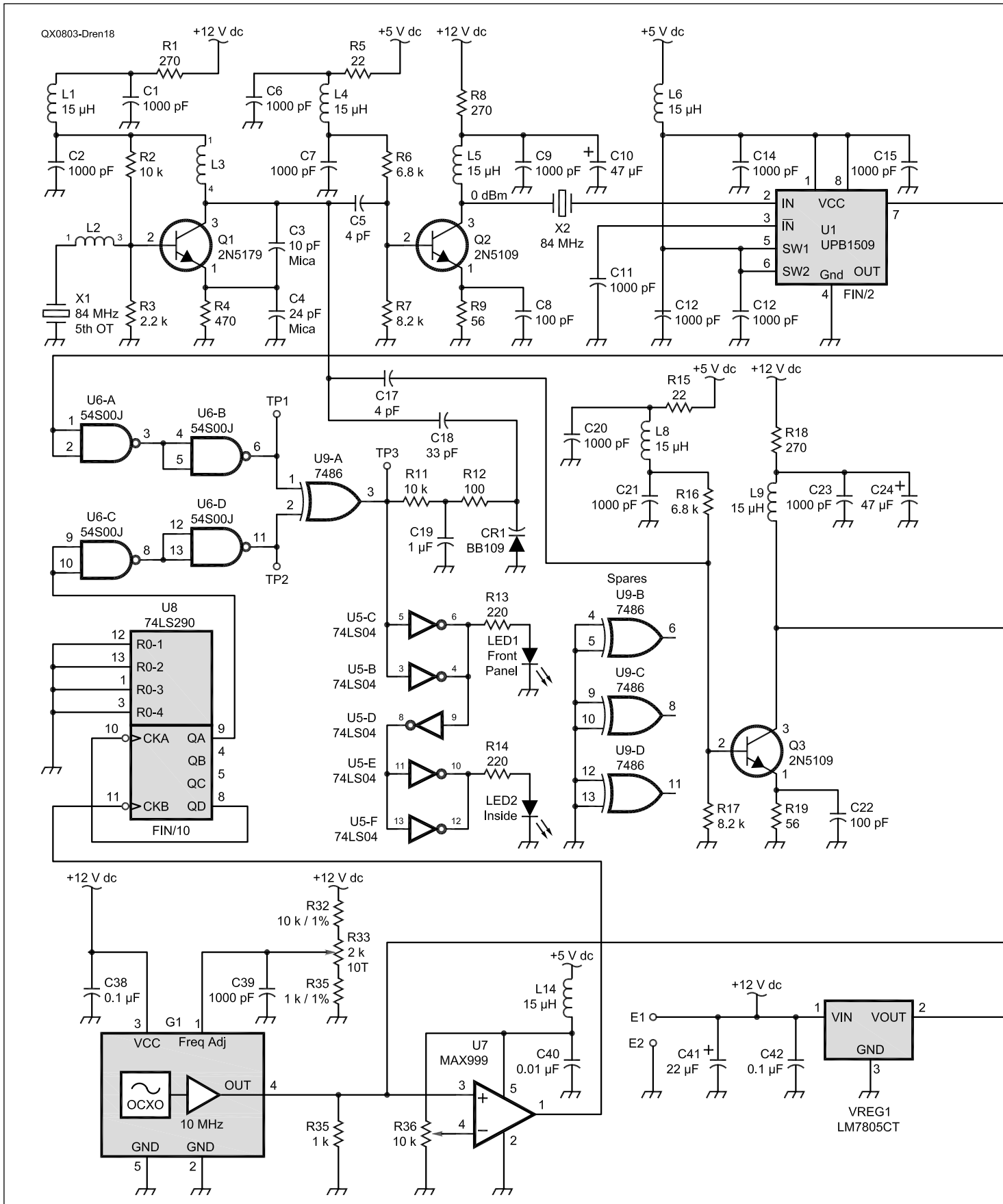
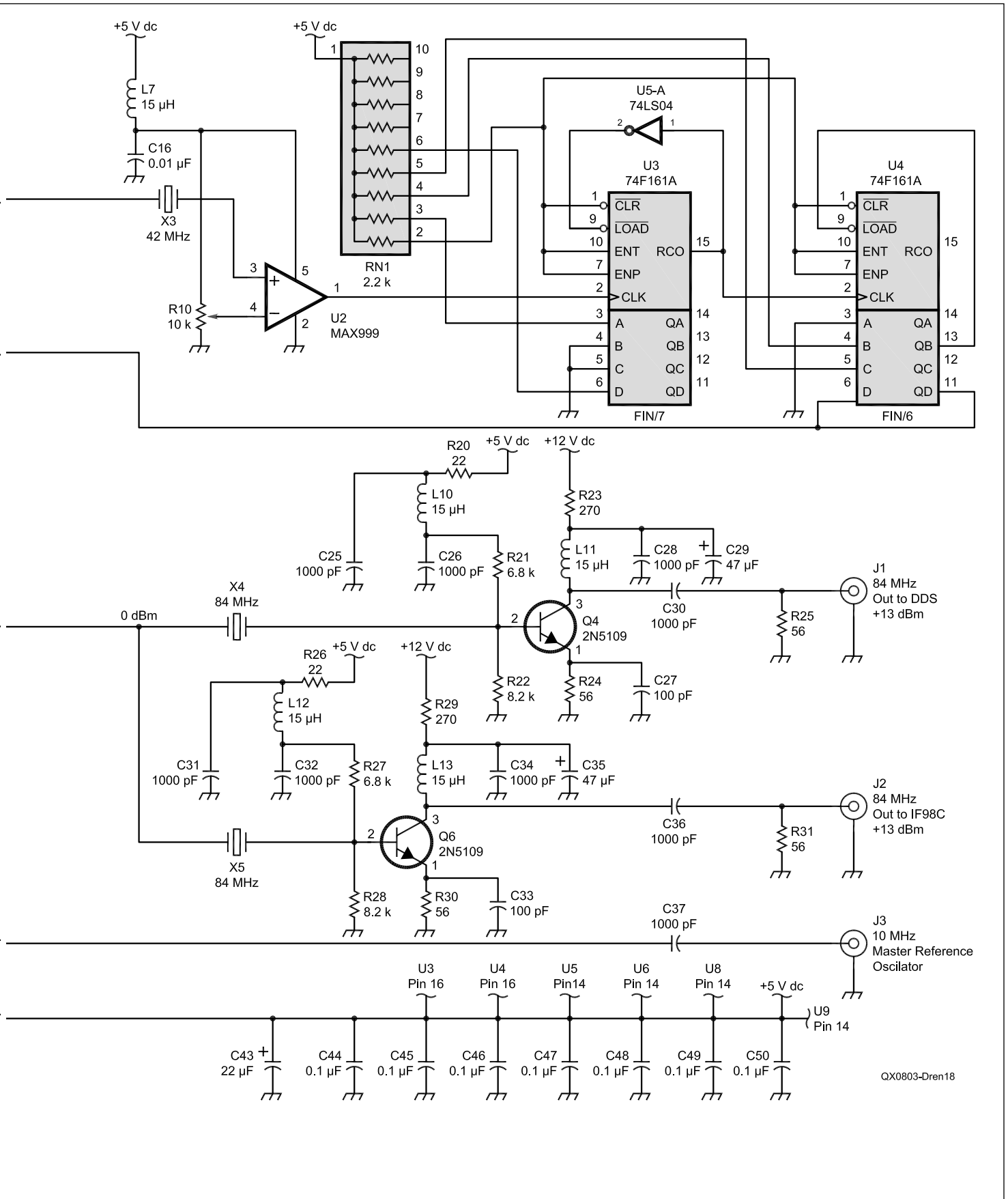


Figure 18 — Circuit diagram of the MRU.



either the main loop DDS-Driven PLL or the BFO DDS. The main synthesizer loop (the DDS-Driven phase-locked microwave loop) is controlled through direct keypad entry as taken over by the optoencoder. When in the mode select mode, the keypad controls the microprocessor such that the BFO/DDS-2 follows a fixed programmed function/frequency offsets from the nominal 9 MHz and as changed by the USB, LSB, CW, CWN, AFSK commands requirements. This programmability along with the entire transceiver's frequency sources programmability was previously shown in Table 1 of Part 1. Up/Down arrow commands are used on the keypad to enter RIT and RX and TX - PBT offsets. The PBT function allows selected TX or RX offsets to vary ± 1.5 kHz moving the IF BW and other sources in either side of the zero in either transmit or receive by using the main tuning knob. Once set, the IF PBT remains memorized, to be reset back only by the power off function. The RIT function accessible through the main knob when in RIT mode, allows for ± 9.9 kHz received frequency offset from nominal and gets reset to nominal zero by turning the transceiver power off. The schematic diagram of the DFCB assembly is shown in Figure 24.

Looking at Figure 24, the heart of the command and control system, DFCB is the PIC-17C44 microprocessor at U4. As can be seen, all I/O ports have been thoroughly used by the *Star-10* design. The microprocessor runs at 32 MHz as shown using the Quartz crystal oscillator X1 at pins 19 and 20. The reason for this frequency choice was described in Part 1 of this article series. Harmonics and products of this oscillator are outside of the receiver bandwidth. The switching RF noise produced by the display (which can be heard on a pocket AM Broadcast radio held in front of the display) does not impact the receiver because of the considerable shielding of the assemblies. There is absolutely no impact on the receiver MDS.

The keypad interface is shown on the left side of the drawing. The keys are arranged in a matrix of switches that address the microprocessor through closing user commanded keys via J4 A and B and through the 74HCT138 decoder demultiplexer at U2. Two OPTREX DMC-16230 N - EB displays (DISP 1 and DISP 2) using multiple green LEDs behind a dot matrix LCD for backlighting, are wired and addressed in parallel from the I/O ports as shown. Contrast adjustments are provided through R2 and R3. A switched "bright" function is facilitated by pulling more current through the display LEDs via the IFR510 FET at Q1. The bright command as well as the sound feedback command are implemented via the microprocessor by touch-pushing the main

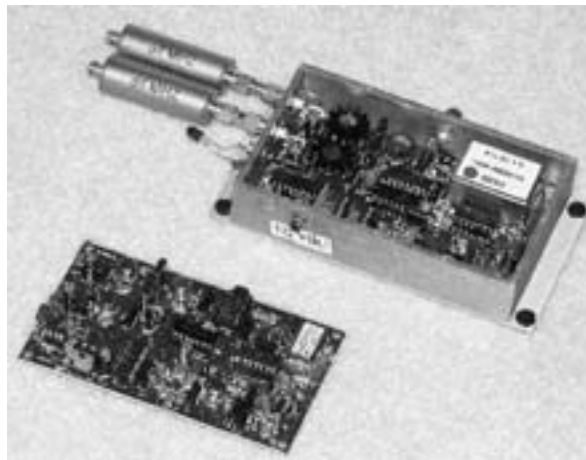


Figure 19 — The *Star-10* MRU assembly uses an 84 MHz PLXO for good phase noise as locked to a 10 MHz OCXO (WWV compared) for long term stability of 1×10^{-8} . A simplified version was also developed using a 16.8 MHz TCXO (bottom photo) but was abandoned due to the inferior stability of the TCXO as compared with the OCXO.

tuning knob through the push-push switch provided in the optoencoder. The optoencoder is an inexpensive 32 positions Clarostat unit wired through J2 directly into the I/O ports as shown. The 99 memories function is provided by the permanent memory IC, 25C060 at U1. Memorizing a frequency is easy by using the MR and ENTR functions on the keypad. The memorized frequencies are not erased with power off. They can only be erased by using the keypad and entering a new frequency in an addressed memory number from 1 to 99. The half-octave filters (receiver band-pass and transmitter low-pass) are selected automatically by the microprocessor and output through another 74HCT138 — a three to eight line decoder demultiplexer at U3 and through a tri-state inverting octal buffer, 74HC240 at U6. These logic signals are further carried via connector J5 to the half-octave filter banks via the mother board connectors located on the back of the main shelf as previously discussed. The logic arrangement at U5 A, B, C and D is intended for debouncing functions through the I/O interface connectors. Additional command and control signals are provided from this assembly to the FSYNTH, IF9RX, IF9TX and the T/R assembly via the J1 and J3 connectors. As with all other assemblies in the *Star-10*, proper voltages and regulation are provided via on-board variable and fixed regulators, in this case, a 7805 at VREG1. For reason of simplicity, the three LEDs that work in conjunction with the AIPA selector have not been shown in Figure 24. This completes the DFCB assembly description.

9 MHz Narrow Band Receiver IF (IF9RX)

I will next discuss the receiver narrow-band IF — IF9RX. Its design was briefly presented in Part 1 of this series. The ultimate receiver bandwidth requirements are established through the IF9RX assembly and its custom made Quartz crystal fil-

ters. Commands are received through the command and control assembly, DFCB. Conversely, the transmitted bandwidth for the SSB/AFSK transmit functions is established through a similar filter bank in the IF9TX assembly. This will be discussed later in Part 3 of this series.

As can be seen from Figure 2 of Part 1, the IF9BC main receiver output is further input to the IF9RX assembly. This IF path achieves the ultimate receiver bandwidth selection and amplification as commanded by the command and control assembly, DFCB.

The IF9RX board provides approximately 100 dB of AGCed gain (80 dB AGC control plus filter insertion loss compensation) using three high dynamic range (+15 dBm IP3) AD-603 logarithmic/linear IF blocks from Analog Devices. This choice was made after an intense search for the right amplifier device. Initially, the old and popular MC-1590 device was considered based on prior art (reference 19). After intense IP3 tests in the KG6NK laboratory using two-tone signals (1.5 kHz apart) at 9 MHz, with and without AGC applied, the IP3 performance of the MC-1590 was found to be inferior. The idea was quickly abandoned.

Several other choices were considered. Among them were the Analog Devices AD600, AD602, AD603, AD604, AD605 and Cougar AGC230. The Cougar device, while offering a third order intercept point of +21 dBm, was too expensive for this application. After ample conversations with Dana Whitlow of Analog Devices, I zeroed in on the AD603, an inexpensive high performance device. This is a low noise device with a bandwidth of 90 MHz, which can be powered from a single 10 V supply. It is a voltage-controlled amplifier, which provides gains of +9 dB to +51 dB (42 dB) and a "linear in dB" accurate and stable range suitable for a linear — in dB — S-meter indicator. It offers a -67 dBm AGC threshold. Its IP3 is +15 dBm. Its noise figure is billed at 8.8 dB. Quick system calculations revealed that if using two AGCed

AD603 devices cascaded with switched in Quartz crystal filters and followed by a third AD603 programmed to compensate for filters insertion loss can provide slightly over 100 dB gain with about 80 dB of AGC. Gain system implications revealed that AGC action and consequently S-meter action would start at approximately -103dBm signal at the receiver antenna input or an S-3 signal level. This was deemed as a good enough compromise considering the circuit complexity and a linear range of 70 dB shown on the S-meter from an S3 to an S9 plus 40 dB signal level.

Several breadboards were constructed and tested together with Dana Whitlow and Constantin Popescu, (KG6NK) using these ideas, and based on Analog Devices recommendations (see reference 20). An actual to-size first cut board was laid out courtesy of Bruno Santalucia (I6YPK). Because of the 100 dB gain provided by this important board, and the limited board size of 5.5 x 4.5 inches, the IF9RX board had to be laid out again to prevent possible oscillation. A special effort was made by KD7KEQ to provide extra ground stitching for the final layout.

The IF9RX concept was briefly discussed in Part 1 of this series. A block diagram and discussion appears in Figure 5 of Part 1. The IF bandwidth selection is provided by four 8-pole crystal filters for a total of 32 possible poles of selectivity. Instead of selecting individual filters as in conventional IF designs, the *Star-10* IF9RX filter assemblies are combined in a cascaded AND function (rather than an OR function) for a total of 32 poles (plus the 8 poles composite roofing filter) of superb selectivity. This cascaded architecture makes the IF9RX a unique design that works in tandem with the system's command and control software.

As shown in Figure 5 of Part 1, two 8 pole crystal filters with a bandwidth of 2.4 kHz are always used at the beginning and the end of the 9 MHz IF chain for good noise management. This idea was inspired by standard RF design procedures and by reference 18. Additional 8 pole crystal filters of narrower bandwidths are inserted or removed between the gain stages (for a maximum of 32 poles in CW Narrow mode) depending on the mode selection and as commanded by the DFCB. The selection is achieved with miniature RF Teledyne relays, just as in the front end of the radio (no diode switching for RF paths in this radio). Automatic insertion loss compensation control is achieved depending on the diverse filters configurations chosen so there is no difference in signal amplitude and S-meter reports when changing filters and bandwidths.

The schematic diagram for the IF9RX is shown in Figure 25 and the actual implementation of the assembly is shown in Figure 26.

Here is how it works. Looking at Figure 25, the 9 MHz receiver IF signal coming from one side of the bottom splitter in IF9BC is input to the IF9RX assembly at J3. It is then passed through the first 8-pole, 2.4-kHz-wide quartz filter, XF1. This filter and XF4 (an exact similar filter intended to limit the noise content of amplifiers) are always in the circuit. Two cascaded AD603 amplifiers U1 and U2 follow the first filter. They are AGCed at point A via the circuit containing Q8, Q9, Q10 and U7A. The AGC signal is derived at U3 as shown. AGC ON/OFF and time constant (FAST/SLOW) functionality from the front panel are provided through J1 along with IF gain and MUTE functions (through Q7). The attack time is fast in all modes (<2 ms) while the fast decay time is 0.5 seconds and the slow decay time is 4 seconds. The output of the AGCed amplifiers at U2 is further cascaded via additional Quartz filters XF2 and XF3. The operator controls the filter selection and insertion loss compensation from DFCB via the keypad depending on the mode and bandwidth selected. The filters are merrily inserted in the circuit or shorted out using miniature Teledyne RF relays as shown. Control signals are applied to U4, U8 and the relays (K1, K2, K3, K4, K5) via J1 and J2 as shown. The output of XF3 is further presented the third AD603 at U3 which inserts fixed gain compensation as set by R33 and R40 depending on the narrow filters selected (XF2 or XF3).

It should be noted that "narrow" means different things in different modes. In SSB for instance, "narrow" means that XF2 (1.8 kHz) was selected, while in CW or AFSK, "narrow" selects XF2 (1.8 kHz) and XF3 (500 Hz) for a total of 32 poles of cascaded selectivity. Conversely, "wide" means different things in different modes: In SSB for instance, "wide" uses XF1 and XF4 (both 2.4 kHz, 16 pole filters) while in CW, "wide" selects XF2 (1.8 kHz) together with XF1 and XF4 for 24 poles of filtering. The intelligence for these selections is actually built into the DFCB assembly and is part of the software design. The computer in DFCB actually understands which mode was selected from the keypad and makes the right decisions accordingly.

Metering functionality by switching from the S-meter function in receive to the RF power meter function in transmit is provided through J2 via K5. IF gain control is wired to the front panel control potentiometer via the J1 connector.

Some of the circuits in IF9RX are powered directly from 12 V dc. The AD603 amplifiers are powered from the +12 V dc input E1 through U5, a programmable LM317 regulator set at 10 V dc. Additional 5 V dc power is supplied to the 75451 line drivers (U4 and U5) via a 5 V dc regulator, U6.

Despite its relatively simple apparent design, the IF9RX assembly has been a challenging IF to implement, because of the very high gain requirements and the relatively small space available on the board. Its novel cascaded functionality has proven to be well worth the extra effort of diverting from the classic "one filter at the time" mode selection of the past.

This concludes Part 2 of this article series. In Part 3, I will discuss the receiver product detector Assembly (PDAF), the transmit / receive (T/R) controller, the 9 MHz transmitter IF (IF9TX), additional assemblies, power linear amplifier, the EMI-quiet switching power supply, putting it all together, the final performance tests and conclusions as well as the lessons learned.

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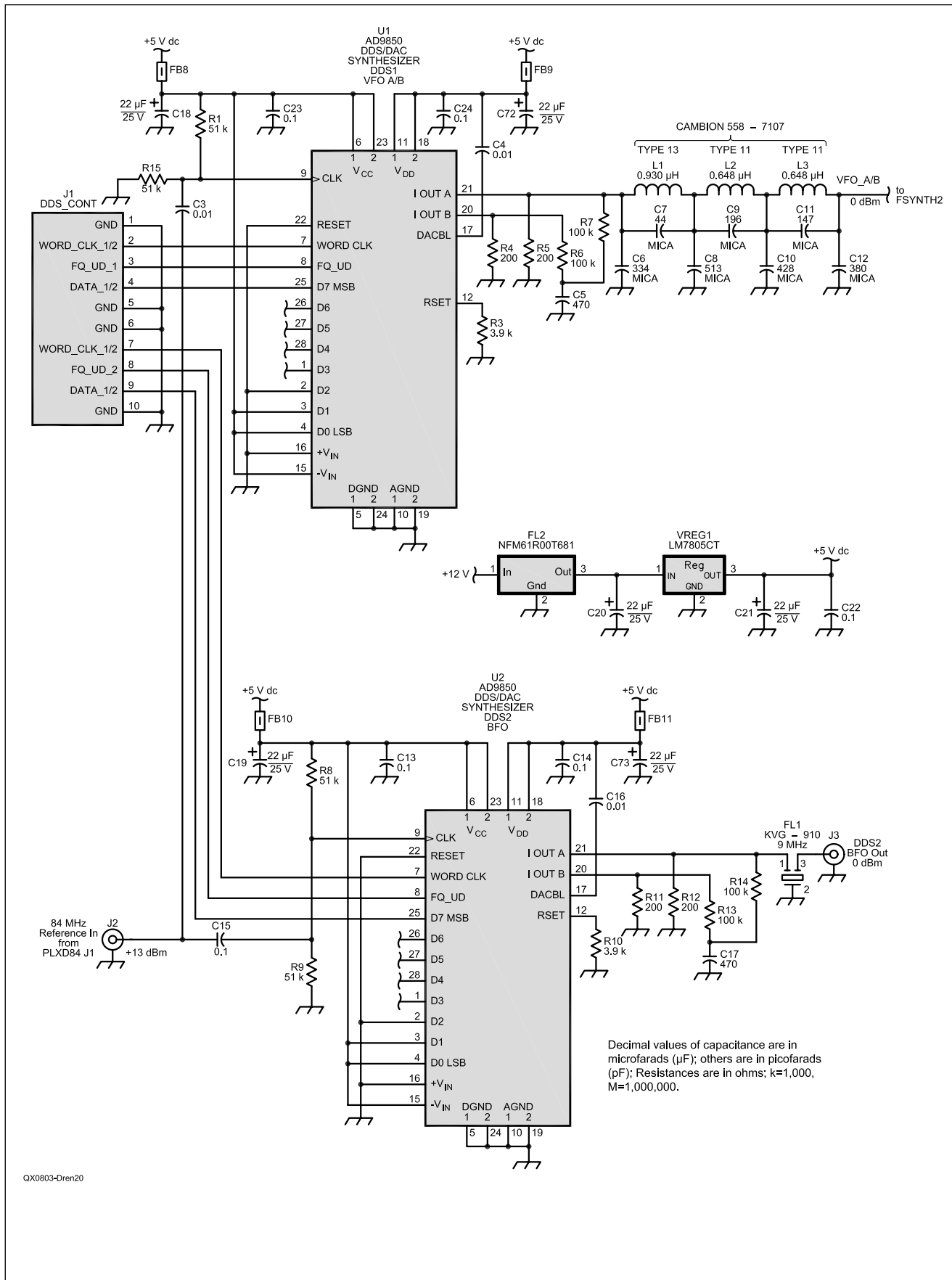
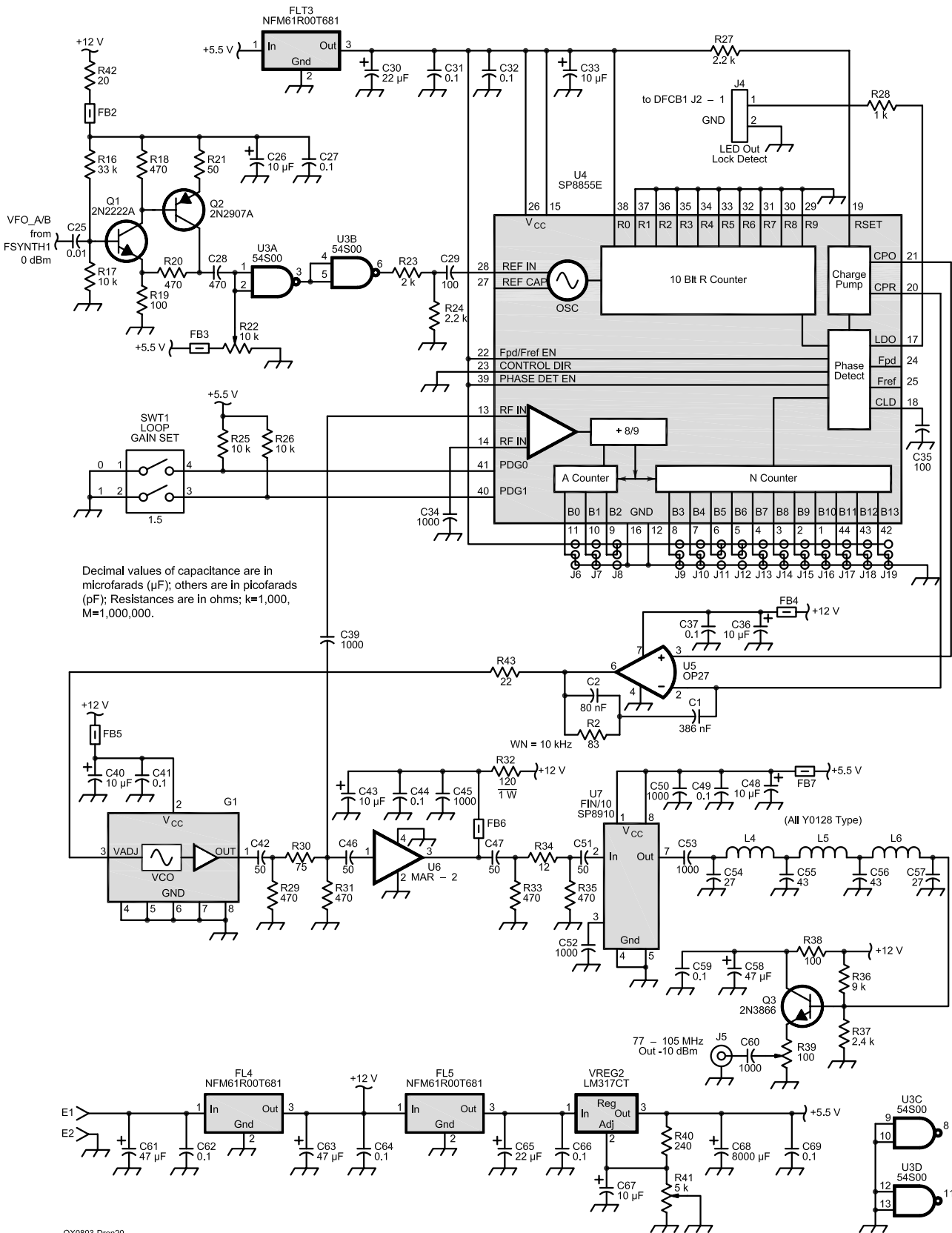


Figure 20 — Schematic diagram for the *Star-10* frequency reference unit (FRU), FSYNTH.



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Figure 21 — Actual FSYNTH assembly implementation.

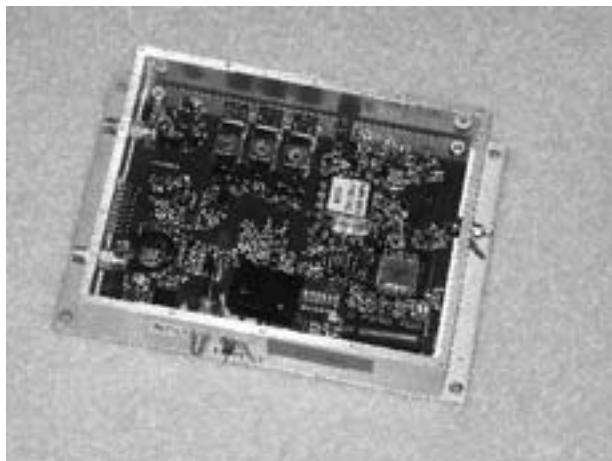


Figure 22 — Phase noise performance of the Star-10 FSYNTH assembly shows a close in performance of -133 dBc/Hz at 4 kHz. The photo shows total performance from 500 Hz to 20 kHz from the carrier. This test was performed directly at the output of the synthesizer at 89.2 MHz (14.2 MHz). A rather tight loop bandwidth was chosen (see reference 17) and shows the normal "hump" created by the super imposing of the VCO phase noise with the loop bandwidth. The FSYNTH loop bandwidth is optimized here for close in performance (from 500 Hz through 4 kHz) since this noise content is reflected dB per dB through the transceiver's mixers especially in the receiver performance.

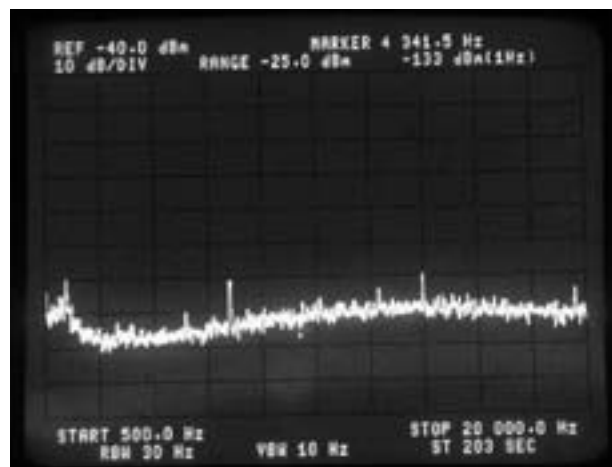
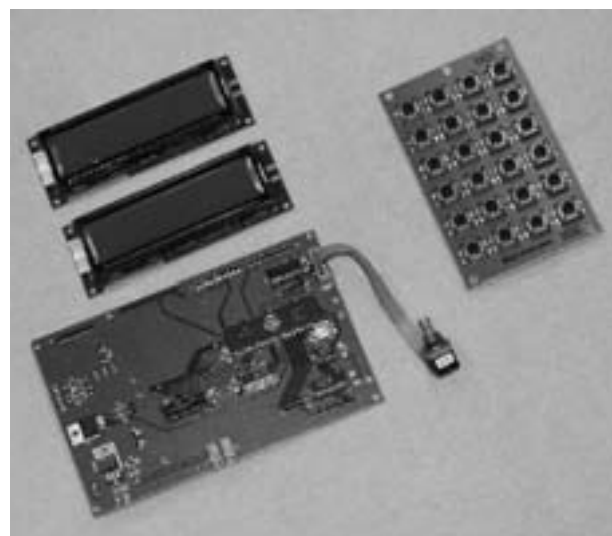


Figure 23 — The command and control assemblies behind the front panel contain the main DFCB board (with microprocessor shown), the optoencoder, the 64 characters displays that plug into DFCB board and the key pad board, all interconnected with ribbon cables. See text.



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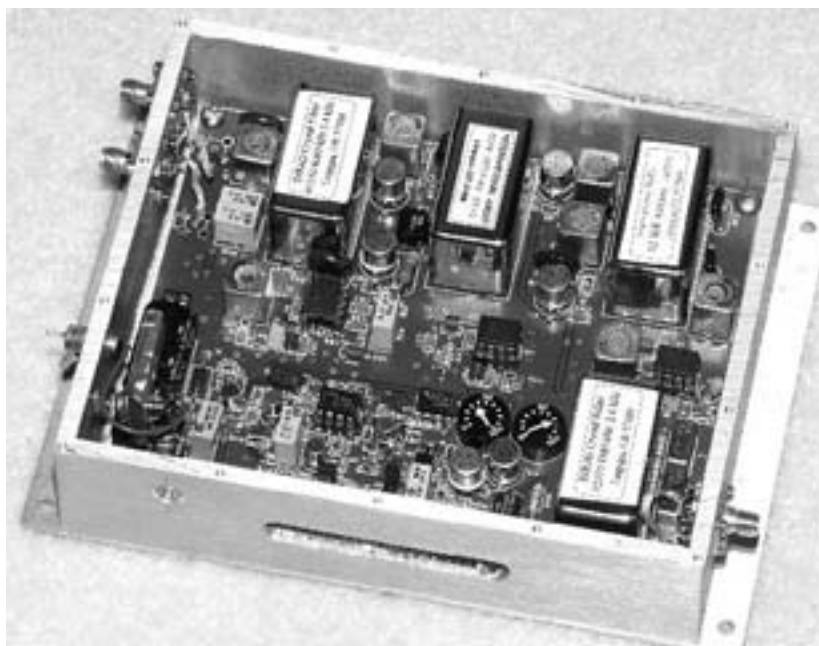


Figure 26 — Actual implementation of the IF9RX assembly. A specific double side ground plane stitched - plated through layout is used to maximize isolation between input circuits and output circuits in order to prevent oscillation in this very high gain (100 dB) assembly. All Quartz filters on the assembly have been expressly manufactured for the Star-10 by International Filter Company.

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Cornell Drentea, KW7CD, has been a ham since 1957. He has built many radios and transceivers and made his passion for designing "radios" his lifelong profession. As an amateur radio operator, he is known for his extensive RF technology articles in magazines such as ham radio, Communications Quarterly, RF Design, and QEX. Professionally, Cornell is an accomplished RF technologist, an engineer and a scientist with over 40 years of hands-on experience in the aerospace, telecommunications and electronics industry. He received his formal education abroad with continuing studies and experience achieved in the United States. Cornell has presented extensively on RF design topics at technical forums such as IEEE, RF-Expo, Sensors-Expo and has given comprehensive professional postgraduate courses in RF receiver design, synthesizer design, sensors and communications. He has published over 80 professional technical papers and articles. He is the author of the book, Radio Communications Receivers, McGraw Hill, ISBN 0-8306-2393-0 and ISBN 0-8306-1393-5, 1982. You can find out more about Cornell, on his web site: members.aol.com/cdrentea/myhomepage/

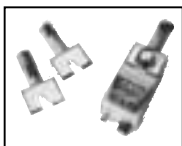
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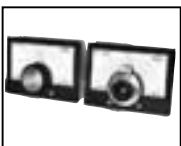
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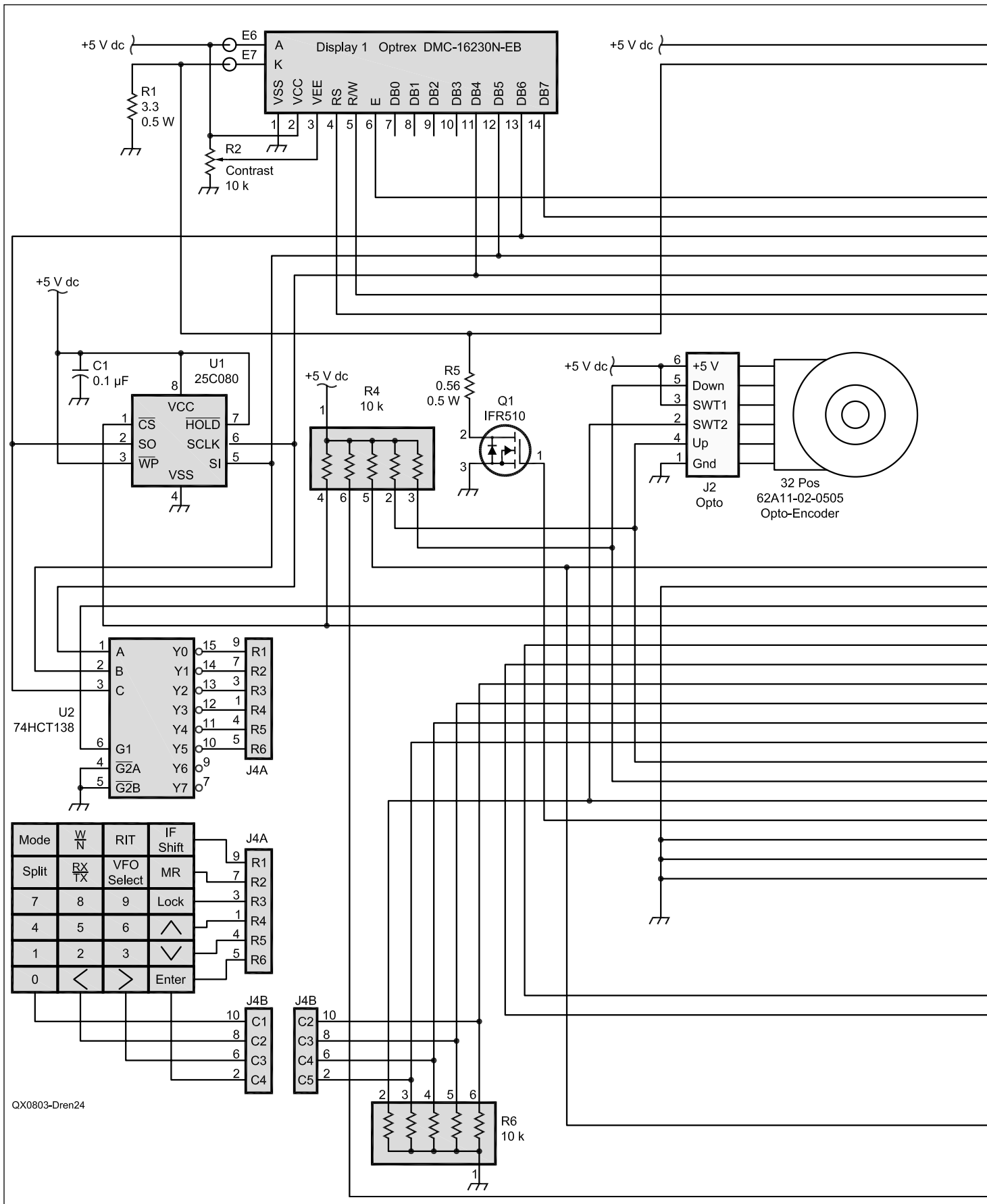
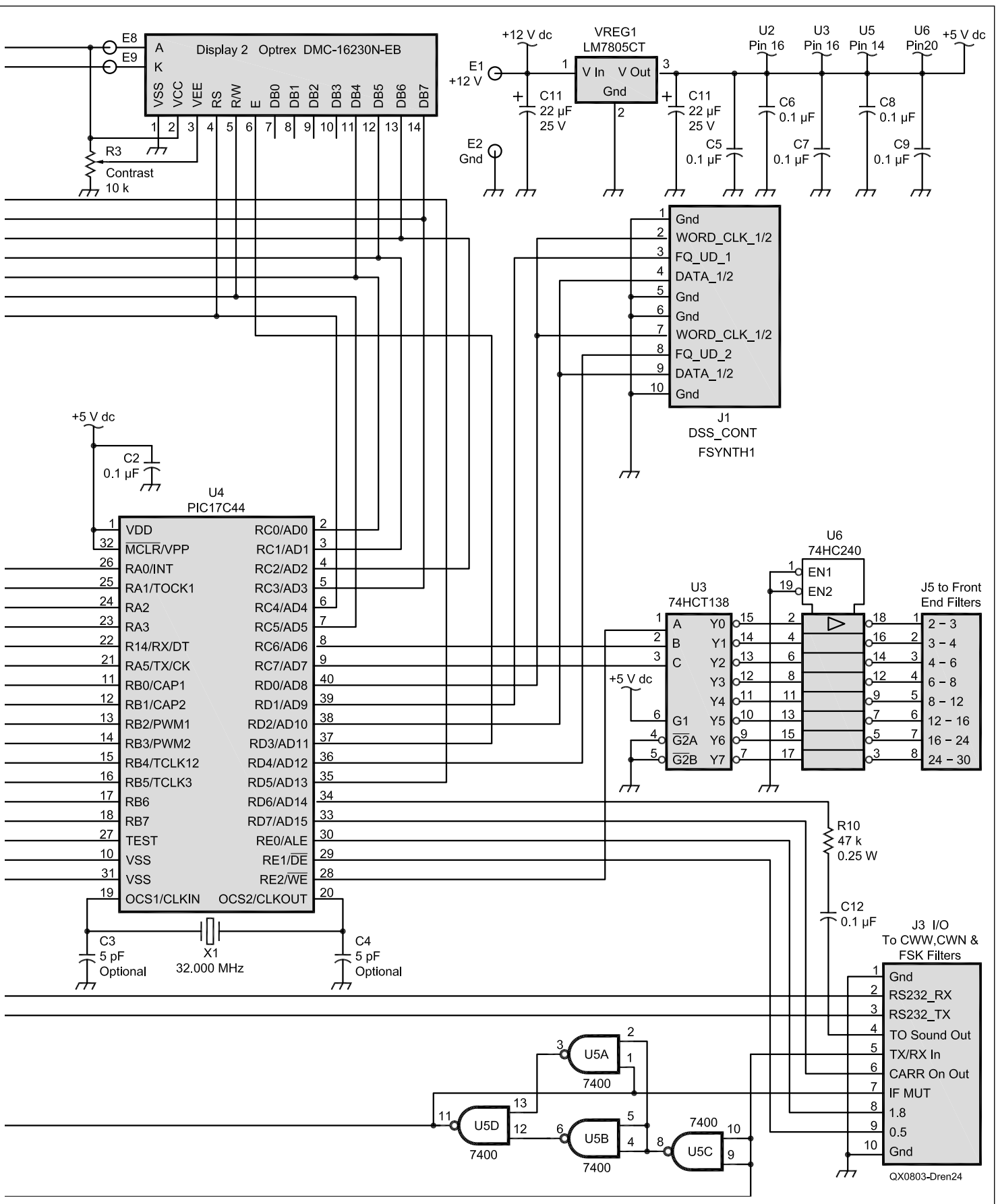


Figure 24 — Schematic diagram of the DFCB command and control system.



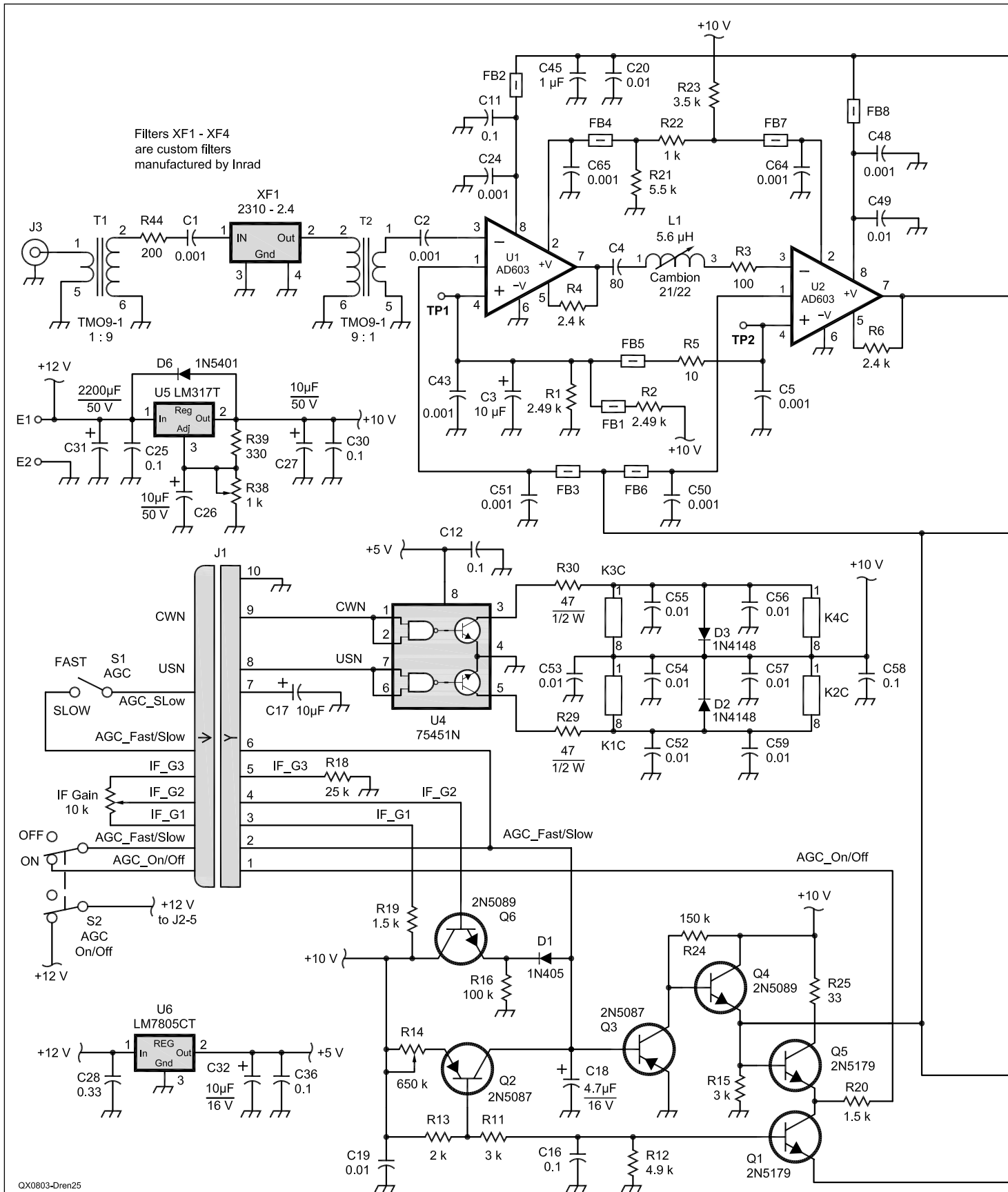
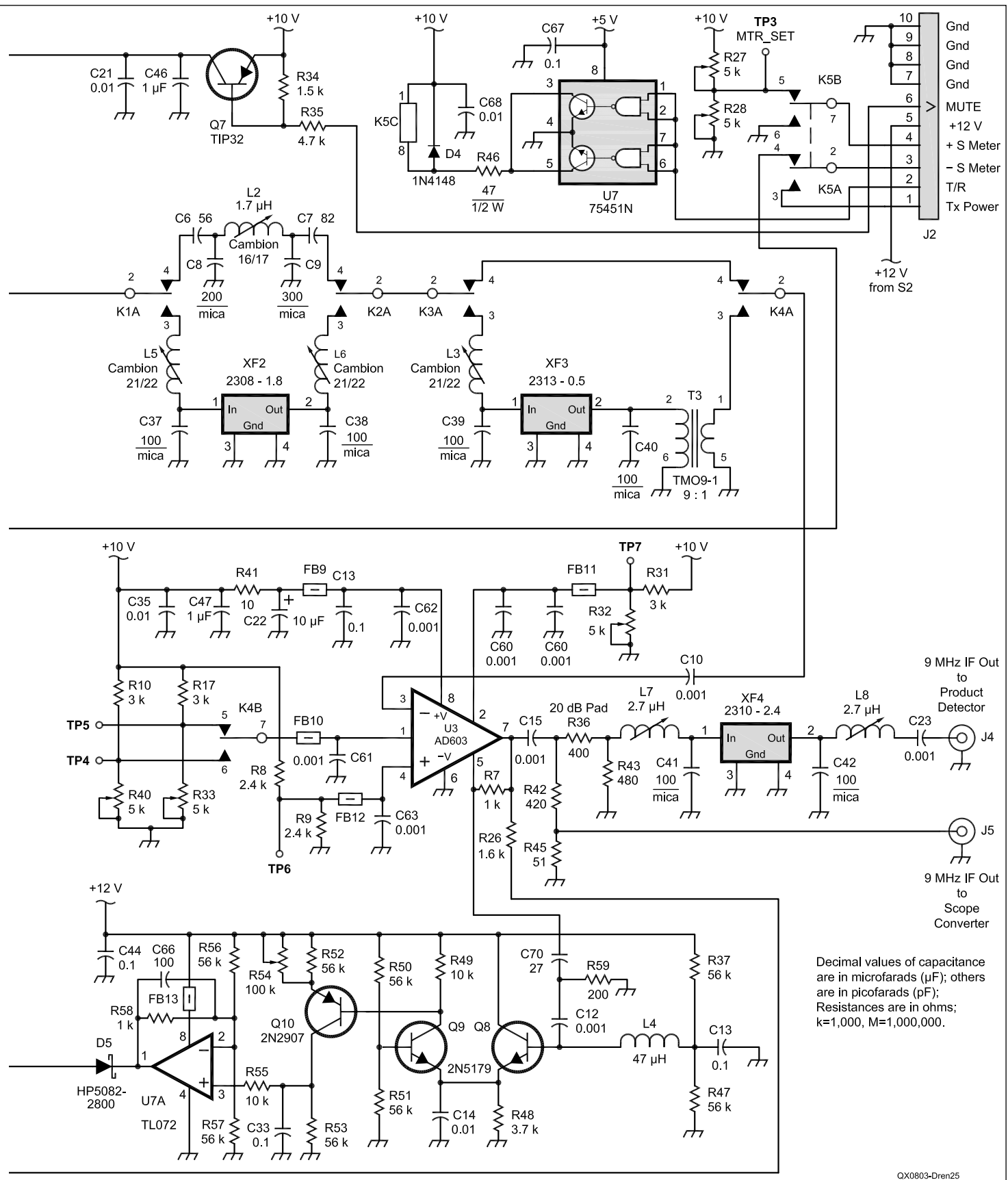


Figure 25 — Schematic diagram of the IF9RX assembly. Two 2.4 kHz - wide filters (one at the IF input and one at the IF output) are always in the circuit. Additional filters for SSB narrow (1.8 kHz) and CW/AFSK narrow (500 Hz) are inserted or shorted out from the command and control DFCB assembly using the keypad and the intelligence built into DFCB microprocessor. Two AD603s are used for AGCed gain and



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a third AD603 is used after the 1.8 kHz filter and the 500 Hz filter to compensate for the insertion loss of the selected filters. All filters are cascaded in an AND function rather than selected individually in an OR function, to optimize shape factor and depending on the mode and bandwidth selection. 32 poles of maximum filtering are possible.

