Calgary 4 Bits OLED Module Application Instruction

Application Note AN018

For any discrepancies between this document and the product specifications, the product specifications take precedence.

Introduction

The objective of this application note is to serve as a design and application guideline for Calgary OLED display module with SSD0323 driver mounted on the SSD1325T6 TAB. The information presented covers device electrical description and operation, performance, programming parameters, and interfacing to a module controller. Reference to this document is the SSD0323 OLED driver datasheet.

Electrical & Mechanical Description

A single chip CMOS OLED driver with controller and internal 128x80x4 Graphic Display Data RAM allows 4-bit grayscale operation of the Calgary display, which consists of 128x64 pixels. The built-in controller also allows for software operation of the display module with its command set and data transfer through a parallel or serial communication interface. Each of 128 segment drivers is capable of providing the maximum source current of 300 µA to each column. The display is passive matrix and operated at a duty cycle of 1/64. Each row driver is capable of sinking 40 mA.

Figure 1 is a block diagram of Calgary module. It consists of a glass cell, COF tab and interface flex. The user supplies a display controller with an Intel 80-series or Motorola 68-series CPU. A 30-pin interface flex is provided at the end of flex circuit for interfacing with the controller. The module is configured to use internal oscillator and external OLED driver power (VCC); **Internal DC – DC converter (VCC) for this design is not available**. The detailed pin-outs of the 30-pin interface flex shown in **Table 1**. **Figure 2** depicts the module driver connection diagram (*Please refer to **Appendix** for recommended interfacing details*).

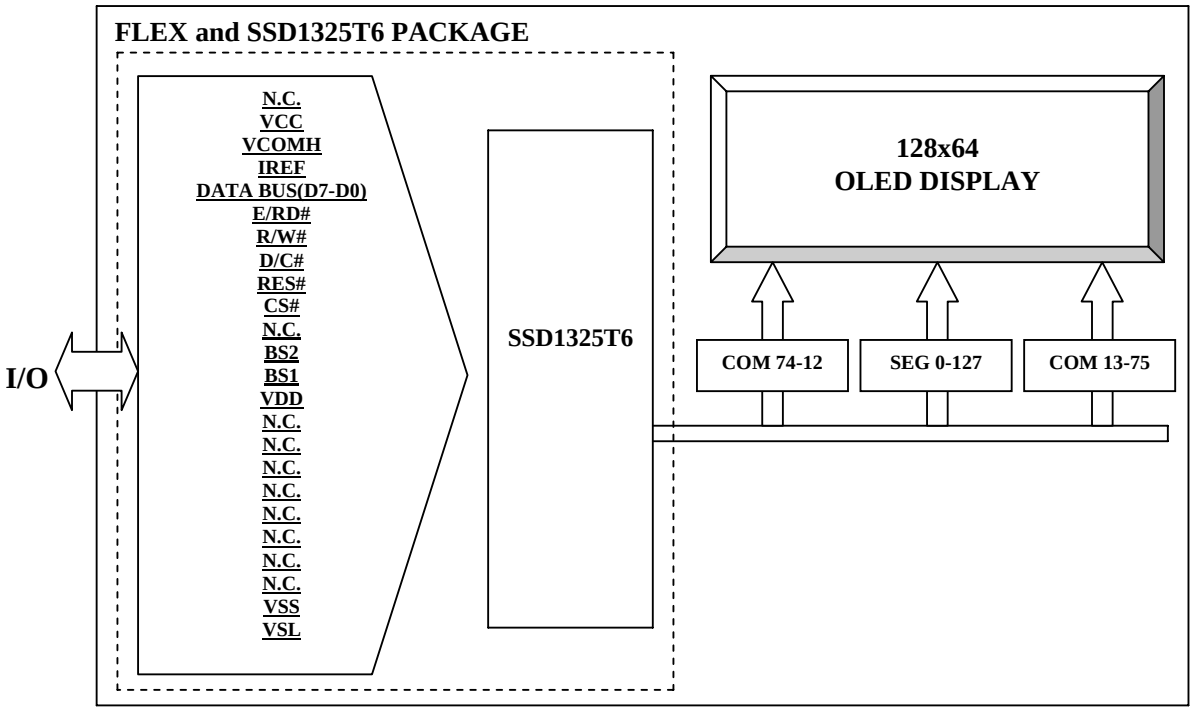


Figure 1: Product Block Diagram

Basic Specifications

Display Specifications

1) Display Mode : Passive Matrix
2) Display Color : Monochrome
3) Drive Duty : 1/64 Duty

Mechanical Specifications

1) Number of Pixels : 128 x 64
2) Panel Size : 74.00 x 41.86 x 2.20 mm
3) Active Area : 61.41 x 30.69 mm
4) Pixel Pitch : 0.48 x 0.48
5) Pixel Size : 0.45 x 0.45

Driver Connection Diagram

Recommended Components				
Part Name	Part Number	Description	Case	Qty
C1	EMK325F106ZF-T	Chip Cap 10uF 16V	1210	1
C2	F921C475MBA	Chip Cap 4.7uF 16V	1210(B)	1
C3	JMK107BJ105KA-T	Chip Cap 1uF 6.3V	0603	1
C4	JMK212F475ZD-T	Chip Cap 4.7uF 6.3V	0805	1
R1	RMC1/16-824FTP	Chip Resistor 820K Ohm	0603	1

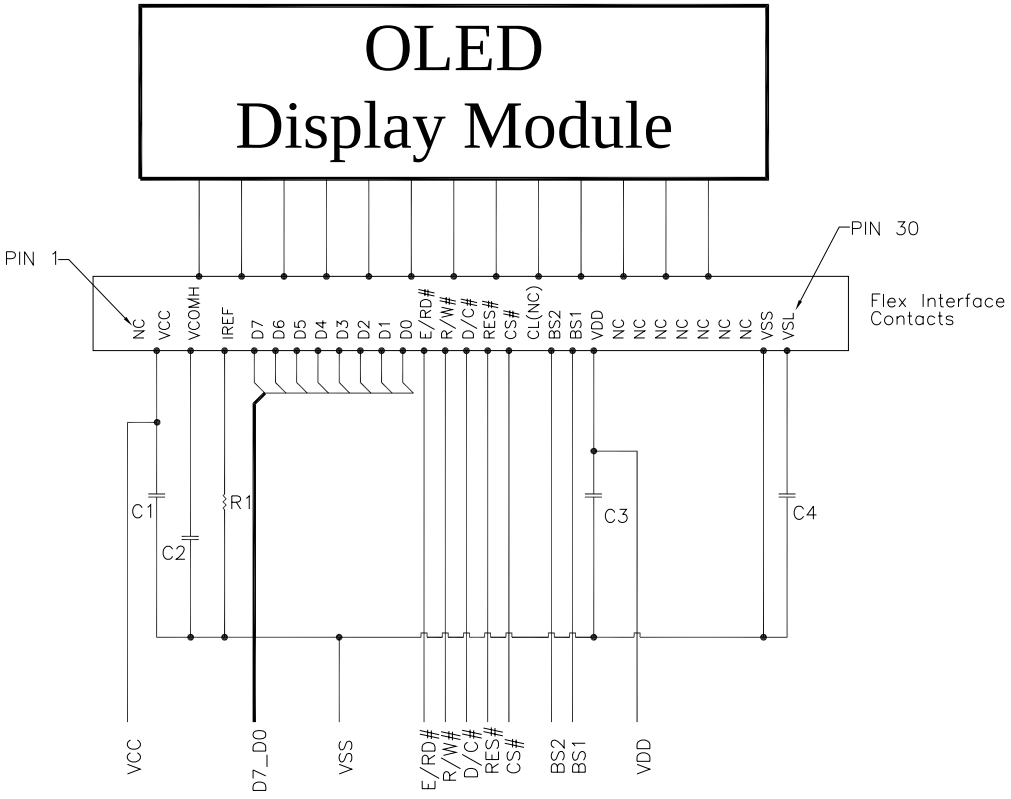


Figure 2: Driver Connection Diagram

In order to understand the way to connect the SSD0323, the input and output pins are classified according to their functionalities.

- Power supply pins
  - GND, VDD, VCC, VSS
- MCU interface pins
  - D0 – D7, E/RD, R/W, D/C, RES, CS, IREF, BS1, BS2
- Row and column output pins
  - Row 0 – Row 63, Column 0 – Column 128

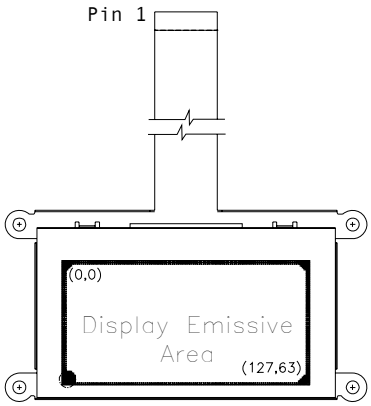


Figure 3: Connector Pad Orientation

The interleave configuration is used in the design of Calgary glass cell. Sixty-four common drivers are physically tied to the OLED glass cell leaving 16 un-connected drivers. The module orientation for this product is as shown in **Figure 3**. **Figure 4** shows the Calgary module driver connections.

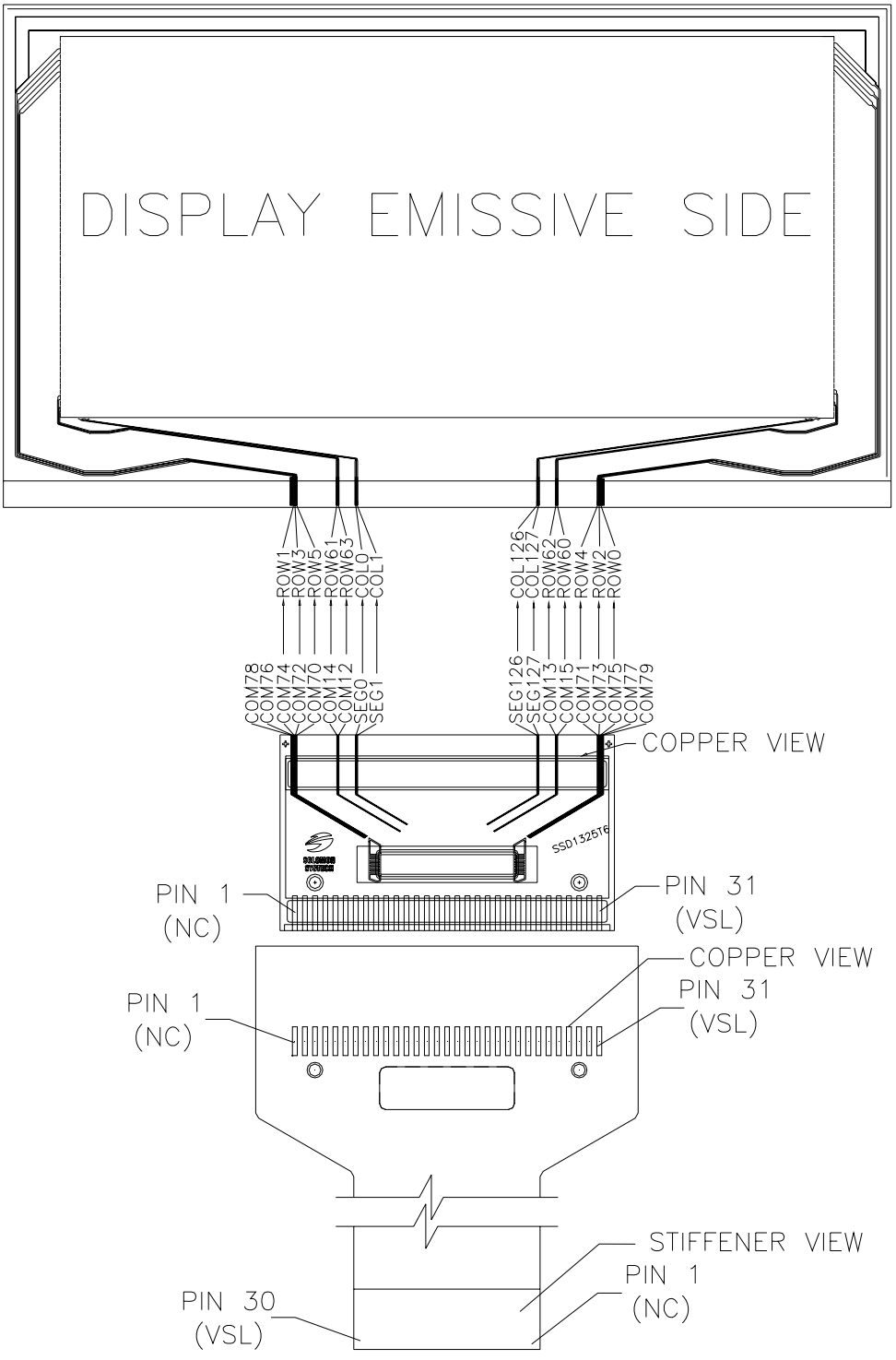


Figure 4: Calgary Module Driver Connection

Communication

Calgary module, H55XX, is configured for an 8-bit parallel or serial interface. The user can choose either the parallel or serial interface through the BS2 (Pin # 19) as described in **Table 1**. Detailed communication timing diagram is available in SSD0323 data sheet.

PIN	Name	DESCRIPTION	
1	NC	No connect.	
2	VCC(VLL)	OLED power supply voltage VCC (VLL)	
3	VCOMH	Common (Row) High Voltage, a capacitor should be connected between this pin and VSS.	
4	IREF	Segment (Column) Current Reference. A resistor should be connected between this pin and VSS.	
		Parallel	**Serial**
5	D7	Parallel Data 7	NC
6	D6	Parallel Data 6	NC
7	D5	Parallel Data 5	NC
8	D4	Parallel Data 4	NC
9	D3	Parallel Data 3	NC
10	D2	Parallel Data 2	NC (must be floating)
11	D1	Parallel Data 1	Serial Data
12	D0	Parallel Data 0	Serial Clock
13	E (RD#)	E clock for 68 series; RD strobe for 80 series	GND
14	R/W (WR#)	Read/Write selector for 68 series; Write strobe for 80 series	GND
15	D/C	HIGH = Bus contains data for DDRAM, LOW = Bus contains command.	
16	RES#	Reset.	
17	CS#	Chip Select.	
18	NC	No Connect.	
19	BS2	Interface Selection Pin 2:	
		6800 Parallel	**8080 Parallel** / **Serial**
	BS1	0	1 / 0
	BS2	1	1 / 0
20	BS1	Interface Selection Pin 1: See BS2 above.	
21	VDD	Positive logic supply voltage	
22	NC	No connect.	
23	NC	No connect.	
24	NC	No connect.	
25	NC	No connect.	
26	NC	No connect.	
27	NC	No connect.	
28	NC	No connect.	
29	VSS	Ground.	
30	VSL	Voltage Segment Low, a capacitor should be connected between this pin and VSS.	

Table 1: Flex Connection Pin Out

Power Up and Down Sequence

To protect the OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

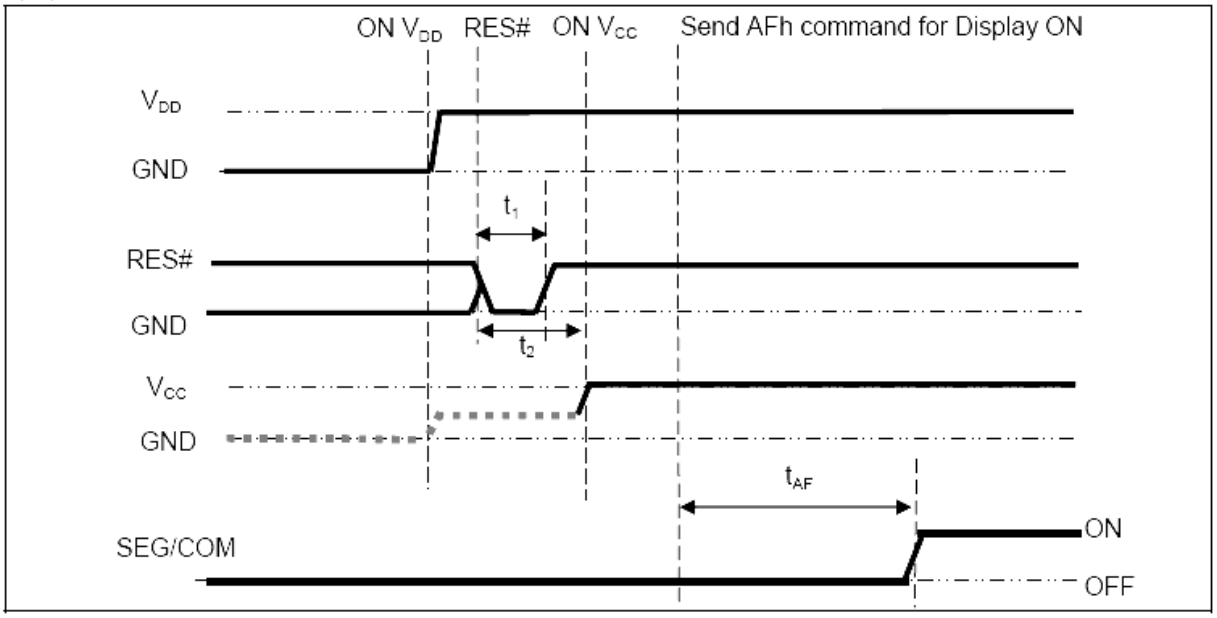
Power-Up Sequence:

i) Power-Up Vdd

ii) After V_{DD} become stable, set RES# pin LOW (logic LOW) for at least 3us (t_1) and then HIGH (logic HIGH)

iii) After set RES# pin LOW (logic LOW), wait for at least 3us (t_2). Then Power ON V_{CC}

iv) After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 30ms (t_{AF}).



Power-Up Diagram

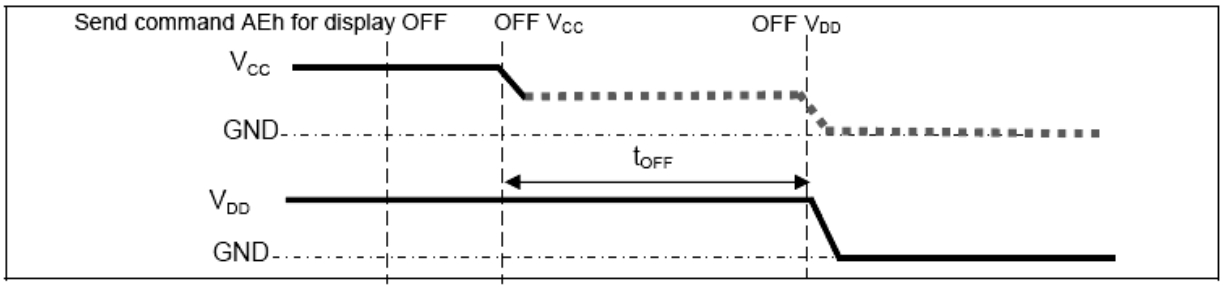
Power-Down Sequence:

i) Send command AEh for Display off

ii) Wait until panel discharges completely

iii) Power down Vcc

iv) Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=30ms)



Power-Down Diagram

Power connection

One ground and two power connections are required to operate Calgary module. The logic power, VDD, is 3 volts, the OLED driver power, VCC, is 12 volts and the ground is common for both logic and analog. Details please refer to product specification.

Packaging

The driver IC SSD0323 is mounted on the SSD1325T6 tab flex. The tab flex is attached to the glass cell using the ACF process. Sealers are applied to the edge of the glass and COF to protect against peeling force due to flex folding. The other end of the tab flex is attached to a long flex using the same ACF process.
A metal bracket is attached to the glass cell for its protection and mounted in a hosting device. Both flex circuits are fit in a metal bracket and adhered to the back of the glass cell. The flex tail is terminated with a 30-pin pad designed to mate with a 0.5 mm pitch ZIF connector. Recommended mating connectors: bottom contact: MOLEX 52893-3095, or equivalent and top contact: MOLEX 54104-3031, or equivalent

Operation

Refer to the “FUNCTIONAL BLOCK DESCRIPTIONS” of the SSD0323 data sheet for more information.

Programming

Refer to the section “COMMAND TABLE” of the SSD0323 product specification for detailed command description.

Initialization

Calgary module requires certain commands to be executed upon a power up for its proper operation. Failure to execute these commands may lead to shortened display lifetime, poor image quality, and incorrect image display. **Table 2** lists the commands that must be executed during an initialization after a power up. A sample initialization software code is exerted from a C source file and provided in **Table 5**.

Clear RAM command

Below is the set of commands, which are needed to clear the internal RAM of the driver IC at the initialization stage.

```
sbit CST                    = P1^0;
sbit DC                     = P1^2;
sbit WRT                    = P1^3;
sbit RST                    = P1^6;
void blank(void)
{
uint i,j;
for (j=0;j<80;j++)          /* 80 row */
{
CST = 0;
DC  = 1;
WRT = 0;
for (i=0;i<64;i++)          /* 128 column (1 byte = 2col ) */
{
wr_dt(0x00);
}
WRT = 1;
}
}
```

Recommended Initialization Command

Command at VDD= 3.0V, ***VCC = 12V***, Frame Frequency = 100 Hz

Refer to IC specification: Solomon SSD0323/SSD1325 OLED/PLED Segment/Common Driver with Controller CMOS. After power up, the commands specified in below **Table 2** must be executed during initialization.

Command	Default on POR	Initialization (Dual Voltage Supply)
Set Column Address	00 3F	Default
Set Row Address	00 4F	00 3F
Set Contrast Control	40	66 *(1) 40 *(2)
Set Current Range	Quarter (84)	Full (86)
Set Re-map	00	41
Set Display Start Line	00	Default
Set Display Offset	00	44
Set Multiplex Ratio	4F	3F
Set Display ON/OFF	AE	AF
Set Display Mode	A4	Default
Set DC-DC Converter	03	02 (disabled)
Set DC-DC Bias Current	F0	Default
Set Row Period	25	46
Set Pre-charge Compensation Enable	08	28
Set Pre-charge Compensation Level	00	07
Set Clock Divide	02	F1
Set Phase Length	P1 = 3, P2 = 5	22 (P1 = 2, P2 = 2)
Set VSL	0E	0D
Set VcomH	11	02 *(1) 00 *(2)
Set Vprecharge	18	10 *(1) 0B *(2)
Set Gray Scale Table	All 1	Refer to Grey Scale Settings Table

Table 2: Recommended Initialization Command

Note:

1. Set Row address = 3F hex for 64 rows
2. Set Contrast Control
   a. 66 hex for 75 nits of brightness for Elegance Yellow Product
   b. 40 hex for 75 nits of brightness for Spring Green Product
3. Set Divide Setting = F1 hex to avoid flickering
4. Set VP = 10 hex for better efficiency

*(1). Elegance Yellow Product
*(2). Spring Green Product

Dimming Options

Dimming options is available for this module by changing initialization command for Contrast Control. **Table 3** depicts the settings for three different luminance.

Initial Luminance, cd/m^2	Initialization Command: Set Contrast Control (in Hex)	
	Elegance Yellow	Spring Green
20	1C	0E
40	33	25
60	52	47

Table 3: Recommended Initialization Command for Different Luminance Settings

Grayscale

The SSD0323 employs a pulse width modulation to control grayscale. The pulse width of each gray level is programmed for the row period during initialization upon power up. One row period is divided into three phases. They are Phase 1, Phase 2 and Phase 3, which define the blanking, pre-charge, and current drive phase, respectively.

Each of the 16 grayscale levels (from GS0 to GS15) with an exception of level 0 (GS0) is adjustable with a pulse width (PW) of current drive phase. Each L value represents an offset to the corresponding grey scale level.

The pulse width of each level should be adjusted such that the luminance of each level changes according to the gamma curve that adjusts for the brightness sensitivity of human eye. **Table 4** demonstrates an example of the grayscale setting. **Figure 8** is a plot of the gamma curve for values specified in the table. Straight line in the plot is a default setting. The total DCLK represents the clock cycles for each grayscale level.

GS level	Phase 1	Phase 2	S/W Set	Phase 3 GS Pulse	Total DCLK
L0	2	2	0	0	4
L1	2	2	1	1	5
L2	2	2	1	3	7
L3	2	2	1	5	9
L4	2	2	2	8	12
L5	2	2	2	11	15
L6	2	2	2	14	18
L7	2	2	3	18	22
L8	2	2	3	22	26
L9	2	2	4	27	31
L10	2	2	4	32	36
L11	2	2	5	38	42
L12	2	2	5	44	48
L13	2	2	6	51	55
L14	2	2	6	58	62
L15	2	2	7	66	70

Table 4: Grayscale Settings Table

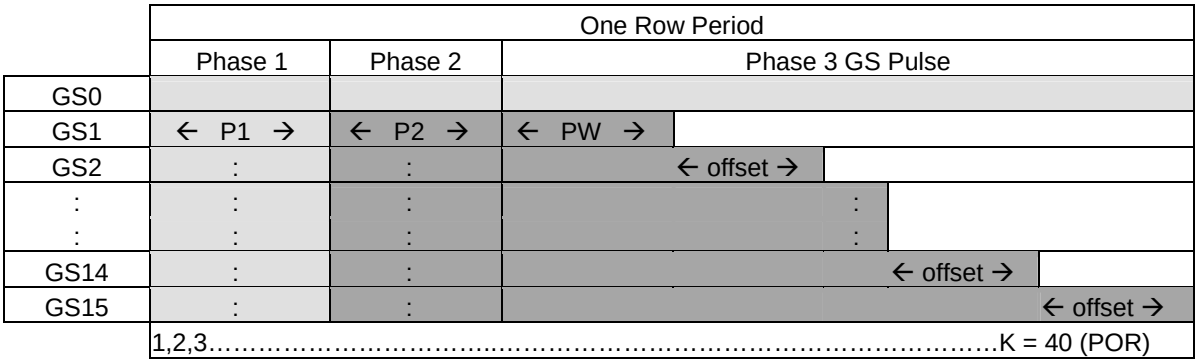


Figure 7: Phases and GS levels

	No pre-charge/drive cycle
	Pre-charge & Current drive cycle
	Current drive

Status check and RAM data read

Read Status command allows for the status of display to be checked whether it is turned on or off. A parallel communication mode allows RAM data to be read from the address specified. The D/C# pin is set low for reading status whereas it is set high for reading data form the RAM. The R/W# pin is set high for both. Note that the first byte read from the RAM is a dummy byte.

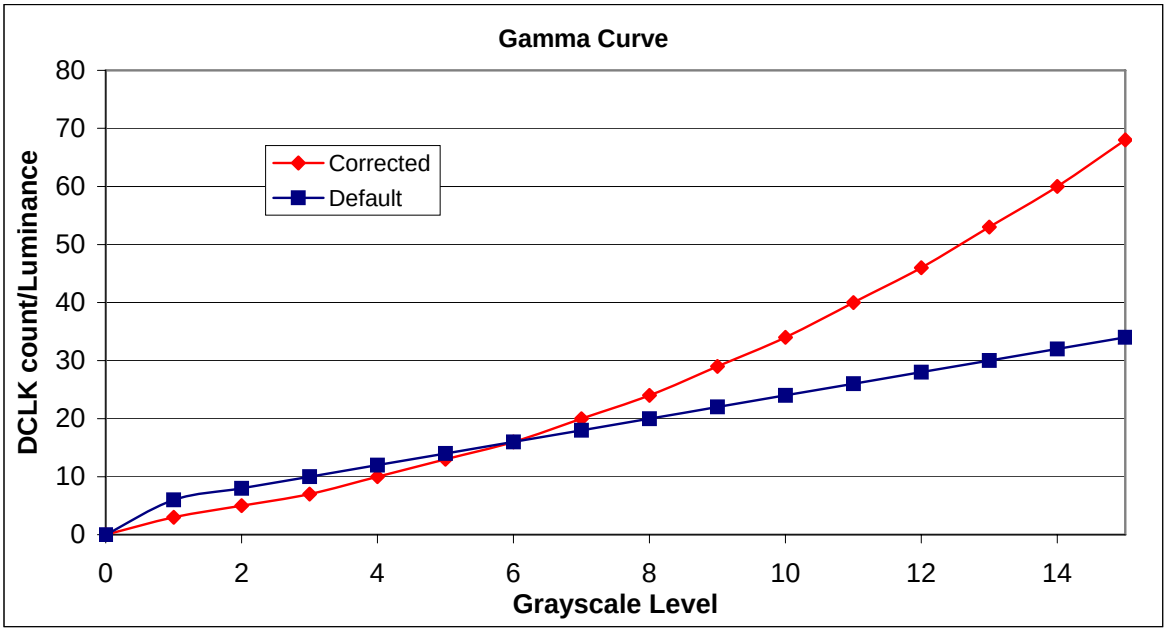


Figure 8: Gamma Curve

Sample Initialization Software Code

```
/*****************************************
// Calgary 4 Bits SSD0323 H555X Initialization Command
*****************************************/
void blank(void)
{
   uint i,j;
   for (j=0;j<80;j++)        /* 80 row */
   {
      CST = 0;
      DC  = 1;
      WRT = 0;
      for (i=0;i<64;i++)     /* 128 column (1 byte = 2col ) */
      {
                             wr_dt(0x00);
      }
      WRT = 1;
   }
}

// Column Address
   WriteCommand(0x15);    /* Set Column Address */
   WriteCommand(0x00);    /* Start = 0 */
   WriteCommand(0x3F);     /* End = 127 */
// Row Address
   WriteCommand(0x75);    /* Set Row Address */
   WriteCommand(0x00);    /* Start = 0 */
   WriteCommand(0x3F);     /* End =  63 */
// Contrast Control
   WriteCommand(0x81);    /* Set Contrast Control (1) */
   WriteCommand(0x66);    /* 0 ~ 127 */
// Current Range
   WriteCommand(0x86);    /* Set Current Range 84h:Quarter,  85h:Half, 86h:Full*/
// Re-map
   WriteCommand(0xA0);    /* Set Re-map */
   WriteCommand(0x41);    /* [0]:MX, [1]:Nibble, [2]:H/V address [4]:MY, [6]:Com Split Odd/Even "1000010"*/
// Display Start Line
   WriteCommand(0xA1);    /* Set Display Start Line */
   WriteCommand(0x00);    /* Top */
// Display Offset
   WriteCommand(0xA2);    /* Set Display Offset */
   WriteCommand(0x44);    /* Offset 76 rows */
// Display Mode
   WriteCommand(0xA4);    /* Set DisplaMode,A4:Normal,     A5:All ON, A6: All OFF, A7:Inverse       */
// Multiplex Ratio
   WriteCommand(0xA8);    /* Set Multiplex Ratio */
   WriteCommand(0x3F);    /* 64 mux*/
// Phase Length
   WriteCommand(0xB1);    /* Set Phase Length */
   WriteCommand(0x22);    /* [3:0]:Phase 1 period of 1~16 clocks */
                          /* [7:4]:Phase 2 period of 1~16 clocks /* POR = 0111 0100 */

// Row Period
   WriteCommand(0xB2);    /* Set Row Period */
   WriteCommand(0x46);    /* [7:0]:18~255, K=P1+P2+GS15 (POR:4+7+29)*/
// Display Clock Divide
   WriteCommand(0xB3);    /* Set Clock Divide (2) */
   WriteCommand(0xF1);    /* [3:0]:1~16, [7:4]:0~16, 70Hz */
      /* POR = 0000 0001 */
// VSL
   WriteCommand(0xBF);    /* Set VSL */
   WriteCommand(0x0D);    /* [3:0]:VSL */
// VCOMH
   WriteCommand(0xBE);    /* Set VCOMH (3) */
   WriteCommand(0x02);    /* [7:0]:VCOMH, (0.51 X Vref = 0.51 X 12.5 V = 6.375V)*/
// VP
```

```
   WriteCommand(0xBC);    /* Set VP (4) */
   WriteCommand(0x10);    /* [7:0]:VP, (0.67 X Vref = 0.67 X 12.5 V = 8.375V) */
// Gamma
   WriteCommand(0xB8);    /* Set Gamma with next 8 bytes */
   WriteCommand(0x01);    /* L1[2:1] */
   WriteCommand(0x11);    /* L3[6:4], L2[2:0] 0001 0001 */
   WriteCommand(0x22);    /* L5[6:4], L4[2:0] 0010 0010 */
   WriteCommand(0x32);    /* L7[6:4], L6[2:0] 0011 1011 */
   WriteCommand(0x43);    /* L9[6:4], L8[2:0] 0100 0100 */
   WriteCommand(0x54);          /* LB[6:4], LA[2:0] 0101 0101 */
   WriteCommand(0x65);          /* LD[6:4], LC[2:0] 0110 0110 */
   WriteCommand(0x76);    /* LF[6:4], LE[2:0] 1000 0111 */

// Set DC-DC
   WriteCommand(0xAD);    /* Set DC-DC */
   WriteCommand(0x02);    /* 03=ON, 02=Off */
// Display ON/OFF
          WriteCommand(0xAF);          /* AF=ON, AE=Sleep Mode */
```

Table 5: Initialization Code

Frame Frequency

Frame frequency is set at the nominal rate of 100 Hz. If a higher rate is desired, it can be adjusted to the desirable rate by varying the oscillator frequency and the value of D with the clock divide command during initialization. Default value of D upon power up is 2 and its range is plotted in red in **Figure 9**. If D value greater than 2 is sets, then the frame frequency output is below 60 Hz and flickering of image becomes visible.

Row period K is optimized at 46 Hex for a proper gray scale operation. Therefore, caution must be taken for re-adjusting.

Higher frame frequency causes the display to dim because of a shorter pixel charge time at each duty cycle. The contrast setting can be increased to restore the required luminance. An operation of the frame rate below 100 Hz is not recommended. A frame frequency is calculated using the following equation.

$$FrameFrequency = OscillatorFreq \times \frac{1}{D \times K \times 64}$$

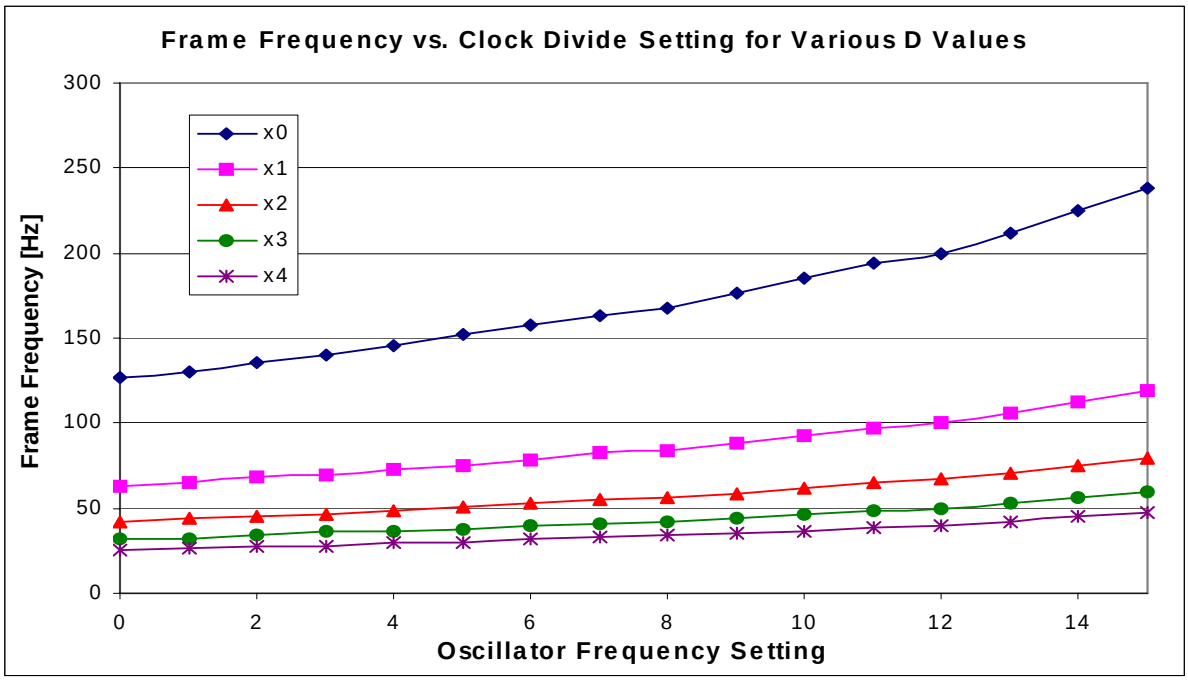


Figure 9: Frame Frequency

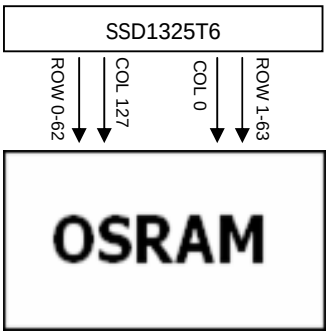
Image Orientation

Along with Re-map (A0 hex) command, Display Offset (A2 hex) command allows image to be displayed and rotated 180°. Corresponding command parameters for normal and mirrored display are shown in **Table 6**.

Command/Parameter	Display Normal	Display 180° rotated
Re-Map	41 hex	52 hex
Offset	44 hex	4C hex

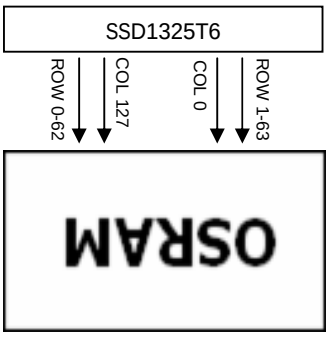
Table 6: S/W setting for X and Y mirror

Display Normal Orientation




```
//Re-map
WriteCommand(0xA0);     /* Set Re-map */
WriteCommand(0x41);     /* [0]:MX, [1]:Nibble, [2]:H/V address [4]:MY, [6]:Com Split Odd/Even "1000010"*/
//Display Offset
WriteCommand(0xA2);     /* Set Display Offset */
WriteCommand(0x44);     /* Offset 76 rows */
```

Display 180º Rotated Orientation




```
//Re-map
WriteCommand(0xA0);     /* Set Re-map */
WriteCommand(0x52);     /* [0]:MX, [1]:Nibble, [2]:H/V address [4]:MY, [6]:Com Split Odd/Even "1000010"*/
//Display Offset
WriteCommand(0xA2);     /* Set Display Offset */
WriteCommand(0x4C);     /* Offset 76 rows */
```

Luminance control and Power consumption

The luminance of an OLED display is proportional to its power consumption. There are two commands that are available for controlling the luminance of the display; one command sets the current range and the other sets the contrast ratio. Both commands control the amplitude of current drive pulse rather than the pulse width.

Figure 10 depicts the linear relationship of two commands vs. segment current. It is observed that the luminance becomes non-linear near the maximum range as the current driver reaches its maximum limit. Quarter, half, and full in legend box, indicate software current setting.

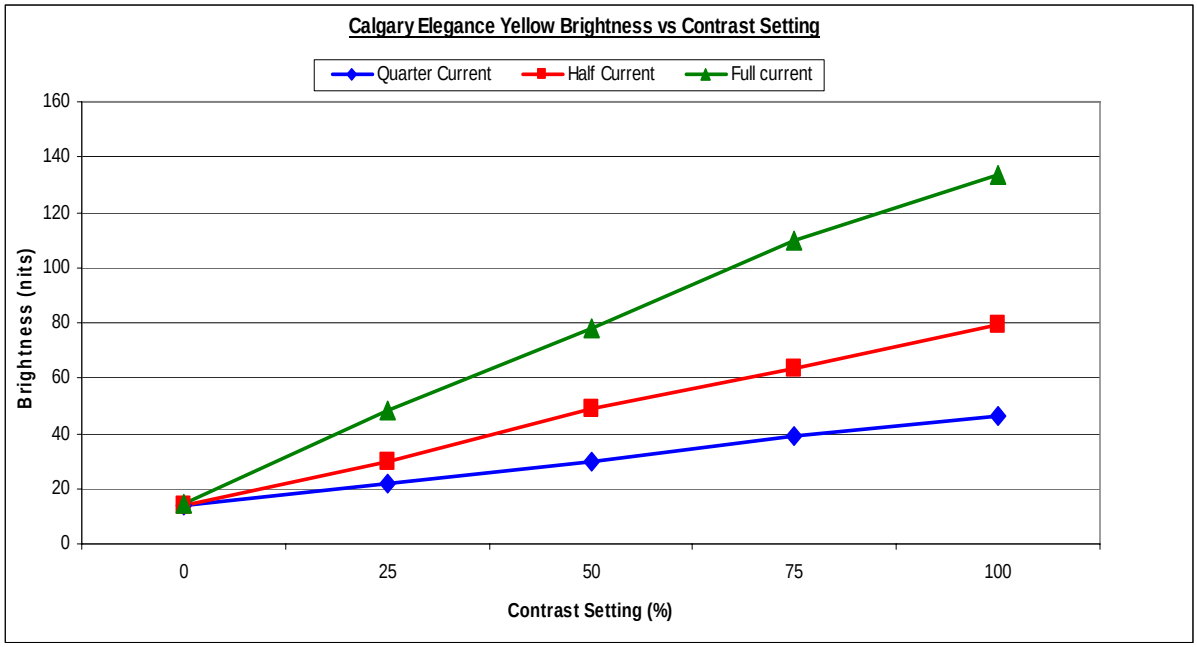


Figure 10: Contrast Setting vs. Contrast Setting

Figure 11 is a plot with all three current settings, Quarter, Half, and Full combined to show a linear relationship of luminance and power consumption. It indicates power usage for a display with 100% of pixels turned on. It implies that any combination of Current and Contrast setting can achieve a desired luminance without concerned with the power consumption characteristics of the module. The current range should be first chosen such that the contrast command has a full control over the desired luminance range of display. Default level at power up is at Quarter range.

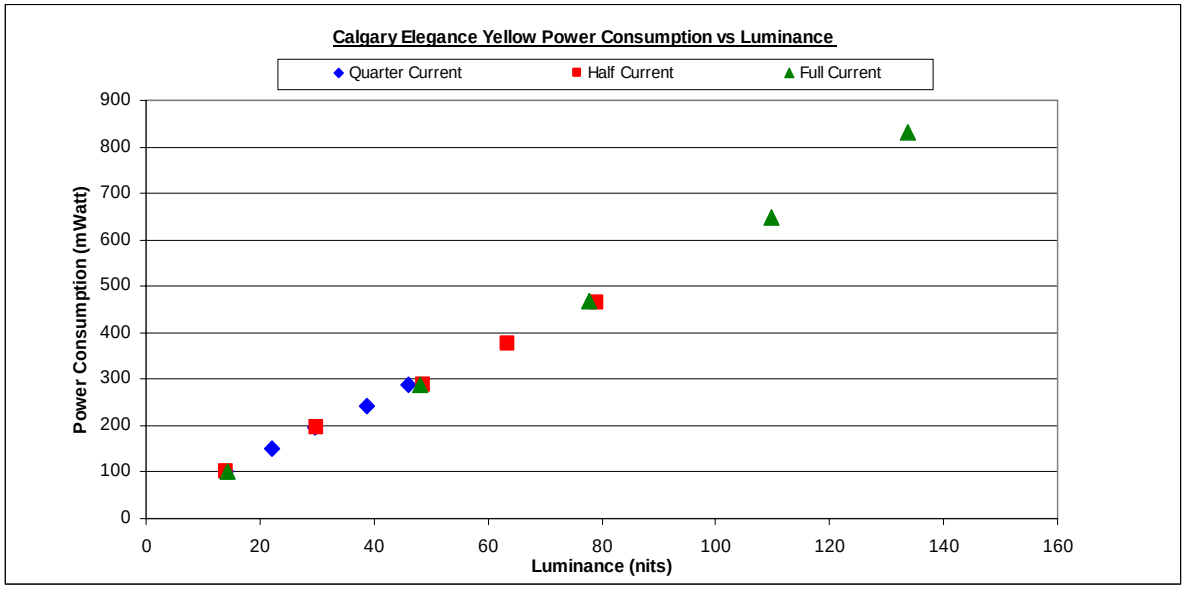


Figure 11: Luminance vs. Power of three current setting

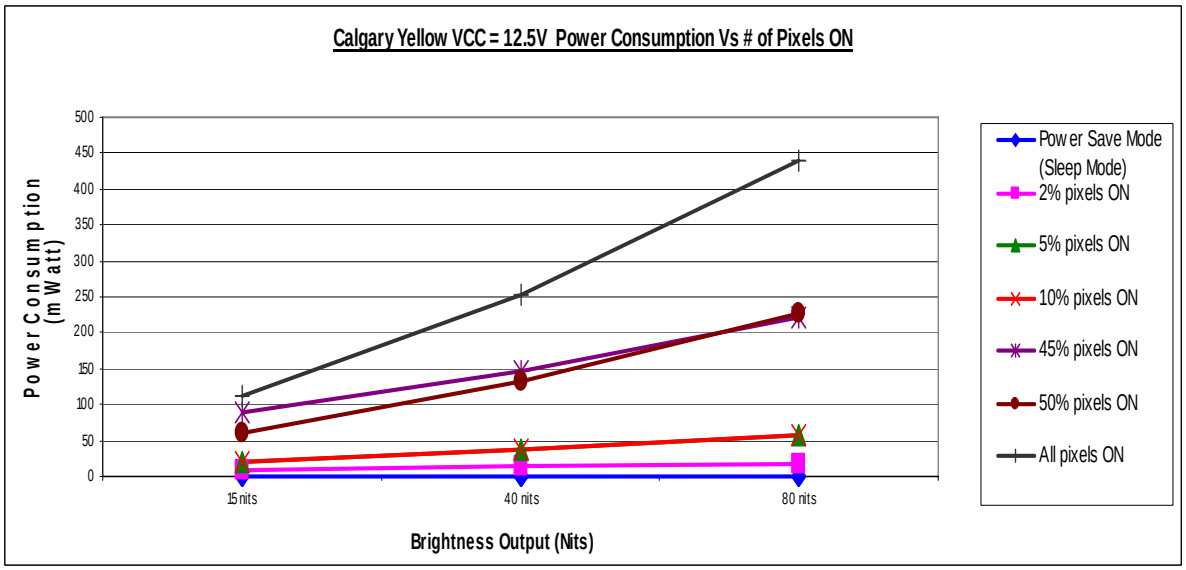


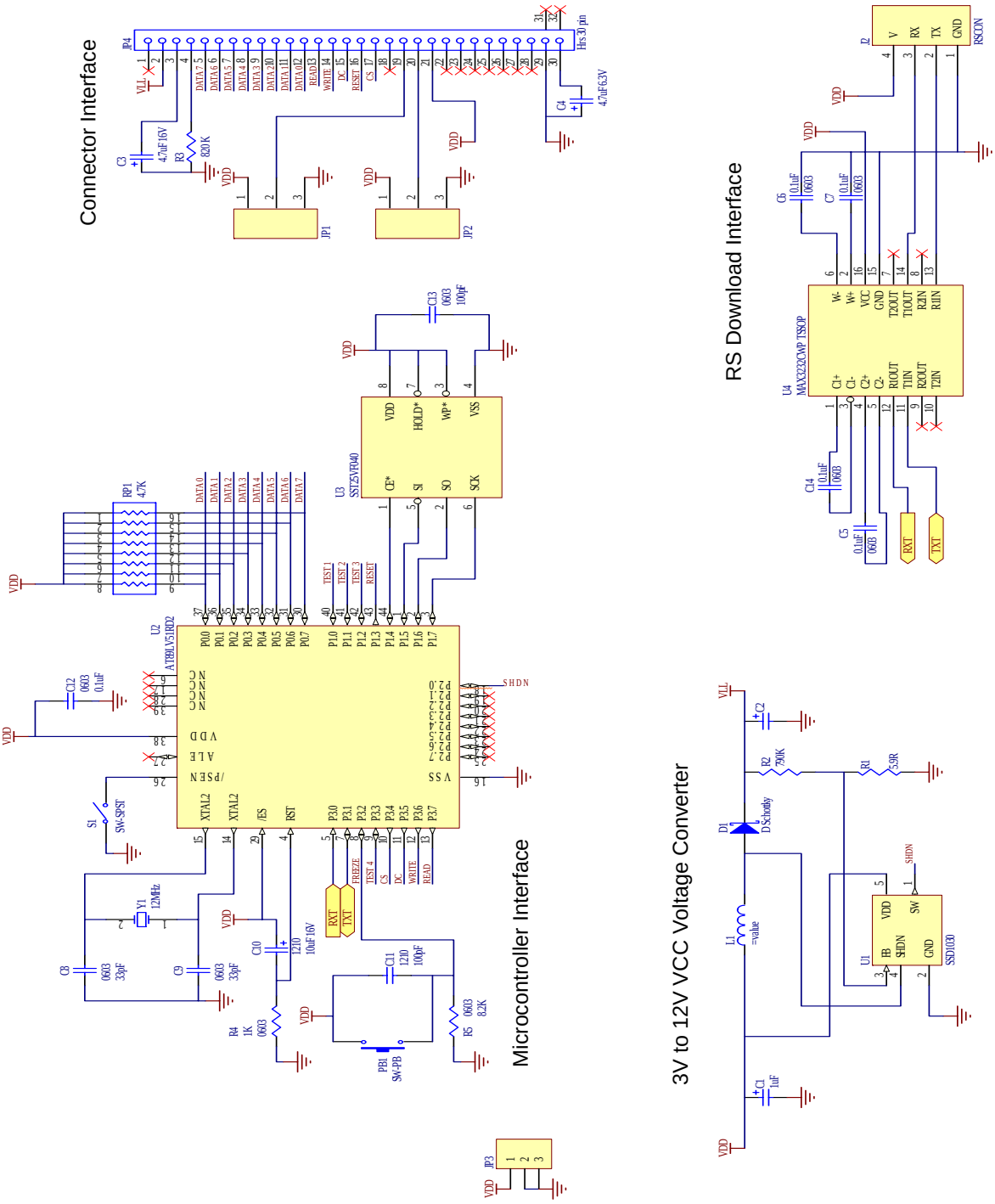
Figure 12: Power Consumption vs. Luminance with different % of pixels on

The power consumption also has a linear relationship with the luminance and number of pixels illuminated. **Figure 12** shows linearly increasing power usage for higher brightness. The higher the number of illuminated pixels is on, the higher the power and brightness is. Note that power consumption is not zero when no pixels are turned on due to the power used by the logic circuit portion of the IC. For this module, Power Save Mode (Sleep Mode) is at 0.016 mW.

Appendix

Interfacing Schematic

1. Figure below shows the recommended interface schematic to drive this product. Other types of interface can be use depending on user's application and specification.
2. The ***3V to 12V VCC Voltage Converter*** shown in the recommended interfacing schematic below is using Solomon's SSD1030 IC. For further details, please refer to Solomon SSD1030 IC Specification.



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