4M ×4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
KM44C4104A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM44C4104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44C4104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44C4104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM44C4104A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C4104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

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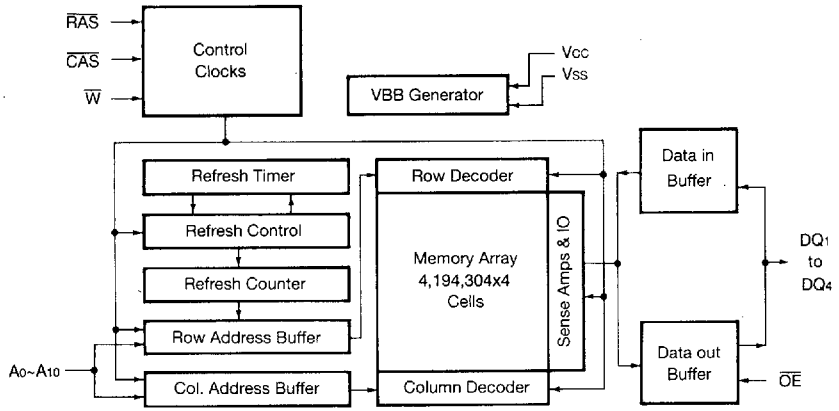
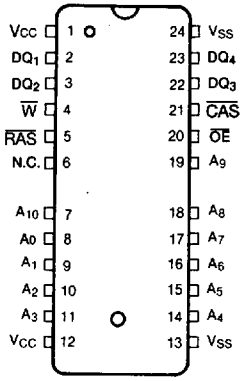
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

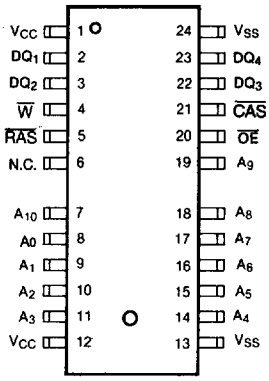
PIN CONFIGURATION (Top Views)

• KM44C4104 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



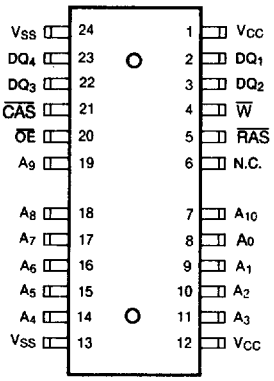
J : 400MIL
K : 300MIL

• KM44C4104 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4104 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1~4	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4104A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C4104A	I_{CC2}	-	2	mA
	KM44C4104AL			1	mA
	KM44C4104ALL			1	mA
	KM44C4104ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4104A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4104A/AL/ALL/ASL-5	I_{CC4}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4104A	I_{CC5}	-	1	mA
	KM44C4104AL			300	μA
	KM44C4104ALL			200	μA
	KM44C4104ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4104A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ1~DQ4=Don't Care t_{RC}=62.5μs(L-Ver.) 125μs(SL-Ver.), t_{RAS}=t_{RAS}≤min~300ns	KM44C4104AL	I_{CC7}	-	400	μA
	KM44C4104ASL			300	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4104ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.4V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		2		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	3	20	3	20	ns	7,15
Transition time (rise and fall)	t_T	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		50		60		ns	16
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	15	10K	20	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	11
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		15		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32		32	ms	
Refresh period (L-ver)	t_{REF}		128		128		128		128	ms	
Refresh period (SL-ver)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ oprecharge to $\overline{W}$ delay time	t_{CPWD}	53		60		70		75		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Hyper Page cycle time	t_{HPC}	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	t_{HPRWC}	62		71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page Cycle)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page Cycle)	t_{RASP}	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	7
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	12
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	7,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		100		μs	16
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		150		ns	16
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		20		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	tHPC	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	tHPRWC	67		76		91		101		ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ pulse width (Hyper Page Cycle)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

The KM44C4104A/AL/ALL/ASL is the CMOS DRAM organizied 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s)the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode". the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM. $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", and "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/4 in cases of N test pattern)

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without tHPC and tHPRWC.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS ≥ tWCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD ≥ tCWD(min), tRWD ≥ tRWD(min) and tAWD ≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tREZ(max), tCEZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before RAS high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. tASC ≥ tCP (min), Assumn tT=2.0ns

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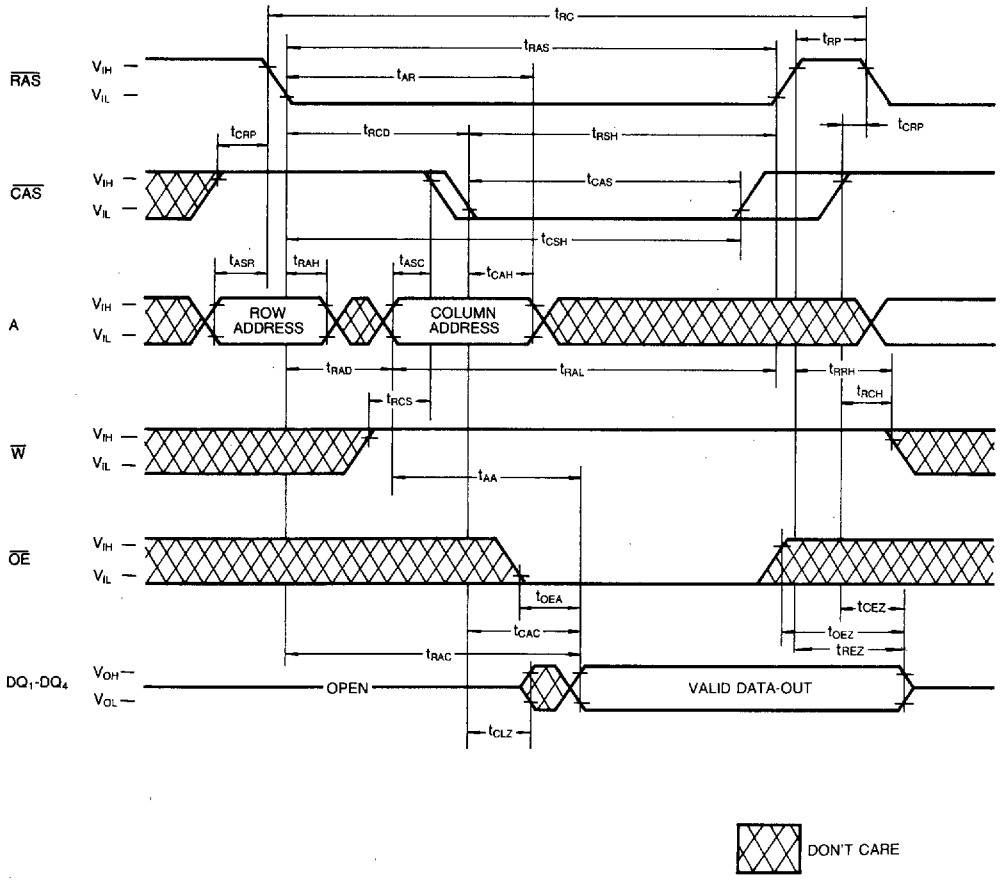
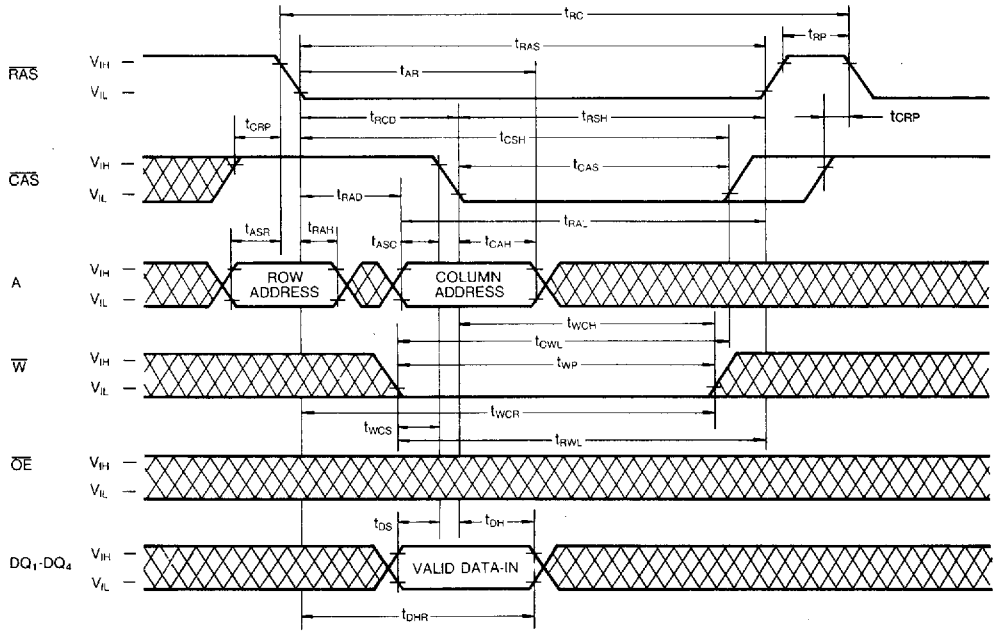
TIMING DIAGRAMS

READ CYCLE

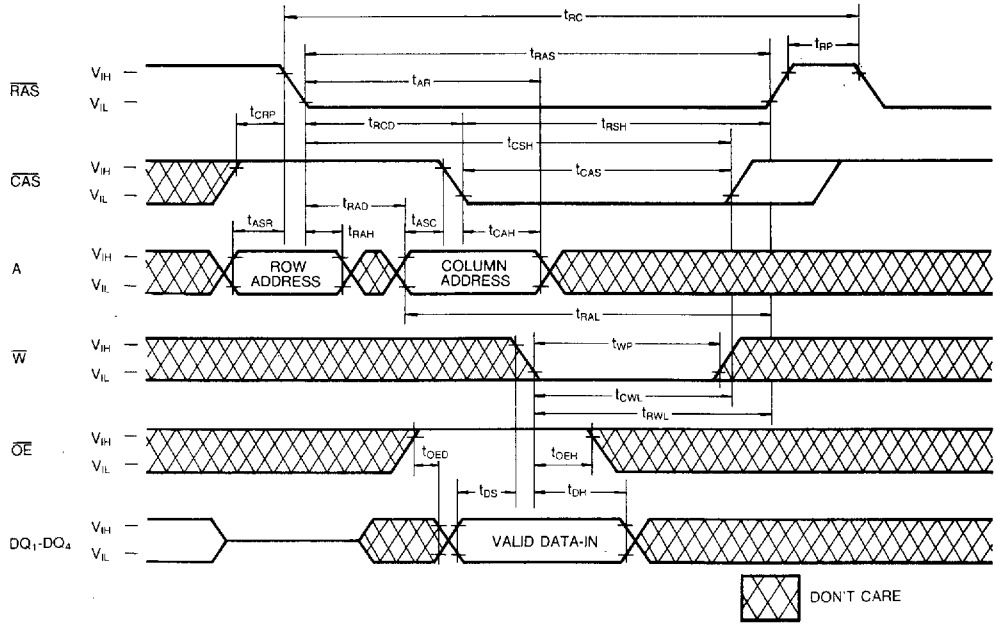


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



WRITE CYCLE (OE CONTROLLED WRITE)



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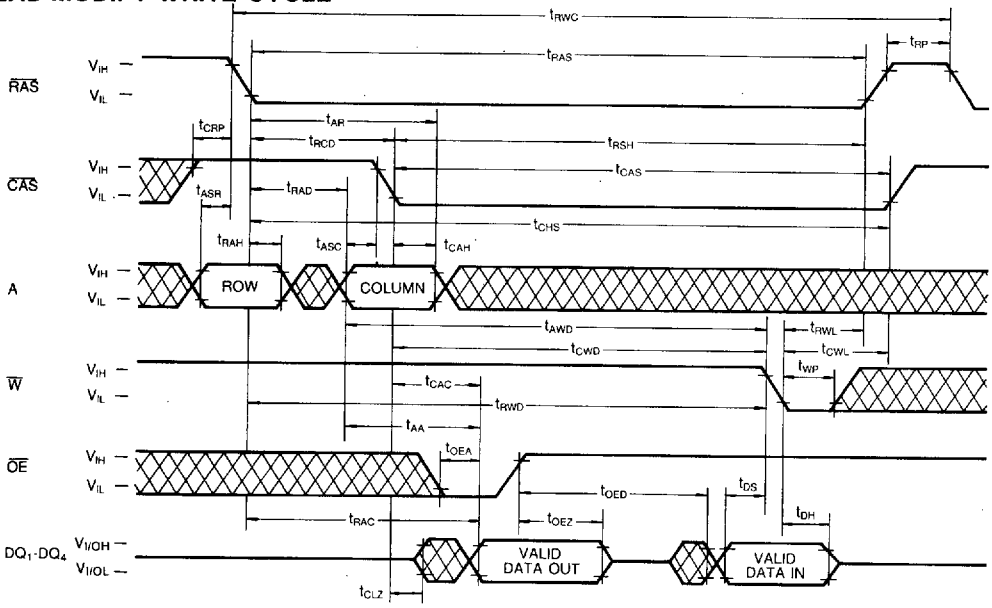
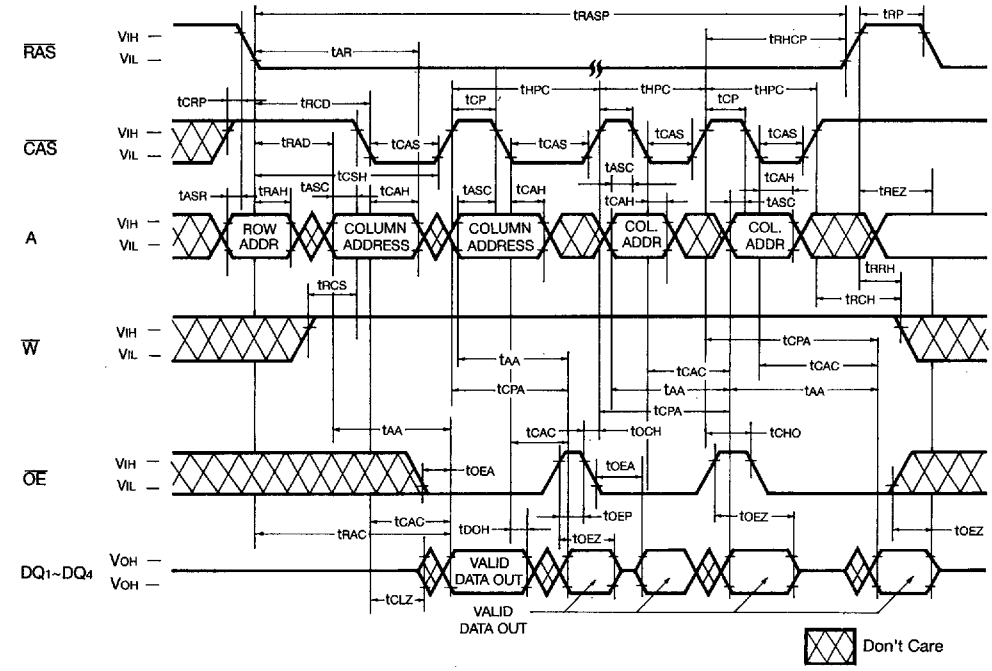
TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE

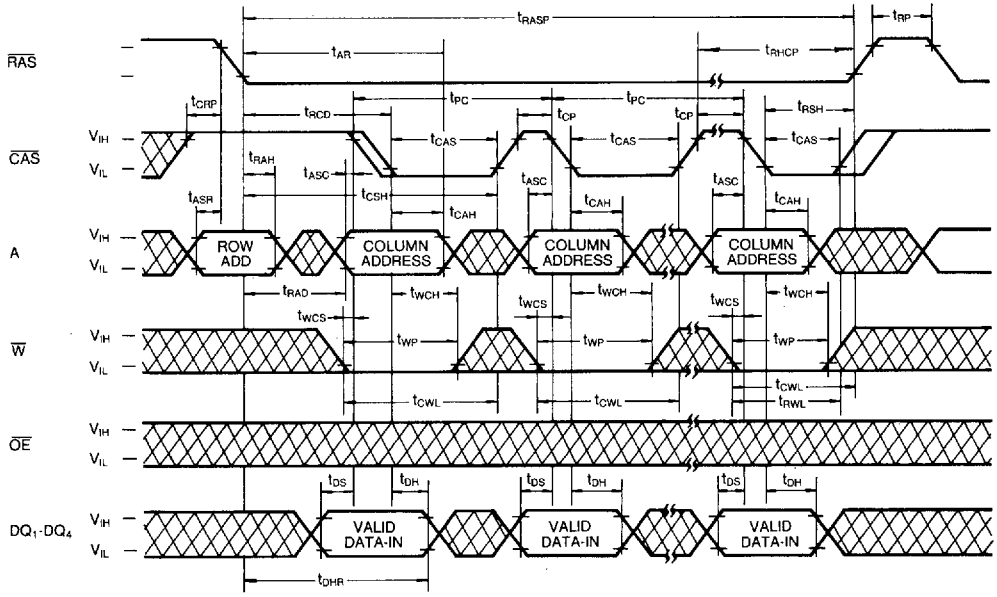


HYPER PAGE READ CYCLE

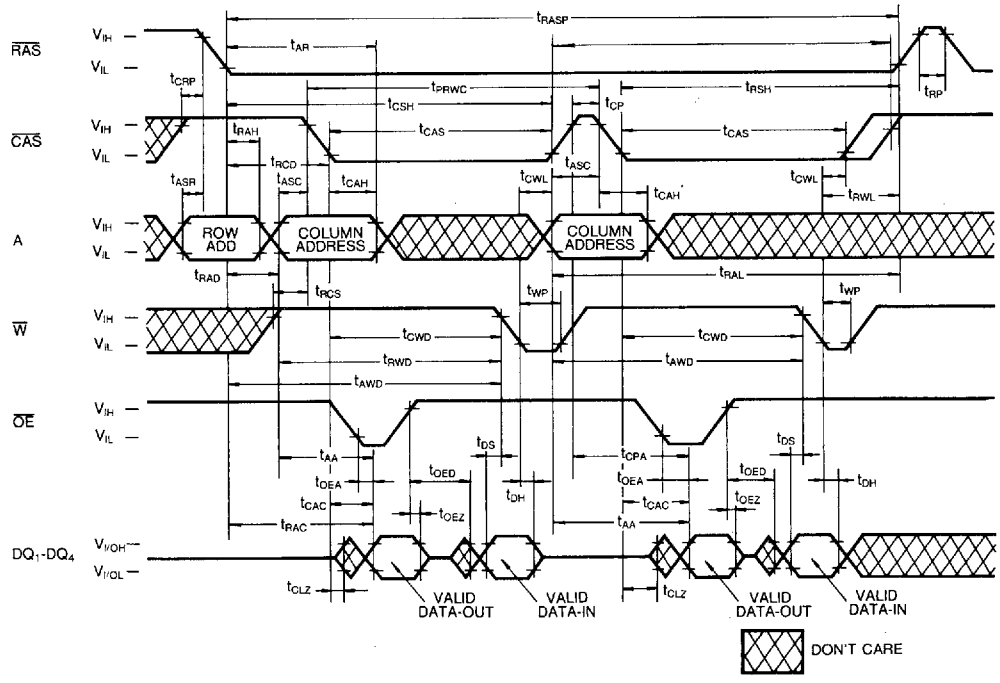


TIMING DIAGRAMS (Continued)

HYPER PAGE WRITE CYCLE (EARLY WRITE)



HYPER PAGE READ-MODIFY-WRITE CYCLE



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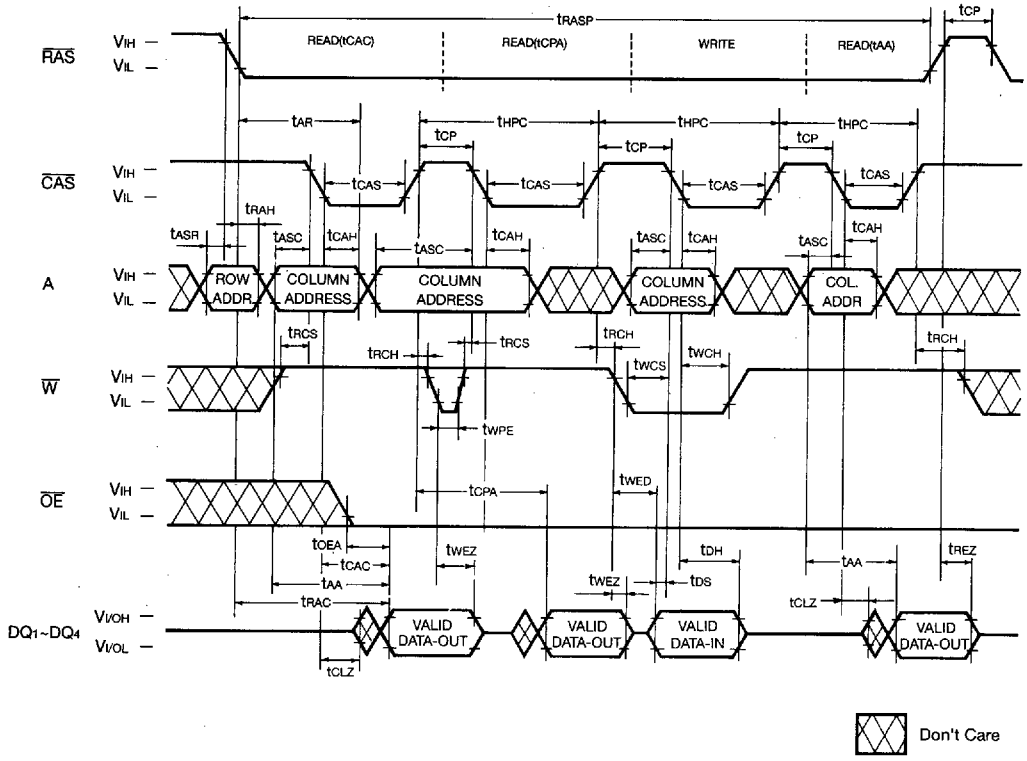
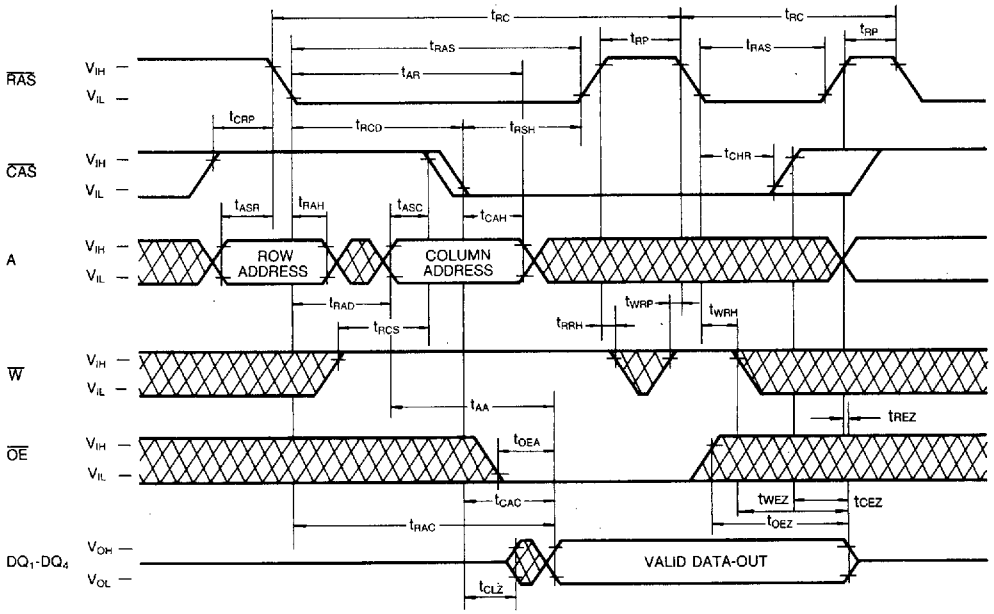
HYPER PAGE READ AND WRITE MIXED CYCLE

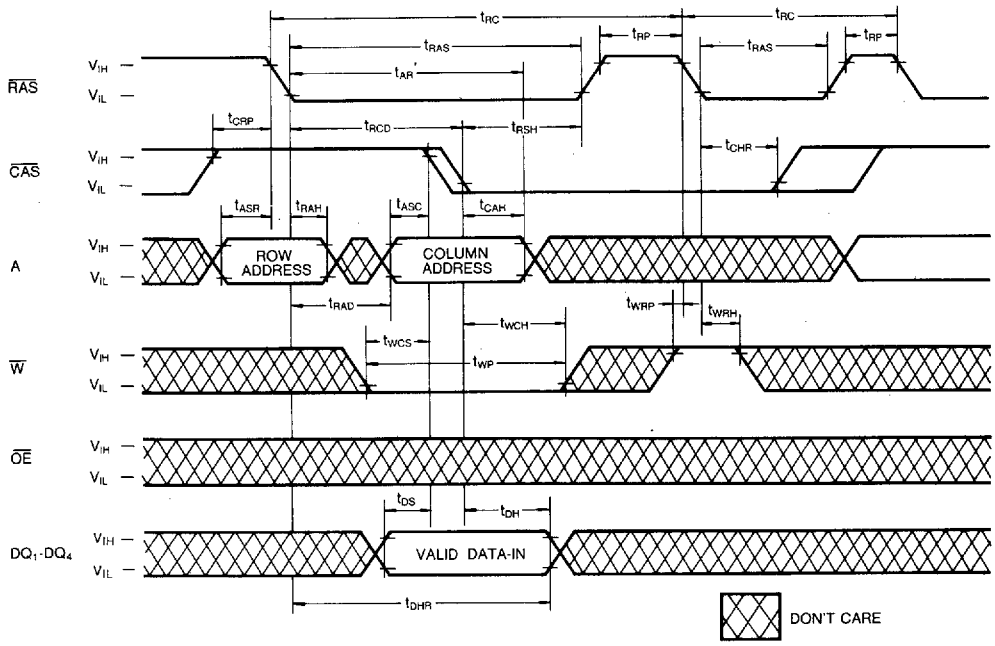


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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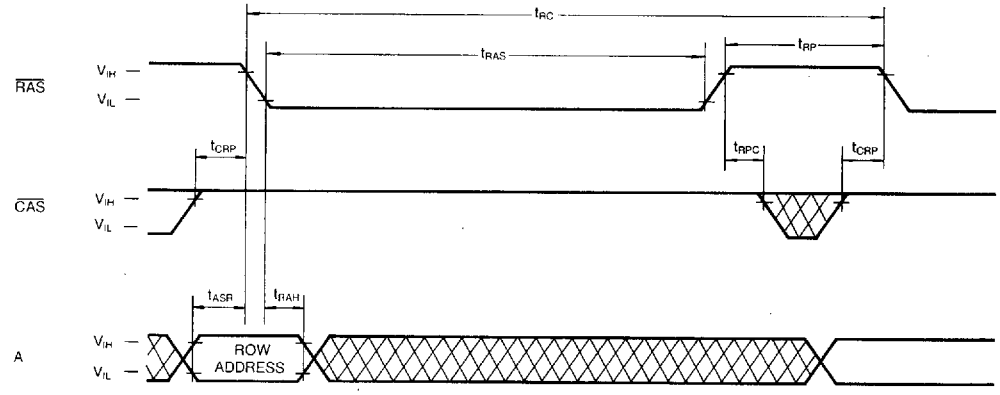
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

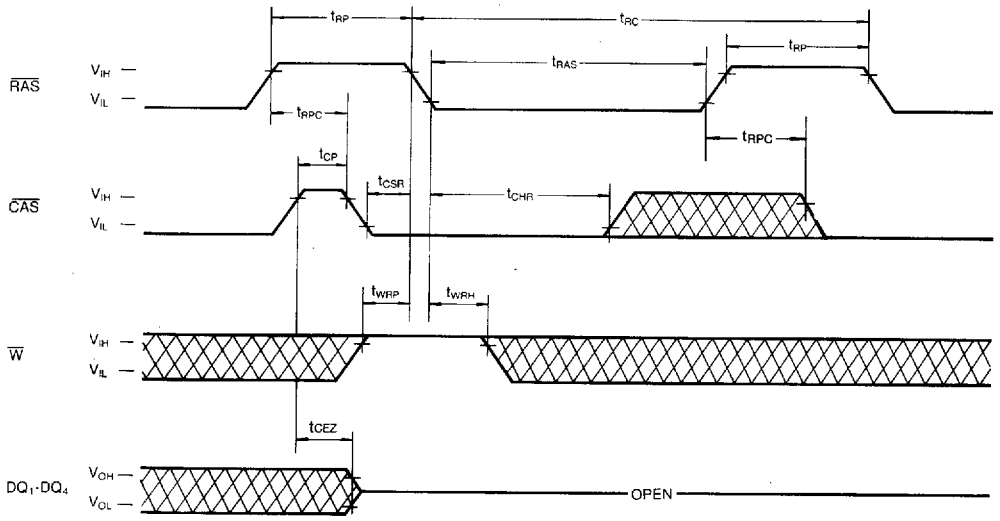
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



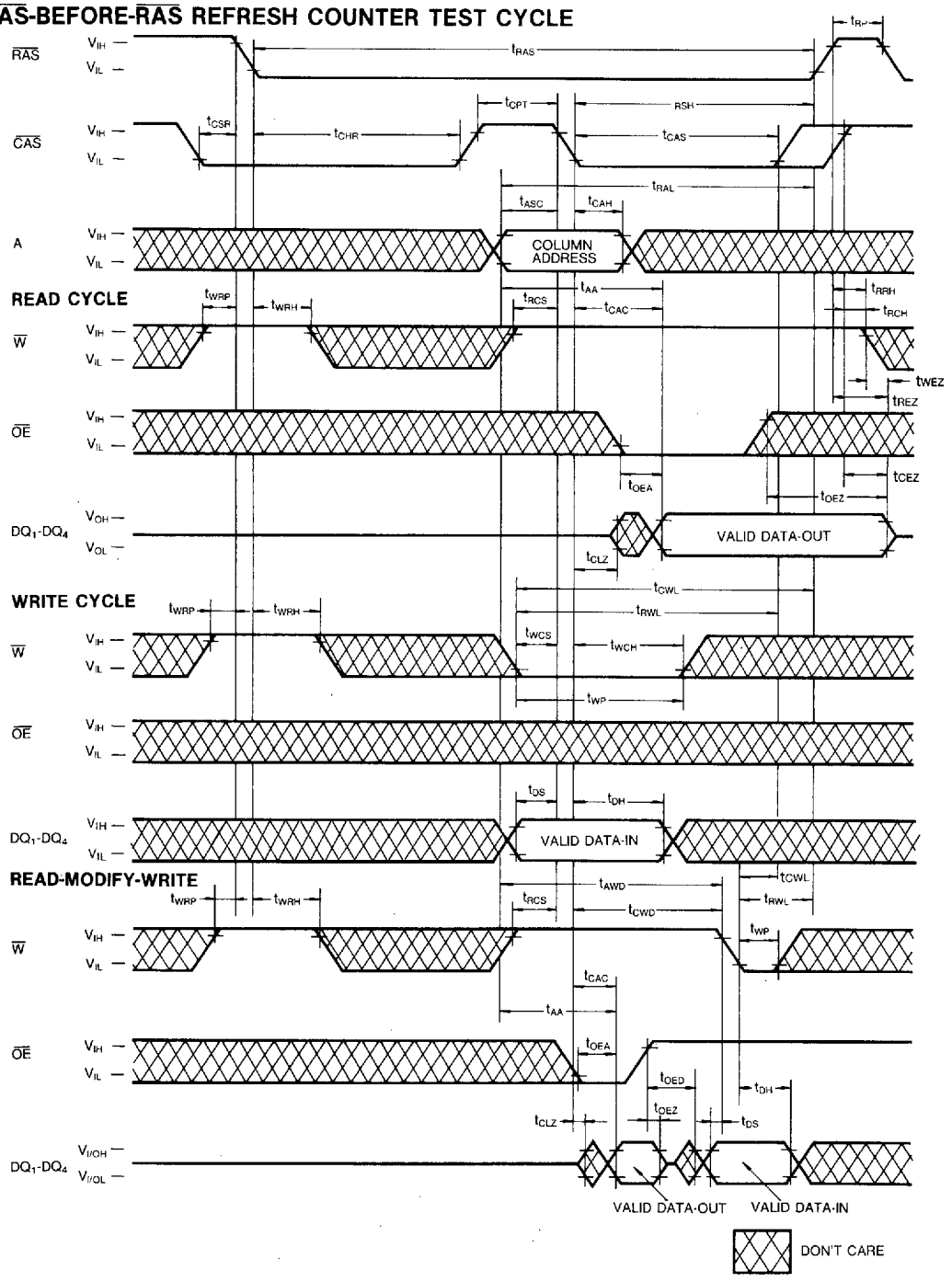
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care



TIMING DIAGRAMS (Continued)

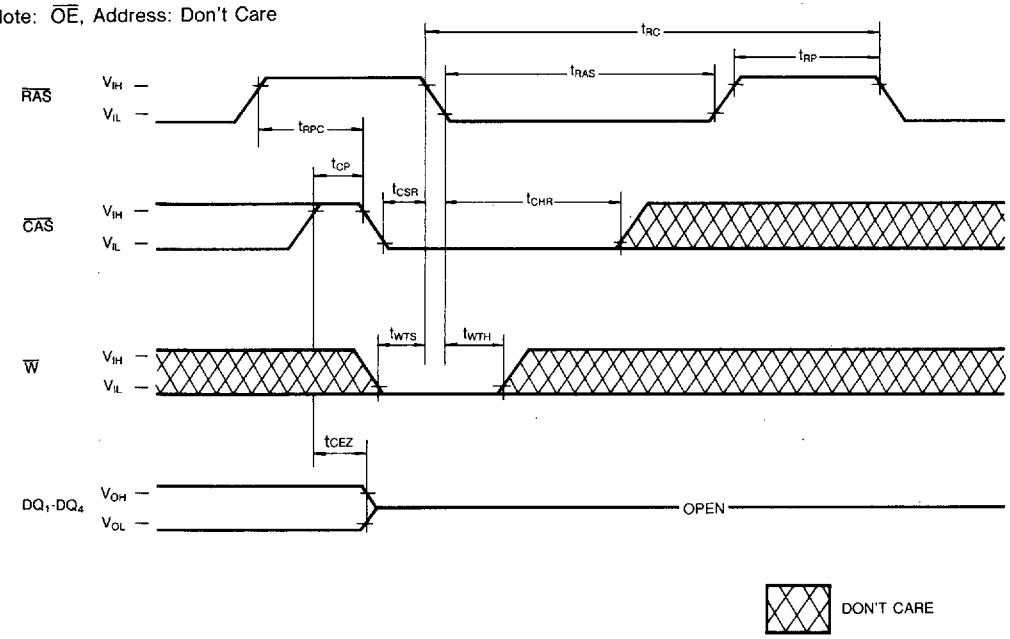
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

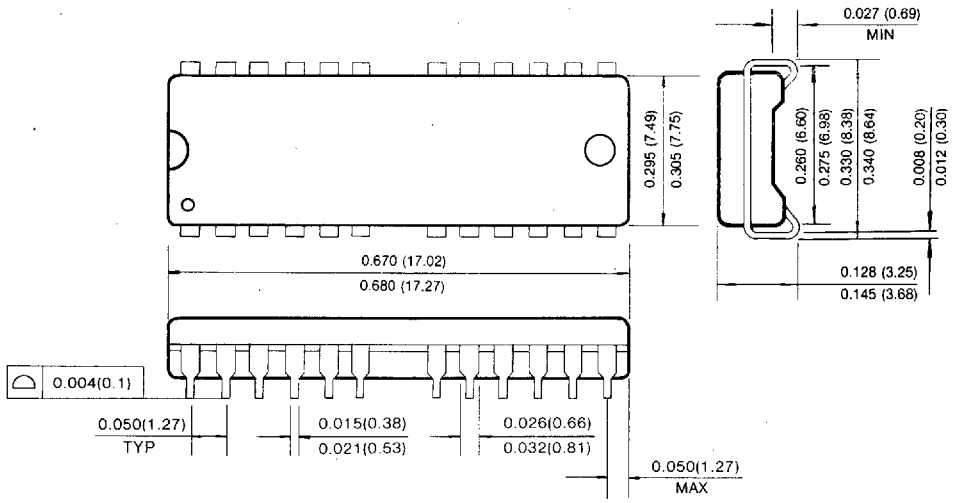
Note: $\overline{OE}$, Address: Don't Care



PACKAGE DIMENSIONS

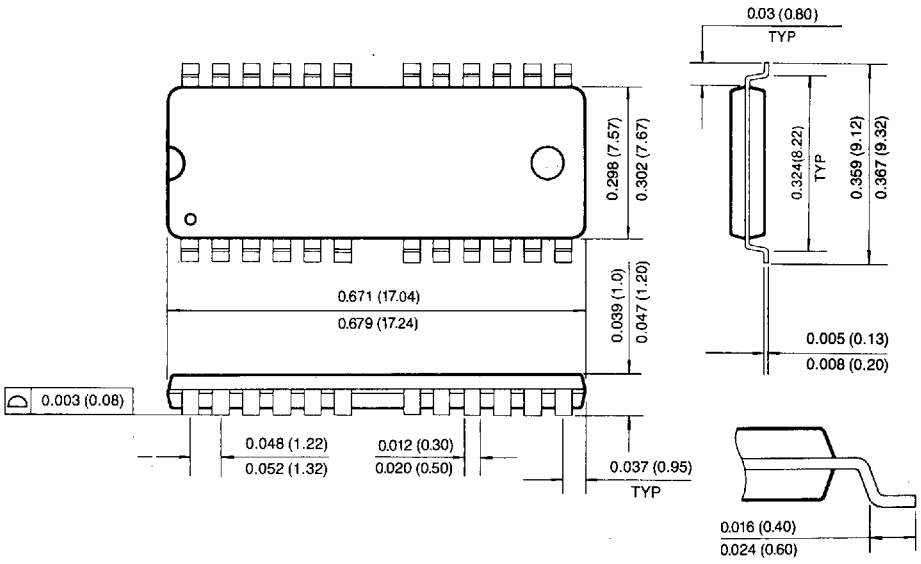
24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



5

24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

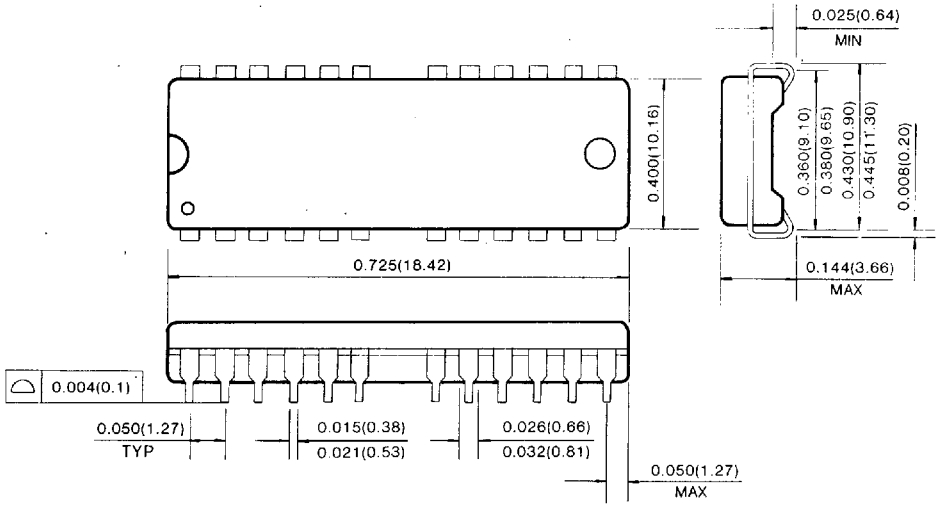


SAMSUNG ELECTRONICS

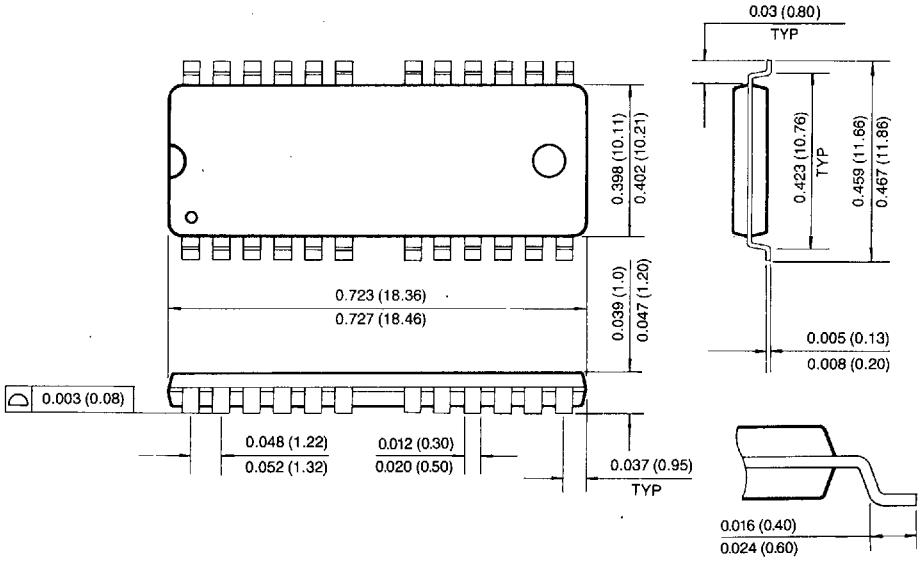
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



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