Metric Pitch BGA & Micro BGA Routing Solutions

The following presentation provides Via fanout and trace routing solutions for various metric pitch Ball Grid Array Packages

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METRIC BGA FEATURE SIZES

- The starting point to solve the metric pitch BGA dilemma is a basic understanding of the metric feature sizes for –
  - BGA ball sizes
  - BGA land pattern pad construction
  - BGA Via anatomy
  - Trace / Space
  - Trace and via routing grid
  - HDI hole size / annular ring

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BGA BALL & PAD SIZES

Table 14-5 Land Approximation (mm) for Collapsible Solder Balls

Nominal Ball Diameter	Reduction	Land Pattern Density Level	Nominal Land Diameter	Land Variation
0.75	25%	A	0.55	0.60 - 0.50
0.65	25%	A	0.50	0.55 - 0.45
0.60	25%	A	0.45	0.50 - 0.40
0.55	25%	A	0.40	0.45 - 0.35
0.50	20%	B	0.40	0.45 - 0.35
0.45	20%	B	0.35	0.40 - 0.30
0.40	20%	B	0.30	0.35 - 0.25
0.35	20%	B	0.30	0.35 - 0.25
0.30	20%	B	0.25	0.25 - 0.20
0.25	20%	B	0.20	0.20 - 0.17
0.20	15%	C	0.17	0.20 - 0.14
0.17	15%	C	0.15	0.18 - 0.12
0.15	15%	C	0.13	0.15 - 0.10

Note: The IPC-7351A LP Calculator Uses this chart for calculations

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BGA 3-TIER BALL SIZE

Table 3-18 Ball Grid Array Components (Unit: mm)

Lead Part	Minimum (Least) Density Level C	Median (Nominal) Density Level B	Maximum (Most) Density Level A
Periphery Collapsing Ball	15% reduction below nominal ball diameter	20% reduction below nominal ball diameter	25% reduction below nominal ball diameter
Periphery Noncollapsing Ball or Column	5% increase above the nominal ball or column diameter	10% increase above the nominal ball or column diameter	15% increase above the nominal ball or column diameter
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.50	1.00	2.00
Ball Grid Array **(BGA)** Construction and land pattern development are described in 14.1 & 14.4			
Column Grid Array **(CGA)** Construction and land pattern development are described in 14.1.3 & 14.4			

ANATOMY OF THE METRIC VIA

- The base value round-off for metric via features are in 0.05 mm increments. This includes –
  - Pad Size
  - Hole Size
  - Solder Mask Size
  - Plane Clearance (Anti-pad) Size
  - Plane Thermal Relief Size or None

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METRIC BGA VIA SIZES FOR DOGBONE VIA FANOUT

BGA Pin Pitch	VIA Name	Pad Size	Hole Size	Plane Clearance	Solder Mask	Thermal ID	Thermal OD	Thermal Spoke Width
1.50mm	VIA60-25-80	0.60	0.25	0.80	0.00	0.55	0.80	0.25 or None
1.50mm	VIA55-25-75	0.55	0.25	0.75	0.00	0.55	0.75	0.25 or None
1.27mm	VIA63-30-85	0.635	0.30	0.85	0.00	0.65	0.85	0.25 or None
1.00mm	VIA55-25-75	0.55	0.25	0.75	0.00	0.55	0.75	0.25 or None
1.00mm	VIA50-25-70	0.50	0.25	0.70	0.00	0.55	0.70	0.25 or None
0.80mm	VIA45-20-65	0.45	0.20	0.65	0.00	0.50	0.65	0.20 or None
0.75mm	VIA40-20-65	0.40	0.20	0.65	0.00	0.50	0.65	0.20 or None

Show via calculator

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METRIC TRACE/SPACE SIZES

- Metric trace widths are in 0.025 mm (1 mil) increments
- Common metric BGA trace widths
  - 0.075 mm (3 mils)
  - 0.1 mm (4 mils)
  - 0.125 mm (5 mils)
  - 0.15 mm (6 mils)
  - 0.2 mm (8 mils)

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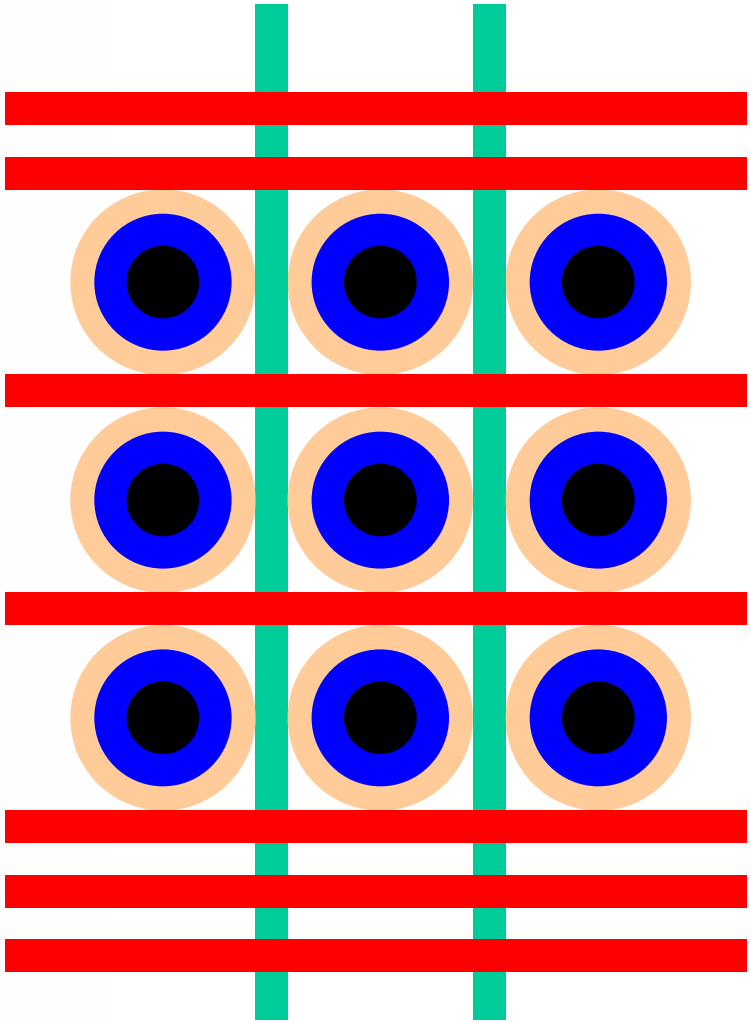
0.4 mm PITCH BGA THROUGH-HOLE / 1 mm PCB



Via-in-Pad Technology

BGA Ball Size: 0.25 (10)
BGA Land Dia: 0.25 (10)
Hole Size: 0.125 (5)
Thermal Relief Required
Plane Clearance: 0.35 (14)
Solder Mask: 1:1 scale

Trace/Space Data

Trace Width: 0.05 (2)
Trace/Trace Space: 0.05
Trace/Via Space: 0.05 (2)
Trace/BGA Land: 0.05 (2)
Routing Grid: 0.05 (2)
Part Place Grid: 0.5 (20)

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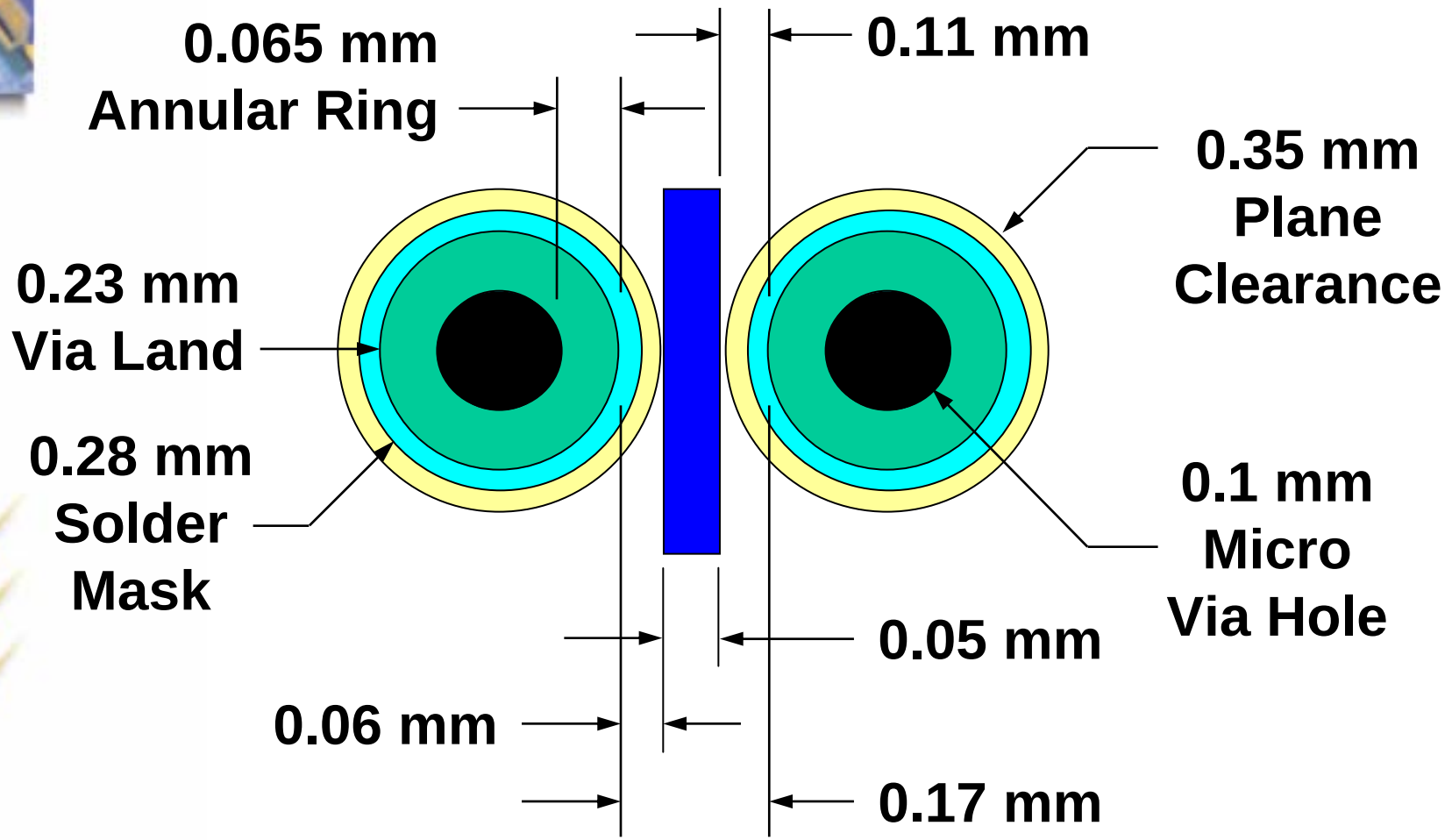
0.4 mm PITCH BGA
MICRO VIA TECHNOLOGY



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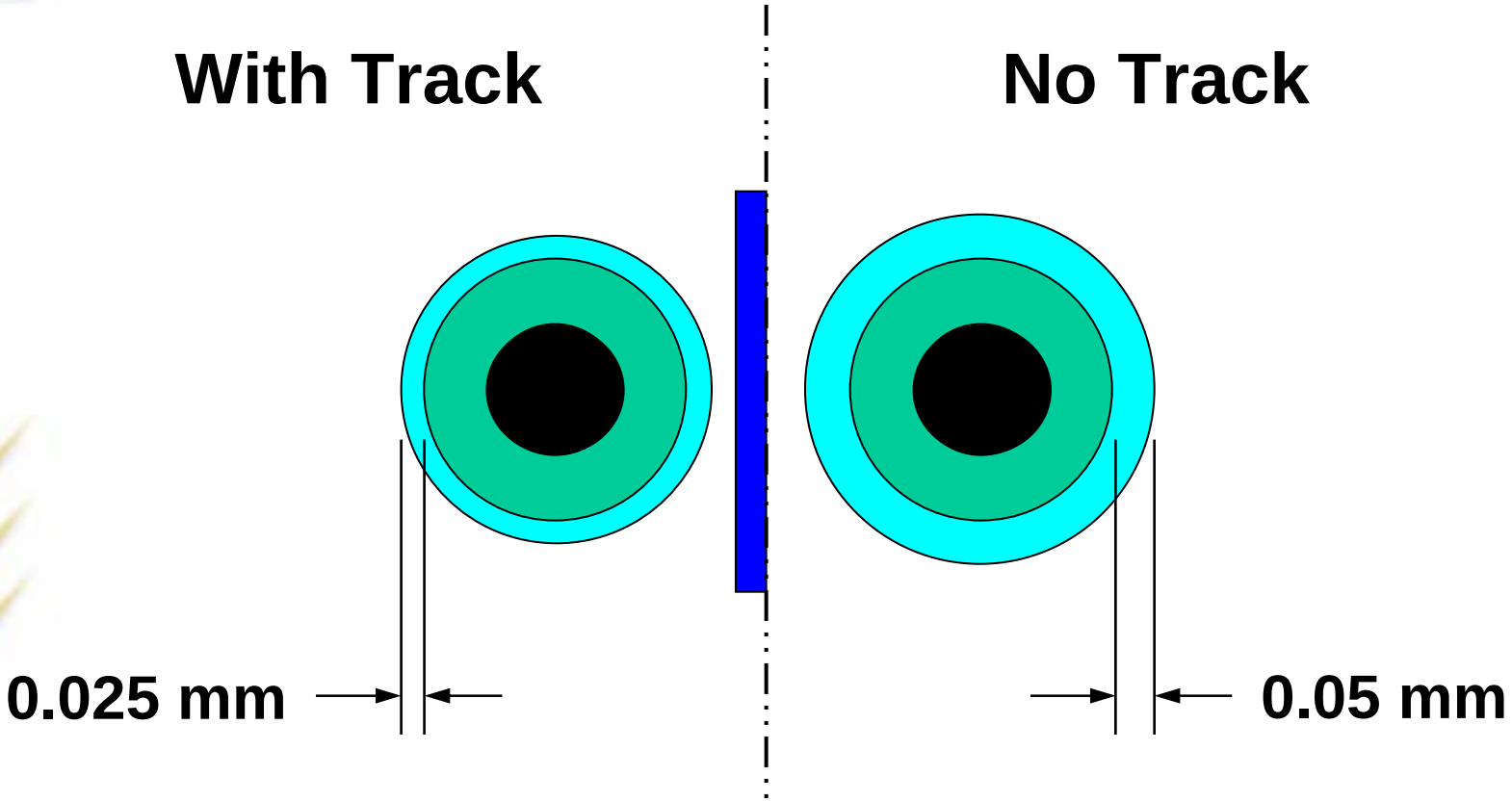
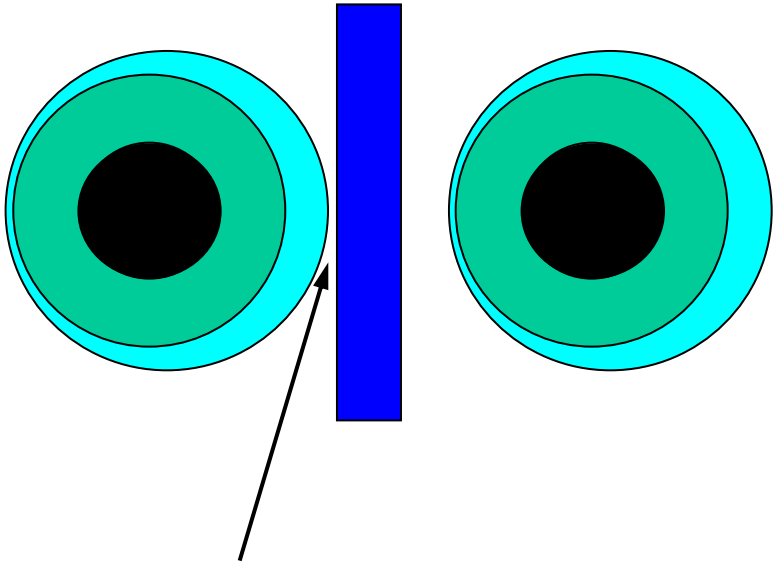
0.4 mm PITCH BGA

Solder Mask Clearance



0.4 mm PITCH BGA

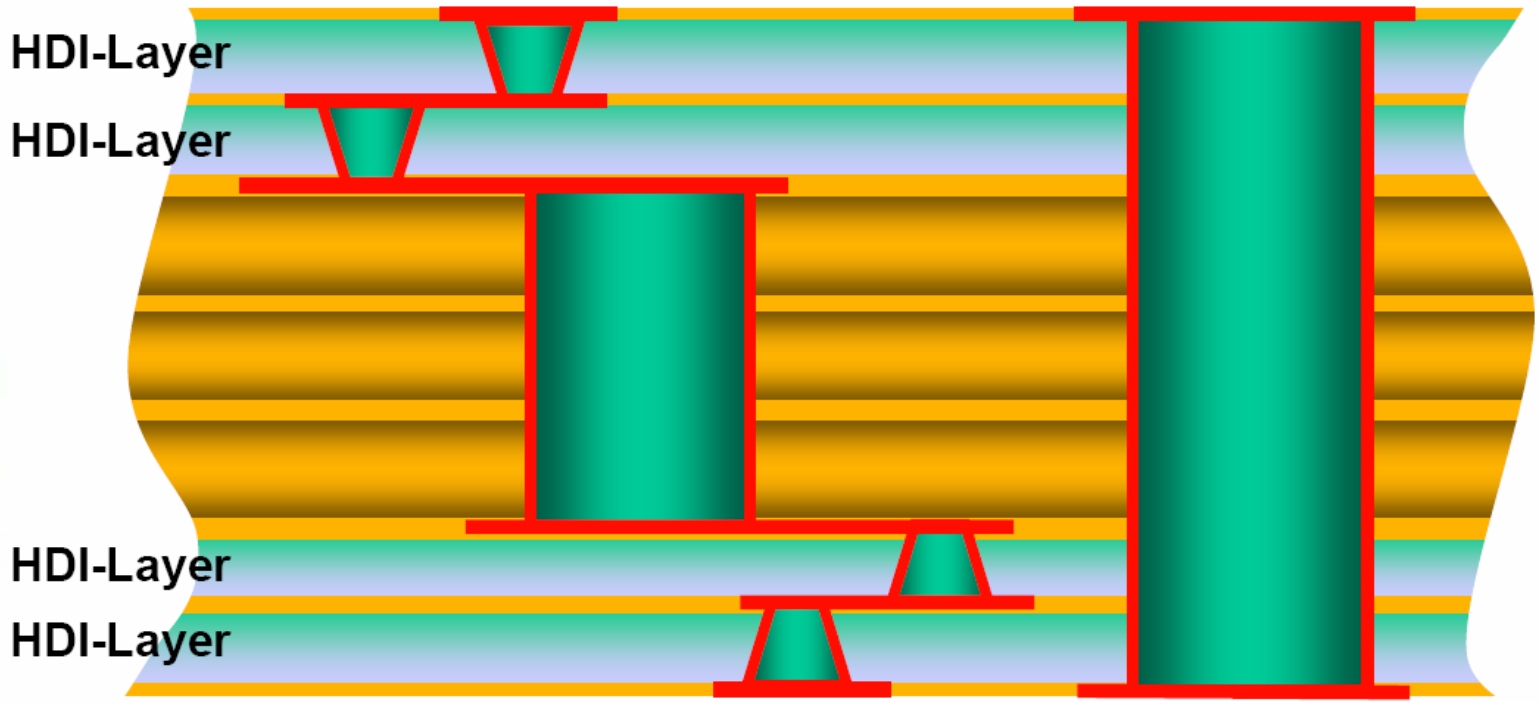
Solder Mask Maximum Offset



Safety distance to allow for coverage of line edge

0.4 mm PITCH BGA

Staggered Micro Vias



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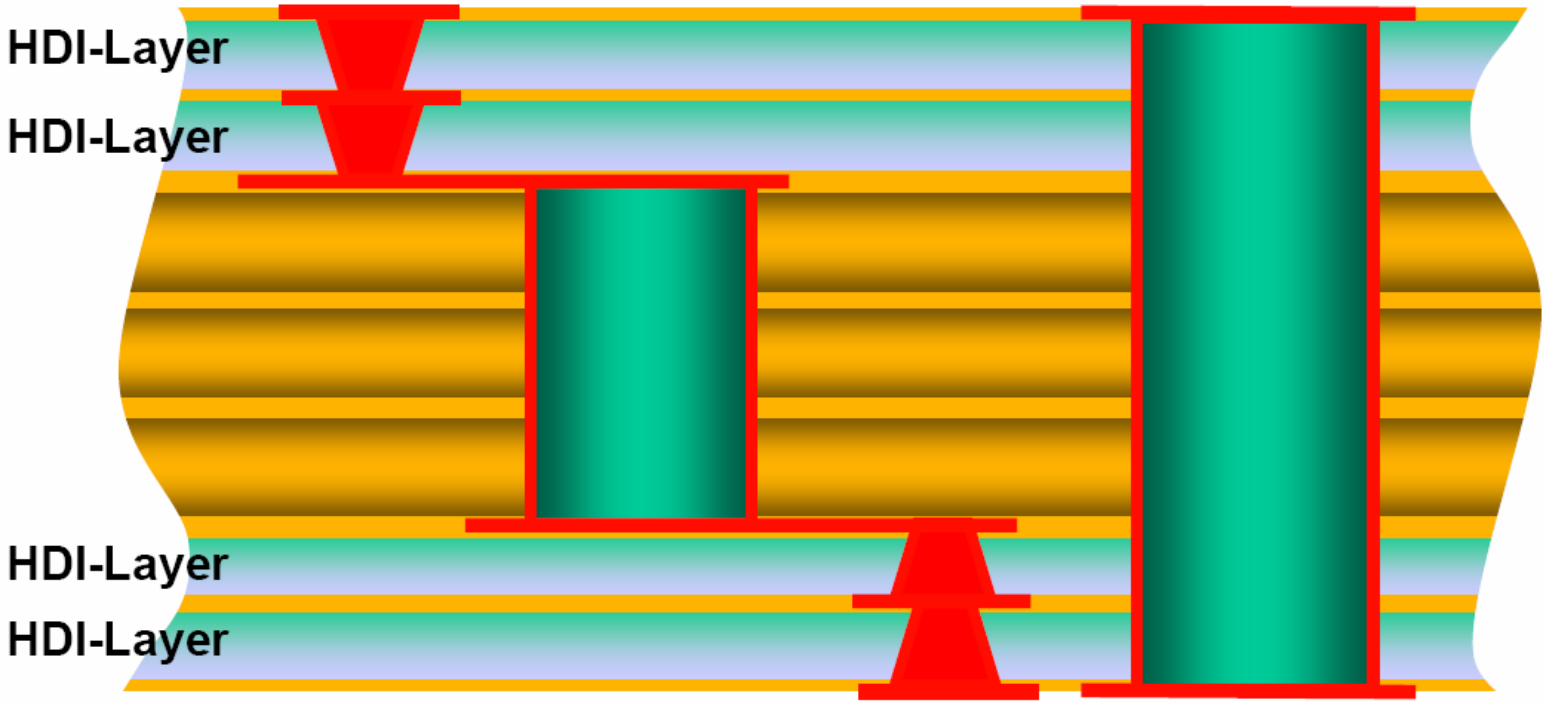
0.4 mm PITCH BGA

Stacked Micro Vias



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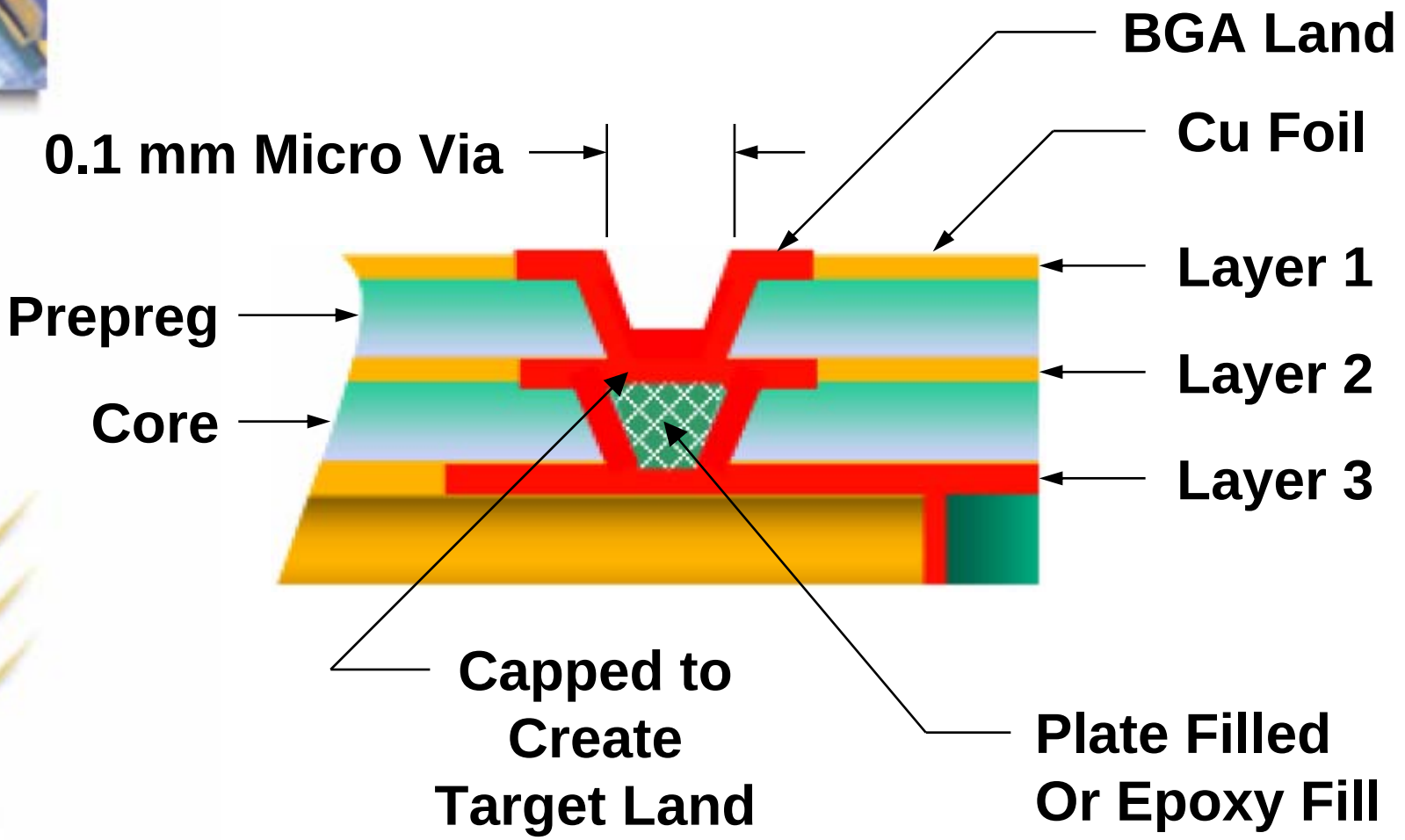
0.4 mm PITCH BGA



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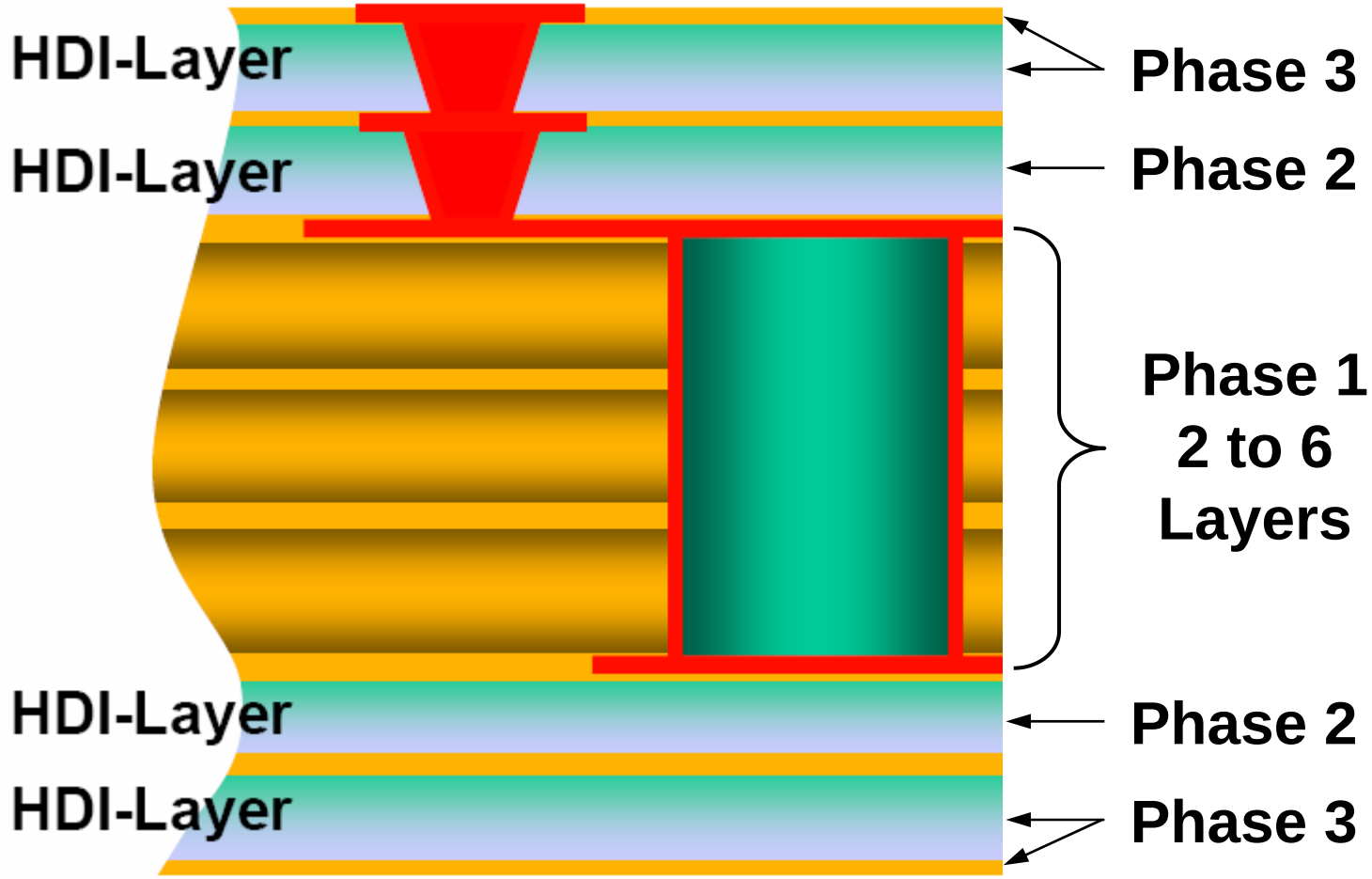
PCB LAYER CONSTRUCTION



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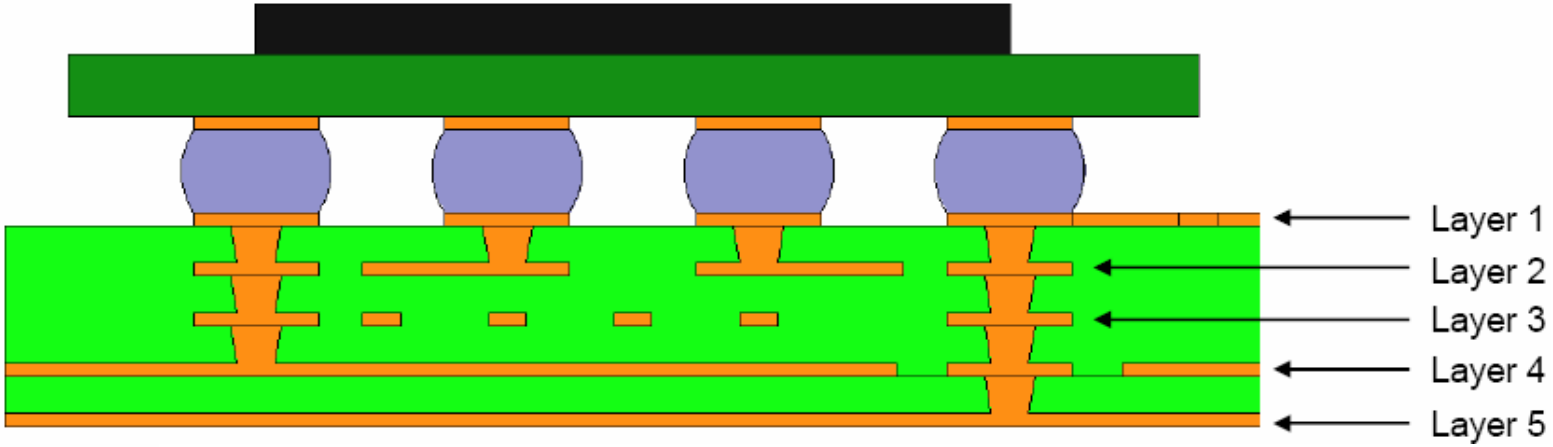
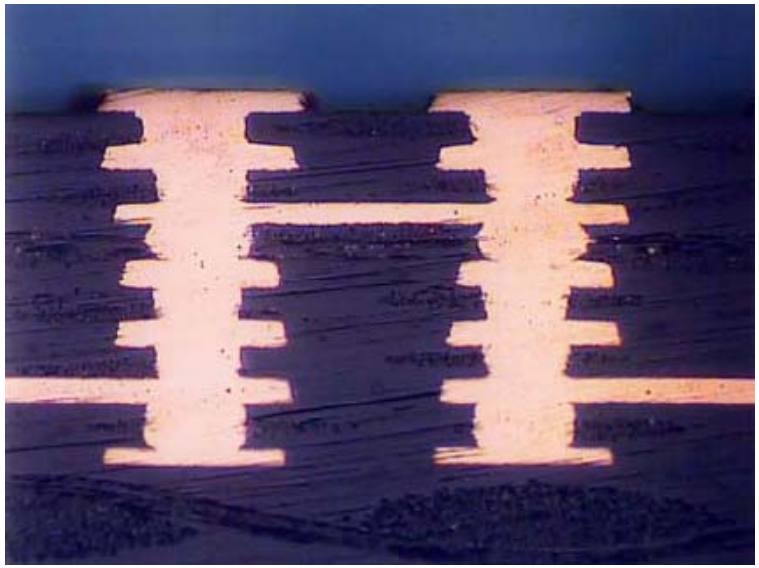
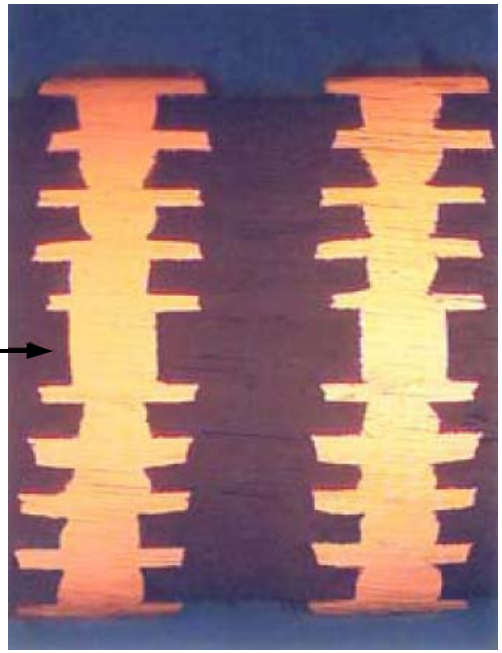
PCB LAYER CROSS SECTION





Core
Drill Bit



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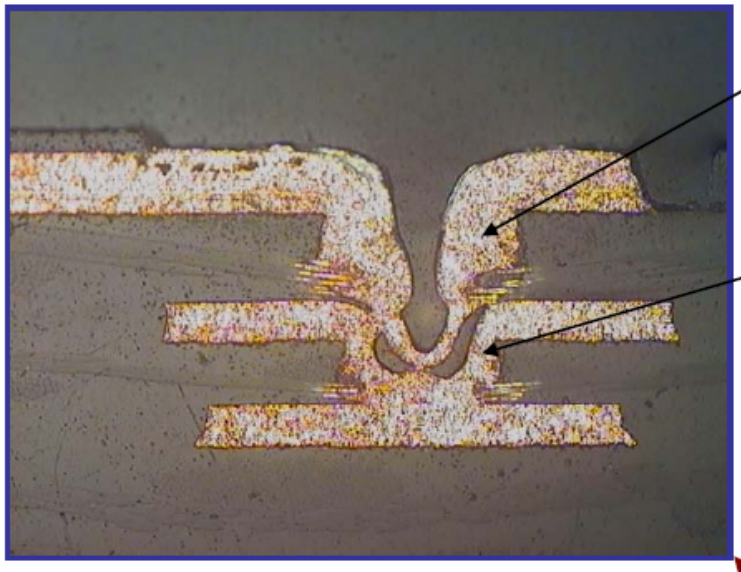
EPOXY FILLED MICRO VIAS

Avoid using epoxy filling for micro vias



1:2 Microvia, laser drilled directly on top of a 2:3 via with no plated copper fill

2:3 Microvia, epoxy filled prior to the laser drilling of the 1:2 via on top

"Brand X" Stacked Microvia

This process provides electrical continuity however, voiding and entrapped material results in failures in minor thermal cycling

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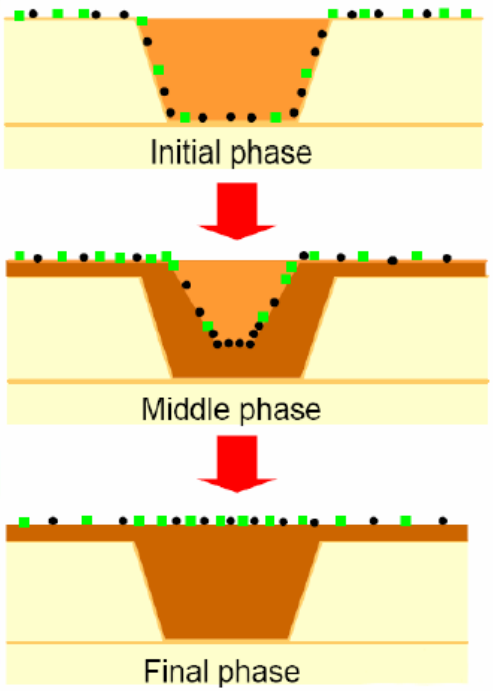
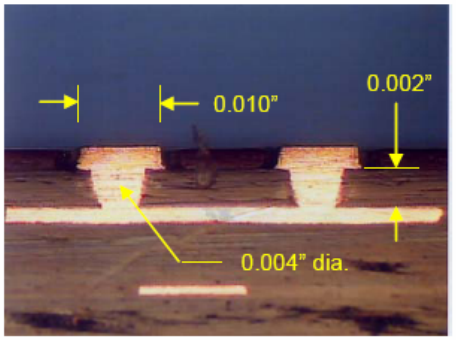
PLATED FILLED MICRO VIAS

Electroplated Copper via filling Mechanism

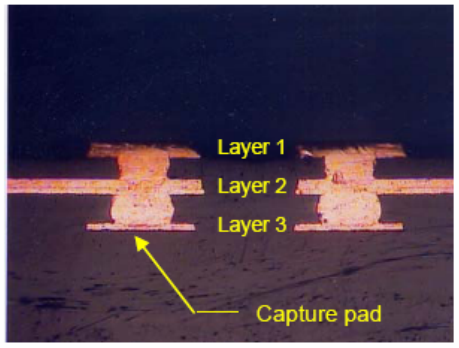


- Bottom-up filling behavior is attributed to the action of organic additives(must be controlled to prescribed limits)
- Suppressor rapidly forms current inhibiting film on Cu surface. Film has little geometric dependence due to high suppressor solution concentration
- Accelerated bottom-up fill behavior is due to a local accumulation of brightener species at the feature base
- As surface area is reduced during deposition, the concentration of brightener species increases, resulting in a non-equilibrium surface concentration. This local concentration of brightener accelerates the plating rate relative to the surface.

Planar Microvia



Stacked Microvia



Source: ROHM HAAS ELECTRONIC MATERIALS CIRCUIT BOARD TECHNOLOGIES

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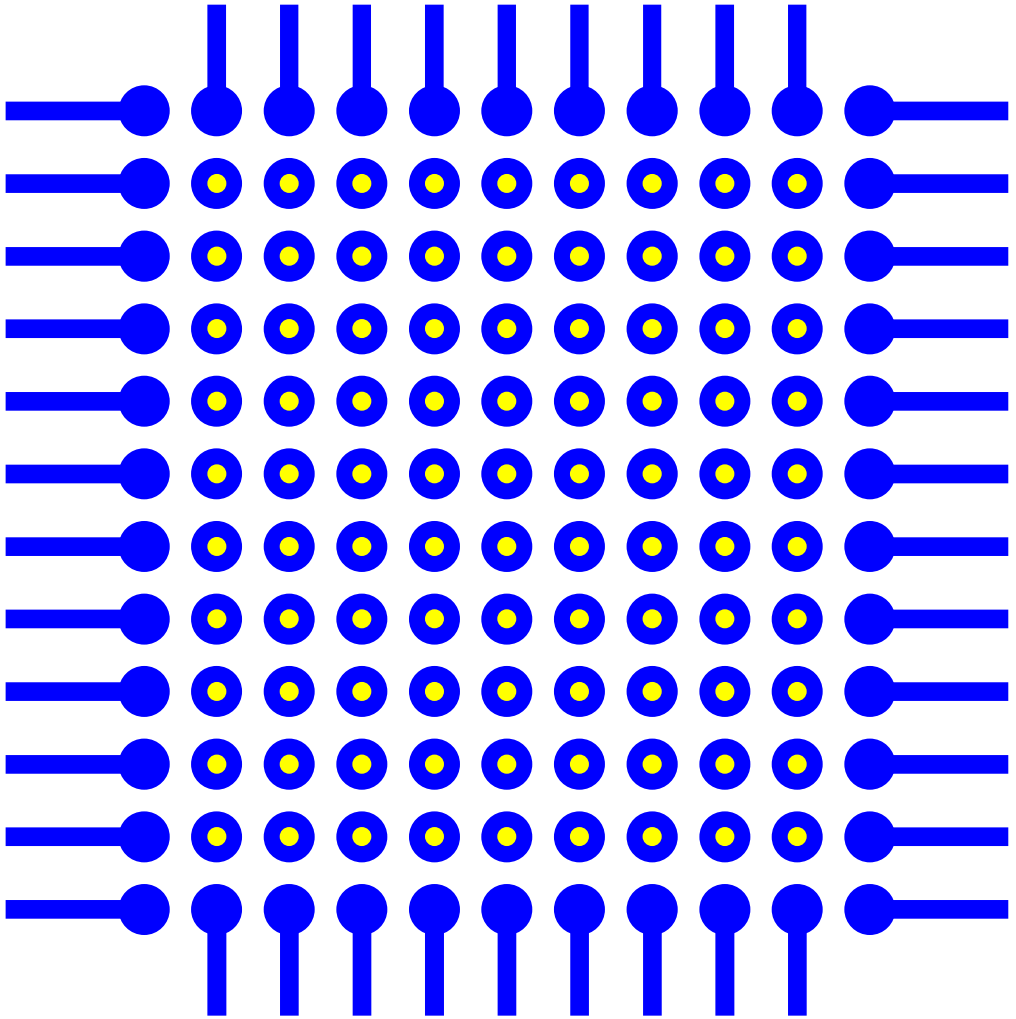
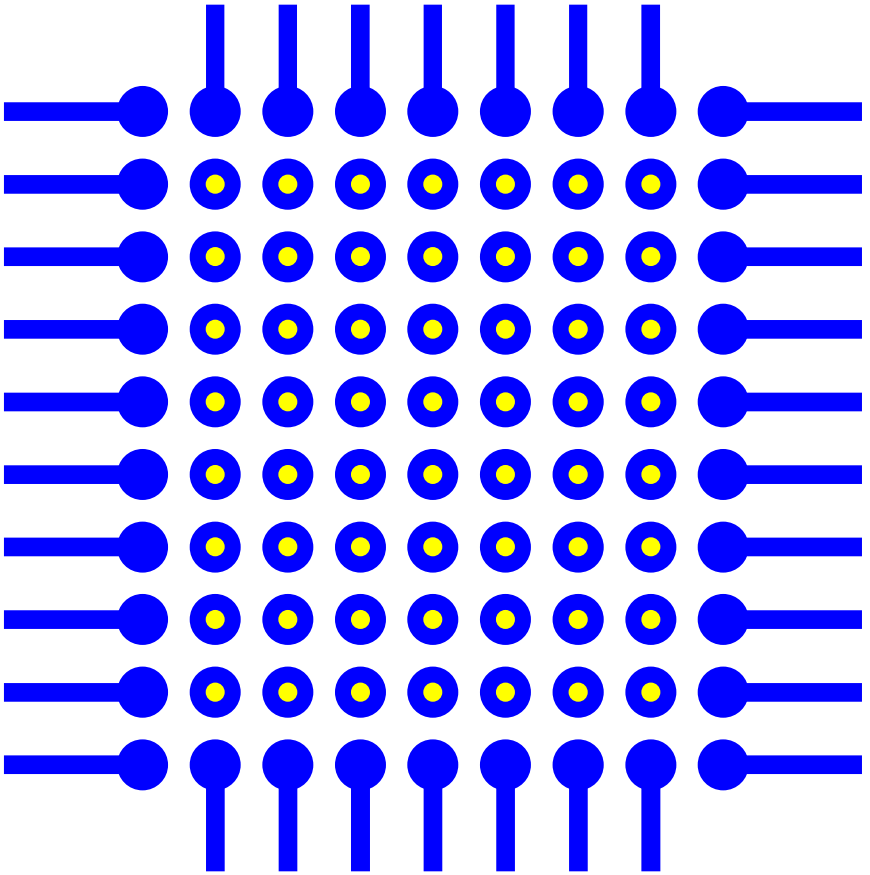
11 X 12 0.4 mm PITCH BGA



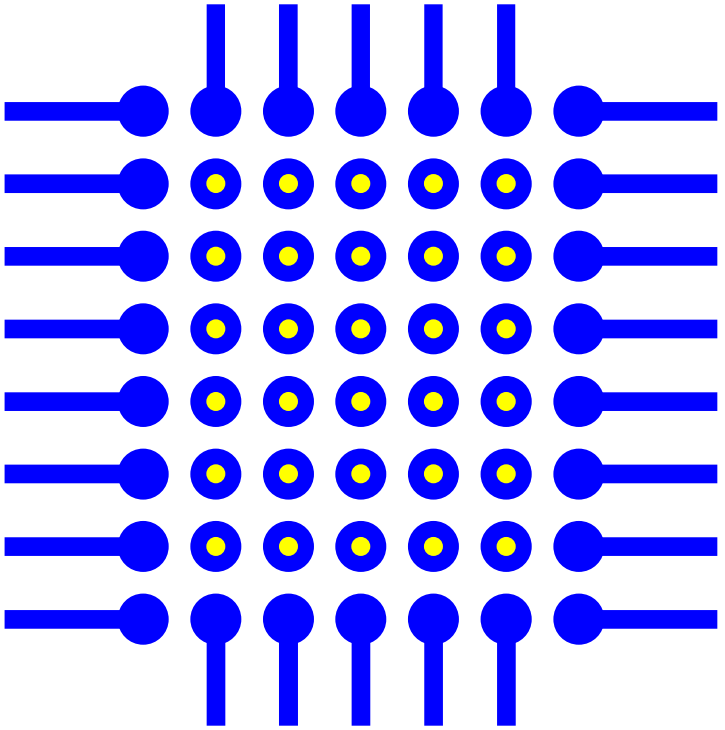
Route outside row on layer 1

11 X 12 0.4 mm PITCH BGA



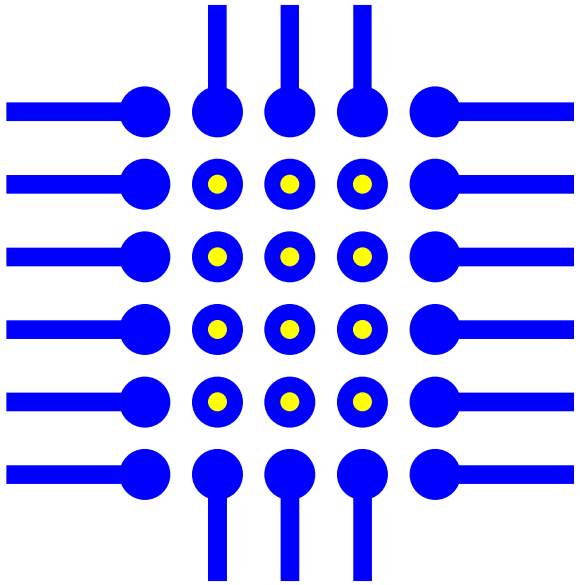
Route outside row on layer 2

11 X 12 0.4 mm PITCH BGA



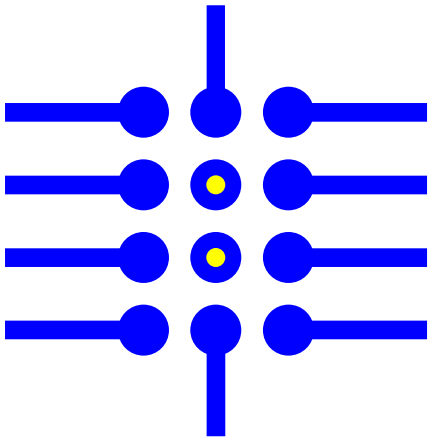
Route outside row on layer 3

11 X 12 0.4 mm PITCH BGA



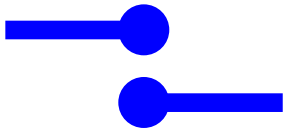
Route outside row on layer 4

11 X 12 0.4 mm PITCH BGA



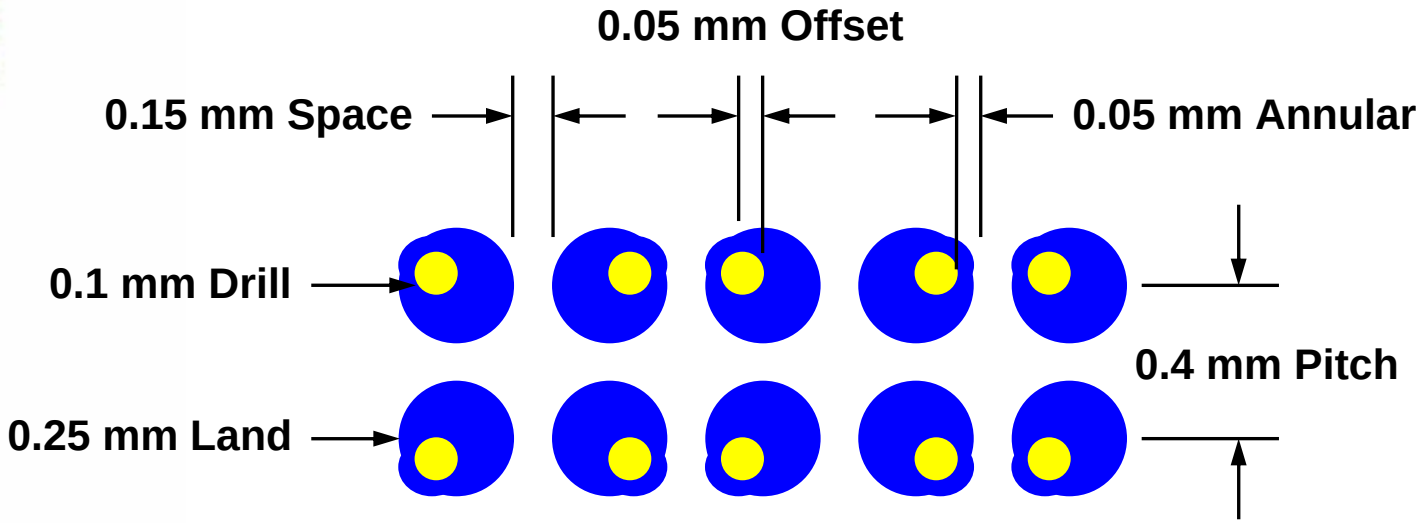
Route outside row on layer 5

11 X 12 0.4 mm PITCH BGA



Route outside row on layer 6

ADVANCED ROUTING TECHNIQUE FOR 0.4 mm BGA



0.4 mm BGA routing option

0.25 mm pad with 0.05 mm snowman for drill AR

LDI Solder Mask = 0.1 mm solder dam

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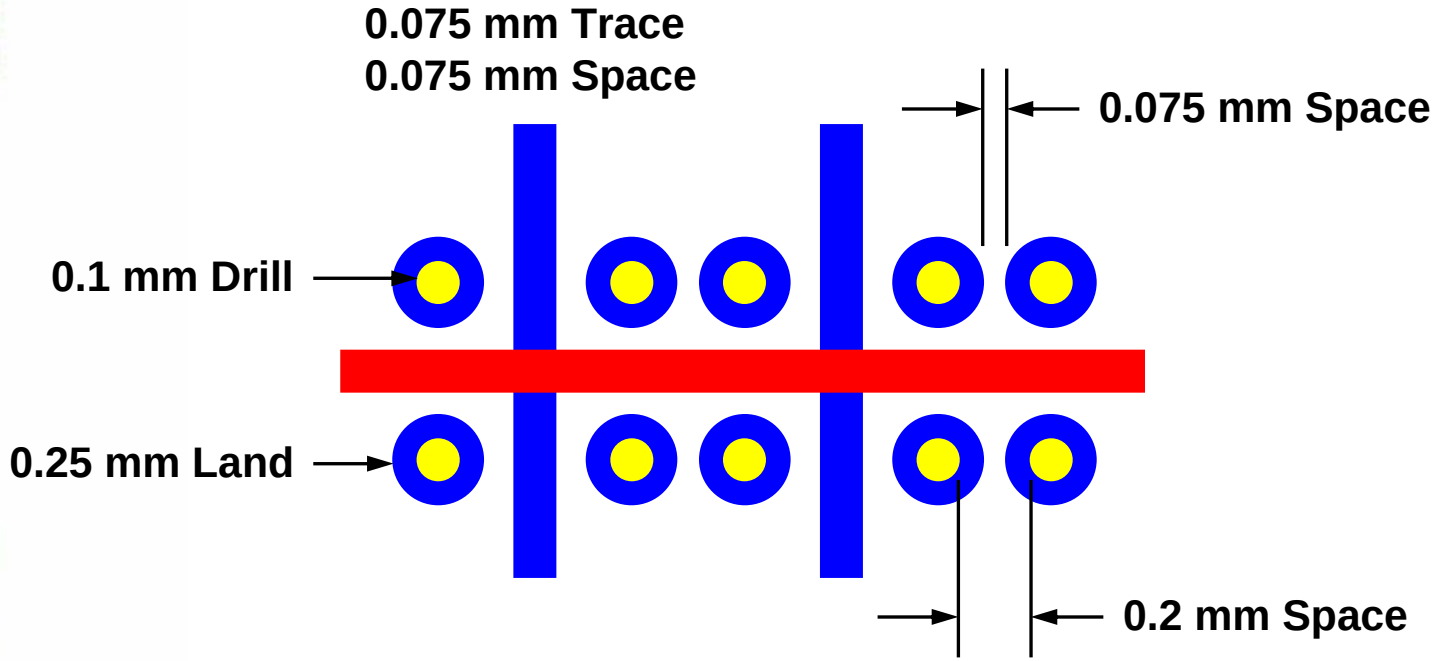
ADVANCED ROUTING TECHNIQUE FOR 0.4 mm BGA



0.4 mm BGA routing option

Route outside row & 50% of channels per layer

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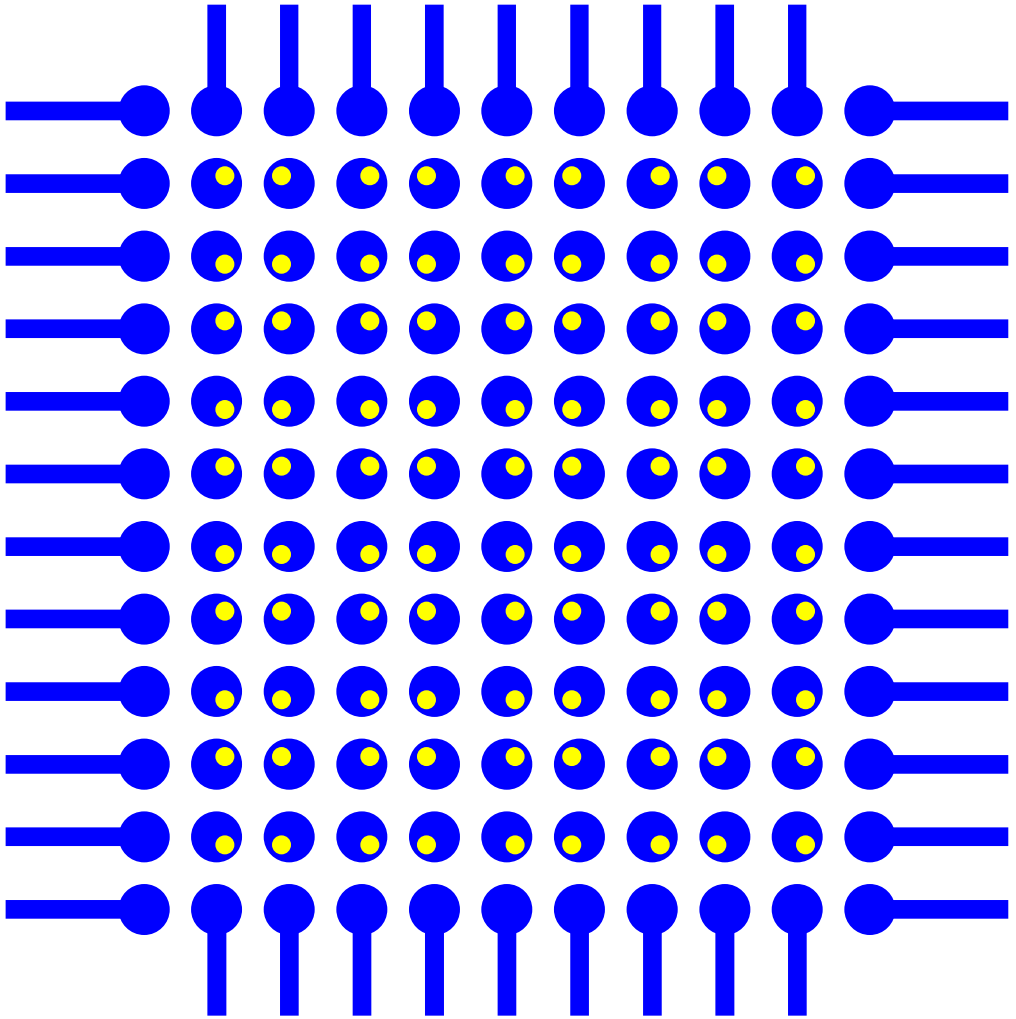
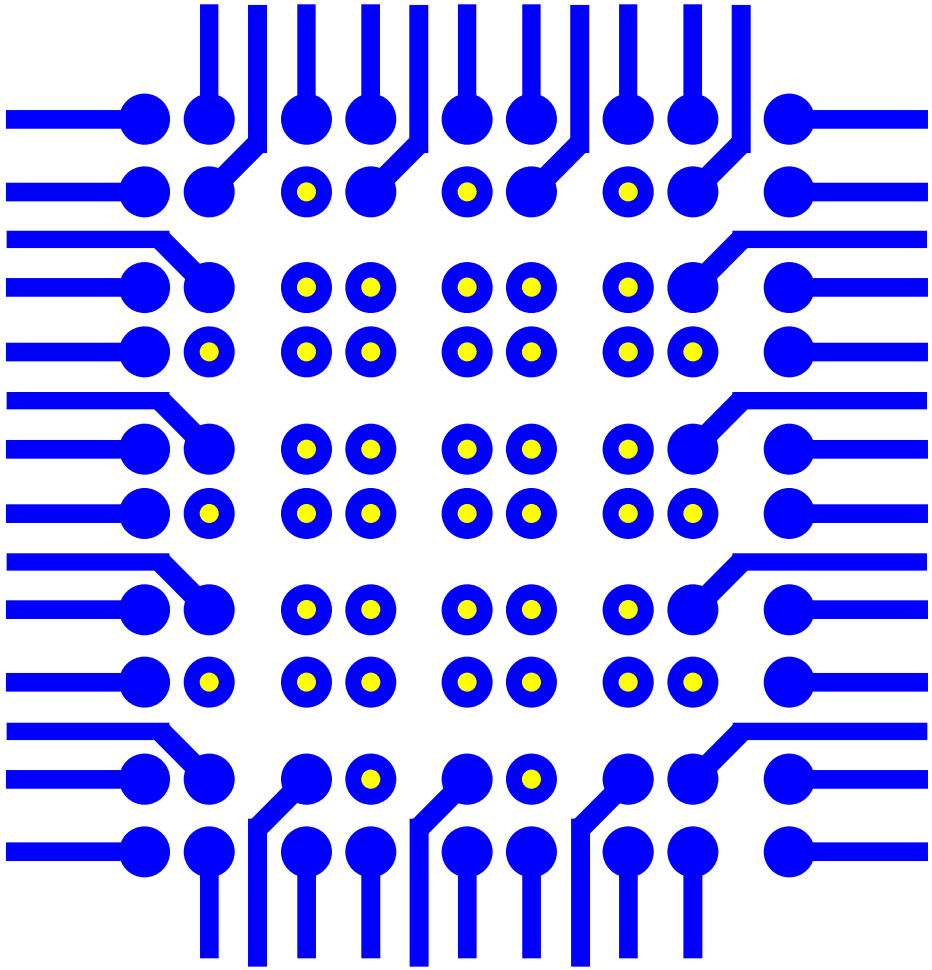
11 X 12 0.4 mm PITCH BGA



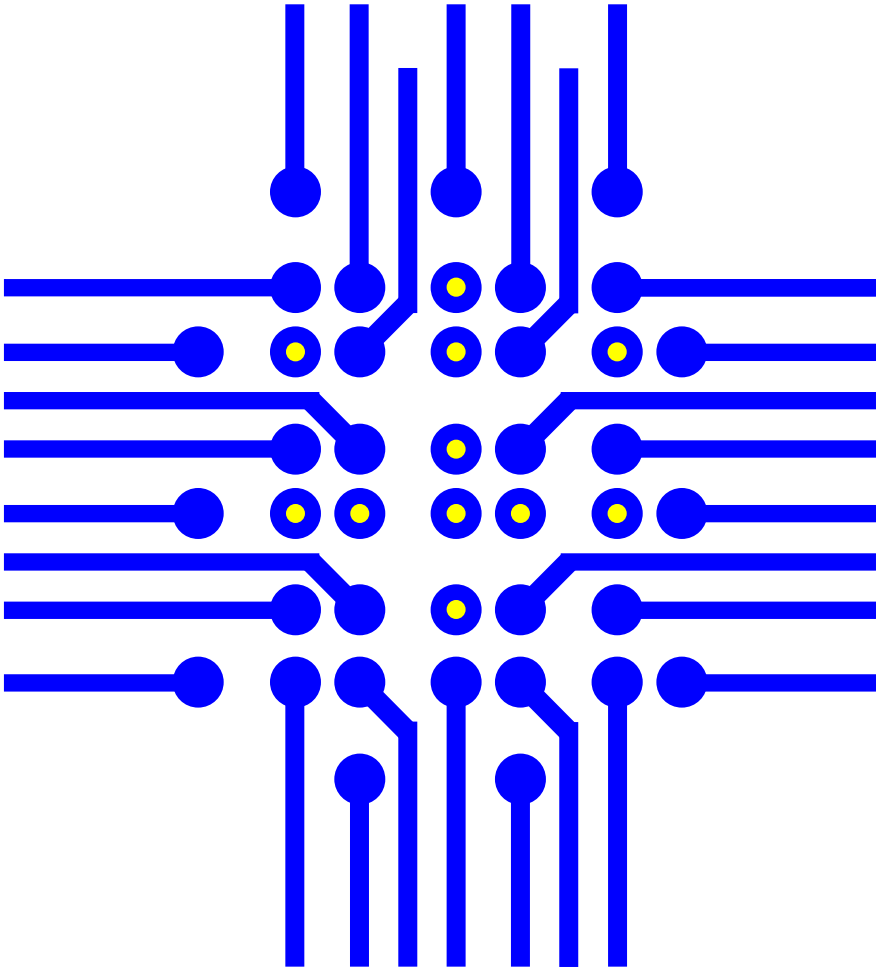
Route outside row on layer 1

11 X 12 0.4 mm PITCH BGA



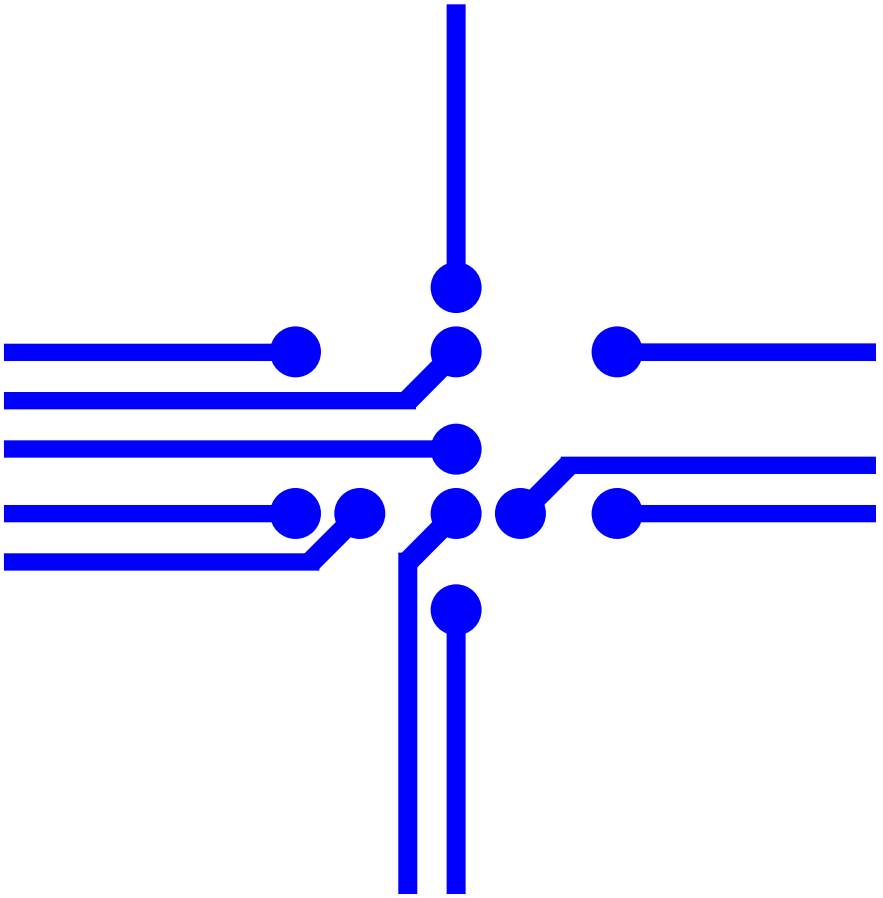
Route outside row on layer 2

11 X 12 0.4 mm PITCH BGA



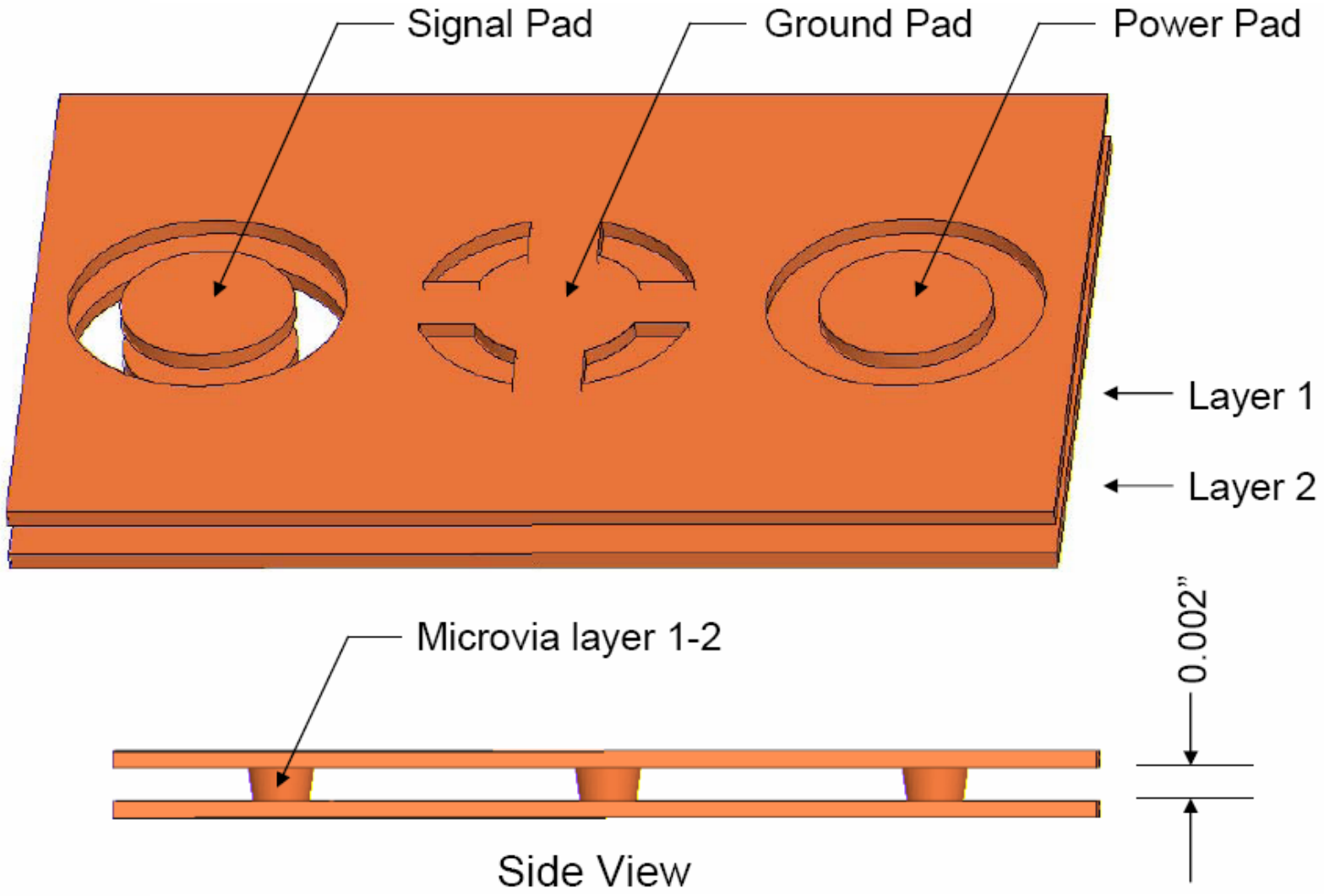
Route outside row on layer 3

11 X 12 0.4 mm PITCH BGA



Route outside row on layer 4

HDI VIA PLANE CONNECTION



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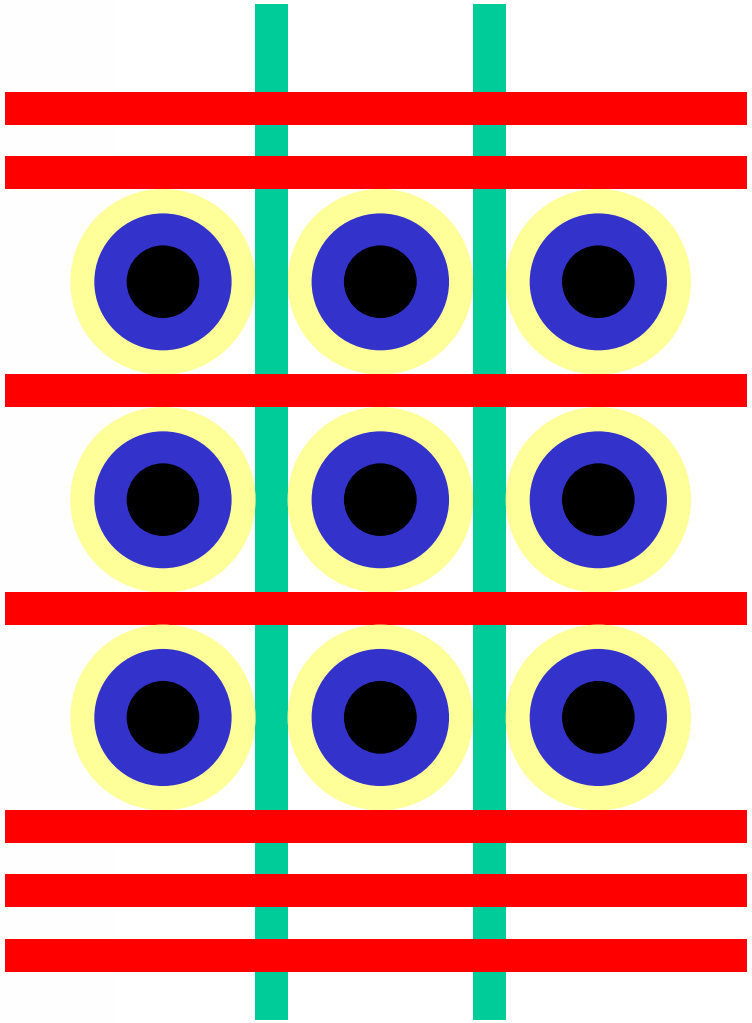
0.5 mm PITCH BGA



Via-in-Pad Technology

BGA Ball Size: 0.30 (12)
BGA Land Dia: 0.275 (11)
Hole Size: 0.15 (6)
Thermal Relief Required
Plane Clearance: 0.425
Solder Mask: 1:1 scale

Trace/Space Data

Trace Width: 0.075 (3)
Trace/Trace Space: 0.075
Trace/Via Space: 0.075 (3)
Trace/BGA Land: 0.075 (3)
Routing Grid: 0.05 (2)
Part Place Grid: 0.5 (20)

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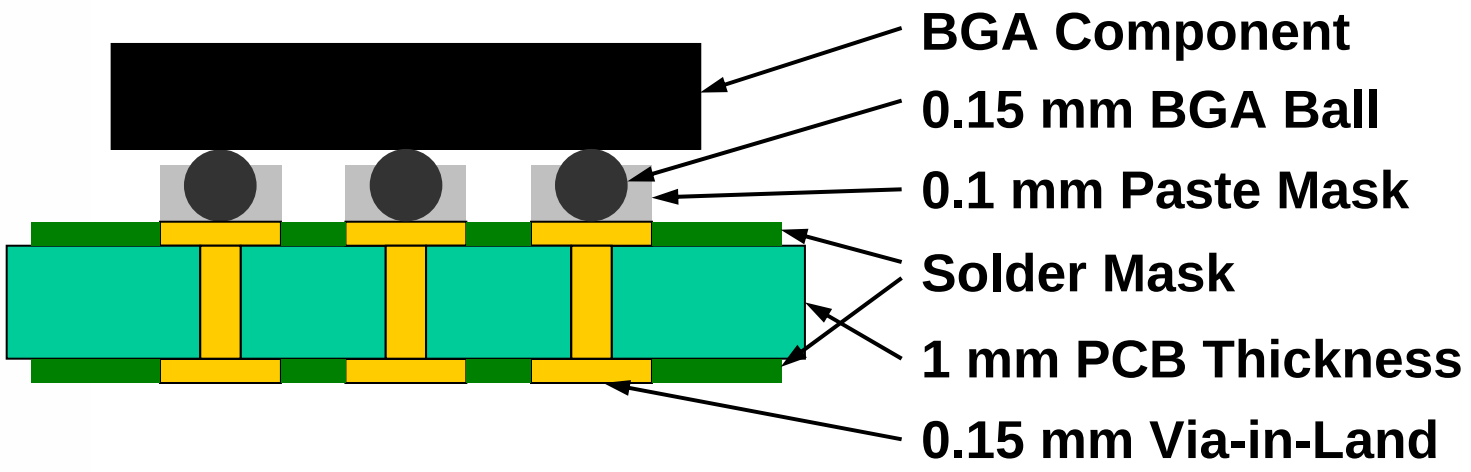
0.5 mm PITCH BGA WITH NON-COLLAPSING BALLS

Via-in-Pad Technology

BGA Ball Size: 0.15 (6)
BGA Land Dia: 0.275 (11)
Hole Size: 0.15 (6)
Plane Clearance: 0.425 (17)
Solder Mask: 1:1 scale

Trace/Space Data

Trace Width: 0.075 (3)
Trace/Trace Space: 0.075
Trace/Via Space: 0.075 (3)
Trace/BGA Land: 0.75 (3)
Routing Grid: 0.05 (2)



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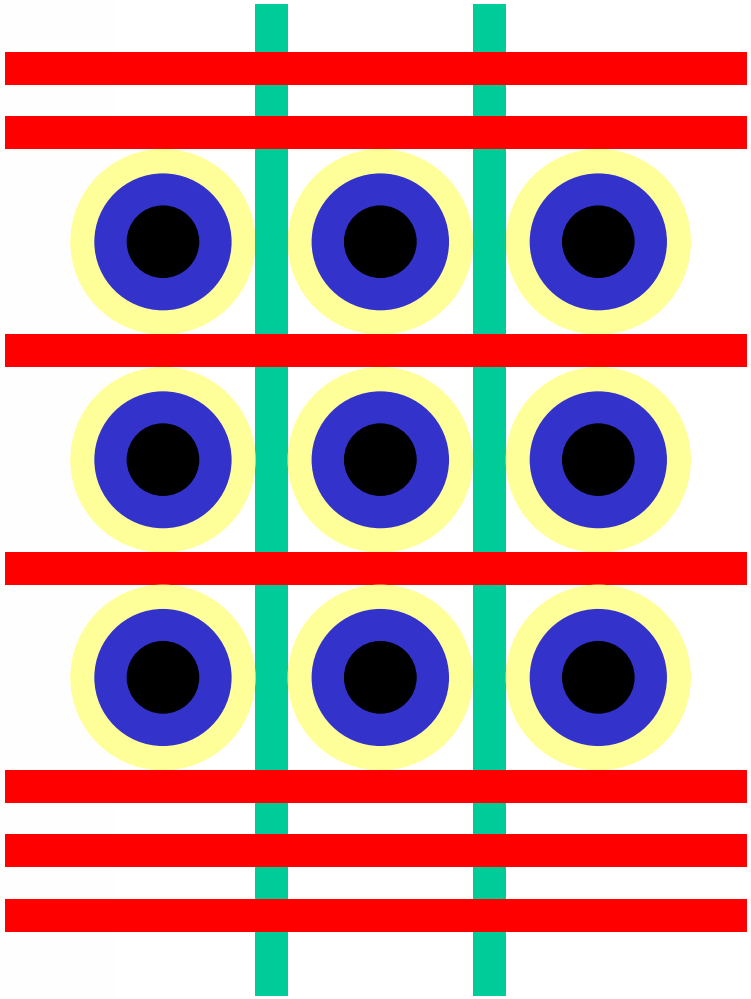
0.65 mm PITCH BGA



Via-in-Pad Technology

BGA Ball Size: 0.4 (16)
BGA Land Dia: 0.4 (16)
Hole Size: 0.15 (6)
Plane Clearance: 0.5 (20)
Solder Mask: 1:1 scale

Trace/Space Data

Trace Width: 0.1 (4)
Trace/Trace Space: 0.1 (4)
Trace/Via Space: 0.1 (4)
Trace/BGA Land: 0.75 (3)
Routing Grid: 0.05 (2)
Part Place Grid: 1 (40)

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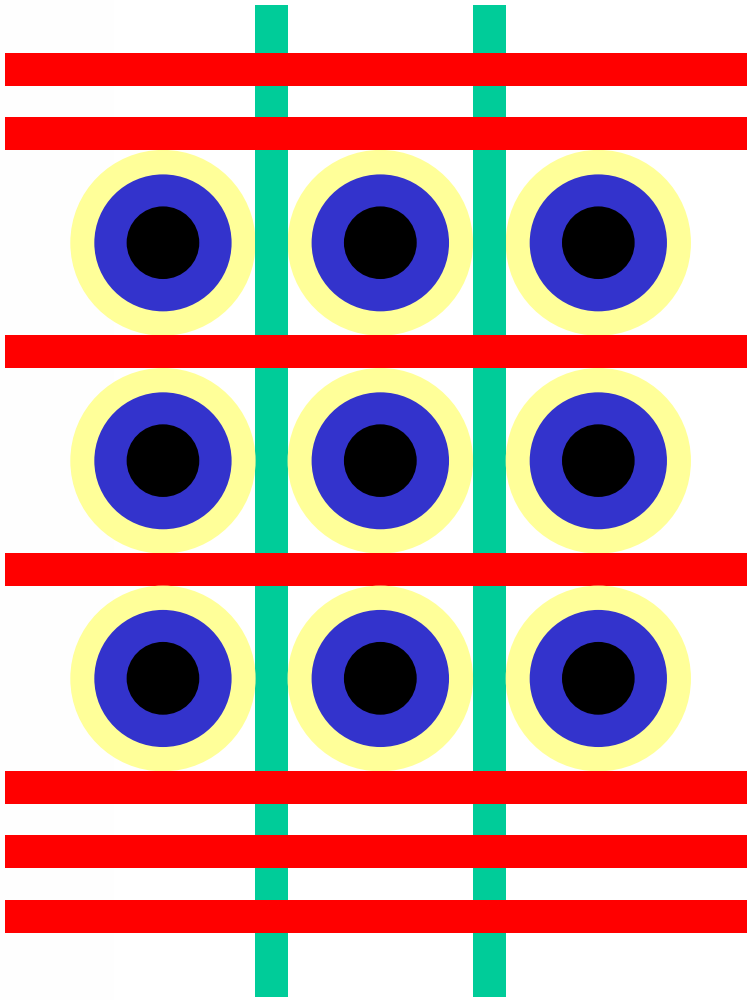
0.65 mm PITCH BGA



Via-in-Pad Technology

BGA Ball Size: 0.4 (16)
BGA Land Dia: 0.425 (17)
Hole Size: 0.2 (8)
Plane Clearance: 0.575
Solder Mask: 1:1 scale

Trace/Space Data

Trace Width: 0.075 (3)
Trace/Trace Space: 0.075
Trace/Via Space: 0.075 (3)
Routing Grid: 0.05 (2)
Via Grid: 0.65 (26)
Part Place Grid: 1 (40)

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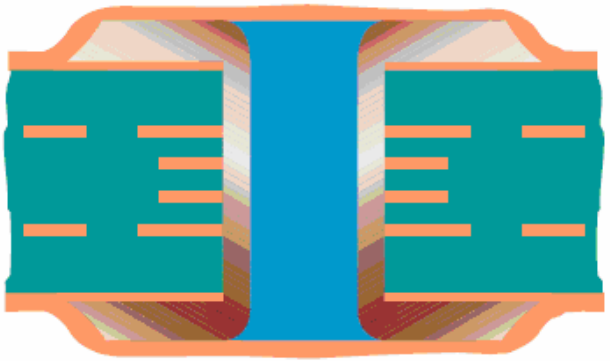
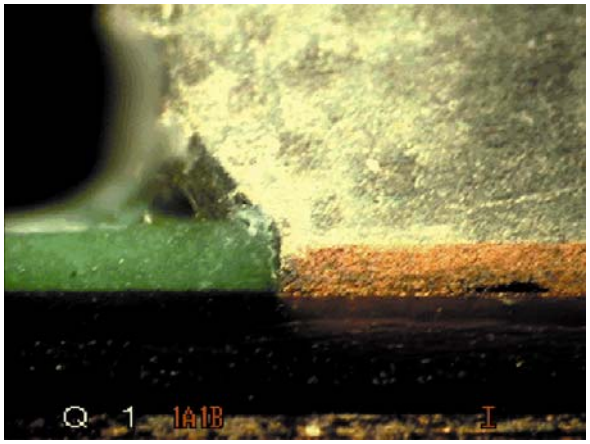
FILLED AND CAPPED VIA

Filled and Capped Via (Type VII Via) - A Type V via with a secondary metallized coating covering the via. The metallization is on both sides.

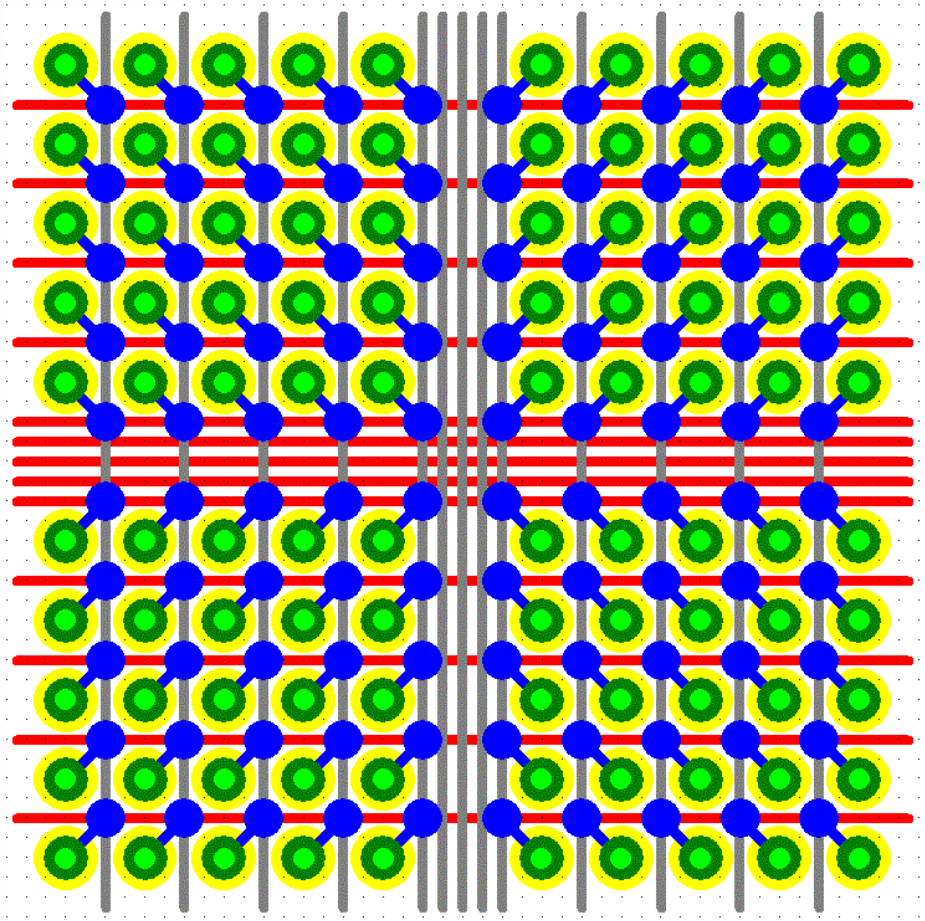
This technique is used for Via-in-pad technology for 0.65mm and 0.5mm BGA pitch devices.

Solder mask is 1:1 scale on the BGA side of PCB and Tented on the opposite side to protect the routed trace.





0.8 mm PITCH BGA



BGA Data

BGA Ball Dia: 0.5 (20)

BGA Land Size: 0.45 (17)

Via Data

Pad Size: 0.5 (20)

Hole Size: 0.25 (10)

Anti-Pad: 0.7 (28)

Trace/Space Data

Trace Width: 0.1 (4)

Trace/Trace Space: 0.1

Trace/Via Space: 0.125

Routing Grid: 0.1 (4)

Via Grid: 0.2 (8)

Part Place Grid: 1 (40)

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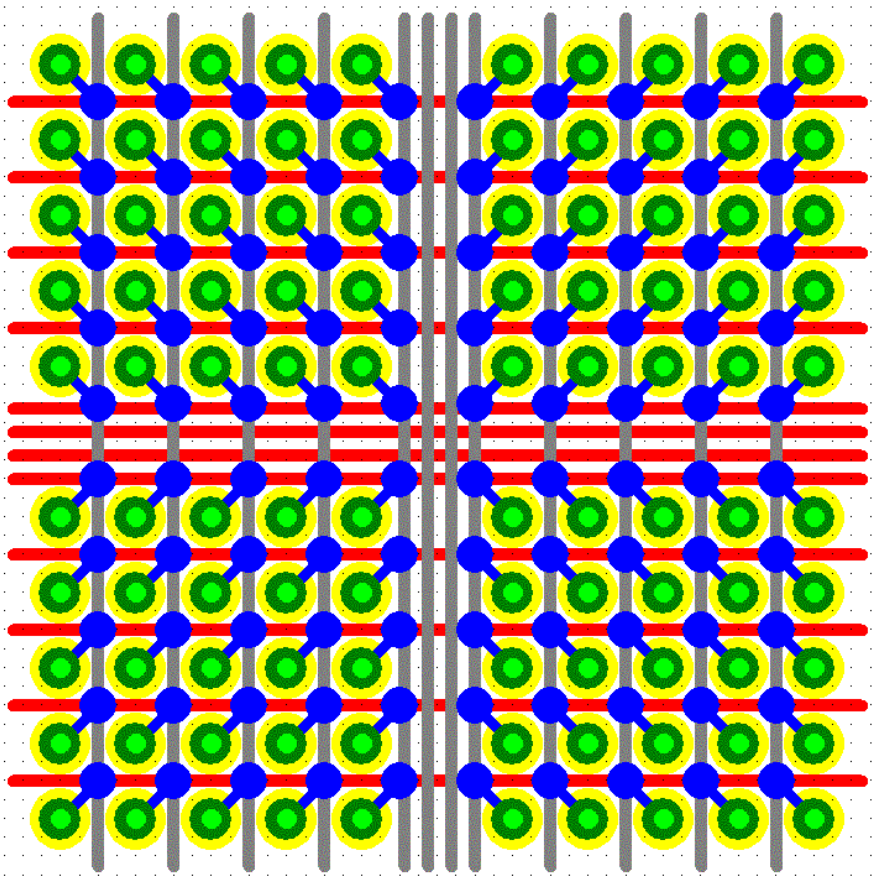
0.8 mm PITCH BGA



BGA Data

BGA Ball Dia: 0.5 (20)

BGA Land Size: 0.45 (17)

Via Data

Pad Size: 0.45 (18)

Hole Size: 0.2 (8)

Anti-Pad: 0.65 (26)

Trace/Space Data

Trace Width: 0.125 (5)

Trace/Trace Space: 0.125

Trace/Via Space: 0.1 (4)

Routing Grid: 0.05 (2)

Via Grid: 0.2 (8)

Part Place Grid: 1 (40)

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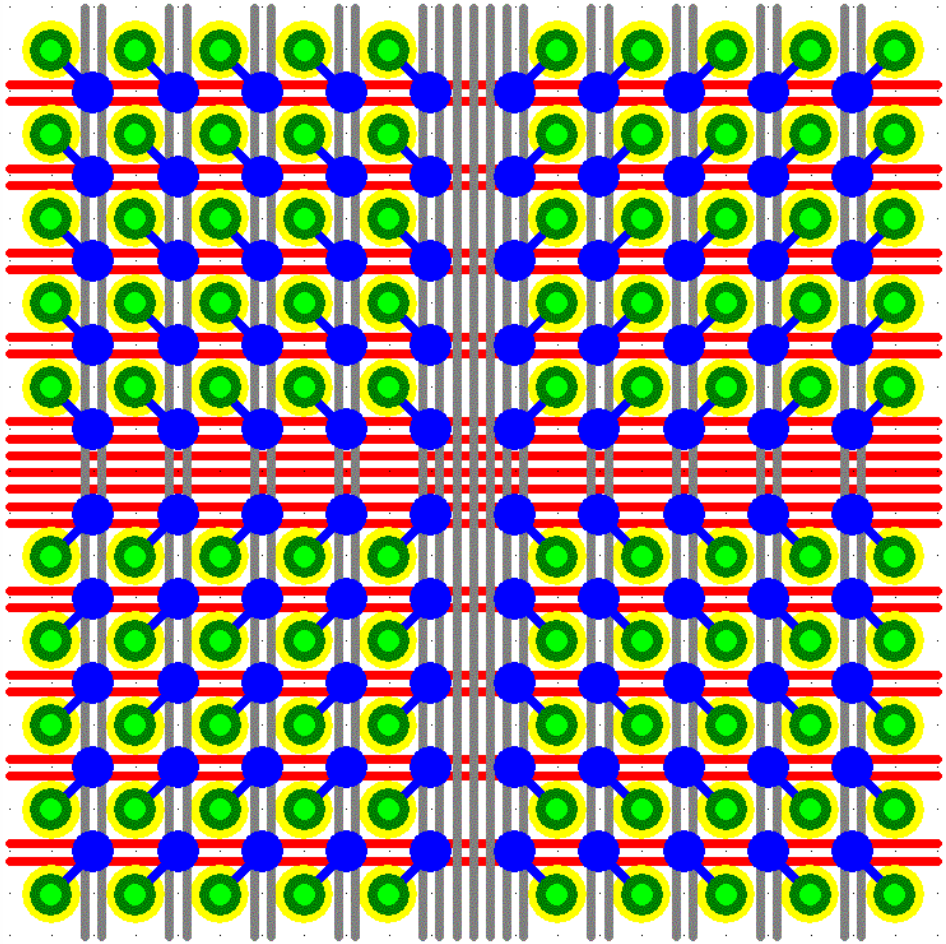
1 mm PITCH BGA



Via Data

Pad Size: 0.50 (20)
Hole Size: 0.25 (10)
Plane Clearance: 0.70

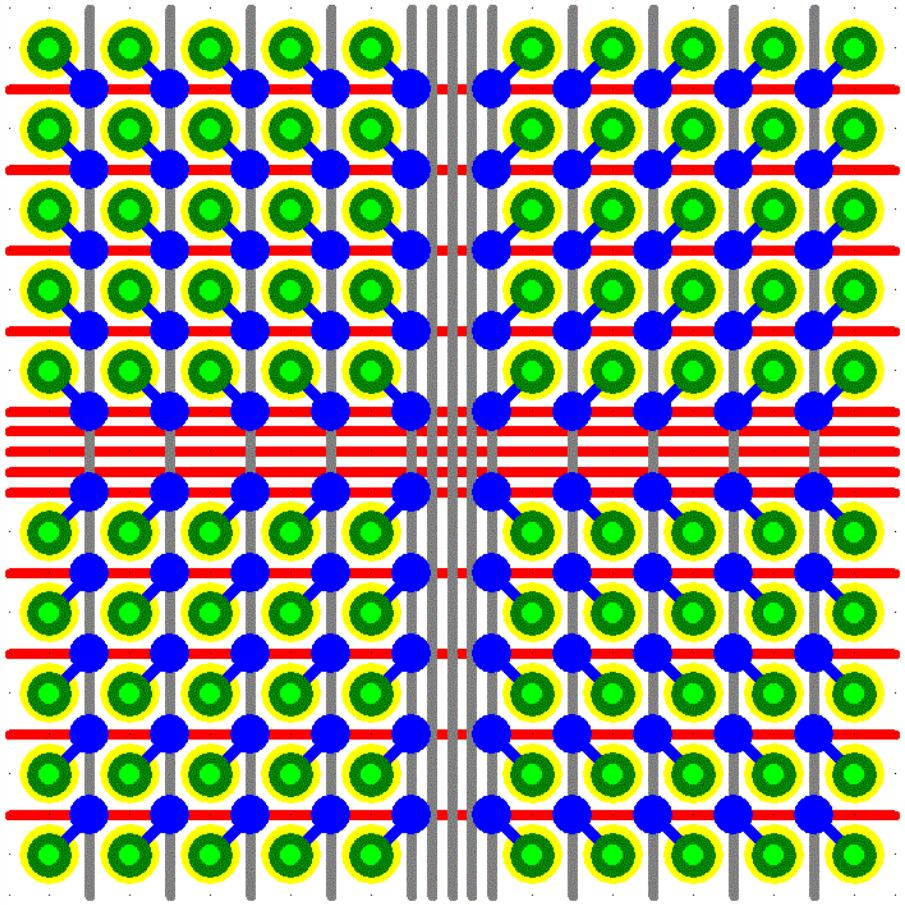
BGA Land Size: 0.5 (20)

Trace/Space Data

Trace Width: 0.1 (4)
Trace/Trace Space: 0.1
Trace/Via Space: 0.1
Routing Grid: 0.1 (4)
Via Grid: 0.5 (20)
Part Place Grid: 0.5 (20)

IPC DESIGNERS COUNCIL

1 mm PITCH BGA



Via Data

Pad Size: 0.55 (22)
Hole Size: 0.25 (10)
Anti-Pad: 0.75 (30)

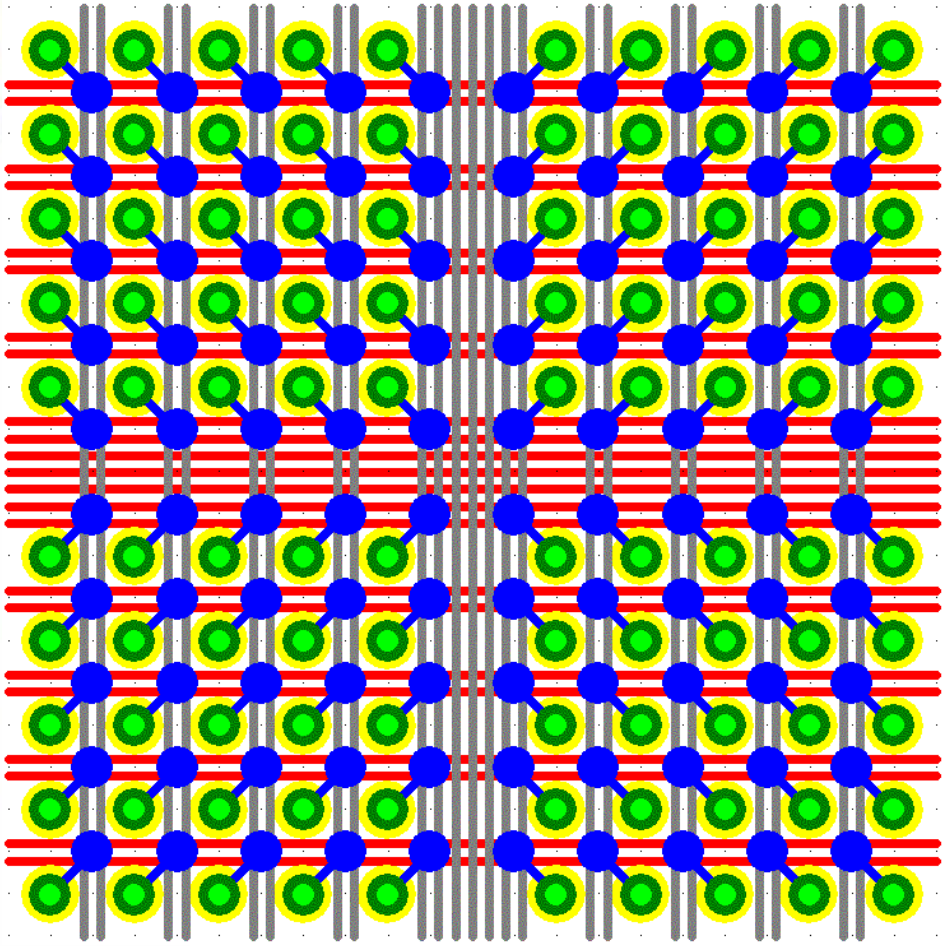
BGA Land Size: 0.5 (20)

Trace/Space Data

Trace Width: 0.125 (5)
Trace/Trace Space: 0.125
Trace/Via Space: 0.16 (6)
Routing Grid: 0.05 (2)
Via Grid: 0.5 (20)
Part Place Grid: 0.5 (20)

IPC DESIGNERS COUNCIL

1 mm PITCH BGA



Via Data

Pad Size: 0.375 (15)

Hole Size: 0.175 (7)

Plane Clearance: 0.625

BGA Land Size: 0.5 (20)

Trace/Space Data

Trace Width: 0.125 (5)

Trace/Trace Space: 0.125

Trace/Via Space: 0.125

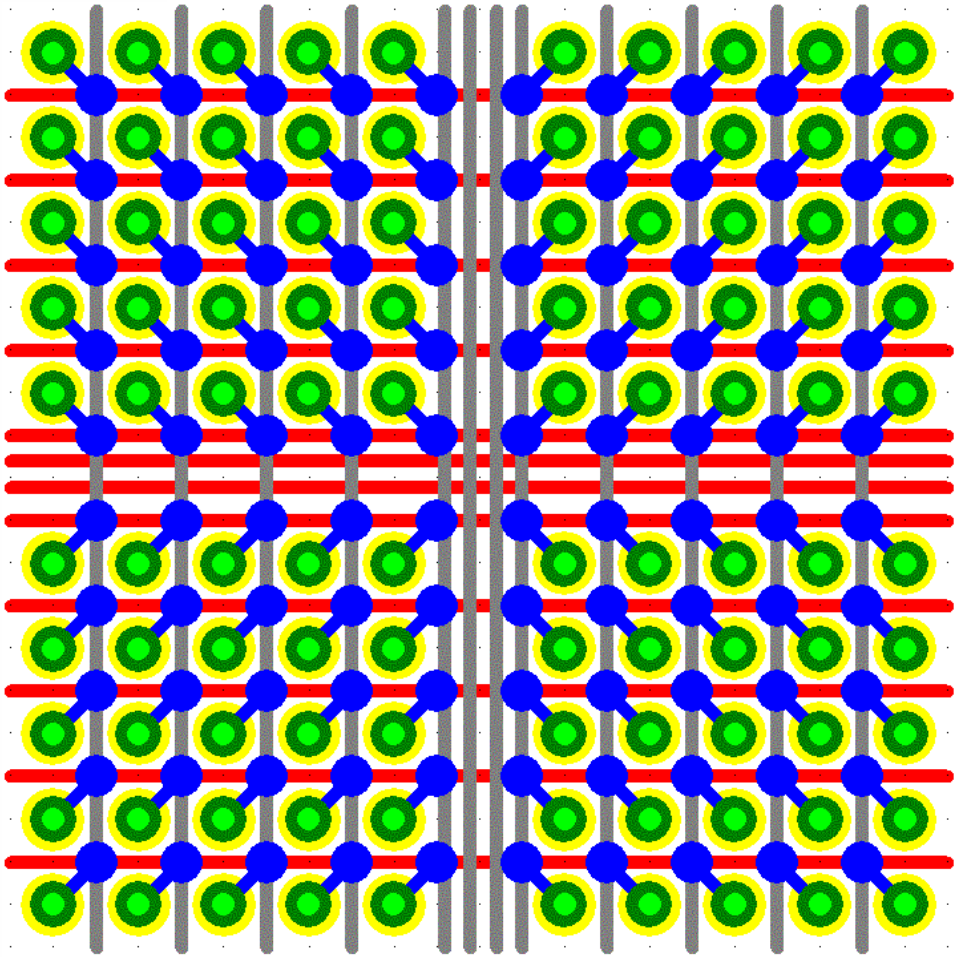
Routing Grid: 0.05 (2)

Via Grid: 0.5 (20)

Part Place Grid: 0.5 (20)

IPC DESIGNERS COUNCIL

1 mm PITCH BGA



Via Data

Pad Size: 0.55 (22)
Hole Size: 0.25 (10)
Plane Clearance: 0.75

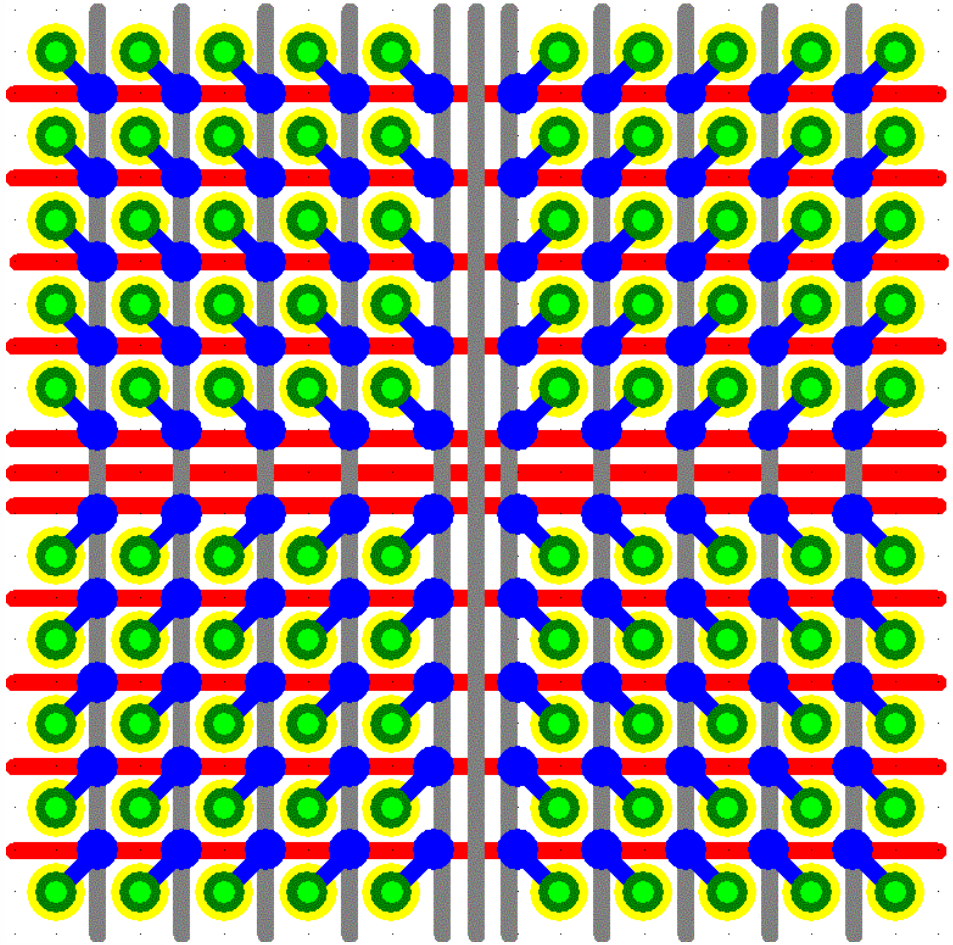
BGA Land Size: 0.5 (20)

Trace/Space Data

Trace Width: 0.15 (6)
Trace/Trace Space:0.15
Trace/Via Space: 0.15
Routing Grid: 0.05 (2)
Via Grid: 0.5 (20)
Part Place Grid: 0.5 (20)

IPC DESIGNERS COUNCIL

1 mm PITCH BGA



Via Data

Land: 0.50 (20)

Hole: 0.25 (10)

Plane Clearance: 0.70

BGA Land Size: 0.5 (20)

Trace/Space Data

Trace Width: 0.2 (8)

Trace/Trace Space: 0.2

Trace/Via Space: 0.15

Routing Grid: 0.1 (4)

Via Grid: 0.5 (20)

Part Place Grid: 0.5 (20)

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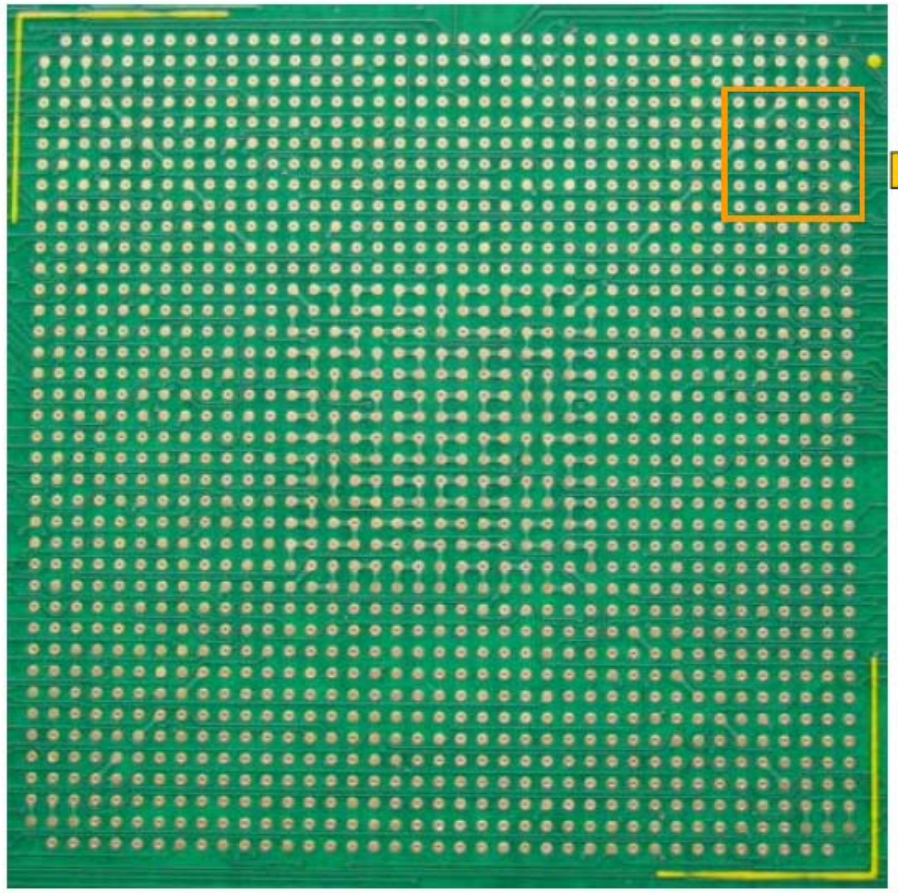
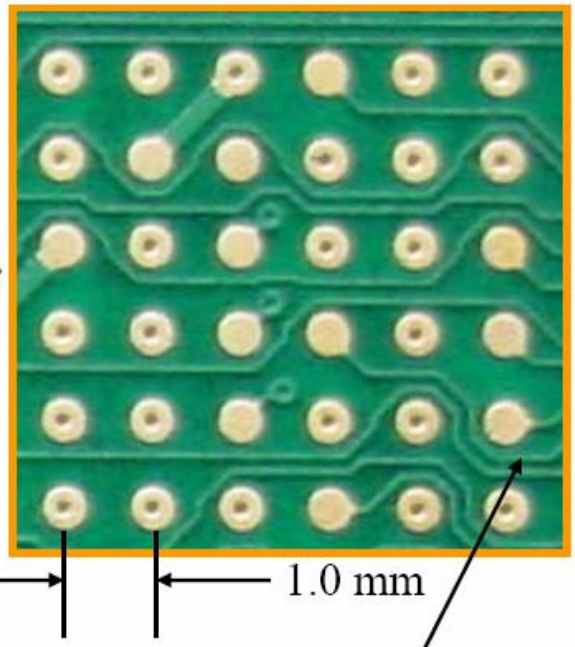
VIA-IN-PAD EXAMPLE

39 x 39 1.0 mm BGA





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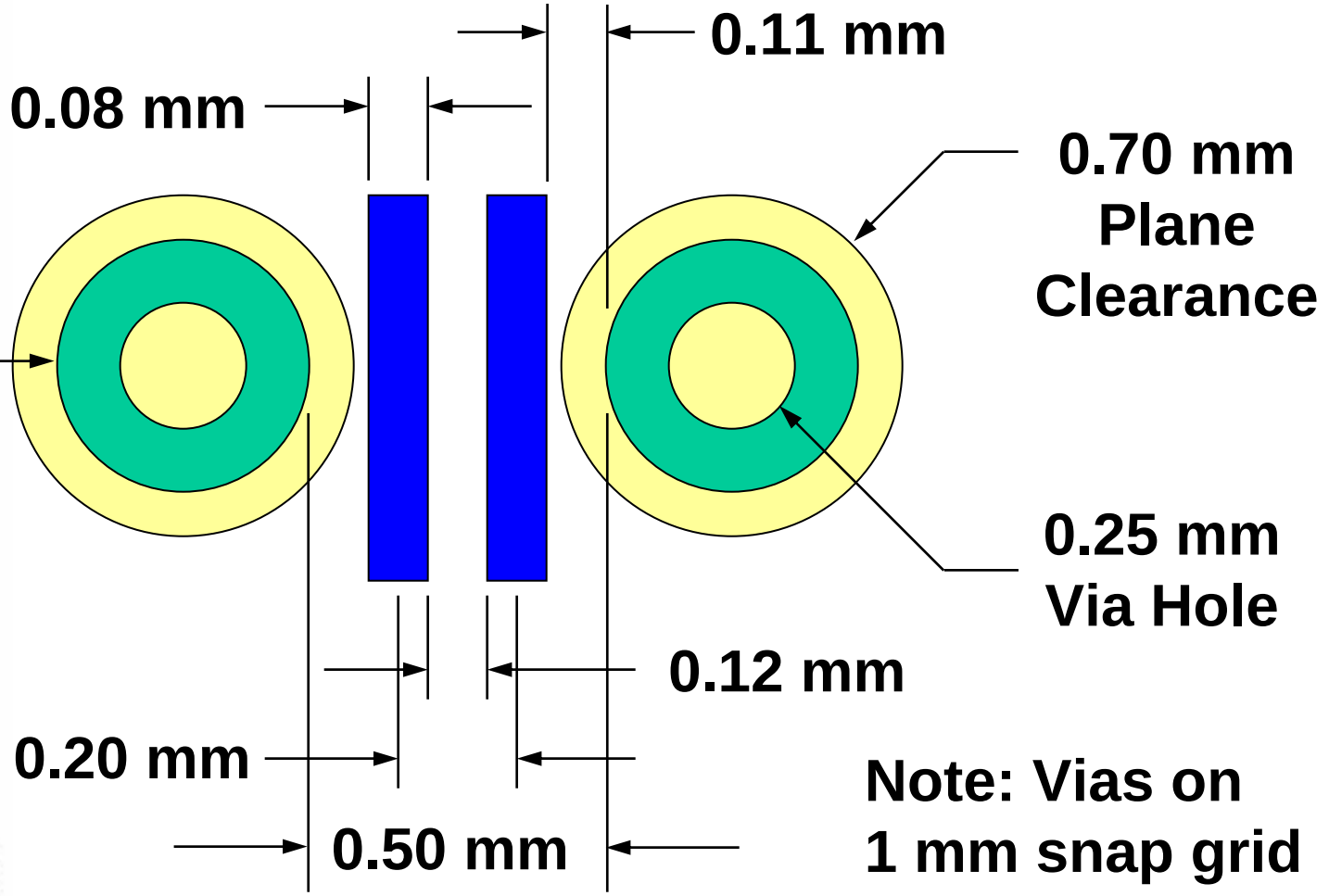
1 mm PITCH BGA

100 Ohm Differential Pairs

Internal Layers (stripline)

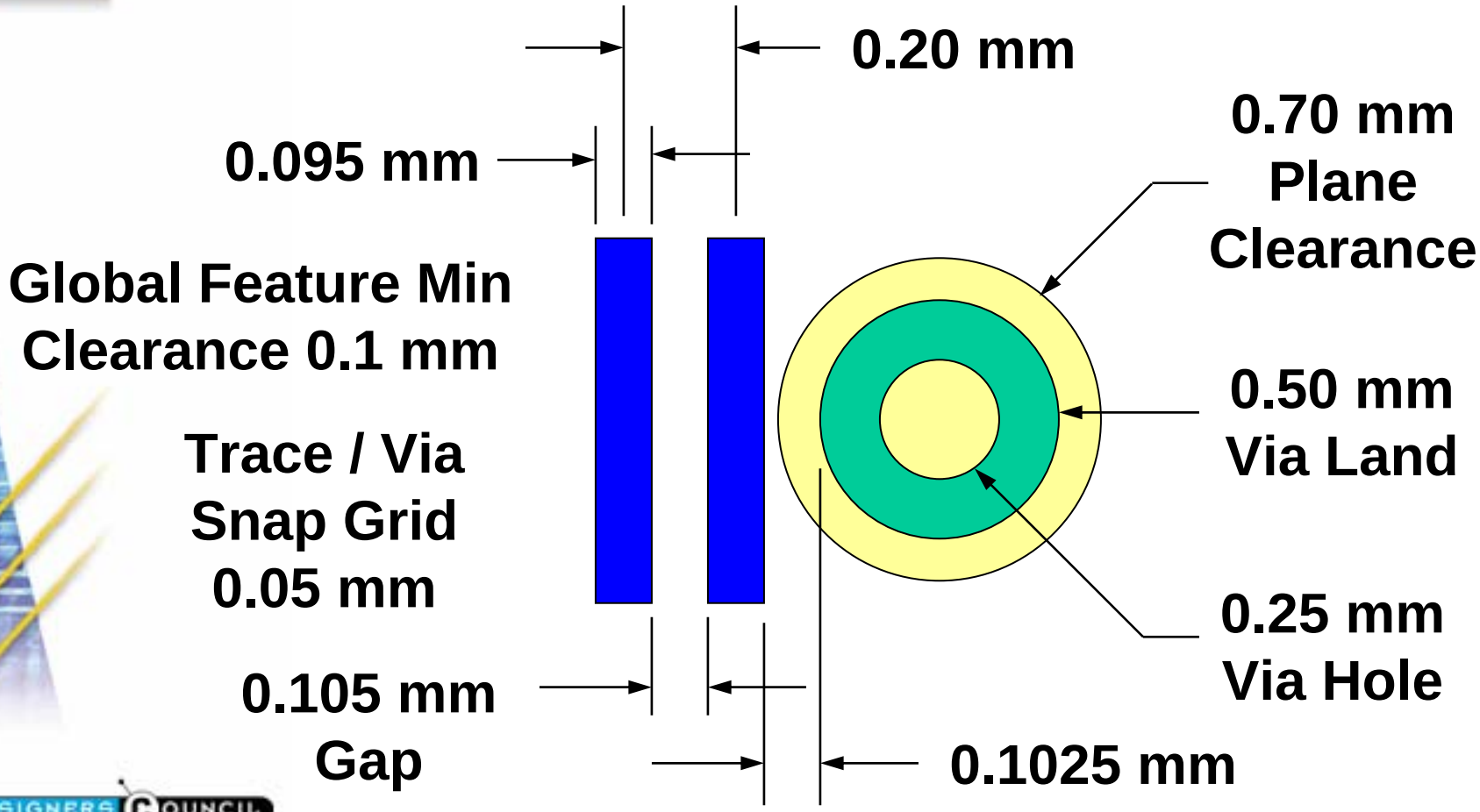


IPC DESIGNERS COUNCIL

1 mm PITCH BGA

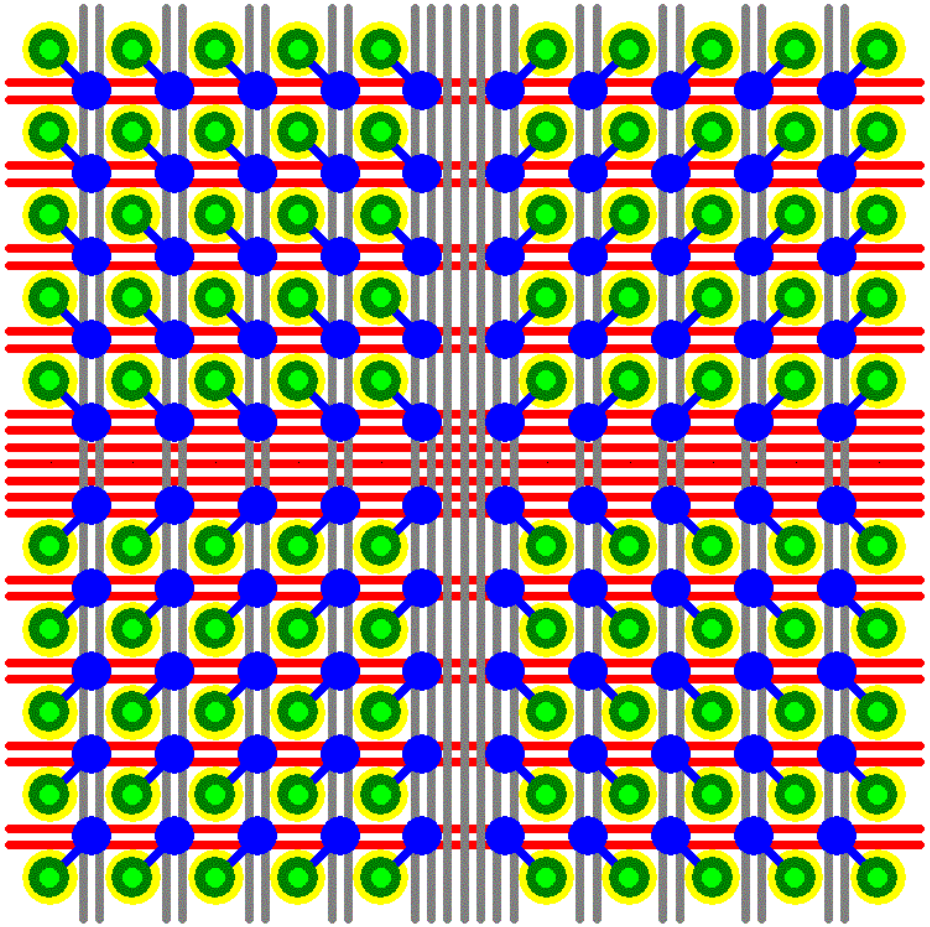
50 Ohm Single Ended Traces

Internal Layers (stripline)



IPC DESIGNERS COUNCIL

1.27 mm PITCH BGA



Via Data

Land: 0.635 (25)
Hole: 0.30 (12)
Plane Clearance: 0.85

BGA Land Size: 0.6 (24)

Trace/Space Data

Trace Width: 0.127 (5)
Trace/Trace Space:.127
Trace/Via Space: 0.127
Routing Grid: 0.127 (5)
Via Grid: 0.635 (25)
Part Place Grid 1: 1.27
Part Place Grid 2: 0.635

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METRIC BGA SNAP GRIDS

Part Placement, Via Fanout and Routing grids should be evenly divisible into 1 mm

Metric Working Grids	Metric Non-Working Grids
1	0.9
0.5	0.8
0.25	0.7
0.2	0.6
0.125	0.4
0.1	0.3
0.05	0.15

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PLACEMENT & VIA FANOUT

- When placing components on a PCB Design, always have your Via Display Grid turned on.
- When you place the parts, place the part pins evenly in-between your Via Display Grid to optimize the via fanout lengths and maximize your available routing channels.
- You may have to use various placement grids to accomplish this, but you will enhance the routing phase of the PCB Design layout.

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OPTIMAL VIA PADSTACKS

- **0.1 Trace Width / 0.1 Route Grid**
  Land Size: 0.5
  Hole Size: 0.25
  Plane Clearance: 0.7 – Avoid Trace Overlap
- **0.125 Trace Width / 0.05 Route Grid**
  Land Size: 0.65
  Hole Size: 0.3
  Plane Clearance: 0.8 – Avoid Trace Overlap
- **0.15 Trace Width / 0.05 Route Grid**
  Land Size: 0.55
  Hole Size: 0.25
  Plane Clearance: 0.75 – Avoid Trace Overlap

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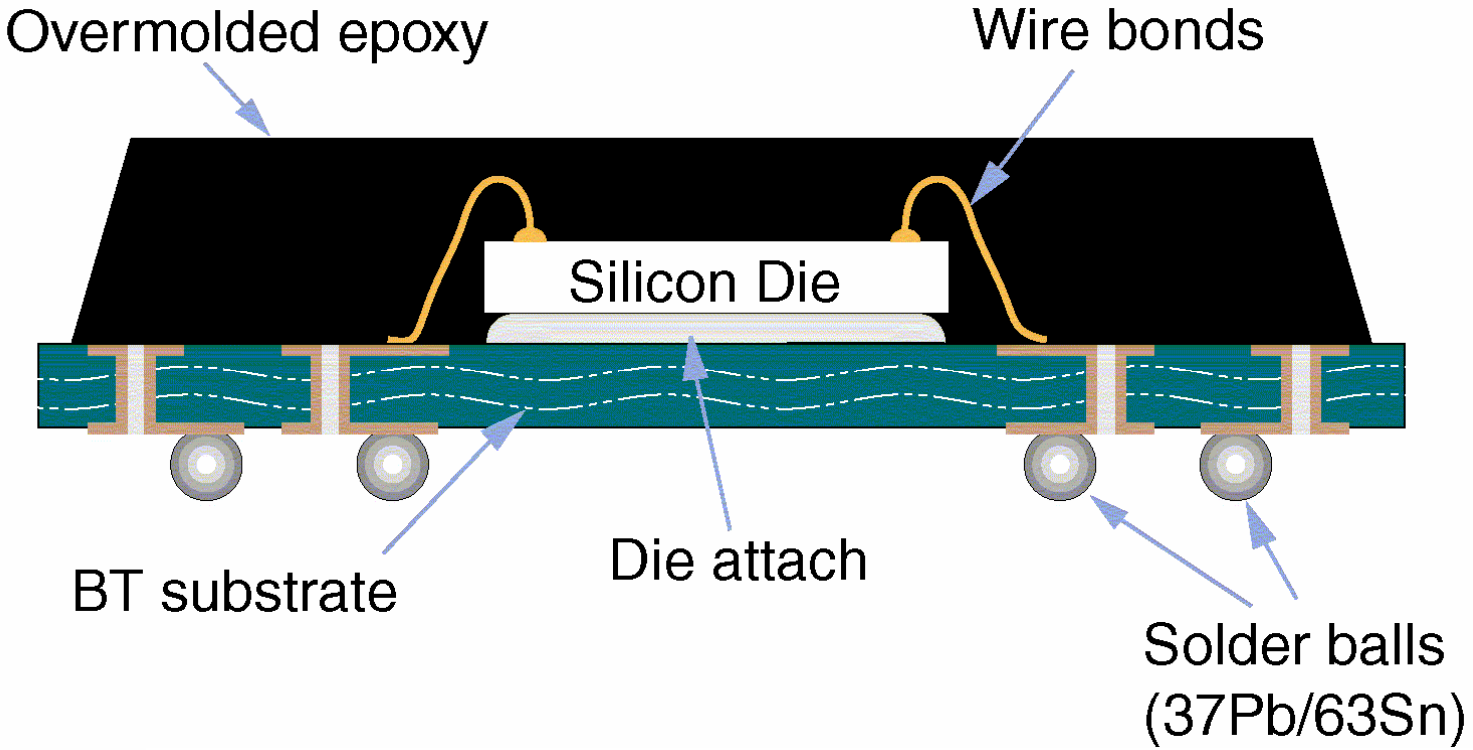
MAXIMIZE ROUTING CHANNELS

- Design your PCB like you are planning a housing development
- First establish where all the freeways are going to go – Buss Routes and Main Arteries
- Then establish the local road map – Trace Routes that don't have to bend
- Then build the houses along each side of the local roads – Via Sites

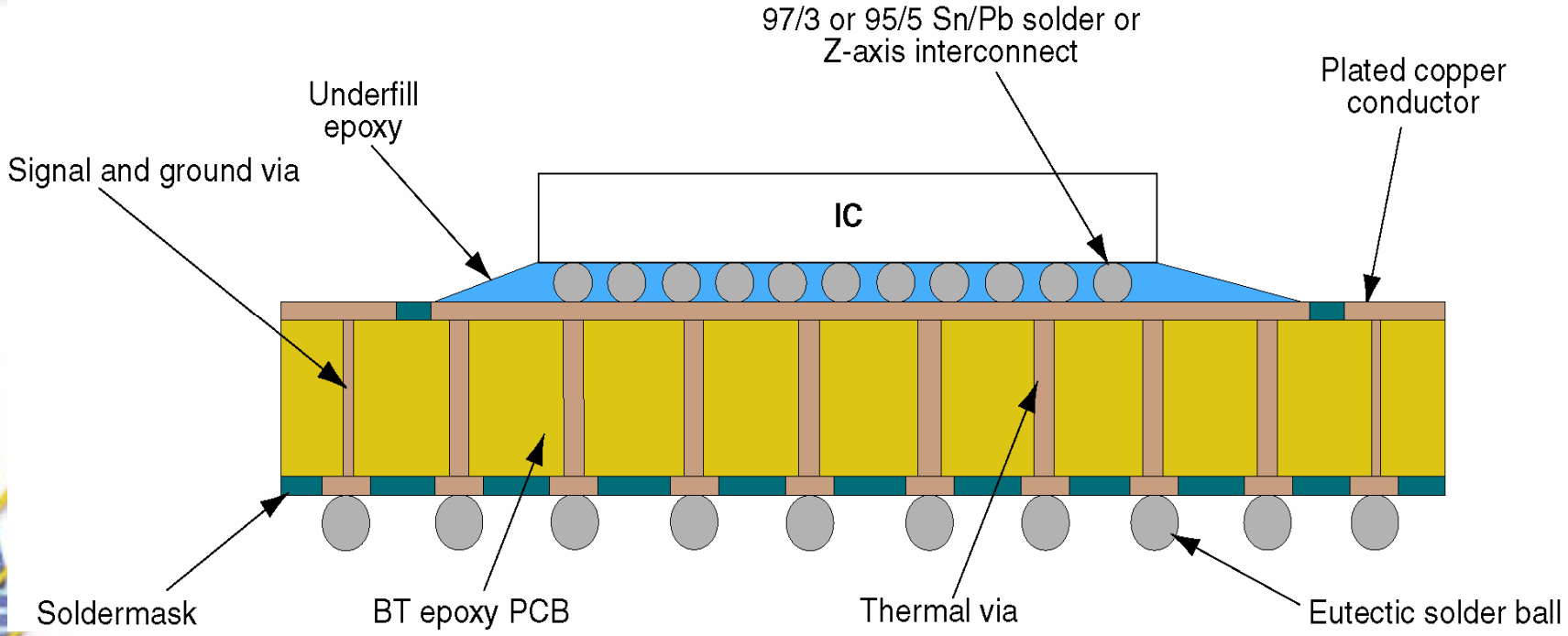
IPC DESIGNERS COUNCIL

PLASTIC BALL GRID ARRAY, CHIP WIRE BONDED



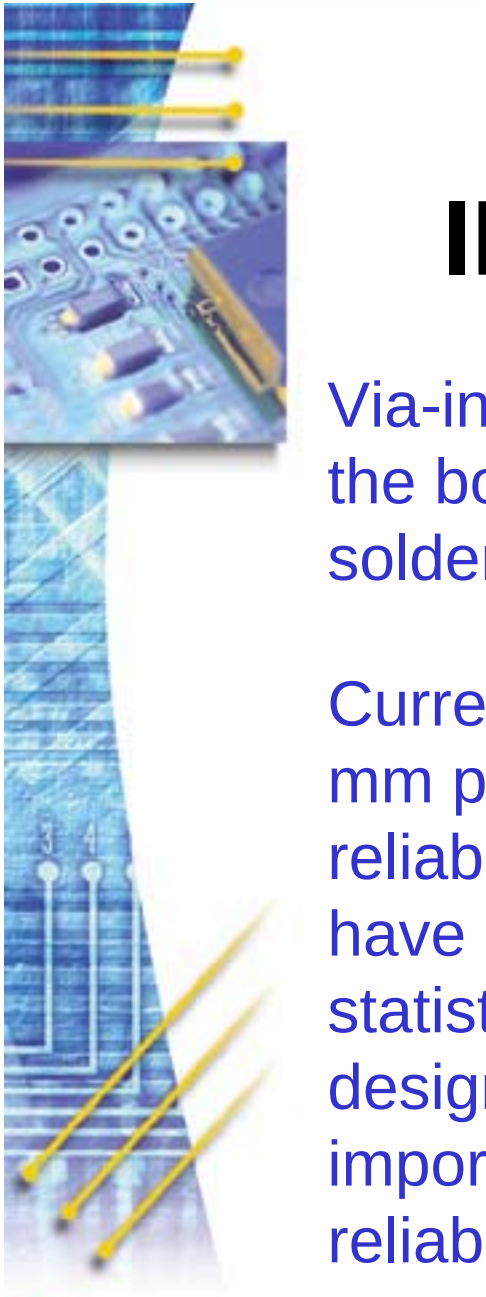
Note: Interposer land area is solder mask defined

BALL GRID ARRAY, FLIP CHIP BONDED



Note: Interposer land area is solder mask defined

IPC DESIGNERS COUNCIL



VIA-IN-PAD AND IMPACT ON RELIABIITY

Via-in-Pad (through-hole via, capped on bottom of the board) for BGA Lands cause voids in the BGA solder joints, which may impact reliability.

Current data indicates that, for the standard 25 - 35 mm package body with 0.75 mm balls, there is no reliability risk from voids. Accelerated aging tests have been performed and the failure rate was statistically equivalent to standard dog bone designs. It appears that void consistency is more important than void size with respect to joint reliability.

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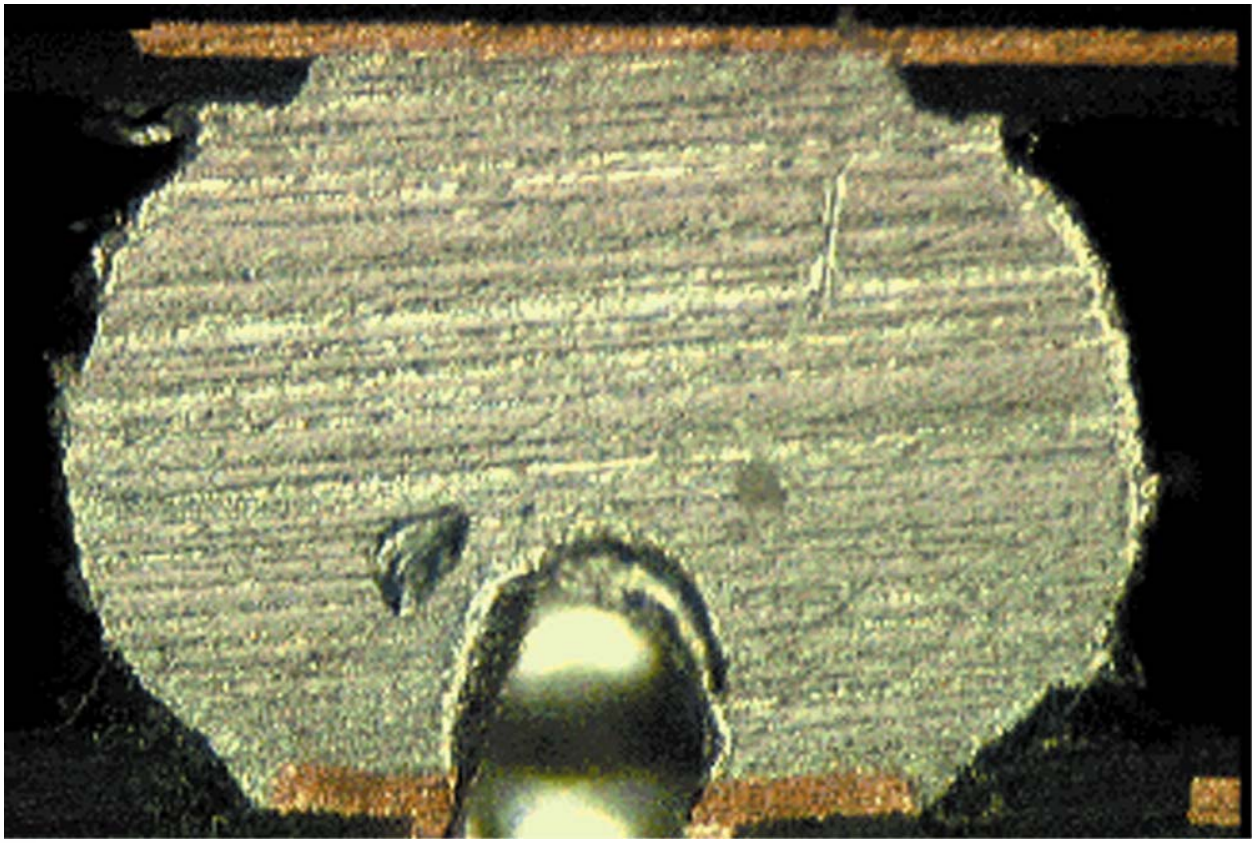
CROSS SECTION OF 0.75mm BALL WITH VIA-IN-PAD STRUCTURE



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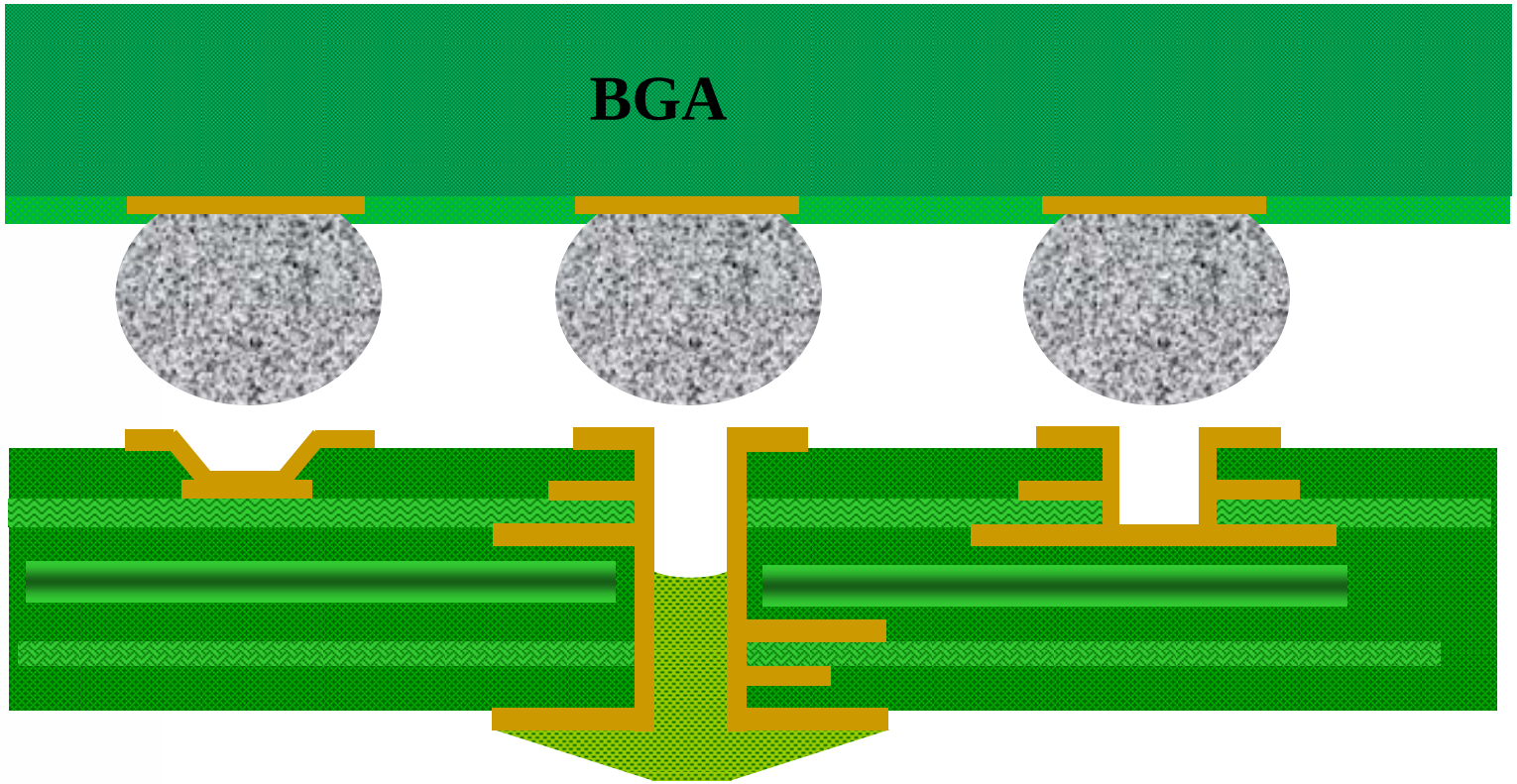
BEFORE ASSEMBLY PROCESS



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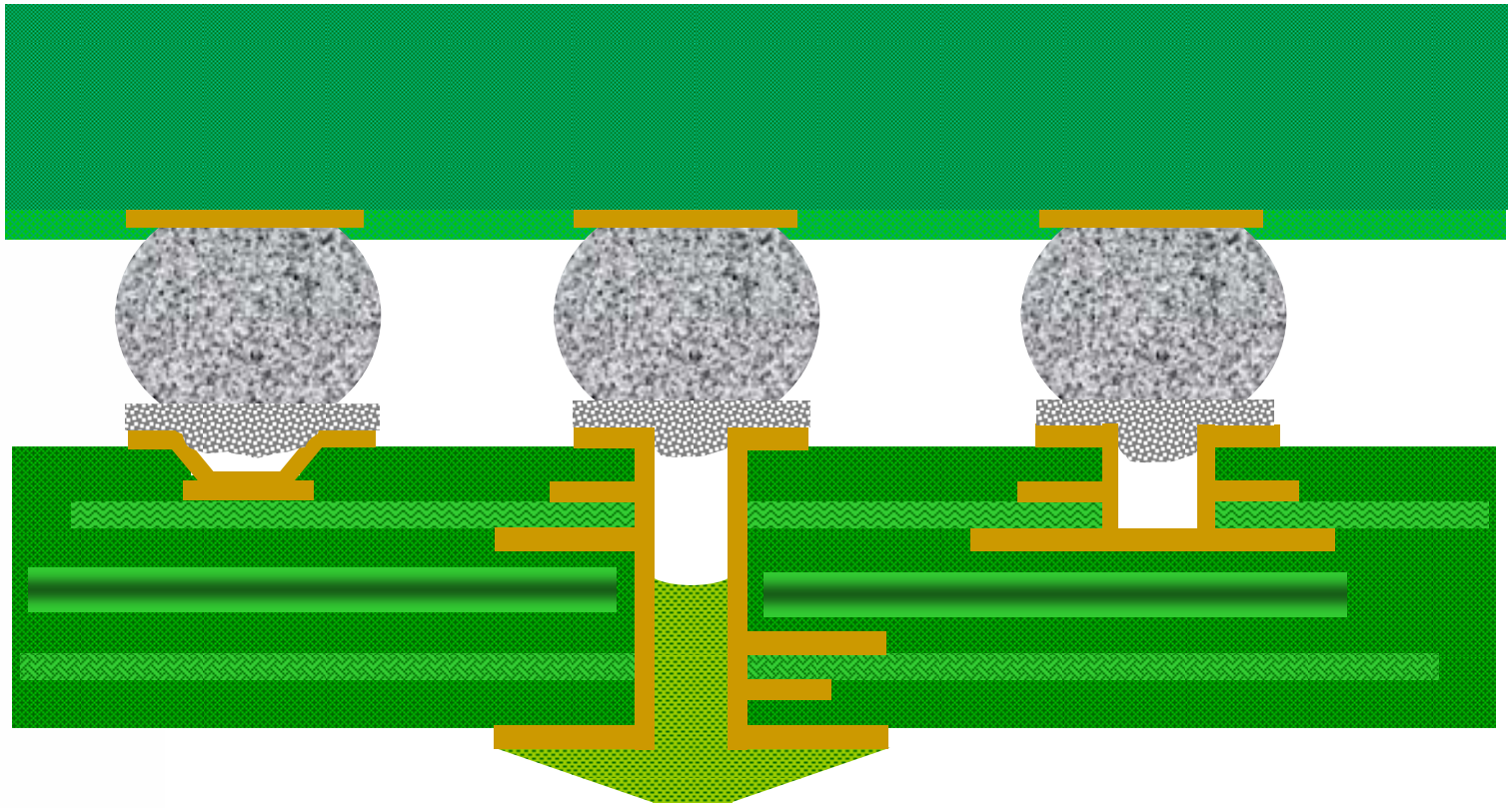
AFTER PRINTING PASTE, AND BGA PLACEMENT



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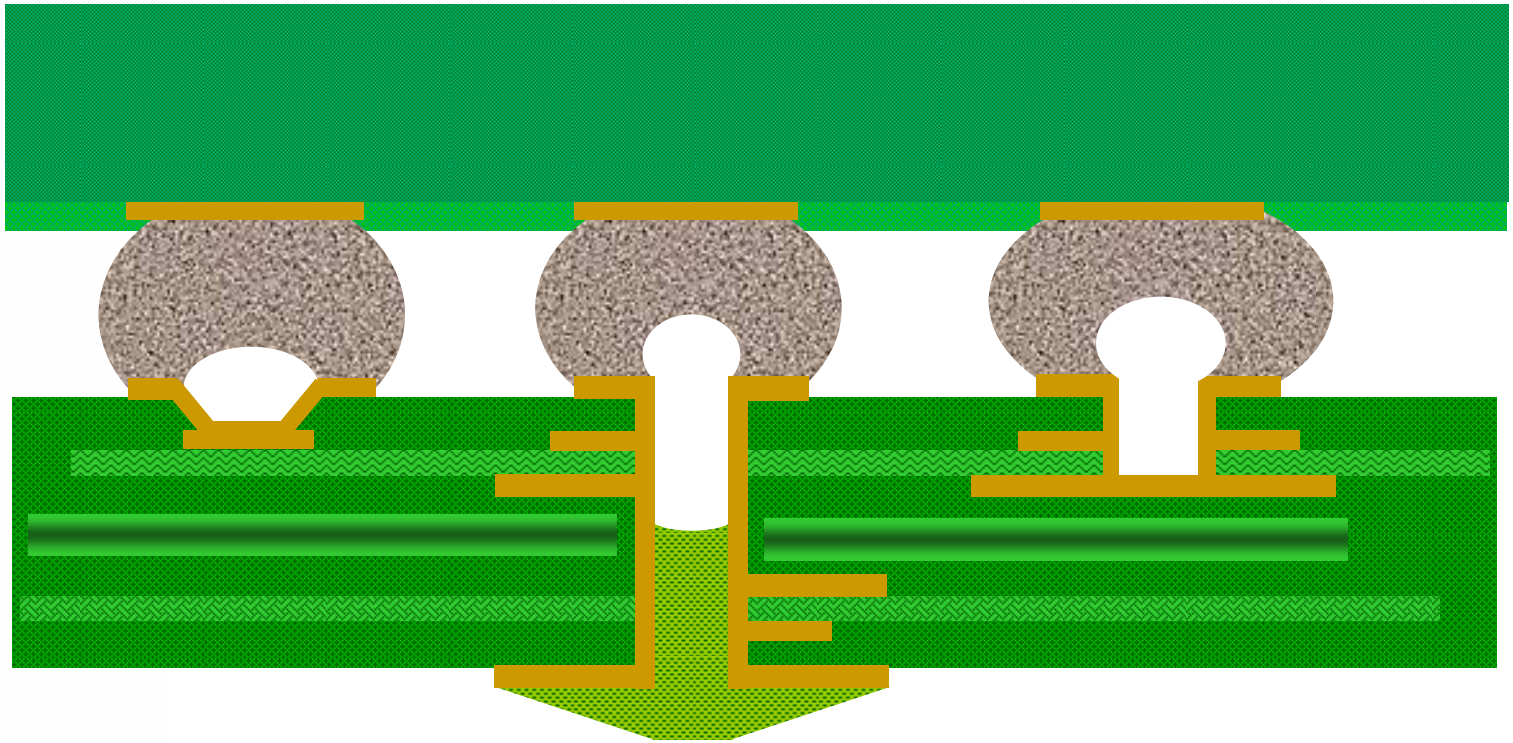
DURING REFLOW SOLDERING



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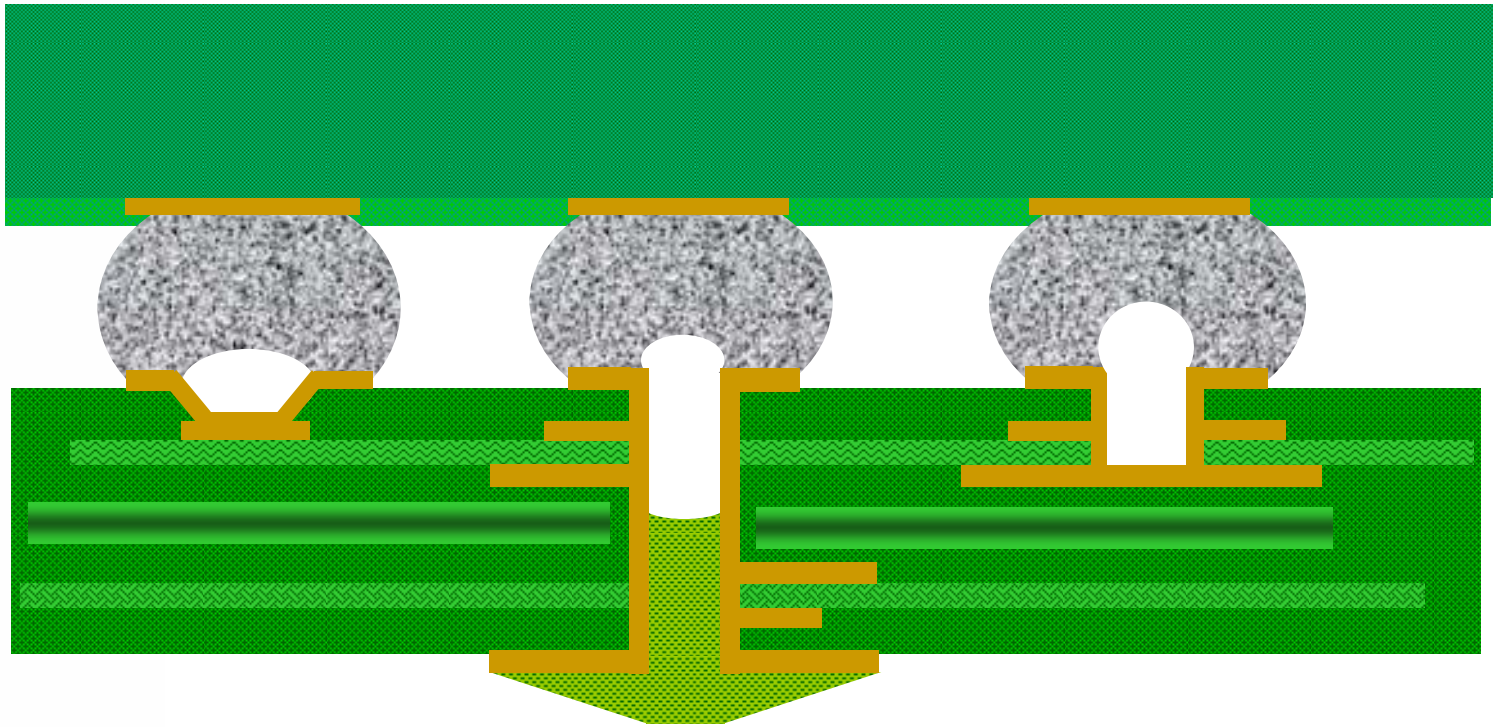
POST REFLOW SOLDERING



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SOLDER MASK VS. METAL DEFINED LAND DESIGN

- Two basic types of solder lands used for BGA packages
  - Non-solder mask defined (NSMD)
  - Solder mask defined (SMD)
- NSMD lands are copper defined - solder mask clearance around land
- SMD lands have solder mask overlapping the copper land

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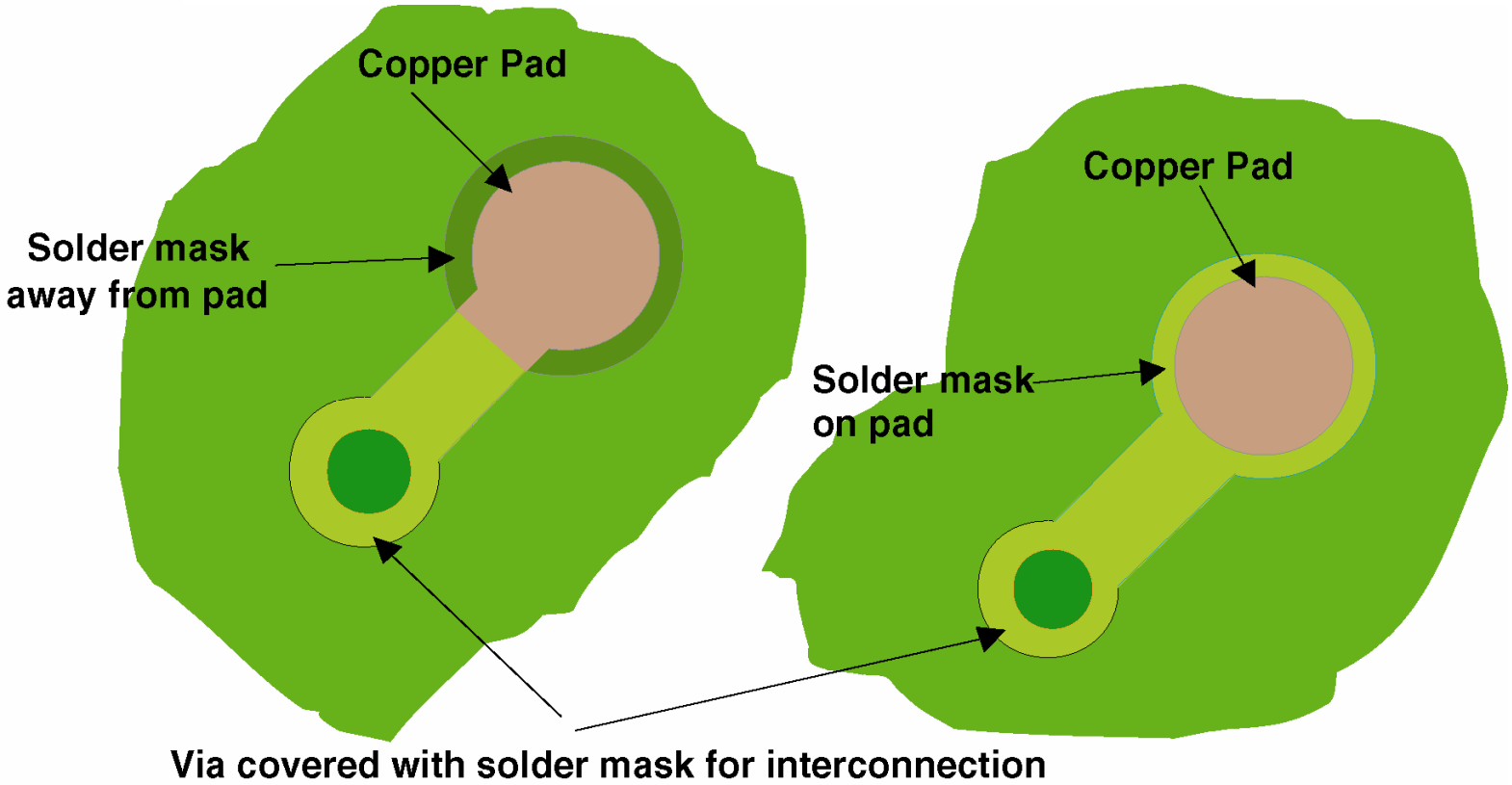
SOLDER LANDS FOR BGA COMPONENTS

Non-Solder Mask Defined Land

Solder Mask Defined Land



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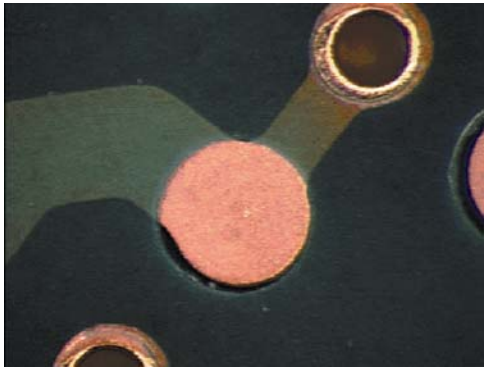
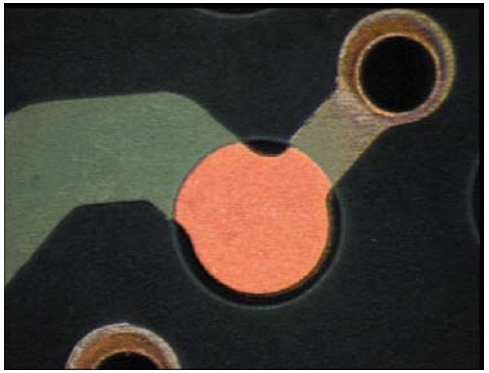
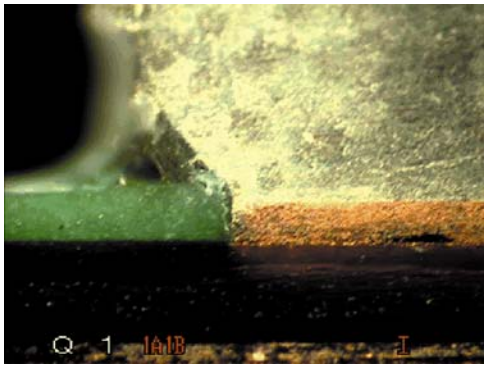
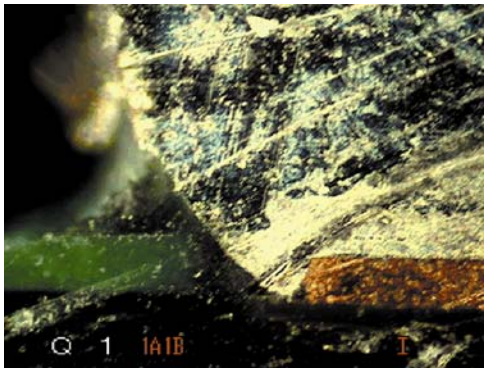
EFFECT OF HAVING SOLDER MASK RELIEF AROUND THE BGA LANDS OF THE BOARD

Solder Mask Relief Around Land	~0 mm	0.15 mm
Top view of land illustrating increase of effective land diameter due to trace connections		
Cross-sectional view of land with solder ball joint illustrating the solder wetting down the edge of the land when there is solder mask relief away from the land edge		

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