







Application Note NC08703

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1 SUMMARY

This report gives a description of a wideband push-pull amplifier for the frequency range 1.6 - 28 MHz. The amplifier has been designed around 2 MOS transistors BLF177 which operate in class-AB at V_{DS} = 50 V and I_{DQ} = 0.5 A/transistor.

The main properties at $P_O = 300$ W are:

Powergain: 22 to 23 dB

Efficiency: 52.5 to 61%

Return losses input: $\leq -15.5 \text{ dB}$

2nd harmonics: $\leq -25 \text{ dB}$

3rd harmonics: $\leq -16 \text{ dB}$

IMD at P_O = 300 W PEP: \leq –33 dB.

2 INTRODUCTION

The BLF177 is an RF Power MOS transistor for the HF and VHF range in a 4 leads flange SOT121 encapsulation. For the frequency range 1.6 - 28 MHz a wideband push-pull power amplifier has been developed with $2 \times$ BLF177 having an output power of 300 W PEP at an intermodulation distortion level below -30 dB. The transistors operate in class-AB at V_{DS} = 50 V and a quiescent current of 0.5 A each.

3 DESIGN OF THE AMPLIFIER

3.1 General

The schematic set-up is given in Fig.1.



The two balance to unbalance transformers are applied to split the single ended input into 2 out of phase driving ports and to add the 2 out of phase output ports into one single ended output. The transformers have an impedance transformation ratio of 4 : 1 and match the low-ohmic in- and output impedance of the transistors to the 50 Ω system impedance. At the input a special circuit takes care of a good input matching and a flat powergain over the whole bandwidth.

3.2 Output circuit

3.2.1 LOAD IMPEDANCE

The output impedance of each transistor can be represented as a combination of the output capacitance C_{oss} and the optimum load resistance. Because of the larger drain voltage swing the effective output capacitance C_O is appr. 15% higher than the value of C_{oss} . So $C_O = 1.15 \times 190 \approx 220$ pF. The optimum load resistance for class-AB can be determined with formula:

$\mathsf{R}_{\mathsf{L}} = (0.85 \times \mathsf{V}_{\mathsf{DS}})^2 / (2 \times \mathsf{P}_{\mathsf{O}})$

For $V_{DS} = 50$ V and $P_O = 150$ W we get $R_L = 6 \Omega$. To keep the transformer simple a transformation ratio of 4 or 9 is preferable. A ratio of 4 gives a load impedance of $50/4 = 12.5 \Omega \rightarrow 6.25 \Omega$ for each transistor. This is very near to the optimum load resistance.

3.2.2 OUTPUT TRANSFORMER

The output transformer has to transform the 50 Ω asymmetrical impedance to the 2 × 6.25 = 12.5 Ω symmetrical load impedance. The reactance (ω L) of the shunting inductance at 1.6 MHz has been chosen at 4 times 50 Ω = 200 Ω . So the inductance is 20 μ H. The transformer has been wound on a ferrite toroid of 4C6 material. Dimensions: 36 × 23 × 15 mm (D × d × h) which gives a volume (A.1) = 8.97E-6m³.

Because the power handling of one toroid is critical two transformers in parallel with an inductance of 40 μ H each have been chosen.

 $\begin{array}{l} n_{sec} = SQR((L.1)/(\mu o \times \mu r \times A)) \\ n_{sec} = SQR((40E-6 \times 9.2E-2)/(4\pi E-7 \times 120 \times 97.6E-6)) = 15.8 \ turns. \\ \text{So } n_{pr} = 8 \ turns \ and \ n_{sec} = 16 \ turns. \end{array}$

For each transformer V_{max} depends on the power over 100 Ω . V_{max} = SQR(2 × P_O × R_L) = SQR(2 × 150 × 100) = 173.2 V

 B_{max} depends on the parallel loss resistance at 1.6 MHz; for a power loss of 1%: $B_{max} = 1.3E - 2T$. The volume A.1 needed per core is: A.1 = $(V_{max}/(\omega \times B_{max}))^2(\mu_o \times \mu_r)/L$.

A.1 = $(1.73.2/(2\pi \times 1.6E + 6 \times 0.013))^2(4\pi E - 7 \times 120)/40E - 6 = 6.62E - 6 m^3$.

Each of the toroids has a volume of $8.97E - 6 \text{ m}^3$. Figure 7 shows one of the two parallel connected output transformers. On each toroid the primary winding has 8 turns of copperfoil (width 5 mm and thickness 0.05 mm). The secondary winding has 16 turns of 2 enamelled copper wires (0.6 mm) in parallel.

So each primary turn has been covered with 2 secondary turns which means 4 wires of 0.6 mm. Both windings are isolated with PTFE-foil (thickness 0.1 mm). To reduce the stray-inductance the transformer has been wound as follows:

- 1. The primary has been wound evenly around the periphery of the toroid
- 2. With the secondary the same has been done with the first 8 turns; the second part of 8 turns has been wound in between the first part. So the secondary has been wound twice around the core.

The measured secondary inductance of each transformer is 38 μ H and L_{str} = 300 nH.

With the aid of a network analyser the parallel combination of these 2 transformers has been corrected. For the higher frequencies at the low-ohmic side a parallel capacitor of 240 pF and for the lower frequencies at the high-ohmic side a series capacitor of 10 nF give return losses below –21 dB over the whole frequency range (see Fig.2).

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Replacing the transistors by resistors of 6.25 Ω the return loss can be measured at the 50 Ω side. Figure 11 gives the return losses of the parallel combination of the two transformers before and after the correction.

3.2.3 THE TAPPED CHOKE

The chokes in the drain circuits are wound around a common ferrite rod of 4B1 material. Dimensions: 50×10 mm (l × d). Figure 3 gives a schematic electrical circuit of the output.



Between both drains the impedance for the even harmonics depends on the coupling factor between both windings. If the coupling factor amounts to 1 both drains will be short circuited for the even harmonics.

Because the voltage over one winding is equal to half of the voltage between both drains, the total inductance between both drains is 4 times the inductance of one winding.

The reactance of the shunting inductance at 1.6 MHz has been chosen at 4 times 12.5 Ω = 50 Ω .

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So the inductance between both drains is 5 μ H, this means for one winding an inductance of 1.25 μ H. According to the Philips Data Handbook *"MA01 on soft ferrites of 1996, the effective permeability"* of a rod with 1/d = 5 and μ_r = 250 is appr. 20.

The number of turns can be calculated with:

$n = SQR(L.1/(\mu_o \times \mu_r \times A))$

n = SQR($1.25E - 6 \times 50E - 3/(4\pi E - 7 \times 20 \times \frac{1}{4}\pi(10E - 3)^2)$ = 5.6 turns. In practice 6 twisted turns of the primary and secondary windings have been wound around the rod. Figure 8 shows the tapped choke. To increase the coupling factor each winding consists of 2 enamelled copper wires (0.8 mm) in parallel. The measured inductance is 1.275 µH.

3.2.4 TUNING OF THE OUTPUT CIRCUIT

For an optimum alignment of the output circuit the 2 transistors have been replaced by dummies consisting of the parallel connection of a resistance and a capacitance. The resistance is equal to the optimum load resistance and the capacitance to the output capacitance (see Section 3.2.1).

Tuning of the output circuit has been carried out by measuring the return losses at the output with a network analyser under swept conditions (see Fig.4).



The measured return losses should be as low as possible by changing the correction capacitors. Figure 12 shows the return losses of the output before and after tuning. For optimum results the capacitance across the primary winding of the output transformer has been reduced from 240 to 150 pF and the low frequency correction capacitor of 10 nF at the output has been changed to an inductance of 100 nH. The last change can be explained as follows:

- 1. The low frequency compensation is taken over by the coupling capacitors between the drain choke and the impedance transformer
- 2. The function of the transformer is not only impedance matching but also transfer from balanced to unbalanced. The latter makes that the interwinding capacitance has more influence. This is so much that a series inductance at the output is needed for high frequency compensation.

3.3 Input circuit

3.3.1 INPUT IMPEDANCE

The input impedance and gain of the transistor can be determined with the aid of a computer model of the BLF177. Table 1 shows the calculated gain and impedances for the frequency range 1.6 to 28 MHz.

BLF177 Vds = 50 V Po = 150 W Class-AB.

Table 1	Calculated	dain and	impedances	of the	BLF177
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f (MHz)	G (dB)	INP.IMP. (Ω)	LOAD IMP. (Ω)
1.6	54.70	2.29 – j133.58	6.23 + j.07
2.5	50.82	2.29 – j85.50	6.23 + j.12
3.5	47.90	2.29 – j61.09	6.23 + j.16
5.0	44.80	2.29 – j42.78	6.22 + j.23
7.0	41.88	2.29 – j30.58	6.21 + j.32
10.0	38.78	2.29 – j21.45	6.18 + j.46
14.0	35.85	2.29 – j15.37	6.13 + j.64
20.0	32.75	2.29 – j10.84	6.03 + j.89
24.0	31.17	2.29 – j9.09	5.95 + j1.05
28.0	29.83	2.29 – j7.85	5.85 + j1.20

By adding a gate-source resistor of 6.25 Ω the power gain reduces from 29.8 to 23.3 dB at 28 MHz.

3.3.2 INPUT MATCHING CIRCUIT

As mentioned in Section 3.1 a special circuit matches the input impedance of each transistor to the 6.25 Ω of the input transformer. The matching network chosen can be treated as the half of a double π -section as described in Ref.1. Removing the in- and output capacitance the circuit changes in a T-section with C_i as capacitor and 2 inductances with a value of half the inductances of the double π -section (see Fig.5).



C_i represents the input capacitance of the BLF177 and can be calculated from the input impedance of Table 1. For 7 MHz: C_i = $1/(2\pi \times 7E + 6 \times 30.58) = 744 \text{ pF}.$

Across this capacitor a constant voltage versus frequency from 1.6 up to 28 MHz has to be developed. Provided C_i is an ideal capacitance the dimensioning of this network is as follows:

 $R_G = R_{gs}$ must be appr. 6 Ω to obtain low I.M. distortion and good stability. This appeared during the development of the narrow band testcircuit as given in the BLF177 publication data. To judge whether this value is also acceptable for wideband operation we calculate the product:

 $W_c \times C_i \times R_{gs}$ in which ω_c is the maximum angular frequency.

Doing so we find:

 $2\pi \times 28E + 6 \times 744E - 12 \times 6.25 = 0.818$

 R_{gs} has been chosen 6.25 Ω for the ease of transformation. Comparing the value of this product with the one given in Ref.2 we see that with a double π -section we can easily reach a bandwidth of 50 MHz. Therefore we have simplified the network as described above. Continuing the calculation we find:

 $L = 0.997 R_G/\omega_c = 35.4 nH$ (So L1 = L2 = 17.7 nH)

With the computer model mentioned in Section 3.3.1 a gain of 22.3 dB has been calculated with R_{gs} = 6.25 Ω .

Starting from this 22.3 dB gain, $L_1 = L_2 = 17.7$ nH and $R_{gs} = 6.25 \Omega$ the input VSWR and gain deviation have been calculated (see Table 2).

Initial results Rs = 6.250Ω ; Gs = 22.300 dBPar.LR: L = 17.700 nH; R = 6.250Ω Ser.Ind.: L = 17.700 nH

 Table 2
 Results before optimization

f (MHz)	VSWR	dG (dB)
1.6	1.010	1.440
2.5	1.016	1.435
3.5	1.023	1.431
5.0	1.032	1.419
7.0	1.046	1.402
10.0	1.068	1.354
14.0	1.100	1.265
20.0	1.161	1.075
24.0	1.214	.910
28.0	1.281	.703

Before optimization the maximum VSWR = 1.28 and the gain = 22.7 dB \pm 0.37 dB. To achieve a maximally flat gain and a low input VSWR a computer optimization program has been used. This optimization results in a gain of 23.3 dB with a maximum Δ Gain = \pm 0.09 dB and a VSWR \leq 1.09, see Table 3. For these results L₁ has been changed from 17.7 nH to 9 nH and L₂ from 17.7 nH to 21.1 nH. the R_{gs} has been decreased from 6.25 Ω to 5.7 Ω .

Final results Rs = 6.250Ω ; Gs = 23.300 dBPar.LR: L = 21.079 nH; R = 5.749Ω Ser.Ind.: L = 8.950 nH

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Table 3 Results after optimization

f (MHz)	VSWR	dG (dB)
1.6	1.087	.072
2.5	1.087	.071
3.5	1.087	.074
5.0	1.086	.076
7.0	1.085	.084
10.0	1.082	.087
14.0	1.076	.086
20.0	1.059	.056
24.0	1.047	.006
28.0	1.044	087

3.3.3 INPUT TRANSFORMER

The input transformer is simular to the output transformer. It transforms the asymmetrical system impedance to the $2 \times 6.25 \Omega = 12.5 \Omega$ symmetrical source impedance. However the lower power handling (<3 W) justifies a toroid of 4C6 material with smaller dimensions: $14 \times 9 \times 5$ mm (D × d × h) which gives a volume A.1 = 0.445E - 6 m³. As described in Section 3.2.2 the primary winding can be calculated for L = 20 μ H.

$$n_{pr} = SQR((L.1)/(\mu_o \times \mu_r \times A))$$

 $n_{pr} = SQR((20E - 6 \times 3.55E - 2)/(4\pi E - 7 \times 120 \times 12.54E - 6) = 19.4 \text{ turns. With } n_{pr} = 20 \text{ turns and a transformation ratio of } 4 : 1 \text{ the } n_{sec} = 10 \text{ turns.}$

 $V_{max} = SQR(2 \times P_i \times R_S) = 17.3 \text{ V} \text{ and } B_{max} = 0.013T.$

The needed core volume A.1 is:

A.1 = $(V_{max}/(\omega \times B_{max}))^2 \times (\mu_o \times \mu_r)/L$

A.1 = $(17.3/(2\pi \times 1.6E + 6 \times 0.013)^2 \times (4\pi E - 7 \times 120)/20E - 6 = 0.14E - 6 \text{ m}^3$

The core used has a volume of $0.445E - 6m^3$.

Figure 9 shows the input transformer. The secondary winding has 10 turns of copperfoil (width 2 mm, thickness 0.05 mm). The primary winding has 20 turns of enamelled copper wire (0.5 mm). Each secondary turn has been covered with 2 primary turns with a PTFE foil of 0.1 mm thickness as isolation between the 2 windings. The method of winding is the same as described for the output transformer in Section 3.2.2. The measured inductance is 20.95 μ H and L_{str} = 250 nH.

The correction method used for the input transformer is the same as described already in Section 3.2.2 (see Fig.6).



The transformer has been corrected with parallel capacitors for the higher frequencies and a series capacitor for the lower frequencies. Figure 13 gives the return losses before and after the correction.

3.3.4 TUNING OF THE INPUTCIRCUIT

For the practical tuning of the input circuit each transistor has been adjusted at V_{DS} = 50 V and a quiescent current of 0.5 A.

The gain and input return losses have been measured in the frequency range 1.6 up to 35 MHz. The best results have been achieved by changing the secondary correction capacitor of the inputtransformer from 220 to 30 pF and the primary correction trimmer from \approx 15 pF to \approx 20 pF. The low frequency correction capacitor at the input has been removed. The inductance in serie with R_{gs} has been increased from 21.6 to 35 nH. Figure 14 gives the complete circuit diagram of the wide band amplifier with 2 BLF177 transistors. Table 5 gives the corresponding parts list.

4 CONSTRUCTION OF THE AMPLIFIER

For the printed circuit board double Cu-clad epoxy fibre glass has been used with a thickness of 1/16" and $\varepsilon_r = 4.5$. The position of the components is on one side and the other side serves as a groundplane. Connections to the groundplane have been made with rivets and with straps under the source leads and at the edges of the PC-board on the in- and output side.

The printed circuit board has been attached to a solid copper plate $(145 \times 120 \times 10 \text{ mm})$ which functions as a heatsink. Around the position of both transistors a tube has been soldered in the copper plate to controle the temperature by means of a watercooling system. For a good thermal contact between heatsink and transistors heatsink compound has been used.

Figure 15 shows the lay-out of the amplifier. The transformers have been fastened above the printed circuit board by means of accessories of Delrin material.

These accessories have been attached through the PC-board in the copper plate.

5 MEASURED PERFORMANCE

5.1 Single tone measurements

Figures 16 to 20 show at a constant outputpower of 300 W at 2 heatsink temperatures the gain, efficiency, input return losses, 2nd and 3rd harmonics at the output as a function of the frequency. In the range 1.6 to 28 MHz the gain is 22 to 23 dB, the efficiency 52.5 to 61%, the input return losses are below -15.5 dB, the second harmonics better then -25 dB and the third harmonics below -16 dB.

At a heatsink temperature of 70 °C the gain decreases about 1.5 dB. The heatsink temperature has only little influence on the other parameters. Figures 21 to 23 shows at 4 frequencies the output power as a function of the input power and the gain and efficiency versus outputpower.

Above 10 MHz the efficiency decreases about 6%. At 20 MHz the gain decreases above $P_0 = 200$ W. At other frequencies this decrease starts at $P_0 = 300$ W.

5.2 Two tone measurements

The two tone measurements have been carried out with 2 carriers with a frequency distance of 1 KHz. Figure 24 to 27 give as a function of the frequency the gain, efficiency, 3rd order distortion and 5th order distortion at 4 output levels. Over the whole frequency range the gain variation is less than 1 dB at each power level. At $P_0 = 300$ W PEP the efficiency is at least 40%, the 3rd order distortion \leq -33 dB and the 5th order distortion \leq -38 dB.

Figures 28 and 29 give the 3rd and 5th order distortion versus output power at 4 frequencies.

To verify the choice of $I_{DQ} = 1$ A the 2nd and 3rd order distortion have been measured versus I_{DQ} . These measurements have been carried out at the most critical frequency and output level of 20 MHz and 30 W PEP resp. Figure 30 shows that $I_{DQ} = 1A$ for both transistors together was a good choice.

6 BALANCED CIRCUIT

As shown in Table 4 there is a certain amount of unbalance between both drain currents at RF operation. It is possible to improve this by using baluns in front of the input transformer and after the output transformer.

|--|

f (MHz)	I _{D1} (A)	I _{D2} (A)
1.6	5.2	4.8
5	5.1	4.75
10	5.25	4.8
15	5.3	4.95
20	5.7	5.3
25	6.2	5.25
30	5.85	5.15

7 CONCLUSIONS

This report shows that it is possible to design a wideband push-pull amplifier with 2 BLF177 MOS transistors having a very good performance.

The main properties are:

- Bandwidth: 1.6 to 28 MHz
- V_{DS}: 50 V
- I_{DQ}: 1 A
- Gain at $P_0 = 300$ W: 22 to 23 dB
- Efficiency at P_O = 300 W: 52.5 to 61%
- Return losses input at P_O = 300 W: ≤–15.5 dB
- 2nd harmonics output at P_O = 300 W: ≤–25 dB
- 3rd harmonics output at $P_0 = 300 \text{ W}$: \leq -16 dB
- IMD at P_O = 300 W PEP: ≤-33 dB.

8 REFERENCES

G. Lukkassen Application report NCO8602 A wideband power amplifier (25 to 110 MHz) with the MOS transistor BLF245.



Fig.10 Decoupling choke.









Table 5 Parts list of the wide band push-pull amplifier with 2 × BLF277 (1.6 to 28 MHz); note 1

C1	5 – 60 pF film dielectric trimmer (cat.nr.: 2222 809 08003)
C2	30 pF multilayer chip capacitor; note 2
C3	2×100 nF multilayer chip capacitor (cat.nr.: 2222 852 47104)
C4 = C5	3×100 nF metallized film capacitor (car.nr.: 2222 368 21104)
C6 = C7	100 nF multilayer chip capacitor (cat.nr.: 2222 852 47104)
C8	10 µF (63 V) electrolytic capacitor (cat.nr. 2222 030 28109)
C9 = C10	4×10 nF metallized film capacitor (cat.nr. 2222 368 51103)
C11	2×75 pF multilayer chip capacitor; note 2
L1 = L2	\approx 9 nH, printed inductance; I = 47 and w = 6 mm
L3 = L4	35 nH, 3 turns enamelled Cu-wire (0.7 mm) int.dia.: 3 mm, I = 2.35 mm
L5 = L6	$2.2 \mu\text{H}$, 1 turns through modified Ferroxcube choke grade 3B (cat.nr.: 4312 020 36642); see Fig.10
L7	100 nH, 5 turns enamelled Cu-wire (0.8 mm) int.dia.: 5 mm, 1 = 6.1 mm
R1 = R2	5.9 Ω ; 4 metal film resistors of 23.7 Ω (0.4 W) in parallel (cat.nr.: 2322 151 72379)
R3	1 kΩ, metal film resistor (0.4 W) (cat.nr.: 2322 151 71002)
R4	1 MΩ, metal film resistor (0.4 W) (cat.nr.: 2322 151 71005)
R5	500 Ω , Cermet potentiometer (0.75 W)
R6	5.6 kΩ, metal film resistor (1 W) (cat.nr.: 2322 153 55622)
T1	input transformer:
	n _{pr} = 20 turns enamelled Cu-wire (0.5 mm)
	n _{sec} = 10 turns copper foil (width 2 mm), thickness 0.05 mm) wound around toroidal core, grade 4C6,
	dimensions: 14 × 9 × 5 mm (cat.nr. 4322 020 97181) see Fig.9
T2	drain choke: 6 turns of twisted pairs of 0.8 mm Cu-wires (each winding consists of 2 wires in parallel)
	wound on a Ferroxcube rod, grade 4B1, dimensions 10×50 mm, see Fig.8
Т3	n _{pr} = 8 turns copper foil (width 6 mm, thickness 0.05 mm)
	n _{sec} = 16 turns of 2 enamelled Cu-wires (0.6 mm) in parallel wound around toroidal core, grade 4C6,
	dimensions: $36 \times 23 \times 15$ mm (cat.nr. 4322 020 97201) see Fig.7; 2 of these transformers in parallel
	form the complete outputtransformer

Notes

1. PC-board: double Cu-clad, 1/16" epoxy fibre glass (ϵ_r = 4.5)

2. American Technical Ceramics type 100B or capacitor of same quality.























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Argentina: see South America Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466 Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010, Fax. +43 160 101 1210 Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773 Belgium: see The Netherlands Brazil: see South America Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102 Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381 China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700 Colombia: see South America Czech Republic: see Austria Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 0044 Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580920 France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427 Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300 Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240 Hungary: see Austria India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966 Indonesia: see Singapore Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200 Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007 Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557 Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077 Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415 Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880 Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,

Tel. +9-5 800 234 7381 Middle East: see Italy

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399 New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811 Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341 Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474 Poland: UI. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327 Portugal: see Spain Romania: see Italy Russia: Philips Russia, UI. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919 Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. +65 350 2538, Fax. +65 251 6500 Slovakia: see Austria Slovenia: see Italy South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494 South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382 Spain: Balmes 22 08007 BARCELONA Tel. +34 3 301 6312, Fax. +34 3 301 4107 Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 632 2000, Fax. +46 8 632 2745 Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2686, Fax. +41 1 488 3263 Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874 Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd. 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,

Tel. +66 2 745 4090, Fax. +66 2 398 0793 Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,

Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 625 344, Fax.+381 11 635 777

Internet: http://www.semiconductors.philips.com

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