

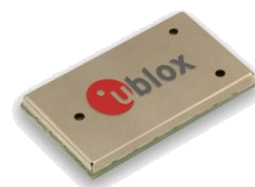
# SARA-G3 and SARA-U2 series GSM/GPRS and GSM/EGPRS/HSPA Cellular Modules

## System Integration Manual

### Abstract

This document describes the features and the system integration of the SARA-G3 series GSM/GPRS cellular modules and the SARA-U2 GSM/EGPRS/HSPA cellular modules.

These modules are complete and cost efficient solutions offering voice and/or data communication over diverse cellular radio access technologies in the same compact SARA form factor: the SARA-G3 series support up to 4-band GSM/GPRS while the SARA-U2 series support 2-band high-speed HSPA and up to 2-band GSM/EGPRS.



**Document Information**

<b>Title</b>	SARA-G3 and SARA-U2 series		
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**Document status explanation**

Objective Specification	Document contains target values. Revised and supplementary data will be published later.		
Advance Information	Document contains data based on early testing. Revised and supplementary data will be published later.		
Early Production Information	Document contains data from product verification. Revised and supplementary data may be published later.		
Production Information	Document contains the final product specification.		

**This document applies to the following products:**

Product name	Type number	Firmware version	SDN / IN / PCN
SARA-G300	SARA-G300-00S-00	08.58	GSM.G2-TN-13007
SARA-G310	SARA-G310-00S-00	08.58	GSM.G2-TN-13007
SARA-G340	SARA-G340-00S-00	08.49	UBX-14000382
	SARA-G340-01S-00	08.70	UBX-14039634
SARA-G350	SARA-G350-00S-00	08.49	GSM.G2-TN-13002
	SARA-G350-01S-00	08.70	UBX-14039634
	SARA-G350-01B-00	TBD	TBD
SARA-G350 ATEX	SARA-G350-00X-00	08.49	GSM.G2-TN-13002
SARA-U260	SARA-U260-00S-00	23.20	UBX-14015739
SARA-U270	SARA-U270-00S-00	23.20	UBX-14015739
SARA-U280	SARA-U280-00S-00	TBD	TBD

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# Preface

## u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **AT Commands Manual:** This document provides the description of the AT commands supported by the u-blox cellular modules.
- **System Integration Manual:** This document provides the description of u-blox cellular modules' system from the hardware and the software point of view, it provides hardware design guidelines for the optimal integration of the cellular modules in the application device and it provides information on how to set up production and final product tests on application devices integrating the cellular modules.
- **Application Notes:** These documents provide guidelines and information on specific hardware and/or software topics on u-blox cellular modules. See Related documents for a list of application notes related to your cellular module.

## How to use this Manual

The SARA-G3 and SARA-U2 series System Integration Manual provides the necessary information to successfully design in and configure these u-blox cellular modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:



An index finger points out key information pertaining to module integration and performance.



**A warning symbol indicates actions that could negatively impact or damage the module.**

## Questions

If you have any questions about u-blox cellular Integration:

- Read this manual carefully.
- Contact our information service on the homepage <http://www.u-blox.com>

## Technical Support

### Worldwide Web

Our website ([www.u-blox.com](http://www.u-blox.com)) is a rich pool of information. Product information and technical documents can be accessed 24h a day.

### By E-mail

If you have technical problems or cannot find the required information in the provided documents, contact the closest Technical Support office. To ensure that we process your request as soon as possible, use our service pool email addresses rather than personal staff email addresses. Contact details are at the end of the document.

### Helpful Information when Contacting Technical Support

When contacting Technical Support, have the following information ready:

- Module type (e.g. SARA-G350) and firmware version
- Module configuration
- Clear description of your question or the problem
- A short description of the application
- Your complete contact details

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Table 2 reports a summary of 2G cellular characteristics of SARA-G3 and SARA-U2 series modules.

Item	SARA-U260	SARA-U270	SARA-G300 / SARA-G340	SARA-G310 / SARA-G350
<b>Protocol stack</b>	3GPP Release 7	3GPP Release 7	3GPP Release 99	3GPP Release 99
<b>MS class</b>	Class B <sup>2</sup>	Class B <sup>2</sup>	Class B <sup>2</sup>	Class B <sup>2</sup>
<b>Bands<sup>3</sup></b>	GSM 850 MHz PCS 1900 MHz	E-GSM 900 MHz DCS 1800 MHz	E-GSM 900 MHz DCS 1800 MHz	GSM 850 MHz E-GSM 900 MHz DCS 1800 MHz PCS 1900 MHz
<b>Power class</b>	Class 4 (33 dBm) for 850 band Class 1 (30 dBm) for 1900 band	Class 4 (33 dBm) for 900 band Class 1 (30 dBm) for 1800 band	Class 4 (33 dBm) for 900 band Class 1 (30 dBm) for 1800 band	Class 4 (33 dBm) for 850/900 bands Class 1 (30 dBm) for 1800/1900 bands
<b>PS data rate<sup>4</sup></b>	GPRS multi-slot class 12 <sup>5</sup> CS 1-4, 85.6 kb/s DL CS 1-4, 85.6 kb/s UL EDGE multi-slot class 12 <sup>5</sup> MCS 1-9, 236.8 kb/s DL MCS 1-4, 70.4 kb/s UL	GPRS multi-slot class 12 <sup>5</sup> CS 1-4, 85.6 kb/s DL CS 1-4, 85.6 kb/s UL EDGE multi-slot class 12 <sup>5</sup> MCS 1-9, 236.8 kb/s DL MCS 1-4, 70.4 kb/s UL	GPRS multi-slot class 10 <sup>6</sup> CS 1-4, 85.6 kb/s DL CS 1-4, 42.8 kb/s UL <sup>4</sup>	GPRS multi-slot class 10 <sup>6</sup> CS 1-4, 85.6 kb/s DL CS 1-4, 42.8 kb/s UL
<b>CS data rate<sup>4</sup></b>	Up to 9.6 kb/s DL/UL Transparent mode Non transparent mode	Up to 9.6 kb/s DL/UL Transparent mode Non transparent mode	Up to 9.6 kb/s DL/UL Transparent mode Non transparent mode	Up to 9.6 kb/s DL/UL Transparent mode Non transparent mode

**Table 2: SARA-G3 series and SARA-U2 series 2G characteristics summary**

Table 3 reports a summary of 3G cellular characteristics of SARA-U2 series modules.

Item	SARA-U260	SARA-U270	SARA-U280
<b>Protocol stack</b>	3GPP Release 7	3GPP Release 7	3GPP Release 7
<b>UE class</b>	Class A <sup>7</sup>	Class A <sup>7</sup>	Class A <sup>7</sup>
<b>Bands</b>	Band V (850 MHz) Band II (1900 MHz)	Band VIII (900 MHz) Band I (2100 MHz)	Band V (850 MHz) Band II (1900 MHz)
<b>Power class</b>	Class 3 (24 dBm) for all bands	Class 3 (24 dBm) for all bands	Class 3 (24 dBm) for all bands
<b>PS data rate<sup>4</sup></b>	HSUPA category 6 5.76 Mb/s UL HSDPA category 8 7.2 Mb/s DL	HSUPA category 6 5.76 Mb/s UL HSDPA category 8 7.2 Mb/s DL	HSUPA category 6 5.76 Mb/s UL HSDPA category 8 7.2 Mb/s DL
<b>CS data rate<sup>4</sup></b>	Up to 64 kb/s DL/UL	Up to 64 kb/s DL/UL	Up to 64 kb/s DL/UL

**Table 3: SARA-U2 series 3G characteristics summary**

<sup>2</sup> Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time.

<sup>3</sup> The 2G 850 / 1900 MHz and 3G 850 / 1900 MHz bands are mainly operative in America. The 2G 900 / 1800 MHz and 3G 900 / 2100 MHz bands are mainly operative in Europe, Asia and other countries.

<sup>4</sup> The maximum bit rate of the module depends on the actual network environmental conditions and settings.

<sup>5</sup> GPRS/EDGE multi-slot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total.

<sup>6</sup> GPRS multi-slot class 10 implies a maximum of 4 slots in DL (reception) and 2 slots in UL (transmission) with 5 slots in total.

<sup>7</sup> Device can work simultaneously in Packet Switch and Circuit Switch mode: voice calls are possible while the data connection is active without any interruption in service.

## 1.2 Architecture

Figure 1 summarizes the architecture of SARA-G300 and SARA-G310 modules, while Figure 2 summarizes the architecture of SARA-G340 and SARA-G350 modules, describing the internal blocks of the modules, consisting of the RF, Baseband and Power Management main sections, and the available interfaces.

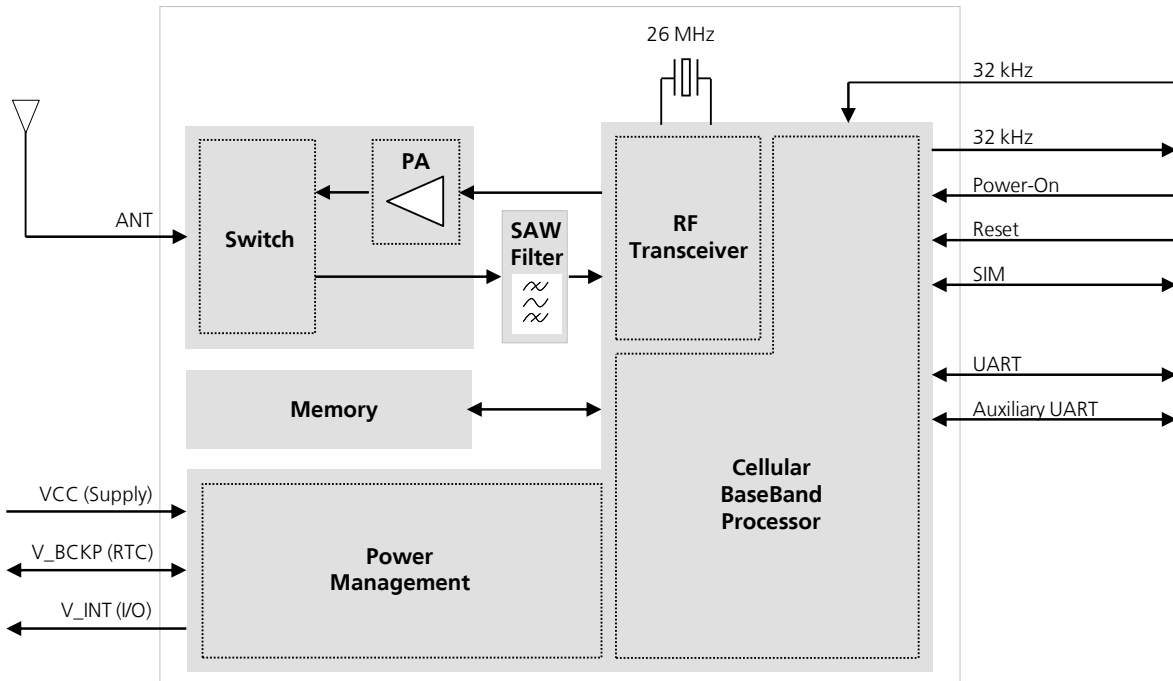


Figure 1: SARA-G300 and SARA-G310 modules block diagram

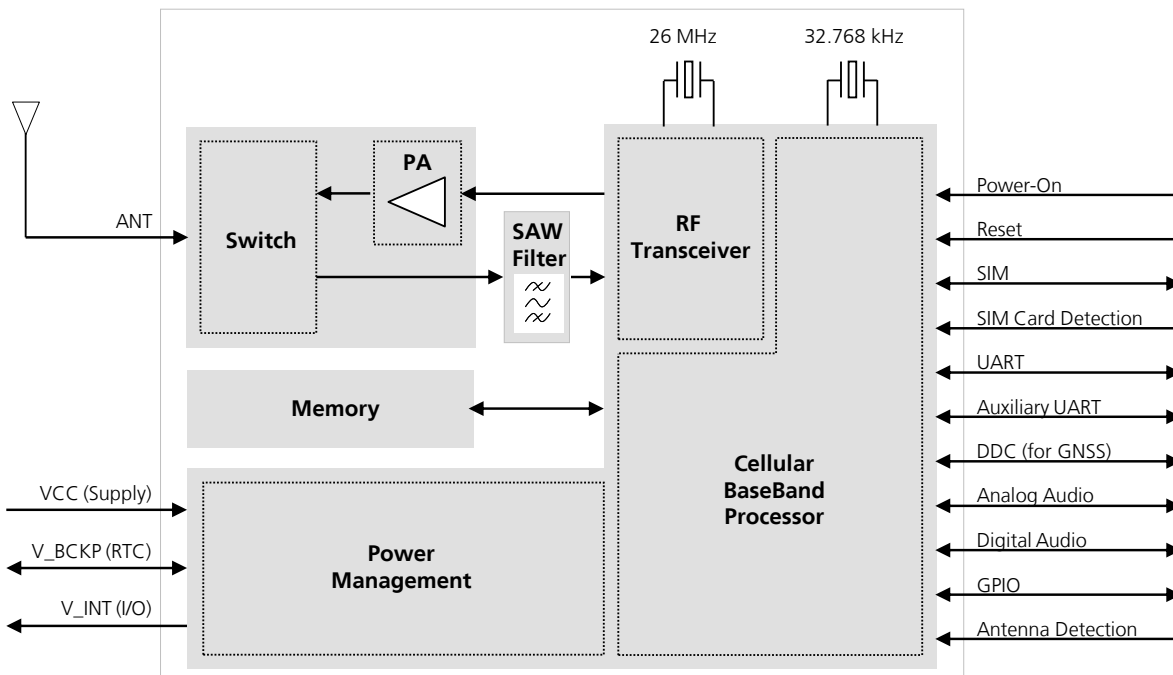


Figure 2: SARA-G340 and SARA-G350 modules block diagram

Figure 3 summarizes the architecture of SARA-U260 and SARA-U270 modules, while Figure 4 summarizes the architecture of SARA-U280 modules, describing the internal blocks of the modules, consisting of the RF, Baseband and Power Management main sections, and the available interfaces.

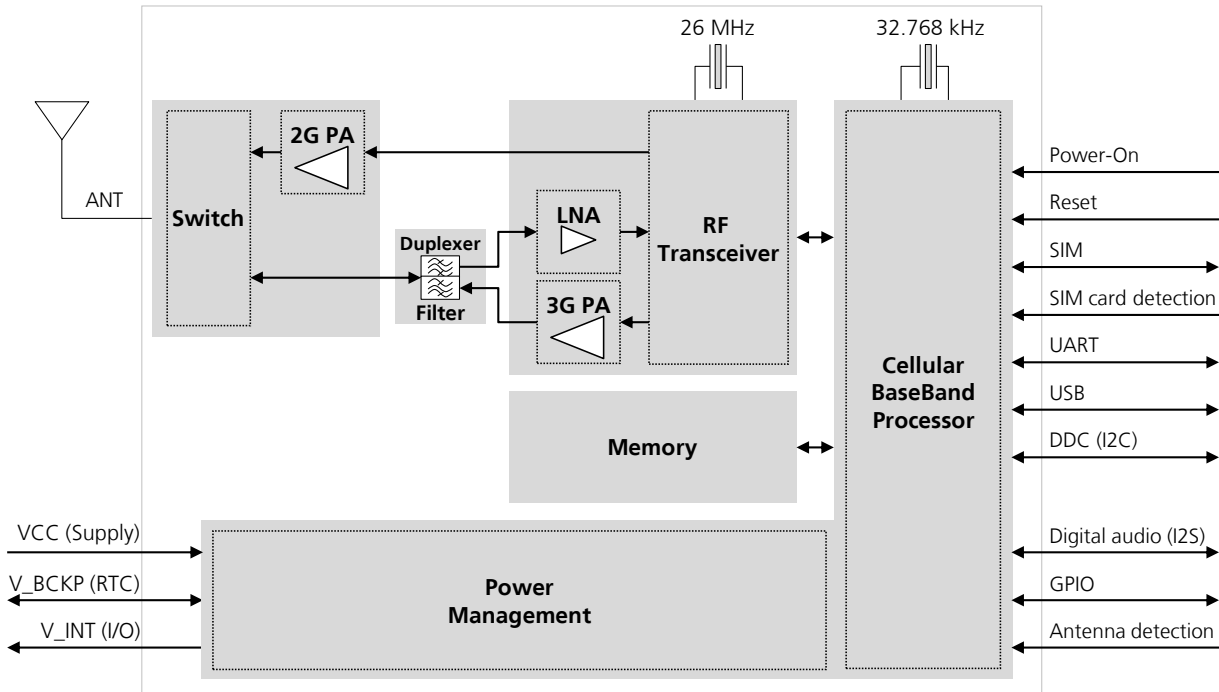


Figure 3: SARA-U260 and SARA-U270 modules block diagram

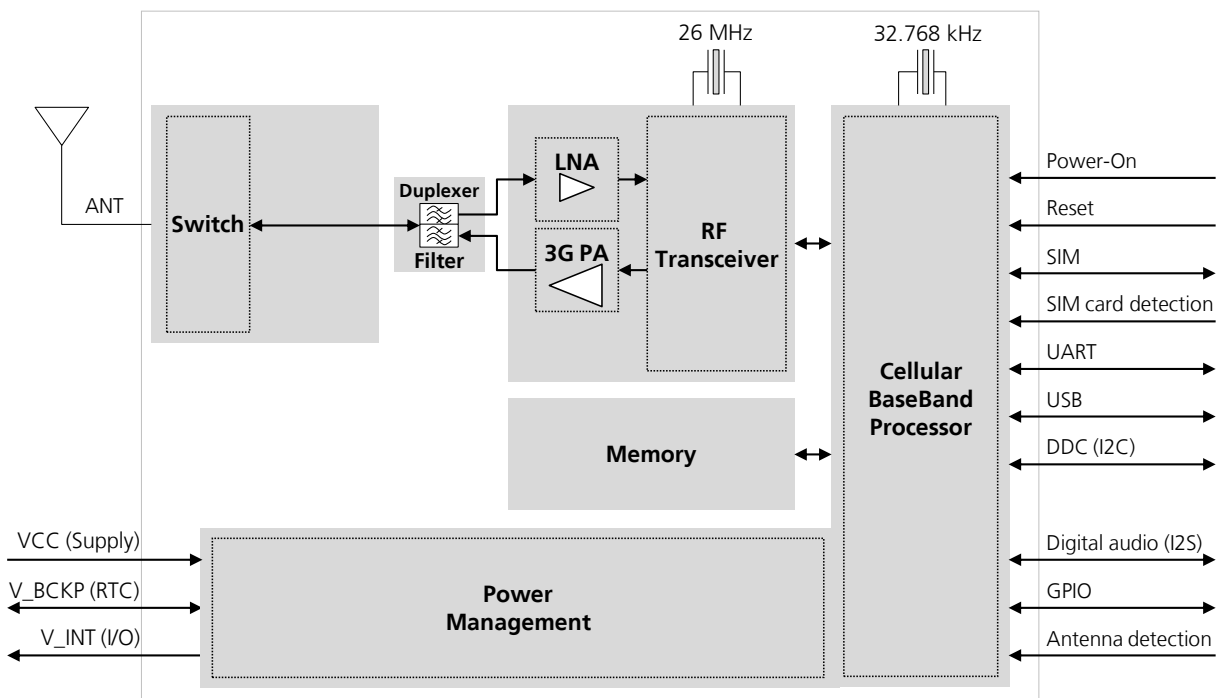


Figure 4: SARA-U280 modules block diagram

## 1.2.1 Internal blocks

SARA-G3 and SARA-U2 series modules internally consist of the RF, Baseband and Power Management sections here described with more details than the simplified block diagrams of Figure 1, Figure 2, Figure 3 and Figure 4.

### RF section

The RF section is composed of the following main elements:

- 2G / 3G RF transceiver performing modulation, up-conversion of the baseband I/Q signals, down-conversion and demodulation of the RF received signals. The RF transceiver includes:
  - Constant gain direct conversion receiver with integrated LNAs
  - Highly linear RF quadrature GMSK demodulator
  - Digital Sigma-Delta transmitter GMSK modulator
  - Fractional-N Sigma-Delta RF synthesizer
  - 3.8 GHz VCO
  - Digital controlled crystal oscillator
- 2G / 3G Power Amplifier, which amplifies the signals modulated by the RF transceiver
- RF switch, which connects the antenna input/output pin (**ANT**) of the module to the suitable RX/TX path
- RX diplexer SAW (band pass) filters
- 26 MHz crystal, connected to the digital controlled crystal oscillator to perform the clock reference in active-mode or connected-mode

### Baseband and Power Management section

The Baseband and Power Management section is composed of the following main elements:

- Baseband processor, a mixed signal ASIC which integrates:
  - Microprocessor for controller functions
  - DSP core for 2G / 3G Layer 1 and audio processing
  - Dedicated peripheral blocks for parallel control of the digital interfaces
  - Audio analog front-end
- Memory system in a multi-chip package integrating two devices:
  - NOR flash non-volatile memory
  - RAM volatile memory
- Voltage regulators to derive all the system supply voltages from the module supply **VCC**
- Circuit for the RTC clock reference in low power idle-mode:
 

SARA-G340, SARA-G350 and SARA-U2 series modules are equipped with an internal 32.768 kHz crystal connected to the oscillator of the RTC (Real Time Clock) block that gives the RTC clock reference needed to provide the RTC functions as well as to reach the very low power idle-mode (with power saving configuration enabled by the AT+UPSV command).

SARA-G300 and SARA-G310 modules are not equipped with an internal 32.768 kHz crystal: a proper 32 kHz signal must be provided at the **EXT32K** input pin of the modules to give the RTC clock reference and to provide the RTC functions as well as to reach the very low power idle-mode (with power saving configuration enabled by AT+UPSV). The **32K\_OUT** output pin of SARA-G300 and SARA-G310 provides a 32 kHz reference signal suitable only to feed the **EXT32K** input pin, furnishes the reference clock for the RTC, and allows low power idle-mode and RTC functions support with modules switched on.

## 1.3 Pin-out

Table 4 lists the pin-out of the SARA-G3 and SARA-U2 series modules, with pins grouped by function.

Function	Pin Name	Module	Pin No	I/O	Description	Remarks
Power	VCC	All	51, 52, 53	I	Module supply input	VCC pins are internally connected each other. VCC supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description and requirements for the VCC module supply. See section 2.2.1 for external circuit design-in.
	GND	All	1, 3, 5, 14, 20-22, 30, 32, 43, 50, 54, 55, 57-61, 63-96	N/A	Ground	GND pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.
	V_BCKP	All	2	I/O	Real Time Clock supply input/output	V_BCKP = 2.3 V (typical) on SARA-G3 series. V_BCKP = 1.8 V (typical) on SARA-U2 series. V_BCKP is generated by internal low power linear regulator when valid VCC supply is present. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in.
	V_INT	All	4	O	Generic Digital Interfaces supply output	V_INT = 1.8 V (typical), generated by internal DC/DC regulator when the module is switched on. See section 1.5.3 for functional description. See section 2.2.3 for external circuit design-in.
System	PWR_ON	All	15	I	Power-on input	High input impedance: input voltage level has to be properly fixed, e.g. adding external pull-up. See section 1.6.1 for functional description. See section 2.3.1 for external circuit design-in.
	RESET_N	All	18	I	External reset input	A series Schottky diode is integrated in the module as protection, and then an internal 10 kΩ pull-up resistor to V_INT is provided. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in.
	EXT32K	SARA-G300 SARA-G310	31	I	32 kHz input	Input for RTC reference clock, needed to enter the low power idle-mode and provide RTC functions. See section 1.6.4 for functional description. See section 2.3.3 for external circuit design-in.
	32K_OUT	SARA-G300 SARA-G310	24	O	32 kHz output	32 kHz output suitable only to feed the EXT32K input giving the RTC reference clock, allowing low power idle-mode and RTC functions support. See section 1.6.5 for functional description. See section 2.3.3 for external circuit design-in.
Antenna	ANT	All	56	I/O	RF input/output for antenna	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7 for functional description and requirements for the antenna RF interface. See section 2.4 for external circuit design-in.
	ANT_DET	SARA-G340 SARA-G350 SARA-U2	62	I	Input for antenna detection	ADC input for antenna detection function. See section 1.7.2 for functional description. See section 2.4.2 for external circuit design-in.

Function	Pin Name	Module	Pin No	I/O	Description	Remarks
SIM	VSIM	All	41	O	SIM supply output	<b>VSIM</b> = 1.80 V typ. or 2.85 V typ. automatically generated according to the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	All	39	I/O	SIM data	Data input/output for 1.8 V / 3 V SIM Internal 4.7 kΩ pull-up to <b>VSIM</b> . See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	All	38	O	SIM clock	3.25 MHz clock output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	All	40	O	SIM reset	Reset output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_DET	All	42	I / I/O	SIM detection / GPIO	1.8 V input for SIM presence detection function. Pin configurable also as GPIO on SARA-U2 series. See section 1.8.2 for functional description. See section 2.5 for external circuit design-in.
UART	RXD	All	13	O	UART data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24, for AT, data, FOAT on SARA-G3 series modules, for AT, data, FOAT, FW upgrade via EasyFlash tool and diagnostic on SARA-U2 series modules. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	TXD	All	12	I	UART data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24, for AT, data, FOAT on SARA-G3 series modules, for AT, data, FOAT, FW upgrade via EasyFlash tool and diagnostic on SARA-U2 series modules. Internal active pull-up to <b>V_INT</b> . See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	CTS	All	11	O	UART clear to send output	1.8 V output, Circuit 106 (CTS) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	All	10	I	UART ready to send input	1.8 V input, Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to <b>V_INT</b> . See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	All	6	O	UART data set ready output	1.8 V output, Circuit 107 (DSR) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RI	All	7	O	UART ring indicator output	1.8 V output, Circuit 125 (RI) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	All	9	I	UART data terminal ready input	1.8 V input, Circuit 108/2 (DTR) in ITU-T V.24. Internal active pull-up to <b>V_INT</b> . See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DCD	All	8	O	UART data carrier detect output	1.8 V input, Circuit 109 (DCD) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.

Function	Pin Name	Module	Pin No	I/O	Description	Remarks
Auxiliary UART	RXD_AUX	SARA-G3	28	O	Auxiliary UART data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24, for FW upgrade via EasyFlash tool and diagnostic. Access by external test-point is recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	TXD_AUX	SARA-G3	29	I	Auxiliary UART data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24, for FW upgrade via EasyFlash tool and diagnostic. Access by external test-point is recommended. Internal active pull-up to <b>V_INT</b> . See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
USB	VUSB_DET	SARA-U2	17	I	USB detect input	High-Speed USB 2.0 interface input for VBUS (5 V typical) USB supply sense. USB available for AT, data, FOAT, FW upgrade via EasyFlash tool and diagnostic. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	USB_D-	SARA-U2	28	I/O	USB Data Line D-	High-Speed USB 2.0 interface data line for AT, data, FOAT, FW upgrade via EasyFlash tool and diagnostic. 90 Ω nominal differential impedance. Pull-up, pull-down and series resistors as required by USB 2.0 specifications [14] are part of the USB pin driver and need not be provided externally. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	USB_D+	SARA-U2	29	I/O	USB Data Line D+	High-Speed USB 2.0 interface data line for AT, data, FOAT, FW upgrade via EasyFlash tool and diagnostic. 90 Ω nominal differential impedance. Pull-up, pull-down and series resistors as required by USB 2.0 specifications [14] are part of the USB pin driver and need not be provided externally. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
DDC	SCL	SARA-G340 SARA-G350 SARA-U2	27	O	I <sup>2</sup> C bus clock line	1.8 V open drain, for the communication with the u-blox positioning modules / chips. Communication with other external I <sup>2</sup> C-slave devices as an audio codec is additionally supported by SARA-U2 series. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
	SDA	SARA-G340 SARA-G350 SARA-U2	26	I/O	I <sup>2</sup> C bus data line	1.8 V open drain, for the communication with u-blox positioning modules / chips. Communication with other external I <sup>2</sup> C-slave devices as an audio codec is additionally supported by SARA-U2 series. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.

Function	Pin Name	Module	Pin No	I/O	Description	Remarks
<b>Analog Audio</b>	<b>MIC_BIAS</b>	SARA-G340 SARA-G350	46	O	Microphone supply output	Supply output (2.2 V typ) for external microphone. See section 1.10.1 for functional description. See section 2.7.1 for external circuit design-in.
	<b>MIC_GND</b>	SARA-G340 SARA-G350	47	I	Microphone analog reference	Local ground for the external microphone (reference for the analog audio uplink path). See section 1.10.1 for functional description. See section 2.7.1 for external circuit design-in.
	<b>MIC_N</b>	SARA-G340 SARA-G350	48	I	Differential analog audio input (negative)	Differential analog audio signal input (negative) shared for all the analog uplink path modes: handset, headset, hands-free mode. No internal DC blocking capacitor. See section 1.10.1 for functional description. See section 2.7.1 for external circuit design-in.
	<b>MIC_P</b>	SARA-G340 SARA-G350	49	I	Differential analog audio input (positive)	Differential analog audio signal input (positive) shared for all the analog uplink path modes: handset, headset, hands-free mode. No internal DC blocking capacitor. See section 1.10.1 for functional description. See section 2.7.1 for external circuit design-in.
	<b>SPK_P</b>	SARA-G340 SARA-G350	44	O	Differential analog audio output (positive)	Differential analog audio signal output (positive) shared for all the analog downlink path modes: earpiece, headset and loudspeaker mode. See section 1.10.1 for functional description. See section 2.7.1 for external circuit design-in.
	<b>SPK_N</b>	SARA-G340 SARA-G350	45	O	Differential analog audio output (negative)	Differential analog audio signal output (negative) shared for all the analog downlink path modes: earpiece, headset and loudspeaker mode. See section 1.10.1 for functional description. See section 2.7.1 for external circuit design-in.
<b>Digital Audio</b>	<b>I2S_CLK</b>	SARA-G340 SARA-G350 SARA-U2	36	O / I/O	I <sup>2</sup> S clock / GPIO	1.8 V serial clock for PCM / normal I <sup>2</sup> S modes. Pin configurable also as GPIO on SARA-U2 series. See section 1.10.2 for functional description. See section 2.7.2 for external circuit design-in.
	<b>I2S_RXD</b>	SARA-G340 SARA-G350 SARA-U2	37	I / I/O	I <sup>2</sup> S receive data / GPIO	1.8 V data input for PCM / normal I <sup>2</sup> S modes. Pin configurable also as GPIO on SARA-U2 series. Internal active pull-down to GND. See section 1.10.2 for functional description. See section 2.7.2 for external circuit design-in.
	<b>I2S_TXD</b>	SARA-G340 SARA-G350 SARA-U2	35	O / I/O	I <sup>2</sup> S transmit data / GPIO	1.8 V data output for PCM / normal I <sup>2</sup> S modes. Pin configurable also as GPIO on SARA-U2 series. See section 1.10.2 for functional description. See section 2.7.2 for external circuit design-in.
	<b>I2S_WA</b>	SARA-G340 SARA-G350 SARA-U2	34	O / I/O	I <sup>2</sup> S word alignment / GPIO	1.8 V word alignment for PCM / normal I <sup>2</sup> S modes. Pin configurable also as GPIO on SARA-U2 series. See section 1.10.2 for functional description. See section 2.7.2 for external circuit design-in.
	<b>CODEC_CLK</b>	SARA-U2	19	O	Clock output	1.8 V master clock output for external audio codec. See section 1.10.2 for functional description. See section 2.7.2 for external circuit design-in.



Function	Pin Name	Module	Pin No	I/O	Description	Remarks
GPIO	GPIO1	SARA-G340 SARA-G350 SARA-U2	16	I/O	GPIO	1.8 V GPIO by default configured as pin disabled. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO2	SARA-G340 SARA-G350 SARA-U2	23	I/O	GPIO	1.8 V GPIO by default configured to provide the custom GNSS supply enable function. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO3	SARA-G340 SARA-G350 SARA-U2	24	I/O	GPIO	1.8 V GPIO by default configured to provide the custom GNSS data ready function. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO4	SARA-G340 SARA-G350 SARA-U2	25	I/O	GPIO	1.8 V GPIO by default configured to provide the custom GNSS RTC sharing function. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
Reserved	RSVD	All	33	N/A	RESERVED pin	This pin must be connected to ground. See section 2.9
	RSVD	SARA-G3	17, 19	N/A	RESERVED pin	Leave unconnected. See section 2.9
	RSVD	SARA-G340 SARA-G350 SARA-U2	31	N/A	RESERVED pin	Internally not connected. Leave unconnected. See section 2.9
	RSVD	SARA-G300 SARA-G310	16, 23, 25-27, 34-37	N/A	RESERVED pin	Pin disabled. Leave unconnected. See section 2.9
	RSVD	SARA-G300 SARA-G310 SARA-U2	44-49	N/A	RESERVED pin	Leave unconnected. See section 2.9
	RSVD	SARA-G300 SARA-G310	62	N/A	RESERVED pin	Leave unconnected. See section 2.9

**Table 4: SARA-G3 and SARA-U2 series modules pin definition, grouped by function**

## 1.4 Operating modes

SARA-G3 modules have several operating modes. The operating modes defined in Table 5 and described in detail in Table 6 provide general guidelines for operation.

General Status	Operating Mode	Definition
Power-down	Not-Powered Mode	VCC supply not present or below operating range: module is switched off.
	Power-Off Mode	VCC supply within operating range and module is switched off.
Normal Operation	Idle-Mode	Module processor core runs with 32 kHz reference, that is generated by: <ul style="list-style-type: none"> <li>The internal 32 kHz oscillator (SARA-G340, SARA-G350 and SARA-U2 series)</li> <li>The 32 kHz signal provided at the <b>EXT32K</b> pin (SARA-G300 and SARA-G310)</li> </ul>
	Active-Mode	Module processor core runs with 26 MHz reference generated by the internal oscillator.
	Connected-Mode	Voice or data call enabled and processor core runs with 26 MHz reference.

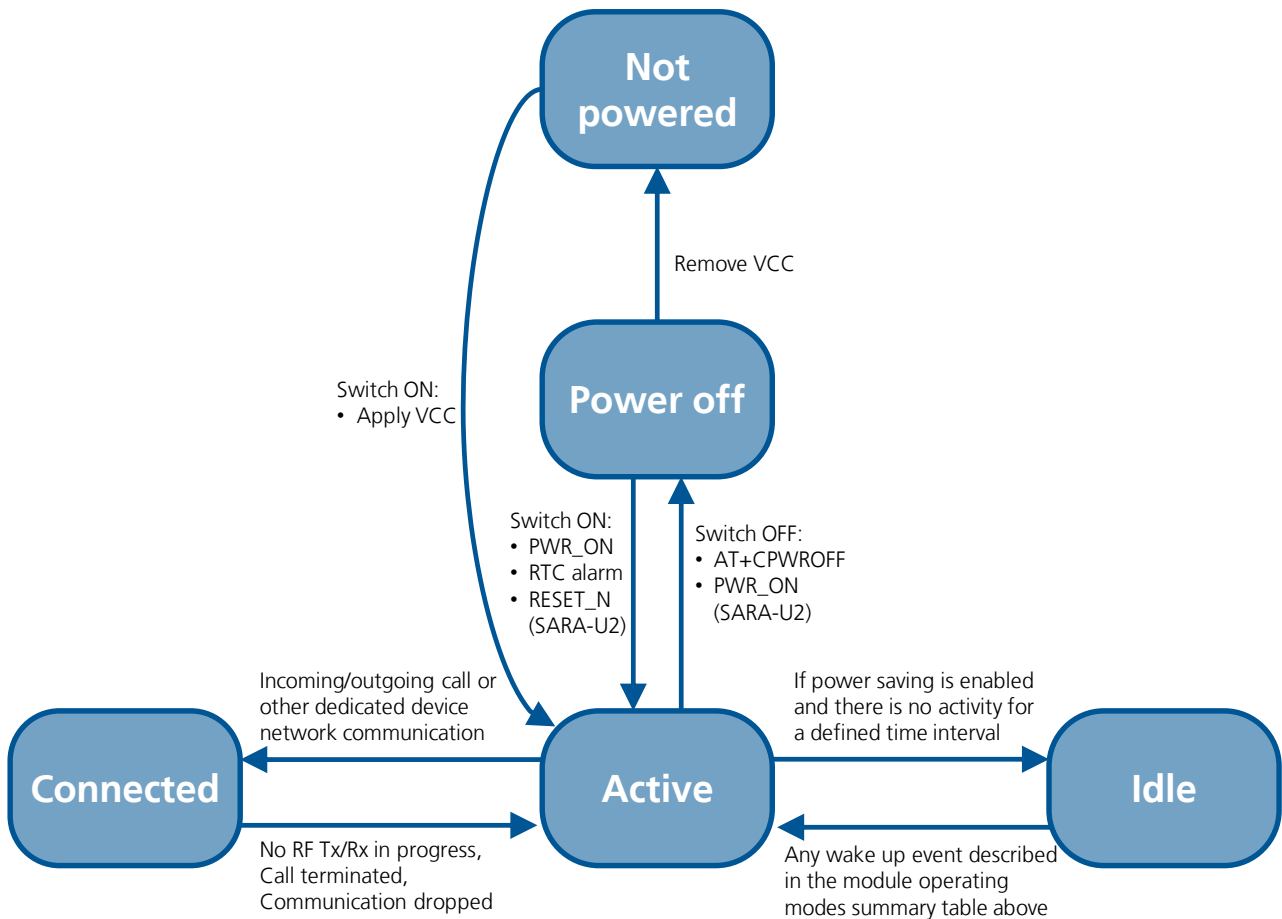
Table 5: Module operating modes definition

Operating Mode	Description	Transition between operating modes
<b>Not-Powered</b>	<p>Module is switched off.</p> <p>Application interfaces are not accessible.</p> <p>Internal RTC operates on SARA-G340/G350, SARA-U2 if a valid voltage is applied to <b>V_BCKP</b>. Additionally, a proper external 32 kHz signal must be fed to <b>EXT32K</b> on SARA-G300/G310 modules to let internal RTC timer running.</p>	<p>When <b>VCC</b> supply is removed, the module enters not-powered mode.</p> <p>When in not-powered mode, the modules cannot be switched on by <b>PWR_ON</b>, <b>RESET_N</b> or RTC alarm.</p> <p>When in not-powered mode, the modules can be switched on applying <b>VCC</b> supply (see 2.3.1) so that the module switches from not-powered to active-mode.</p>
<b>Power-Off</b>	<p>Module is switched off: normal shutdown by an appropriate power-off event (see 1.6.2).</p> <p>Application interfaces are not accessible.</p> <p>Internal RTC operates on SARA-G340/G350, SARA-U2 as <b>V_BCKP</b> is internally generated.</p> <p>A proper external 32 kHz signal must be fed to the <b>EXT32K</b> pin on SARA-G300/G310 to let RTC timer running that otherwise is not in operation.</p>	<p>When the module is switched off by an appropriate power-off event (see 1.6.2), the module enters power-off mode from active-mode.</p> <p>When in power-off mode, the modules can be switched on by <b>PWR_ON</b>, <b>RESET_N</b> or RTC alarm (see 2.3.1): the module switches from power-off to active-mode.</p> <p>When <b>VCC</b> supply is removed, the module switches from power-off mode to not-powered mode.</p>
<b>Idle</b>	<p>The module is not ready to communicate with an external device by means of the application interfaces as configured to reduce consumption.</p> <p>The module automatically enters idle-mode whenever possible if power saving is enabled by the AT+UPSV command (see u-blox AT Commands Manual [3]), reducing power consumption (see section 1.5.1.4).</p> <p>The <b>CTS</b> output line indicates when the UART interface is disabled/enabled due to the module idle/active-mode according to power saving and HW flow control settings (see 1.9.1.3, 1.9.1.4).</p> <p>Power saving configuration is not enabled by default: it can be enabled by AT+UPSV (see the u-blox AT Commands Manual [3]).</p> <p>A proper 32 kHz signal must be fed to the <b>EXT32K</b> pin of SARA-G300/G310 modules to let idle-mode that otherwise cannot be reached (this is not needed for the other SARA-G3 and SARA-U2 series modules).</p>	<p>The module automatically switches from active-mode to idle-mode whenever possible if power saving is enabled (see sections 1.5.1.4, 1.9.1.4 and to the u-blox AT Commands Manual [3], AT+UPSV).</p> <p>The module wakes up from idle to active mode in the following events:</p> <ul style="list-style-type: none"> <li>Automatic periodic monitoring of the paging channel for the paging block reception according to network conditions (see 1.5.1.4, 1.9.1.4)</li> <li>Automatic periodic enable of the UART interface to receive and send data, if AT+UPSV=1 power saving is set (see 1.9.1.4)</li> <li>RTC alarm occurs (see u-blox AT Commands Manual [3], +CALA)</li> <li>Data received on UART interface, according to HW flow control (AT&amp;K) and power saving (AT+UPSV) settings (see 1.9.1.4)</li> <li><b>RTS</b> input line set to the ON state by the DTE, if HW flow control is disabled by AT&amp;K3 and AT+UPSV=2 is set (see 1.9.1.4)</li> <li><b>DTR</b> input line set to the ON state by the DTE, if AT+UPSV=3 power saving is set (see 1.9.1.4)</li> <li>USB detection, applying 5 V (typ.) to <b>VUSB_DET</b> input (see 1.9.3)</li> <li>The connected USB host forces a remote wakeup of the module as USB device (see 1.9.3)</li> <li>GNSS data ready: when the <b>GPIO3</b> pin is informed by the connected u-blox GNSS receiver that it is ready to send data over the DDC (I<sup>2</sup>C) communication interface (see 1.11, 1.9.4)</li> </ul>

Operating Mode	Description	Transition between operating modes
<b>Active</b>	The module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by the AT+UPSV command (see sections 1.5.1.4, 1.9.1.4 and to the u-blox AT Commands Manual [3]).	When the module is switched on by an appropriate power-on event (see 2.3.1), the module enters active-mode from not-powered or power-off mode. If power saving configuration is enabled by the AT+UPSV command, the module automatically switches from active to idle-mode whenever possible and the module wakes up from idle to active-mode in the events listed above (see idle to active transition description). When a voice call or a data call is initiated, the module switches from active-mode to connected-mode.
<b>Connected</b>	A voice call or a data call is in progress. The module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by the AT+UPSV command (see sections 1.5.1.4, 1.9.1.4 and the u-blox AT Commands Manual [3]).	When a voice call or a data call is initiated, the module enters connected-mode from active-mode. When a voice call or a data call is terminated, the module returns to the active-mode.

**Table 6: Module operating modes description**

Figure 5 describes the transition between the different operating modes.



**Figure 5: Operating modes transition**

## 1.5 Supply interfaces

### 1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

The **VCC** pins are internally connected to the RF power amplifier and to the integrated Power Management Unit: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators, including **V\_BCKP** Real Time Clock supply, **V\_INT** digital interfaces supply and **VSIM** SIM card supply.

During operation, the current drawn by the SARA-G3 and SARA-U2 series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the high peak of current consumption during GSM transmitting bursts at maximum power level in connected-mode (as described in section 1.5.1.2), to the low current consumption during low power idle-mode with power saving enabled (as described in section 1.5.1.4).

#### 1.5.1.1 VCC supply requirements

Table 7 summarizes the requirements for the **VCC** module supply. See section 2.2.1 for all the suggestions to properly design a **VCC** supply circuit compliant to the requirements listed in Table 7.

 **VCC supply circuit affects the RF compliance of the device integrating SARA-G3 and SARA-U2 series modules with applicable required certification schemes as well as antenna circuit design. Compliance is guaranteed if the VCC requirements summarized in the Table 7 are fulfilled.**

 For the additional specific requirement for SARA-G350 ATEX modules integration in potentially explosive atmospheres applications, see section 2.14.

Item	Requirement	Remark
<b>VCC</b> nominal voltage	Within <b>VCC</b> normal operating range: 3.35 V min. / 4.50 V max for SARA-G3 series 3.30 V min. / 4.40 V max for SARA-U2 series	The module cannot be switched on if <b>VCC</b> voltage value is below the normal operating range minimum limit. Ensure that the input voltage at <b>VCC</b> pins is above the minimum limit of the normal operating range for at least more than 3 s after the module switch-on.
<b>VCC</b> voltage during normal operation	Within <b>VCC</b> extended operating range: 3.00 V min. / 4.50 V max for SARA-G3 series 3.10 V min. / 4.50 V max for SARA-U2 series	The module may switch off when <b>VCC</b> voltage drops below the extended operating range minimum limit. Operation above extended operating range limit is not recommended and may affect device reliability.
<b>VCC</b> average current	Support with adequate margin the highest averaged <b>VCC</b> current consumption value in connected-mode conditions specified in SARA-G3 series Data Sheet [1] and in SARA-U2 series Data Sheet [2].	The highest averaged <b>VCC</b> current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and <b>VCC</b> voltage. See 1.5.1.2, 1.5.1.3 for connected-mode current profiles.
<b>VCC</b> peak current	Support with margin the highest peak <b>VCC</b> current consumption value specified in SARA-G3 series Data Sheet [1] and in SARA-U2 series Data Sheet [2].	The specified highest peak of <b>VCC</b> current consumption occurs during GSM single transmit slot in 850/900 MHz connected-mode, in case of mismatched antenna. See 1.5.1.2 for 2G connected-mode current profiles.
<b>VCC</b> voltage drop during 2G Tx slots	Lower than 400 mV	<b>VCC</b> voltage drop directly affects the RF compliance with applicable certification schemes. Figure 7 describes <b>VCC</b> voltage drop during Tx slots.
<b>VCC</b> voltage ripple during 2G/3G Tx	Lower than 30 mVpp if $f_{\text{ripple}} \leq 200$ kHz Lower than 10 mVpp if $200 \text{ kHz} < f_{\text{ripple}} \leq 400$ kHz Lower than 2 mVpp if $f_{\text{ripple}} > 400$ kHz	<b>VCC</b> voltage ripple directly affects the RF compliance with applicable certification schemes. Figure 7 describes <b>VCC</b> voltage ripple during Tx slots.
<b>VCC</b> under/over-shoot at start/end of Tx slots	Absent or at least minimized	<b>VCC</b> under/over-shoot directly affects the RF compliance with applicable certification schemes. Figure 7 describes <b>VCC</b> voltage under/over-shoot.

**Table 7: Summary of VCC supply requirements**

### 1.5.1.2 VCC current consumption in 2G connected-mode

When a GSM call is established, the **VCC** consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The current consumption peak during a transmission slot is strictly dependent on the transmitted power, which is regulated by the network. The transmitted power in the transmit slot is also the more relevant factor for determining the average current consumption.

If the module is transmitting in 2G single-slot mode (as in GSM talk mode) in the 850 or 900 MHz bands, at the maximum RF power control level (approximately 2 W or 33 dBm in the Tx slot/burst), the current consumption can reach a high peak / pulse (see SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2]) for 576.9  $\mu$ s (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), so with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access).

If the module is transmitting in 2G single-slot mode in the 1800 or 1900 MHz bands, the current consumption figures are quite less high than the one in the low bands, due to 3GPP transmitter output power specifications.

During a GSM call, current consumption is not so significantly high in receiving or in monitor bursts and it is low in the bursts unused to transmit / receive.

Figure 6 shows an example of the module current consumption profile versus time in GSM talk mode.

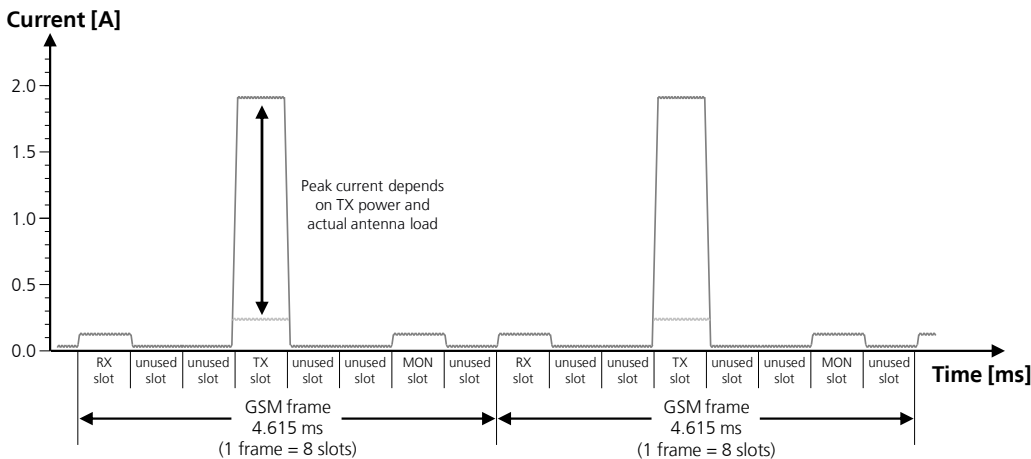


Figure 6: VCC current consumption profile versus time during a GSM call (1 TX slot, 1 RX slot)

Figure 7 illustrates **VCC** voltage profile versus time during a GSM call, according to the related **VCC** current consumption profile described in Figure 6.

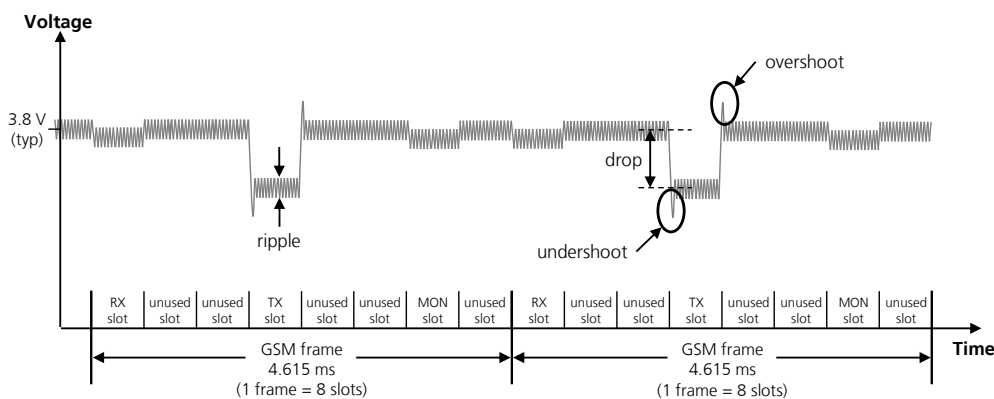


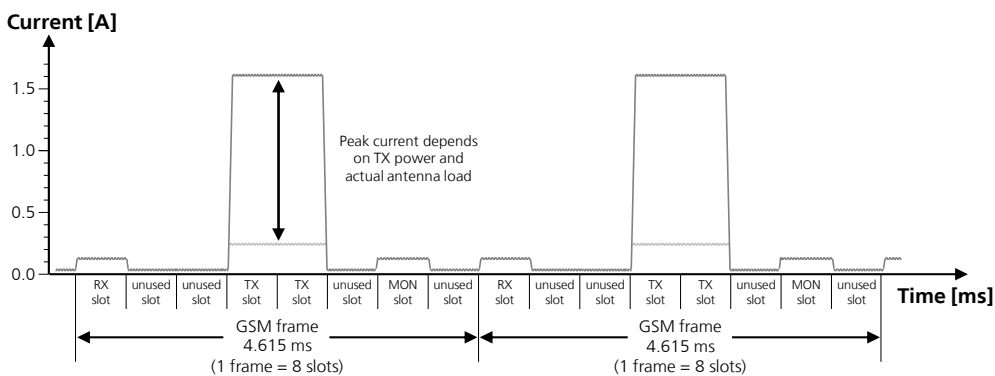
Figure 7: Description of the VCC voltage profile versus time during a GSM call (1 TX slot, 1 RX slot)

When a GPRS connection is established, more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on network conditions, which set the peak current consumption, but following the GPRS specifications the maximum transmitted RF power is reduced if more than one slot is used to transmit, so the maximum peak of current is not as high as can be in case of a GSM call.

If the module transmits in GPRS multi-slot class 10 or 12, in 850 or 900 MHz bands, at maximum RF power level, the consumption can reach a quite high peak but lower than the one achievable in 2G single-slot mode. This happens for 1.154 ms (width of the 2 Tx slots/bursts) in case of multi-slot class 10 or for 2.308 ms (width of the 4 Tx slots/bursts) in case of multi-slot class 12, with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/4 or 1/2 duty cycle, according to GSM TDMA.

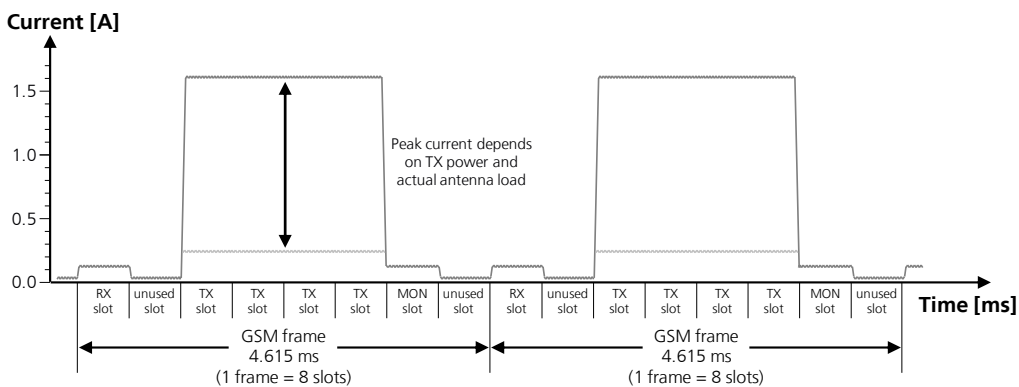
If the module is in GPRS connected-mode in 1800 or 1900 MHz bands, consumption figures are lower than in the 850 or 900 MHz band, due to 3GPP Tx power specifications.

Figure 8 reports the current consumption profiles in GPRS connected-mode, in the 850 or 900 MHz bands, with 2 slots used to transmit and 1 slot used to receive, as for the GPRS multi-slot class 10.



**Figure 8: VCC current consumption profile versus time during a GPRS multi-slot class 10 connection (2 TX slots, 1 RX slot)**

Figure 9 reports the current consumption profiles in GPRS connected-mode, in the 850 or 900 MHz bands, with 4 slots used to transmit and 1 slot used to receive, as for the GPRS multi-slot class 12.



**Figure 9: VCC current consumption profile versus time during a GPRS multi-slot class 12 connection (4 TX slots, 1 RX slot)**

For detailed current consumption values during 2G single-slot or multi-slot connection see SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2].

### 1.5.1.3 VCC current consumption in 3G connected mode

During a 3G connection, the SARA-U2 modules can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation with the Wideband Code Division Multiple Access (WCDMA).

The current consumption depends again on output RF power, which is always regulated by network commands. These power control commands are logically divided into a slot of 666  $\mu$ s, thus the rate of power change can reach a maximum rate of 1.5 kHz.

There are no high current peaks as in the 2G connection, since transmission and reception are continuously enabled due to FDD WCDMA implemented in the 3G that differs from the TDMA implemented in the 2G case.

In the worst scenario, corresponding to a continuous transmission and reception at maximum RF output power (approximately 250 mW or 24 dBm), the average current drawn by the module at the VCC pins is high (see the SARA-U2 series Data Sheet [2]). Even at lowest RF output power level (approximately 0.01  $\mu$ W or -50 dBm), the average current is still not so low as in the equivalent 2G case, also due to module continuous baseband processing and transceiver activity.

Figure 10 shows an example of current consumption profile of SARA-U2 series modules in 3G WCDMA/HSPA continuous transmission and reception mode. For detailed current consumption values during a 3G connection see the SARA-U2 series Data Sheet [2].

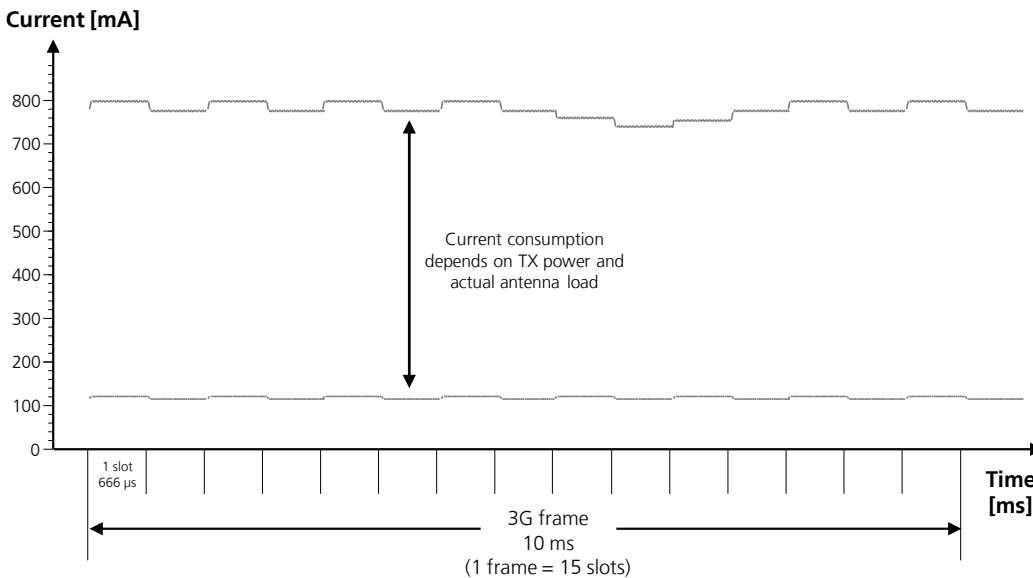


Figure 10: VCC current consumption profile versus time during a 3G connection (TX and RX continuously enabled)

### 1.5.1.4 VCC current consumption in cyclic idle/active-mode (power saving enabled)

The power saving configuration is by default disabled, but it can be enabled using the appropriate AT command (see u-blox AT Commands Manual [3], AT+UPSV command). When power saving is enabled, the module automatically enters low power idle-mode whenever possible, reducing current consumption.

During idle-mode, the module processor runs with 32 kHz reference clock:

- the internal oscillator automatically generates the 32 kHz clock on SARA-G340, SARA-G350, SARA-U2 series
- a valid 32 kHz signal must be properly provided to the **EXT32K** input pin of the SARA-G300 and SARA-G310 modules to let low power idle-mode, that otherwise cannot be reached by these modules.

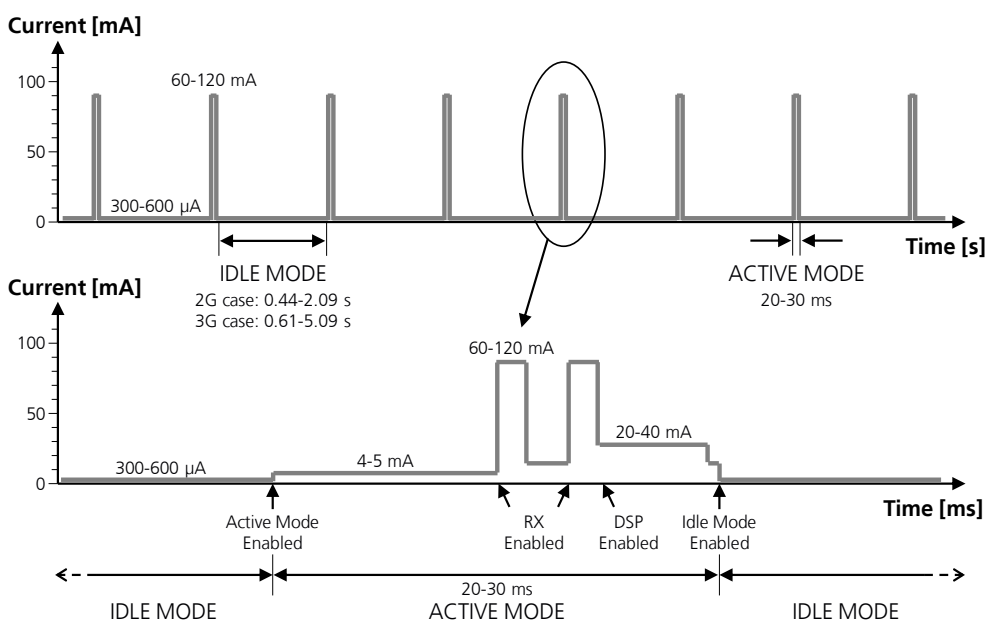
When the power saving configuration is enabled and the module is registered or attached to a network, the module automatically enters the low power idle-mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to the 2G or 3G system requirements, even if connected-mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active-mode, to enable the reception of paging block. In between, the module switches to low power idle-mode. This is known as discontinuous reception (DRX).

The module processor core is activated during the paging block reception, and automatically switches its reference clock frequency from 32 kHz to the 26 MHz used in active-mode.

The time period between two paging block receptions is defined by the network. This is the paging period parameter, fixed by the base station through broadcast channel sent to all users on the same serving cell.

- In case of 2G radio access technology, the paging period varies from 470.8 ms (DRX = 2, length of 2 x 51 2G frames = 2 x 51 x 4.615 ms) up to 2118.4 ms (DRX = 9, length of 9 x 51 2G frames = 9 x 51 x 4.615 ms)
- In case of 3G radio access technology, the paging period can vary from 640 ms (DRX = 6, i.e. length of 26 3G frames = 64 x 10 ms) up to 5120 ms (DRX = 9, length of 29 3G frames = 512 x 10 ms).

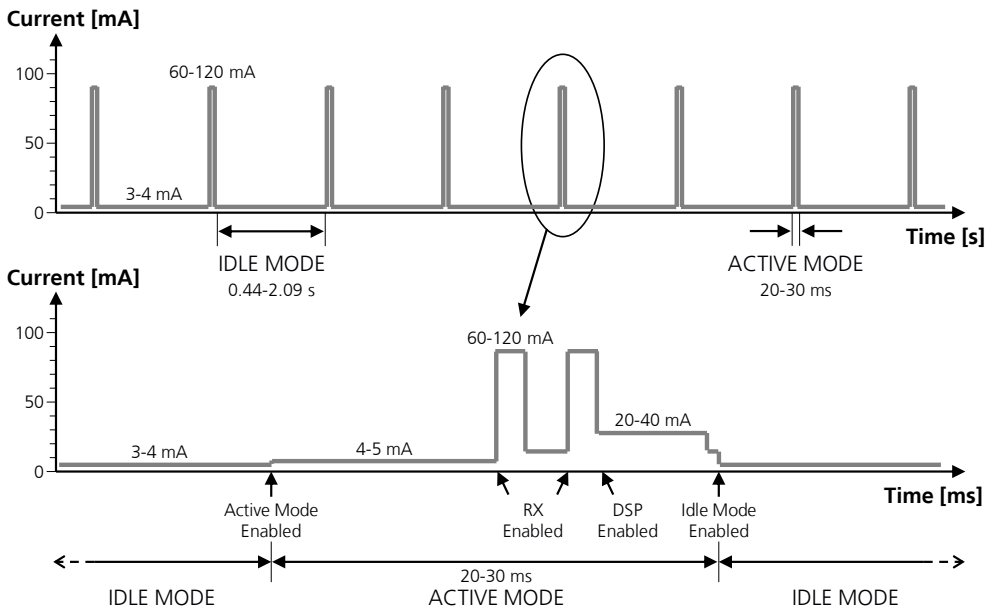
Figure 11 roughly describes the current consumption profile of SARA-G300 and SARA-G310 modules (when their **EXT32K** input pin is fed by an external 32 kHz signal with characteristics compliant to the one specified in SARA-G3 series Data Sheet [1]), or the SARA-G340 and SARA-G350 modules, or the SARA-U2 modules, when power saving is enabled. The module is registered with the network, automatically enters the very low power idle-mode, and periodically wakes up to active-mode to monitor the paging channel for paging block reception.



**Figure 11: VCC current consumption profile versus time of the SARA-G300 and SARA-G310 modules (with the EXT32K input fed by a proper external 32 kHz signal), or the SARA-G340 and SARA-G350 modules, or the SARA-U2 modules, when registered with the network, with power saving enabled: the very low power idle-mode is reached and periodical wake up to active-mode are performed to monitor the paging channel**



Figure 12 roughly describes the current consumption profile of SARA-G300 and SARA-G310 modules when the **EXT32K** input pin is fed by the **32K\_OUT** output pin provided by these modules, when power saving is enabled. The module is registered with the network, automatically enters the low power idle-mode and periodically wakes up to active-mode to monitor the paging channel for paging block reception.



**Figure 12: VCC current consumption profile versus time of the SARA-G300 and SARA-G310 modules (with the EXT32K input pin fed by the 32K\_OUT output pin provided by these modules), when registered with the network, with power saving enabled: the low power idle-mode is reached and periodical wake up to active-mode are performed to monitor the paging channel**

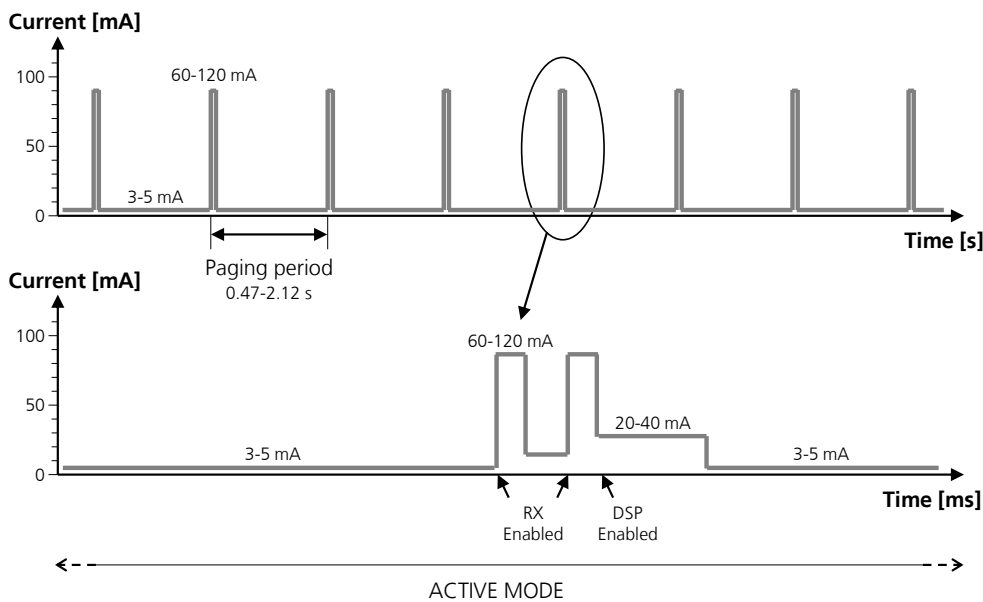
For detailed current consumption values with the module registered with 2G or 3G network with power saving enabled (cyclic idle/active-mode) see SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2].

### 1.5.1.5 VCC current consumption in fixed active-mode (power saving disabled)

Power saving configuration is by default disabled, or it can be disabled using the appropriate AT command (see u-blox AT Commands Manual [3], AT+UPSV command). When power saving is disabled, the module does not automatically enter idle-mode whenever possible: the module remains in active-mode.

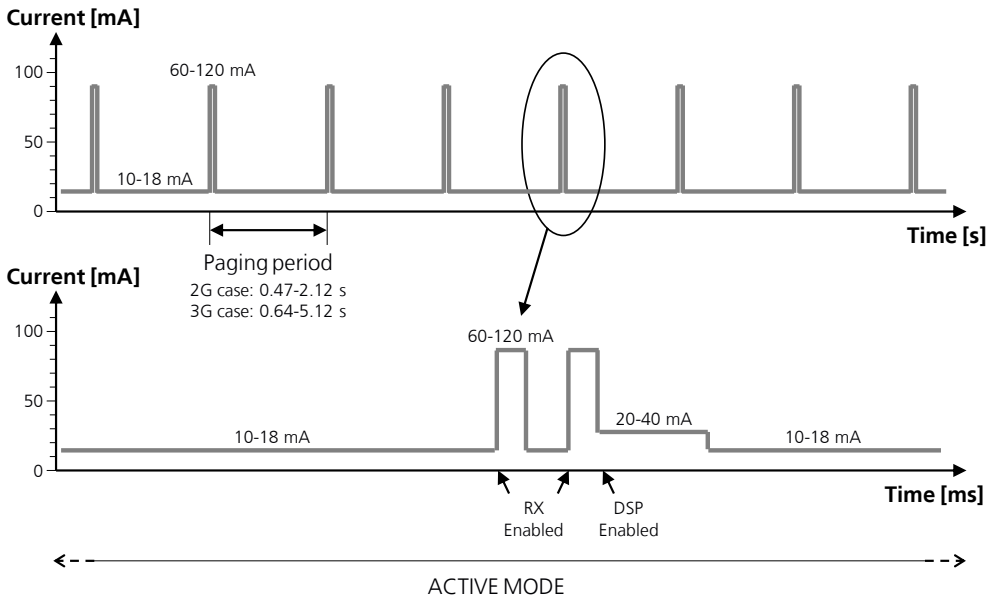
The module processor core is activated during active-mode, and the 26 MHz reference clock frequency is used.

Figure 13 roughly describes the current consumption profile of the SARA-G300 and SARA-G310 modules (when the **EXT32K** input pin is fed by external 32 kHz signal with characteristics compliant to the one specified in SARA-G3 series Data Sheet [1], or by the **32K\_OUT** output pin provided by these modules), or the SARA-G340 and SARA-G350 modules (except '00' versions), when power saving is disabled: the module is registered with the network, active-mode is maintained, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception.



**Figure 13: VCC current consumption profile versus time of the SARA-G300 and SARA-G310 modules (with the EXT32K input pin fed by proper external 32 kHz signal or by 32K\_OUT output pin), or SARA-G340 and SARA-G350 modules (except '00' versions), when registered with the network, with power saving disabled: the active-mode is always held, and the receiver and the DSP are periodically activated to monitor the paging channel**

Figure 14 roughly describes the current consumption profile of the SARA-G300 and SARA-G310 modules (when their **EXT32K** input is not fed by a signal, i.e. left unconnected), or the SARA-G340 and SARA-G350 modules ('00' versions only), or the SARA-U2 modules, when power saving is disabled: the module is registered with the network, active-mode is maintained, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception.



**Figure 14: VCC current consumption profile versus time of the SARA-G300 and SARA-G310 modules (when their EXT32K input is not fed by a signal), or the SARA-G340 and SARA-G350 modules ('00' versions only), or the SARA-U2 modules, when registered with the network, with power saving disabled: the active-mode is always held, and the receiver and the DSP are periodically activated to monitor the paging channel**

For detailed current consumption values with the module registered with 2G or 3G network with power saving disabled (fixed active-mode) see the SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2].

### 1.5.2 RTC supply input/output (V\_BCKP)

The **V\_BCKP** pin of SARA-G3 and SARA-U2 series modules connects the supply for the Real Time Clock (RTC) and Power-On internal logic. This supply domain is internally generated by a linear LDO regulator integrated in the Power Management Unit, as described in Figure 15. The output of this linear regulator is always enabled when the main voltage supply provided to the module through the **VCC** pins is within the valid operating range, with the module switched off or switched on.

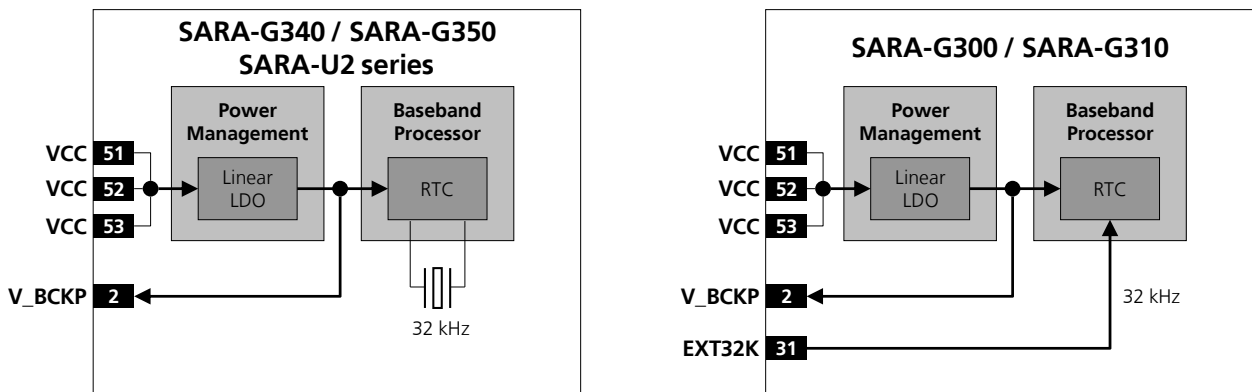


Figure 15: RTC supply input/output (V\_BCKP) and 32 kHz RTC timing reference clock simplified block diagram

The RTC provides the module time reference (date and time) that is used to set the wake-up interval during the idle-mode periods between network paging, and is able to make available the programmable alarm functions.

The RTC functions are available also in power-down mode when the **V\_BCKP** voltage is within its valid range (specified in the "Input characteristics of Supply/Power pins" table in the SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2]) and, for SARA-G300 / SARA-G310 modules only, when their **EXT32K** input pin is fed by an external 32.768 kHz signal with proper characteristics (specified in the "EXT32K pin characteristics" table in SARA-G3 series Data Sheet [1]). See the u-blox AT Commands Manual [3] for more details.

The RTC can be supplied from an external back-up battery through the **V\_BCKP**, when the main voltage supply is not provided to the module through **VCC**. This lets the time reference (date and time) run until the **V\_BCKP** voltage is within its valid range, even when the main supply is not provided to the module.

The RTC oscillator does not necessarily stop operation (i.e. the RTC counting does not necessarily stop) when **V\_BCKP** voltage value drops below the specified operating range minimum limit (1.00 V): the RTC value read after a system restart could be not reliable, as explained in Table 8.

V_BCKP voltage value	RTC value reliability	Notes
$1.00\text{ V} < V_{\text{BCKP}} < 2.40\text{ V}$	RTC oscillator does not stop operation RTC value read after a restart of the system is reliable	<b>V_BCKP</b> within operating range
$0.05\text{ V} < V_{\text{BCKP}} < 1.00\text{ V}$	RTC oscillator does not necessarily stop operation RTC value read after a restart of the system is not reliable	<b>V_BCKP</b> below operating range
$0.00\text{ V} < V_{\text{BCKP}} < 0.05\text{ V}$	RTC oscillator stops operation RTC value read after a restart of the system is reliable	<b>V_BCKP</b> below operating range

Table 8: RTC value reliability as function of V\_BCKP voltage value

Consider that the module cannot switch on if a valid voltage is not present on **VCC** even when the RTC is supplied through **V\_BCKP** (meaning that **VCC** is mandatory to switch on the module).

The RTC has very low power consumption, but is highly temperature dependent. For example at 25 °C, with the **V\_BCKP** voltage equal to the typical output value, the current consumption is approximately 2 µA (see the “Input characteristics of Supply/Power pins” table in the SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2] for the detailed specification), whereas at 70 °C and an equal voltage the current consumption increases to 5-10 µA.

If **V\_BCKP** is left unconnected and the module main voltage supply is removed from **VCC**, the RTC is supplied from the bypass capacitor mounted inside the module. However, this capacitor is not able to provide a long buffering time: within few milliseconds the voltage on **V\_BCKP** will go below the valid range (1 V min). This has no impact on cellular connectivity, as all the module functionalities do not rely on date and time setting.

### 1.5.3 Generic digital interfaces supply output (V\_INT)

The same 1.8 V voltage domain used internally to supply the generic digital interfaces of SARA-G3 and SARA-U2 series modules is also available on the **V\_INT** supply output pin, as described in Figure 16.

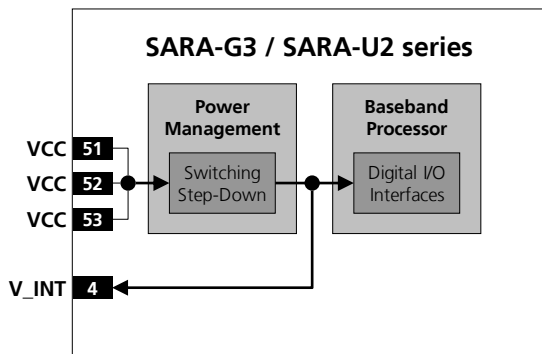


Figure 16: SARA-G3 and SARA-U2 series interfaces supply output (V\_INT) simplified block diagram

The internal regulator that generates the **V\_INT** supply is a switching step-down converter that is directly supplied from **VCC**. The voltage regulator output is set to 1.8 V (typical) when the module is switched on and it is disabled when the module is switched off.

The switching regulator operates in Pulse Width Modulation (PWM) for greater efficiency at high output loads when the module is in active-mode or in connected-mode. When the module is in low power idle-mode between paging periods and with power saving configuration enabled by the appropriate AT command, it automatically switches to Pulse Frequency Modulation (PFM) for greater efficiency at low output loads. See the u-blox AT Commands Manual [3], +UPSV command.

## 1.6 System function interfaces

### 1.6.1 Module power-on

#### 1.6.1.1 Switch-on events

Table 9 summarizes the possible switch-on events for the SARA-G3 and SARA-U2 series modules.

	SARA-G3	SARA-U2
<b>From Not-Powered Mode</b>	Applying valid <b>VCC</b> supply voltage (i.e. <b>VCC</b> rise edge), ramping from 2.5 V to 3.2 V within 4 ms	Applying valid <b>VCC</b> supply voltage (i.e. <b>VCC</b> rise edge), ramping from 2.5 V to 3.2 V within 1 ms
<b>From Power-Off Mode</b>	Low level on <b>PWR_ON</b> pin for 5 ms min.	Low pulse on <b>PWR_ON</b> pin for 50 $\mu$ s min. / 80 $\mu$ s max.
	RTC alarm programmed by AT+CALA command (Not supported by SARA-G300 / SARA-G310)	RTC alarm programmed by AT+CALA command
		<b>RESET_N</b> pin released from low level

**Table 9: Summary of SARA-G3 and SARA-U2 modules' switch-on events**

When the SARA-G3 and SARA-U2 series modules are in the not-powered mode (i.e. switched off with the **VCC** module supply not applied), they can be switched on by:

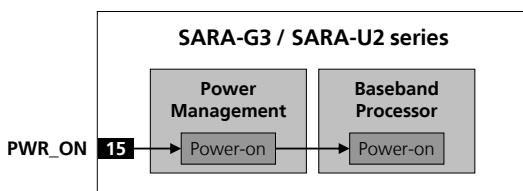
- Rising edge on the **VCC** supply input to a valid voltage for modules supply: the modules switch on applying **VCC** supply starting from a voltage value lower than 2.25 V, providing a fast **VCC** voltage slope, as it must ramp from 2.5 V to 3.2 V within 4 ms on SARA-G3 modules and within 1 ms on SARA-U2 modules, and reaching a proper nominal **VCC** voltage value within the normal operating range.
- Alternately, the **RESET\_N** pin can be held low during the **VCC** rising edge, so that the module switches on by releasing the **RESET\_N** pin when the **VCC** voltage stabilizes at its nominal value within the normal range.

The status of the **PWR\_ON** input pin of SARA-G3 and SARA-U2 series modules while applying the **VCC** module supply is not relevant: during this phase the **PWR\_ON** pin can be set high or low by the external circuit.

When the SARA-G3 and SARA-U2 series modules are in the power-off mode (i.e. switched off by means of the AT+CPWROFF command, with valid **VCC** module supply applied), they can be switched on by:

- Low level / pulse on **PWR\_ON** pin, which is normally set high by an external pull-up, for a valid time period.

As described in Figure 17, there is no internal pull-up resistor on the **PWR\_ON** pin of the modules: the pin has high input impedance and is weakly pulled high by the internal circuit. Therefore the external circuit must be able to hold the high logic level stable, e.g. providing an external pull-up resistor (for design-in see section 2.3.1). The **PWR\_ON** input voltage thresholds are different from the other generic digital interfaces of the modules: refer to SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2] for detailed electrical characteristics.



**Figure 17: PWR\_ON input description**

The SARA-G340, SARA-G350 and SARA-U2 series can be also switched on from power-off mode by:

- RTC alarm pre-programmed by AT+CALA command at specific time (see u-blox AT Commands Manual [3]).

The SARA-U2 series modules can be also switched on from power-off mode by:

- Low pulse on the **RESET\_N** pin, which is normally set high by an internal pull-up (refer to section 1.6.3 and to the SARA-U2 series Data Sheet [2] for the description of the **RESET\_N** input electrical characteristics).

### 1.6.1.2 Switch-on sequence from not-powered mode

Figure 18 shows the modules power-on sequence from the not-powered mode, describing the following phases:

- The external supply is applied to the **VCC** module supply inputs, representing the start-up event.
- The status of the **PWR\_ON** input pin while applying the **VCC** module supply is not relevant: during this phase the **PWR\_ON** pin can be set high or low by the external circuit, but in Figure 18 it is assumed that the **PWR\_ON** line rise suddenly to high logic level due to external pull-up connected to **V\_BCKP** or **VCC**.
- The **V\_BCKP** RTC supply output is suddenly enabled by the module as **VCC** reaches a valid voltage value.
- The **RESET\_N** line of SARA-U2 series rise suddenly to high logic level due to internal pull-up to **V\_BCKP**.
- All the generic digital pins of the modules are tri-stated until the switch-on of their supply source (**V\_INT**): any external signal connected to the generic digital pins must be tri-stated or set low at least until the activation of the **V\_INT** supply output to avoid latch-up of circuits and allow a proper boot of the module.
- The **V\_INT** generic digital interfaces supply output is enabled by the integrated power management unit.
- The **RESET\_N** line of SARA-G3 series rise suddenly to high logic level due to internal pull-up to **V\_INT**.
- The internal reset signal is held low by the integrated power management unit: the baseband processor core and all the digital pins of the modules are held in reset state.
- When the internal reset signal is released by the integrated power management unit, the processor core starts to configure the digital pins of the modules to each default operational state.
- The duration of this pins' configuration phase differs within generic digital interfaces (3 s typical) and the USB interface due to specific host / device enumeration timings (5 s typical, see section 1.9.3). The host application processor should not send any AT command over the AT interfaces (USB, UART) of the modules until the end of this interfaces' configuration phase to allow a proper boot of the module.
- After the interfaces' configuration phase, the application can start sending AT commands, and the following starting procedure is suggested to check the effective completion of the module internal boot sequence: send AT and wait for the response with a 30 s timeout, iterate it 4 times without resetting or removing the **VCC** supply of the module, and then run the application

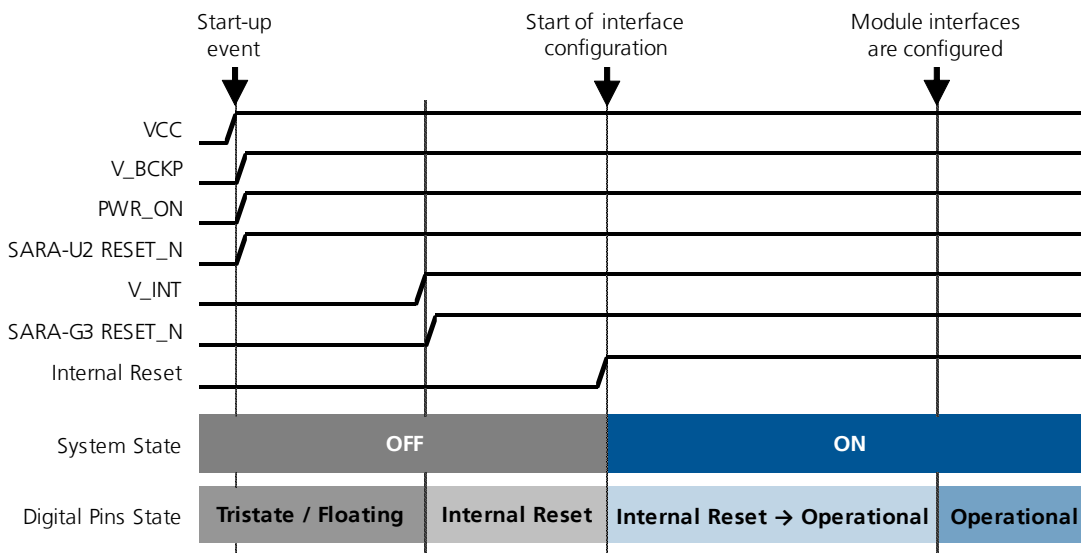


Figure 18: SARA-G3 and SARA-U2 series power-on sequence from not-powered mode



The Internal Reset signal is not available on a module pin, but the application can monitor the **V\_INT** pin to sense the start of the power-on sequence.



Before the switch-on of the generic digital interface supply source (**V\_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the modules.

### 1.6.1.3 Switch-on sequence from power-off mode

Figure 19 shows the modules power-on sequence from the power-off mode, describing the following phases:

- The external supply is still applied to the **VCC** inputs as it is assumed that the module has been previously switched off by means of the AT+CPWROFF command: the **V\_BCKP** output is internally enabled as proper **VCC** is present, the **RESET\_N** of SARA-U2 series is set to high logic level due to internal pull-up to **V\_BCKP**, the **PWR\_ON** is set to high logic level due to external pull-up connected to **V\_BCKP** or **VCC**.
- The **PWR\_ON** input pin is set low for a valid time period, representing the start-up event.
- All the generic digital pins of the modules are tri-stated until the switch-on of their supply source (**V\_INT**): any external signal connected to the generic digital pins must be tri-stated or set low at least until the activation of the **V\_INT** supply output to avoid latch-up of circuits and allow a proper boot of the module.
- The **V\_INT** generic digital interfaces supply output is enabled by the integrated power management unit.
- The **RESET\_N** line of SARA-G3 series rise suddenly to high logic level due to internal pull-up to **V\_INT**.
- The internal reset signal is held low by the integrated power management unit: the baseband processor core and all the digital pins of the modules are held in reset state.
- When the internal reset signal is released by the integrated power management unit, the processor core starts to configure the digital pins of the modules to each default operational state.
- The duration of this pins' configuration phase differs within generic digital interfaces (3 s typical) and the USB interface due to specific host / device enumeration timings (5 s typical, see section 1.9.3). The host application processor should not send any AT command over the AT interfaces (USB, UART) of the modules until the end of this interfaces' configuration phase to allow a proper boot of the module.
- After the interfaces' configuration phase, the application can start sending AT commands, and the following starting procedure is suggested to check the effective completion of the module internal boot sequence: send AT and wait for the response with a 30 s timeout, iterate it 4 times without resetting or removing the **VCC** supply of the module, and then run the application.

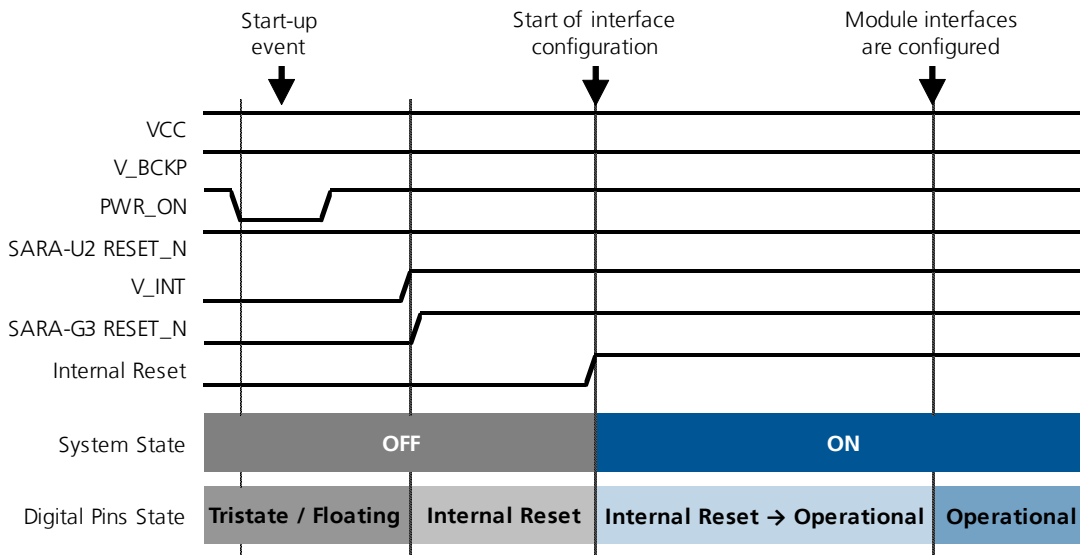


Figure 19: SARA-G3 and SARA-U2 series power-on sequence from power-off mode



The Internal Reset signal is not available on a module pin, but the application can monitor the **V\_INT** pin to sense the start of the power-on sequence.



Before the switch-on of the generic digital interface supply source (**V\_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the modules.



## 1.6.2 Module power-off

### 1.6.2.1 Switch-off events

The SARA-G3 and SARA-U2 series modules can be properly switched off by:

- AT+CPWROFF command (more details in u-blox AT Commands Manual [3]).

The SARA-U2 series modules can be properly switched off also by:

- Low pulse on the **PWR\_ON** pin, which is normally set high by an external pull-up, for a valid time period (see the SARA-U2 series Data Sheet [2] for the detailed electrical characteristics of the **PWR\_ON** input).

In both the cases listed above, the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed: these are the correct ways to switch off the modules.

An abrupt under-voltage shutdown occurs on SARA-G3 and SARA-U2 series modules when the **VCC** module supply is removed, but in this case the current parameter settings are not saved in the module's non-volatile memory and a proper network detach cannot be performed.



It is highly recommended to avoid an abrupt removal of the **VCC** supply during SARA-G3 and SARA-U2 series modules normal operations: the power off procedure must be properly started by the application, as by the AT+CPWROFF command, waiting the command response for a proper time period (see u-blox AT Commands Manual [3]), and then a proper **VCC** supply must be held at least until the end of the modules' internal power off sequence, which occurs when the generic digital interfaces supply output (**V\_INT**) is switched off by the module.

An abrupt hardware shutdown occurs on SARA-U2 modules when a low level is applied to the **RESET\_N** input. In this case, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.



It is highly recommended to avoid an abrupt hardware shutdown of the module by forcing a low level on the **RESET\_N** input pin during module normal operation: the **RESET\_N** line should be set low only if reset or shutdown via AT commands fails or if the module does not reply to a specific AT command after a time period longer than the one defined in the u-blox AT Commands Manual [3].

An over-temperature or an under-temperature shutdown occurs on SARA-G3 and SARA-U2 series modules when the temperature measured within the cellular module reaches the dangerous area, if the optional Smart Temperature Supervisor feature is enabled and configured by the dedicated AT command. For more details see section 1.13.10 and to the u-blox AT Commands Manual [3], +USTS AT command.



The Smart Temperature Supervisor feature is not supported by SARA-G300 and SARA-G310.

### 1.6.2.2 Switch-off sequence by AT+CPWROFF

Figure 20 describes the SARA-G3 and SARA-U2 series modules power-off sequence, properly started sending the AT+CPWROFF command, allowing storage of current parameter settings in the module's non-volatile memory and a proper network detach, with the following phases:

- When the +CPWROFF AT command is sent, the module starts the switch-off routine.
- The module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V\_INT**), except the RTC supply (**V\_BCKP**).
- Then, the module remains in power-off mode as long as a switch on event does not occur (e.g. applying a proper low level to the **PWR\_ON** input, or applying a proper low level to the **RESET\_N** input), and enters not-powered mode if the supply is removed from the **VCC** pins.

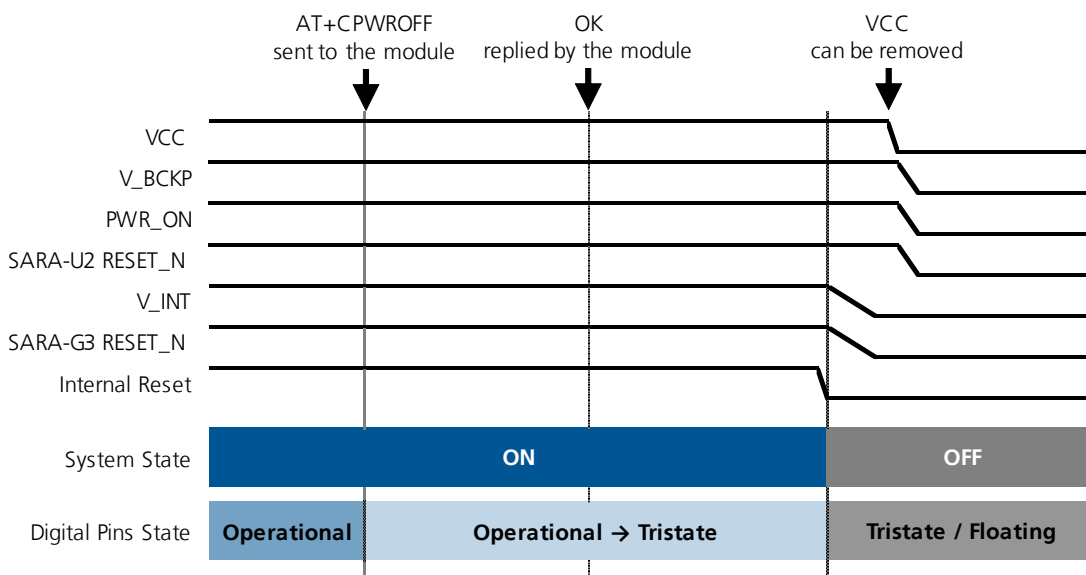


Figure 20: SARA-G3 and SARA-U2 series power-off sequence description



The Internal Reset signal is not available on a module pin, but the application can monitor the **V\_INT** pin to sense the end of the SARA-G3 and SARA-U2 series power-off sequence.



The duration of each phase in the SARA-G3 and SARA-U2 series modules' switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

### 1.6.3 Module reset

SARA-G3 and SARA-U2 series modules can be properly reset (rebooted) by:

- AT+CFUN command (see the u-blox AT Commands Manual [3] for more details).

This command causes an “internal” or “software” reset of the module, which is an asynchronous reset of the module baseband processor. The current parameter settings are saved in the module’s non-volatile memory and a proper network detach is performed: this is the proper way to reset the modules.

An abrupt hardware reset occurs on SARA-G3 and SARA-U2 series modules when a low level is applied on the **RESET\_N** input pin for a specific time period. In this case, the current parameter settings are not saved in the module’s non-volatile memory and a proper network detach is not performed.



It is highly recommended to avoid an abrupt hardware reset of the module by forcing a low level on the **RESET\_N** input during modules normal operation: the **RESET\_N** line should be set low only if reset or shutdown via AT commands fails or if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the u-blox AT Commands Manual [3].

As described in Figure 21, both the SARA-G3 and SARA-U2 series modules are equipped with an internal pull-up resistor which pulls the line to the high logic level when the **RESET\_N** pin is not forced low from the external. The pull-up is internally biased by **V\_INT** on SARA-G3 modules and is biased by **V\_BCKP** on SARA-U2 modules. A series Schottky diode is mounted inside the SARA-G3 modules, increasing the **RESET\_N** input voltage range. Refer to the SARA-G3 series Data Sheet [1] and the SARA-U2 series Data Sheet [2] for the detailed electrical characteristics of the **RESET\_N** input.

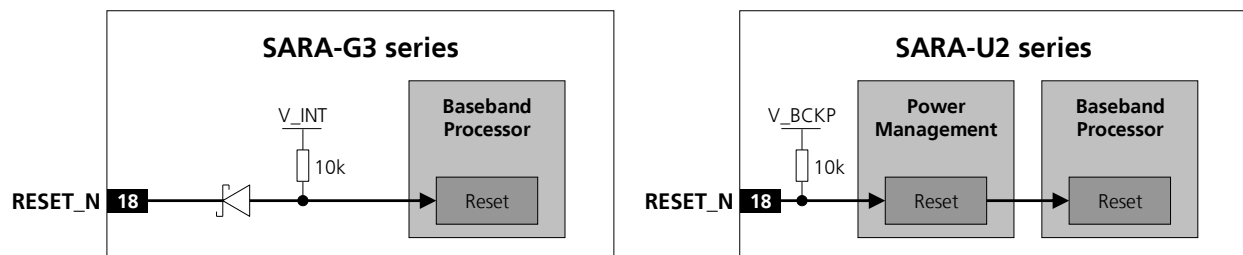


Figure 21: **RESET\_N** input description

When a low level is applied to the **RESET\_N** input, it causes an “external” or “hardware” reset of the modules, with the following behavior of SARA-G3 and SARA-U2 series modules due to different internal circuits:

- SARA-G3 modules: reset of the processor core, excluding the Power Management Unit and the RTC block. The **V\_INT** generic digital interfaces supply is switched on and each digital pin is set in its internal reset state. The **V\_BCKP** supply and the RTC block are switched on.
- SARA-U2 modules: reset of the processor core and the Power Management Unit, excluding the RTC block. The **V\_INT** generic digital interfaces supply is switched off and all digital pins are tri-stated (not supplied). The **V\_BCKP** supply and the RTC block are switched on.



Before the switch-on of the generic digital interface supply source (**V\_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the modules.



The internal reset state of all digital pins is reported in the pin description table in the SARA-G3 series Data Sheet [1] and in the SARA-U2 series Data Sheet [2].

## 1.6.4 External 32 kHz signal input (EXT32K)



The **EXT32K** pin is not available on SARA-G340, SARA-G350 and SARA-U2 series modules.

The **EXT32K** pin of SARA-G300 / SARA-G310 modules is an input pin that must be fed by a proper 32 kHz signal to make available the reference clock for the Real Time Clock (RTC) timing, used by the module processor when in the low power idle-mode.

SARA-G300 / SARA-G310 modules can enter the low power idle-mode only if a proper 32 kHz signal is provided at the **EXT32K** input pin, with power saving configuration enabled by the AT+UPSV command. In this way the different current consumption figures can be reached with the **EXT32K** input fed by the **32K\_OUT** output or by a proper external 32 kHz signal (for more details see section 1.5.1.4 and to “Current consumption” section in SARA-G3 series Data Sheet [1]).

SARA-G300 / SARA-G310 modules can provide the RTC functions (as RTC timing by AT+CCLK command and RTC alarm by AT+CALA command) only if a proper 32 kHz signal is provided at the **EXT32K** input pin. The RTC functions will be available only when the module is switched on if the **EXT32K** input is fed by the **32K\_OUT** output, or they will be available also when the module is not powered or switched off if the **EXT32K** input is fed by a proper external 32 kHz signal.

SARA-G3 series Data Sheet [1] describes the detailed electrical characteristics of the **EXT32K** input pin.

The 32 kHz reference clock for the RTC timing is automatically generated by the internal oscillator provided on the SARA-G340, SARA-G350 and SARA-U2 series modules: the same pin (31) is a reserved (**RSVD**) pin internally not connected, since an external 32 kHz signal is not needed to enter the low power idle-mode and to provide the RTC functions.

## 1.6.5 Internal 32 kHz signal output (32K\_OUT)



The **32K\_OUT** pin is not available on SARA-G340, SARA-G350 and SARA-U2 series modules.

The **32K\_OUT** pin of SARA-G300 / SARA-G310 modules is an output pin that provides a 32 kHz reference signal generated by the module, suitable only to feed the **EXT32K** input pin of SARA-G300 / SARA-G310 modules, to make available the reference clock for the Real Time Clock (RTC) timing, so that the modules can enter the low power idle-mode and can provide the RTC functions with modules switched on.

The **32K\_OUT** pin does not provide the 32 kHz output signal when the SARA-G300 / SARA-G310 modules are in power down mode: the **EXT32K** input pin must be fed by an external proper 32 kHz signal to make available the RTC functions when the modules are not powered or switched off.

SARA-G340, SARA-G350 and SARA-U2 series modules do not provide the **32K\_OUT** output, as there is no **EXT32K** input to feed on the modules: the pin 24 constitute the **GPIO3** on these modules.

## 1.7 Antenna interface

### 1.7.1 Antenna RF interface (ANT)

The **ANT** pin of SARA-G3 and SARA-U2 series modules represents the RF input/output for 2G or 3G cellular RF signals reception and transmission. The **ANT** pin has a nominal characteristic impedance of  $50\ \Omega$  and must be connected to the antenna through a  $50\ \Omega$  transmission line for proper RF signals reception and transmission.


#### 1.7.1.1 Antenna RF interface requirements

Table 10 summarizes the requirements for the antenna RF interface (**ANT**). See section 2.4.1 for suggestions to properly design an antenna circuit compliant to these requirements.

 **The antenna circuit affects the RF compliance of the device integrating SARA-G3 and SARA-U2 series module with applicable required certification schemes. Compliance is guaranteed if the antenna RF interface (ANT) requirements summarized in Table 10 are fulfilled.**

Item	Requirements	Remarks
<b>Impedance</b>	$50\ \Omega$ nominal characteristic impedance	The nominal characteristic impedance of the antenna RF connection must match the <b>ANT</b> pin $50\ \Omega$ impedance.
<b>Frequency Range</b>	See the SARA-G3 series Data Sheet [1] and the SARA-U2 series Data Sheet [2]	The required frequency range of the antenna depends on the operating bands supported by the cellular module.
<b>Return Loss</b>	$S_{11} < -10\ \text{dB}$ (VSWR $< 2:1$ ) recommended $S_{11} < -6\ \text{dB}$ (VSWR $< 3:1$ ) acceptable	The Return loss or the $S_{11}$ , as the VSWR, refers to the amount of reflected power, measuring how well the RF antenna connection matches the $50\ \Omega$ impedance. The impedance of the antenna RF termination must match as much as possible the $50\ \Omega$ impedance of the <b>ANT</b> pin over the operating frequency range, reducing as much as possible the amount of reflected power.
<b>Efficiency</b>	$> -1.5\ \text{dB}$ ( $> 70\%$ ) recommended $> -3.0\ \text{dB}$ ( $> 50\%$ ) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The efficiency needs to be enough high over the operating frequency range to comply with the Over-The-Air radiated performance requirements, as Total Radiated Power and Total Isotropic Sensitivity, specified by certification schemes
<b>Maximum Gain</b>	See section 4.2.2 for maximum gain limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the maximum gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to <b>ANT</b> pin must not exceed the values stated in section 4.2.2 to comply with regulatory agencies radiation exposure limits.
<b>Input Power</b>	$> 2\ \text{W}$ peak	The antenna connected to <b>ANT</b> pin must support the maximum power transmitted by the modules.
<b>Detection</b>	Application board with antenna detection circuit	If antenna detection is required by the custom application, proper antenna detection circuit must be implemented on the application board as described in section 2.4.2.
	Antenna assembly with built-in diagnostic circuit	If antenna detection is required by the custom application, the external antenna assembly must be provided with proper diagnostic circuit as described in section 2.4.2.

**Table 10: Summary of antenna RF interface (ANT) requirements**

 For the additional specific requirements applicable to the integration of SARA-G350 ATEX modules in applications intended for use in potentially explosive atmospheres, see section 2.14.

## 1.7.2 Antenna detection interface (ANT\_DET)



Antenna detection interface (**ANT\_DET**) is not supported by SARA-G300 and SARA-G310 modules.

The antenna detection is based on ADC measurement. The **ANT\_DET** pin is an Analog to Digital Converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by **ANT\_DET** pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. See the u-blox AT Commands Manual [3] for more details on this feature.

The **ANT\_DET** pin generates a DC current (20  $\mu$ A for 5.4 ms on SARA-G340 / SARA-G350, 10  $\mu$ A for 128  $\mu$ s on SARA-U2 modules) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.2 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

## 1.8 SIM interface

### 1.8.1 (U)SIM card interface

SARA-G3 and SARA-U2 series modules provide a high-speed SIM/ME interface, including automatic detection and configuration of the voltage required by the connected (U)SIM card or chip.

Both 1.8 V and 3 V SIM types are supported: activation and deactivation with automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The **VSIM** supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations.

The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values determined by the SIM Card.

SIM Application Toolkit is supported by all SARA-G3 and SARA-U2 series except SARA-G300 and SARA-G310.

### 1.8.2 SIM card detection interface (SIM\_DET)



Not supported by SARA-G300-00S and SARA-G310-00S modules.

The **SIM\_DET** pin is configured as an external interrupt to detect the SIM card mechanical / physical presence. The pin is configured as input with an internal active pull-down enabled, and it can sense SIM card presence only if properly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **SIM\_DET** input pin is recognized as SIM card not present
- High logic level at **SIM\_DET** input pin is recognized as SIM card present

The SIM card detection function provided by **SIM\_DET** pin is an optional feature that can be implemented / used or not according to the application requirements: an Unsolicited Result Code (URC) is generated each time that there is a change of status (for more details see the u-blox AT Commands Manual [3], "simind" value of the <descr> parameter of the +CIND and +CMER commands.

The optional function "SIM card hot insertion/removal" can be additionally enabled on the SARA-U2 modules' **SIM\_DET** pin by AT commands (see section 1.11 and u-blox AT Commands Manual [3], +UGPIOC, +UDCONF).

## 1.9 Serial interfaces

SARA-G3 and SARA-U2 series modules provide the following serial communication interfaces:

- UART interface: 9-wire unbalanced 1.8 V asynchronous serial interface available for AT commands, data communication, FW upgrades by means of the FOAT feature (see 1.9.1)
- Auxiliary UART interface (not supported by SARA-U2 series): 3-wire unbalanced 1.8 V asynchronous serial interface available for FW upgrades by means of the u-blox EasyFlash tool and for diagnostic (see 1.9.2)
- USB interface (not supported by SARA-G3 series): High-Speed USB 2.0 compliant interface available for AT commands, data communication, FW upgrades by means of the FOAT feature, FW upgrades by means of the u-blox EasyFlash tool and for diagnostic (see 1.9.3)
- DDC interface (not supported by SARA-G300 / SARA-G310): I<sup>2</sup>C compatible 1.8 V interface available for the communication with u-blox positioning chips / modules and additionally, except for SARA-G3 series, with other external I<sup>2</sup>C devices as an audio codec (see 1.9.4)

### 1.9.1 Asynchronous serial interface (UART)

#### 1.9.1.1 UART features

The UART interface is a 9-wire 1.8 V unbalanced asynchronous serial interface available for AT commands and for packet-switched / circuit-switched data communication on all the SARA-G3 and SARA-U2 series modules.

The UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation (more details available in ITU Recommendation [10]), with CMOS compatible signal levels: 0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state. For detailed electrical characteristics see SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2].

SARA-G3 and SARA-U2 series modules are designed to operate as a 2G or 3G cellular modem, which represents the Data Circuit-terminating Equipment (DCE) according to the ITU-T V.24 Recommendation [10]. The application processor connected to the module through the UART interface represents the Data Terminal Equipment (DTE).



The signal names of SARA-G3 and SARA-U2 series modules' UART interface conform to the ITU-T V.24 Recommendation [10]: e.g. the **TXD** line represents the data transmitted by the DTE (application processor data line output) and received by the DCE (module data line input).

All flow control handshakes are supported by the UART interface and can be set by appropriate AT commands (see u-blox AT Commands Manual [3], &K, +IFC, \Q AT commands): hardware flow control (RTS/CTS), software flow control (XON/XOFF), or none flow control.



Hardware flow control is enabled by default.

SARA-G3 modules support the autobauding: the baud rate automatic detection is performed each time the DTE sends AT commands. After the detection the module works at the detected baud rate and the baud rate can be runtime changed by the DTE or by AT command (see u-blox AT Commands Manual [3], +IPR command).

SARA-U2 modules support only the one-shot autobauding: the baud rate automatic detection is performed only once, at module start up. After the detection the module works at the detected baud rate and the baud rate can only be changed by AT command (see u-blox AT Commands Manual [3], +IPR command).



SARA-G3 modules' autobauding and SARA-U2 modules' one-shot autobauding are enabled by default.

The following baud rates can be configured by AT command (see u-blox AT Commands Manual [3], +IPR):

- 1200 b/s
- 2400 b/s
- 4800 b/s
- 9600 b/s
- 19200 b/s
- 38400 b/s
- 57600 b/s
- 115200 b/s, default value when the autobauding or the one-shot autobauding are disabled
- 230400 b/s
- 460800 b/s
- 921600 b/s

- 460800 b/s and 921600 b/s baud rates are not supported by SARA-G3 series modules.
- 1200 b/s and 230400 b/s baud rates cannot be automatically detected by SARA-G3 series modules.
- 460800 b/s and 921600 b/s baud rates cannot be automatically detected by SARA-U2 series modules.

SARA-G3 modules support the automatic frame recognition in conjunction with autobauding.

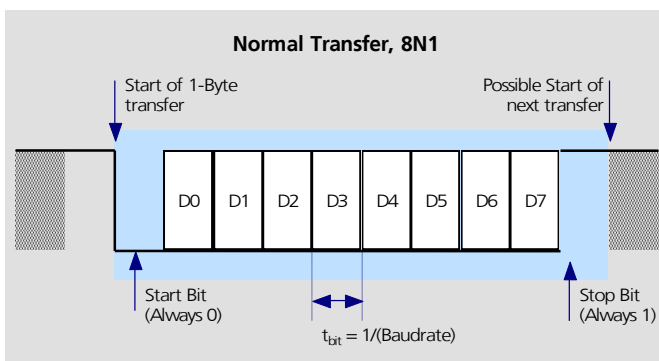
SARA-U2 modules support the one-shot automatic frame recognition in conjunction with one-shot autobauding.

- SARA-G3 series modules' automatic frame recognition and SARA-U2 series modules' one-shot automatic frame recognition are enabled by default, as autobauding and one-shot autobauding.

The following frame formats can be configured by AT command (see u-blox AT Commands Manual [3], +ICF):

- 8N1 (8 data bits, No parity, 1 stop bit), default frame configuration with fixed baud rate
- 8E1 (8 data bits, even parity, 1 stop bit)
- 8O1 (8 data bits, odd parity, 1 stop bit)
- 8N2 (8 data bits, No parity, 2 stop bits)
- 7E1 (7 data bits, even parity, 1 stop bit)
- 7O1 (7 data bits, odd parity, 1 stop bit)

Figure 22 describes the 8N1 frame format, which is the default configuration with fixed baud rate.



**Figure 22: Description of UART default frame format (8N1) with fixed baud rate**



The module firmware can be updated over the UART interface by means of:

- the Firmware upgrade Over AT (FOAT) feature, on all the SARA-G3 and SARA-U2 series modules
- the u-blox EasyFlash tool, on SARA-U2 series modules only

For more details on FW upgrade procedures see section 1.13 and Firmware update application note [25].

### 1.9.1.2 UART AT interface configuration

The UART interface of SARA-G3 and SARA-U2 series modules is available as AT command interface with the default configuration described in Table 11 (for more details and information about further settings, see the u-blox AT Commands Manual [3]).

Interface	AT Settings	Comments
UART interface	AT interface: enabled	AT command interface is enabled by default on the UART physical interface
	AT+IPR=0	Automatic baud rate detection enabled by default on SARA-G3 series One-shot automatic baud rate detection enabled by default on SARA-U2 series
	AT+ICF=0	Automatic frame format recognition enabled by default on SARA-G3 series One-shot automatic frame format recognition enabled by default on SARA-U2 series
	AT&K3	HW flow control enabled by default
	AT&S1	DSR line set ON in data mode <sup>8</sup> and set OFF in command mode <sup>8</sup>
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command mode <sup>8</sup> and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
	MUX protocol: disabled	Multiplexing mode is disabled by default and it can be enabled by AT+CMUX command. The following virtual channels are defined: <ul style="list-style-type: none"> <li>• Channel 0: control channel</li> <li>• Channel 1: AT and Data</li> <li>• Channel 2: AT and Data</li> <li>• Channel 3: AT and Data (not available on SARA-G300 / SARA-G310 modules)</li> <li>• Channel 4: AT and Data (not available on SARA-G300 / SARA-G310 modules)</li> <li>• Channel 5: AT and Data (not available on SARA-G300 / SARA-G310 modules)</li> <li>• Channel 6: GNSS tunneling (not available on SARA-G300 / SARA-G310 modules)</li> <li>• Channel 7: SIM Access Profile (not available on SARA-G3 series modules)</li> </ul>

**Table 11: Default UART AT interface configuration**

<sup>8</sup> Refer to the u-blox AT Commands Manual [3] for the definition of the interface data mode, command mode and online command mode.

### 1.9.1.3 UART signal behavior

At the module switch-on, before the UART interface initialization (as described in the power-on sequence reported in Figure 18 or Figure 19), each pin is first tri-stated and then is set to its related internal reset state<sup>9</sup>. At the end of the boot sequence, the UART interface is initialized, the module is by default in active-mode, and the UART interface is enabled as AT commands interface.

The configuration and the behavior of the UART signals after the boot sequence are described below. See section 1.4 for definition and description of module operating modes referred to in this section.

#### RXD signal behavior

The module data output line (**RXD**) is set by default to the OFF state (high level) at UART initialization. The module holds **RXD** in the OFF state until the module does not transmit some data.

#### TXD signal behavior

The module data input line (**TXD**) is set by default to the OFF state (high level) at UART initialization. The **TXD** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **TXD** input.

#### CTS signal behavior

The module hardware flow control output (**CTS** line) is set to the ON state (low level) at UART initialization.

If the hardware flow control is enabled, as it is by default, the **CTS** line indicates when the UART interface is enabled (data can be sent and received). The module drives the **CTS** line to the ON state or to the OFF state when it is either able or not able to accept data from the DTE over the UART (see 1.9.1.4 for more details).



If hardware flow control is enabled, then when the **CTS** line is OFF it does not necessarily mean that the module is in low power idle-mode, but only that the UART is not enabled, as the module could be forced to stay in active-mode for other activities, e.g. related to the network or related to other interfaces.



When the multiplexer protocol is active, the **CTS** line state is mapped to FCon / FCOFF MUX command for flow control issues outside the power saving configuration while the physical **CTS** line is still used as a power state indicator. For more details, see Mux Implementation Application Note [23].

The **CTS** hardware flow control setting can be changed by AT commands (for more details, see u-blox AT Commands Manual [3], AT&K, ATQ, AT+IFC AT command).

If the hardware flow control is not enabled, the **CTS** line after the UART initialization behaves as following:

- on SARA-U2 modules the **CTS** line is always held in the ON state
- on SARA-G3 modules the **CTS** line is set in the ON or OFF state accordingly to the power saving state as illustrated in Figure 25 if AT+UPSV=2 is set, and the **CTS** line is held in the ON state otherwise



When the power saving configuration is enabled and the hardware flow-control is not implemented in the DTE/DCE connection, data sent by the DTE can be lost: the first character sent when the module is in the low power idle-mode will not be a valid communication character (see 1.9.1.4 for more details).

<sup>9</sup> Refer to the pin description table in the SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2].

### RTS signal behavior

The hardware flow control input (**RTS** line) is set by default to the OFF state (high level) at UART initialization. The module then holds the **RTS** line in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **RTS** input.

If the HW flow control is enabled, as it is by default, the module monitors the **RTS** line to detect permission from the DTE to send data to the DTE itself. If the **RTS** line is set to the OFF state, any on-going data transmission from the module is interrupted until the subsequent **RTS** line change to the ON state.



The DTE must still be able to accept a certain number of characters after the **RTS** line is set to the OFF state: the module guarantees the transmission interruption within two characters from **RTS** state change.

Module behavior according to **RTS** hardware flow control status can be configured by AT commands (for more details, see u-blox AT Commands Manual [3], AT&K, AT\Q, AT+IFC command descriptions).

If AT+UPSV=2 is set and HW flow control is disabled, the module monitors the **RTS** line to manage the power saving configuration:

- When an OFF-to-ON transition occurs on the **RTS** input line, the UART is enabled and the module wakes up to active-mode: after ~20 ms from the OFF-to-ON transition the UART / module wake up is completed and data can be received without loss. The module cannot enter the low power idle-mode and the UART is kept enabled as long as the **RTS** input line is held in the ON state
- If the **RTS** input line is set to the OFF state by the DTE, the UART is disabled (held in low power mode) and the module automatically enters low power idle-mode whenever possible

For more details, see section 1.9.1.4 and u-blox AT Commands Manual [3], AT+UPSV command.

### DSR signal behavior

If AT&S1 is set, as it is by default, the **DSR** module output line is set by default to the OFF state (high level) at UART initialization. The **DSR** line is then set to the OFF state when the module is in command mode or in online command mode and is set to the ON state when the module is in data mode (see the u-blox AT Commands Manual [3] for the definition of the interface data mode, command mode and online command mode).

If AT&S0 is set, the **DSR** module output line is set by default to the ON state (low level) at UART initialization and is then always held in the ON state.

### DTR signal behavior

The **DTR** module input line is set by default to the OFF state (high level) at UART initialization. The module then holds the **DTR** line in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **DTR** input.

Module behavior according to **DTR** status can be changed by AT command (for more details, see u-blox AT Commands Manual [3], AT&D command description).

If AT+UPSV=3 is set, the **DTR** line is monitored by the module to manage the power saving configuration:

- When an OFF-to-ON transition occurs on the **DTR** input line, the UART is enabled and the module wakes up to active-mode: after ~20 ms from the OFF-to-ON transition the UART / module wake up is completed and data can be received without loss. The module cannot enter the low power idle-mode and the UART is kept enabled as long as the **DTR** input line is held in the ON state
- If the **DTR** input line is set to the OFF state by the DTE, the UART is disabled (held in low power mode) and the module automatically enters low power idle-mode whenever possible

For more details, see section 1.9.1.4 and u-blox AT Commands Manual [3], AT+UPSV command.



AT+UPSV=3 power saving configuration control by the **DTR** input is not supported by SARA-G3 modules.

## DCD signal behavior

If AT&C1 is set, as it is by default, the **DCD** module output line is set by default to the OFF state (high level) at UART initialization. The module then sets the **DCD** line according to the carrier detect status: ON if the carrier is detected, OFF otherwise. For voice calls, **DCD** is set to the ON state when the call is established. For a data call there are the following scenarios (see the u-blox AT Commands Manual [3] for the definition of the interface data mode, command mode and online command mode):

- **Packet Switched Data call:** Before activating the PPP protocol (data mode) a dial-up application must provide the ATD\*99\*\*\*<context\_number># to the module: with this command the module switches from command mode to data mode and can accept PPP packets. The module sets the **DCD** line to the ON state, then answers with a CONNECT to confirm the ATD\*99 command. The **DCD** ON is not related to the context activation but with the data mode
- **Circuit Switched Data call:** To establish a data call, the DTE can send the ATD<number> command to the module which sets an outgoing data call to a remote modem (or another data module). Data can be transparent (non reliable) or non transparent (with the reliable RLP protocol). When the remote DCE accepts the data call, the module **DCD** line is set to ON and the CONNECT <communication baudrate> string is returned by the module. At this stage the DTE can send characters through the serial line to the data module which sends them through the network to the remote DCE attached to a remote DTE



The **DCD** is set to ON during the execution of the +CMGS, +CMGW, +USOWR, +USODL AT commands requiring input data from the DTE: the **DCD** line is set to the ON state as soon as the switch to binary/text input mode is completed and the prompt is issued; **DCD** line is set to OFF as soon as the input mode is interrupted or completed (for more details see the u-blox AT Commands Manual [3]).



The **DCD** line is kept in the ON state, even during the online command mode, to indicate that the data call is still established even if suspended, while if the module enters command mode, the **DSR** line is set to the OFF state. For more details see **DSR** signal behavior description.



For scenarios when the **DCD** line setting is requested for different reasons (e.g. SMS texting during online command mode), the **DCD** line changes to guarantee the correct behavior for all the scenarios. For instance, in case of SMS texting in online command mode, if the data call is released, the **DCD** line is kept to ON till the SMS command execution is completed (even if the data call release would request the **DCD** setting to OFF).

If AT&C0 is set, the **DCD** module output line is set by default to the ON state (low level) at UART initialization and is then always held in the ON state.

## RI signal behavior

The **RI** module output line is set by default to the OFF state (high level) at UART initialization. Then, during an incoming call, the **RI** line is switched from the OFF state to the ON state with a 4:1 duty cycle and a 5 s period (ON for 1 s, OFF for 4 s, see Figure 23), until the DTE attached to the module sends the ATA string and the module accepts the incoming data call. The RING string sent by the module (DCE) to the serial port at constant time intervals is not correlated with the switch of the **RI** line to the ON state.

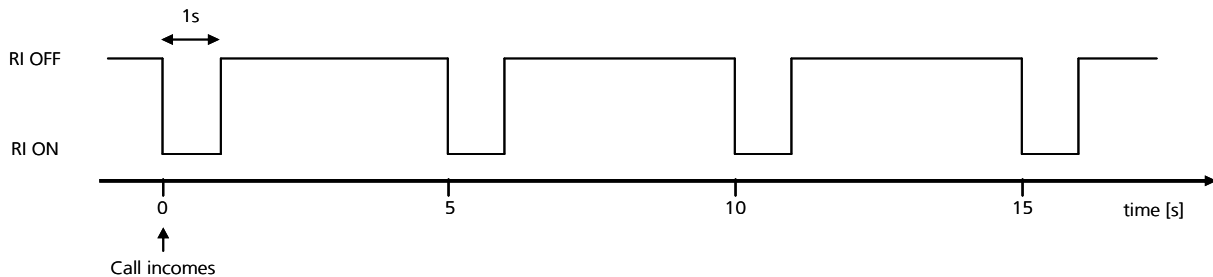


Figure 23: RI behavior during an incoming call

The **RI** line can notify an SMS arrival. When the SMS arrives, the **RI** line switches from OFF to ON for 1 s (see Figure 24), if the feature is enabled by the AT+CNMI command (see the u-blox AT Commands Manual [3]).

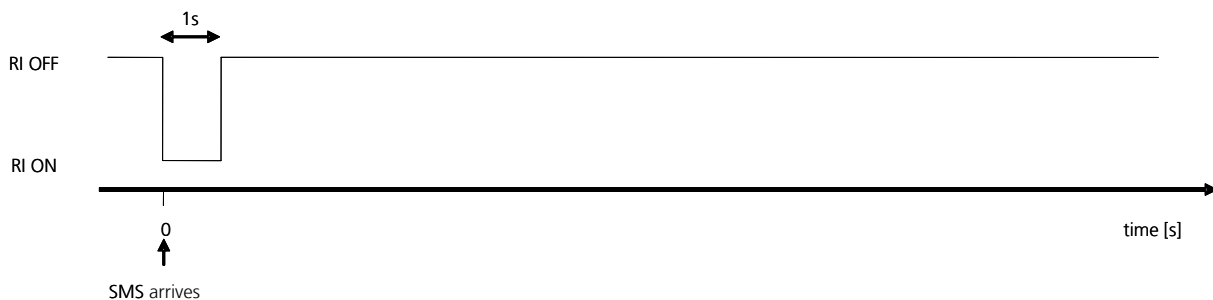


Figure 24: RI behavior at SMS arrival

This behavior allows the DTE to stay in power saving mode until the DCE related event requests service.

For SMS arrival, if several events coincidentally occur or in quick succession each event independently triggers the **RI** line, although the line will not be deactivated between each event. As a result, the **RI** line may stay to ON for more than 1 s.

If an incoming call is answered within less than 1 s (with ATA or if auto-answering is set to ATSO=1) than the **RI** line is set to OFF earlier.

As a result:

- RI** line monitoring cannot be used by the DTE to determine the number of received SMSes.
- For multiple events (incoming call plus SMS received), the **RI** line cannot be used to discriminate the two events, but the DTE must rely on the subsequent URCs and interrogate the DCE with proper commands.

The **RI** line can additionally notify all the URCs and all the incoming data (PPP, Direct Link, sockets, FTP), if the feature is enabled by the AT+URING command (for more details see u-blox AT Commands Manual [3]): the **RI** line is asserted when one of the configured events occur and it remains asserted for 1 s unless another configured event will happen, with the same behavior described in Figure 24.

- The AT+URING command for the notification of all the URCs and all the incoming data (PPP, Direct Link, sockets, FTP) over the **RI** line output is not supported by SARA-G3 modules.

### 1.9.1.4 UART and power-saving

The power saving configuration is controlled by the AT+UPSV command (for the complete description, see u-blox AT Commands Manual [3]). When power saving is enabled, the module automatically enters low power idle-mode whenever possible, and otherwise the active-mode is maintained by the module (see section 1.4 for definition and description of module operating modes referred to in this section).

The AT+UPSV command configures both the module power saving and also the UART behavior in relation to the power saving. The conditions for the module entering idle-mode also depend on the UART power saving configuration.

Three different power saving configurations can be set by the AT+UPSV command:

- AT+UPSV=0, power saving disabled: module forced on active-mode and UART interface enabled (default)
- AT+UPSV=1, power saving enabled: module cyclic active / idle-mode and UART enabled / disabled
- AT+UPSV=2, power saving enabled and controlled by the UART **RTS** input line
- AT+UPSV=3, power saving enabled and controlled by the UART **DTR** input line



The AT+UPSV=3 power saving configuration is not supported by SARA-G3 modules.

The different power saving configurations that can be set by the +UPSV AT command are described in details in the following subsections. Table 12 summarizes the UART interface communication process in the different power saving configurations, in relation with HW flow control settings and **RTS** input line status. For more details on the +UPSV AT command description, refer to u-blox AT commands Manual [3].

AT+UPSV	HW flow control	RTS line	DTR line	Communication during idle-mode and wake up
0	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module is correctly received by the DTE.
0	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE should be buffered by the DTE and will be correctly received by the module when RTS is set to ON. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. <b>RTS</b> line will be ON).
0	Disabled (AT&K0)	ON or OFF	ON or OFF	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
1	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE should be buffered by the DTE and will be correctly received by the module when active-mode is entered. Data sent by the module is correctly received by the DTE.
1	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE should be buffered by the DTE and will be correctly received by the module when active-mode is entered. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. <b>RTS</b> line will be ON).
1	Disabled (AT&K0)	ON or OFF	ON or OFF	The first character sent by the DTE is lost, but after ~20 ms the UART and the module are waked up: recognition of subsequent characters is guaranteed after the complete UART / module wake-up. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
2	Enabled (AT&K3)	ON or OFF	ON or OFF	Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Disabled (AT&K0)	ON	ON or OFF	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
2	Disabled (AT&K0)	OFF	ON or OFF	Data sent by the DTE is lost by SARA-U2 modules. The first character sent by the DTE is lost by SARA-G3 modules, but after ~20 ms the UART and the module are waked up: recognition of subsequent characters is guaranteed after the complete UART / module wake-up. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.

AT+UPSV	HW flow control	RTS line	DTR line	Communication during idle-mode and wake up
3	Enabled (AT&K3)	ON	ON	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE.
3	Enabled (AT&K3)	ON	OFF	Data sent by the DTE is lost by the module. Data sent by the module is correctly received by the DTE.
3	Enabled (AT&K3)	OFF	ON	Data sent by the DTE is correctly received by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. <b>RTS</b> line will be ON).
3	Enabled (AT&K3)	OFF	OFF	Data sent by the DTE is lost by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. <b>RTS</b> line will be ON).
3	Disabled (AT&K0)	ON or OFF	ON	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data are lost.
3	Disabled (AT&K0)	ON or OFF	OFF	Data sent by the DTE is lost by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data are lost.

**Table 12: UART and power-saving summary**

### AT+UPSV=0: power saving disabled, fixed active-mode

The module does not enter idle-mode and the UART interface is enabled (data can be sent and received): the **CTS** line is always held in the ON state after UART initialization. This is the default configuration.

### AT+UPSV=1: power saving enabled, cyclic idle/active-mode

On SARA-G3 modules, when the AT+UPSV=1 command is issued by the DTE, the UART is disabled after the timeout set by the second parameter of the +UPSV AT command (for more details see u-blox AT commands Manual [3]).

On SARA-U2 modules, when the AT+UPSV=1 command is issued by the DTE, the UART is immediately disabled. Afterwards, the UART of SARA-G3 and SARA-U2 series modules is periodically enabled to receive or send data and, if data has not been received or sent over the UART, the interface is automatically disabled whenever possible according to the timeout configured by the second parameter of the +UPSV AT command.

The module automatically enters the low power idle-mode whenever possible but it wakes up to active-mode according to the UART periodic wake up so that the module cyclically enters the low power idle-mode and the active-mode. Additionally, the module wakes up to active-mode according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The UART is enabled, and the module does not enter low power idle-mode, in the following cases:

- During the periodic UART wake up to receive or send data
- If the module needs to transmit some data over the UART (e.g. URC)
- On SARA-G3 modules, during a CSD data call and a PSD data call with external context activation
- On SARA-G3 modules, during a voice call
- If a character is sent by the DTE with HW flow control disabled, the first character sent causes the system wake-up due to the “wake up via data reception” feature described in the following subsection, and the UART will be then kept enabled after the last data received according to the timeout set by the second parameter of the AT+UPSV=1 command

The module, outside an active call, periodically wakes up from idle-mode to active-mode to monitor the paging channel of the current base station (paging block reception), according to 2G or 3G discontinuous reception (DRX) specification.

The time period between two paging receptions is defined by the current base station (i.e. by the network):

- If the module is registered with a 2G network, the paging reception period can vary from ~0.47 s (DRX = 2, i.e. 2 x 51 2G-frames) up to ~2.12 s (DRX = 9, i.e. 9 x 51 2G-frames)
- If the module is registered with a 3G network, the paging reception period can vary from 0.64 s (DRX = 6, i.e. 2<sup>6</sup> 3G-frames) up to 5.12 s (DRX = 9, i.e. 2<sup>9</sup> 3G-frames)

The time period of the UART enable/disable cycle is configured differently when the module is registered with a 2G network compared to when the module is registered with a 3G network:

- 2G: the UART is synchronously enabled to every paging reception on SARA-G3 modules, whereas the UART is not necessarily enabled at every paging reception on SARA-U2 modules: the UART is enabled concurrently to a paging reception, and then, as data has not been received or sent, the UART is disabled until the first paging reception that occurs after a timeout of 2.0 s, and therefore the interface is enabled again
- 3G: the UART is asynchronously enabled to paging receptions, as the UART is enabled for ~20 ms, and then, if data are not received or sent, the UART is disabled for 2.5 s, and afterwards the interface is enabled again
- Not registered: when a module is not registered with a network, the UART is enabled for ~20 ms, and then, if data has not been received or sent, the UART is disabled for ~2.1 s on SARA-G3 modules or for 2.5 s on SARA-U2 modules, and afterwards the interface is enabled again

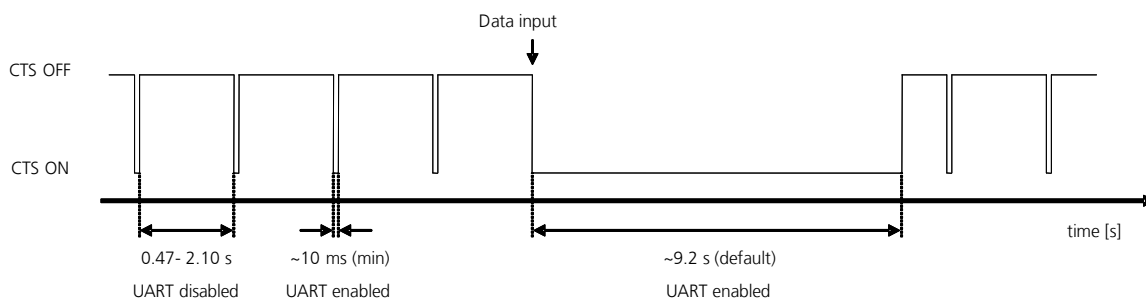
The module active-mode duration outside an active call depends on:

- Network parameters, related to the time interval for the paging block reception (minimum of ~11 ms)
- Duration of UART enable time in absence of data reception (~20 ms)
- The time period from the last data received at the serial port during the active-mode: the module does not enter idle-mode until a timeout expires. The second parameter of the +UPSV AT command configures this timeout, from 40 2G-frames (i.e. 40 x 4.615 ms = 184 ms) up to 65000 2G-frames (i.e. 65000 x 4.615 ms = 300 s). Default value is 2000 2G-frames (i.e. 2000 x 4.615 ms = 9.2 s)

The active-mode duration can be extended indefinitely since every subsequent character received during the active-mode, resets and restarts the timer.

The timeout is ignored only by SARA-U2 modules immediately after AT+UPSV=1 has been sent, so that the UART interface is disabled and the module may enter idle-mode immediately after the AT+UPSV=1 is sent

The hardware flow-control output (**CTS** line) indicates when the UART interface is enabled (data can be sent and received over the UART), if HW flow control is enabled, as illustrated in Figure 25.



**Figure 25: CTS behavior with power saving enabled (AT+UPSV=1) and HW flow control enabled: the CTS output line indicates when the UART interface of the module is enabled (CTS = ON = low level) or disabled (CTS = OFF = high level)**



### AT+UPSV=2: power saving enabled and controlled by the RTS line

This configuration can only be enabled with the module hardware flow control disabled by AT&K0 command.

The UART interface is immediately disabled after the DTE sets the **RTS** line to OFF.

Then, the module automatically enters idle-mode whenever possible according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The UART is disabled as long as the **RTS** line is held to OFF, but the UART is enabled in the following cases:

- If the module needs to transmit some data over the UART (e.g. URC)
- On SARA-G3 modules, during a CSD data call and a PSD data call with external context activation
- On SARA-G3 modules, during a voice call
- On SARA-G3 modules, if a data is sent by the DTE, it causes the system wake-up due to the “wake up via data reception” feature described in the following subsection, and the UART will be then kept enabled after the last data received according to the timeout previously set with the AT+UPSV=1 configuration

When an OFF-to-ON transition occurs on the **RTS** input line, the UART is re-enabled and the module, if it was in idle-mode, switches from idle to active-mode after ~20 ms: this is the UART and module “wake up time”.

If the **RTS** line is set to ON by the DTE the module is not allowed to enter the low power idle-mode and the UART is kept enabled.



On SARA-G3 modules, the **CTS** output line indicates the power saving state as illustrated in Figure 25, even with AT+UPSV=2.

### AT+UPSV=3: power saving enabled and controlled by the DTR line



The AT+UPSV=3 power saving configuration is not supported by SARA-G3 modules.

The AT+UPSV=3 configuration can be enabled regardless the flow control setting on UART. In particular, the HW flow control can be enabled (AT&K3) or disabled (AT&K0) on UART during this configuration.

The UART interface is immediately disabled after the DTE sets the **DTR** line to OFF.

Then, the module automatically enters idle-mode whenever possible according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The UART is disabled as long as the **DTR** line is set to OFF, but the UART is enabled in the following cases:

- If the module needs to transmit some data over the UART (e.g. URC)

When an OFF-to-ON transition occurs on the **DTR** input line, the UART is re-enabled and the module, if it was in idle-mode, switches from idle to active mode after 20 ms: this is the UART and module “wake up time”.

If the **DTR** line is set to ON by the DTE, the module is not allowed to enter idle-mode and the UART is kept enabled until the **DTR** line is set to OFF.

When the AT+UPSV=3 configuration is enabled, the **DTR** input line can still be used by the DTE to control the module behavior according to AT&D command configuration (see u-blox AT Commands Manual [3]).



The **CTS** output line indicates the UART power saving state as illustrated in Figure 25, if HW flow control is enabled with AT+UPSV=3.

### Wake up via data reception

The UART wake up via data reception consists of a special configuration of the module **TXD** input line that causes the system wake-up when a low-to-high transition occurs on the **TXD** input line. In particular, the UART is enabled and the module switches from the low power idle-mode to active-mode within ~20 ms from the first character received: this is the system “wake up time”.

As a consequence, the first character sent by the DTE when UART is disabled (i.e. the wake up character) is not a valid communication character even if the wake up via data reception configuration is active, because it cannot be recognized, and the recognition of the subsequent characters is guaranteed only after the complete system wake-up (i.e. after ~20 ms).

The UART wake up via data reception configuration is active in the following cases:

- On SARA-G3 series, the **TXD** input line is configured to wake up the system via data reception if:
  - AT+UPSV=1 is set with HW flow control disabled
  - AT+UPSV=2 is set with HW flow control disabled, and the **RTS** line is set OFF
- On SARA-U2 series, the **TXD** input line is configured to wake up the system via data reception only if
  - AT+UPSV=1 is set with hardware flow control disabled



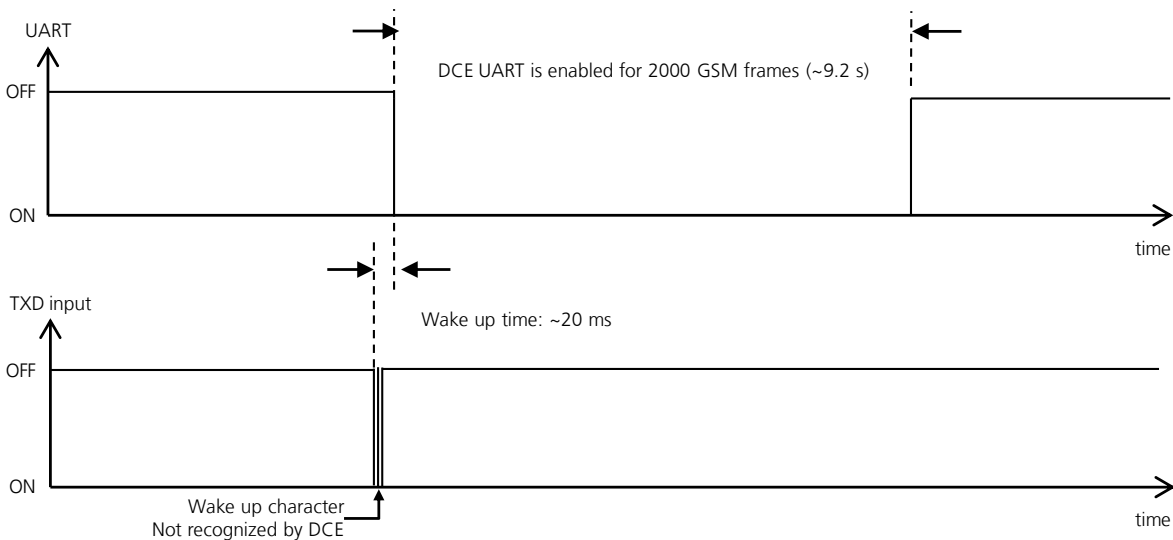
On SARA-U2 series, the UART wake up via data reception configuration is not active on the **TXD** input, and therefore all the data sent by the DTE is lost, if:

- AT+UPSV=2 is set with HW flow control disabled, and the **RTS** line is set OFF
- AT+UPSV=3 is set, regardless HW flow control setting, and the **DTR** line is set OFF

Figure 26 and Figure 27 show examples of common scenarios and timing constraints:

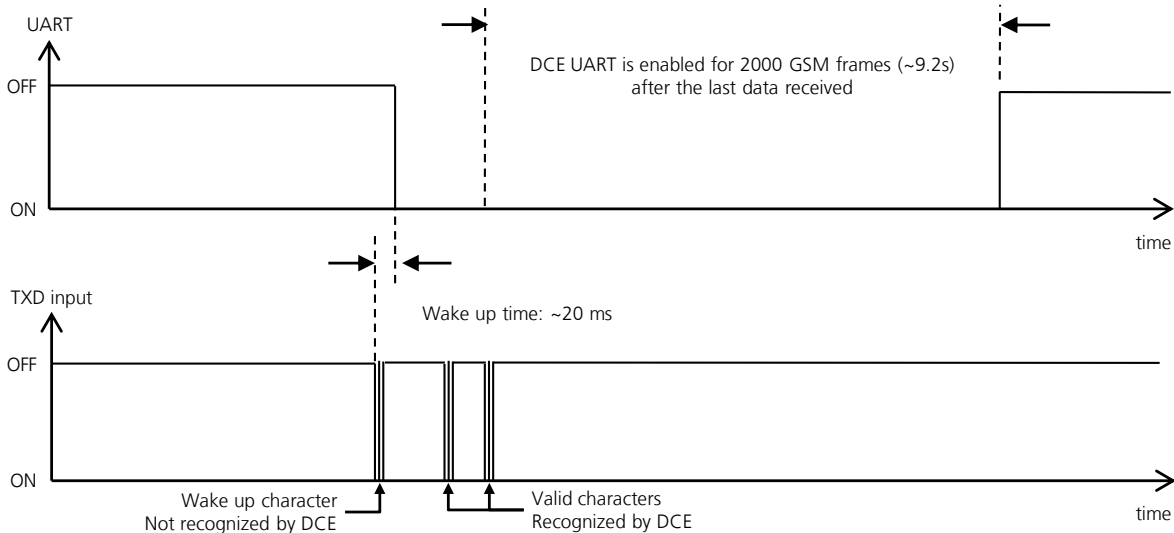
- AT+UPSV=1 power saving configuration is active and the timeout from last data received to idle-mode start is set to 2000 frames (AT+UPSV=1,2000)
- Hardware flow control is disabled

Figure 26 shows the case where the module UART is disabled and only a wake-up is forced. In this scenario the only character sent by the DTE is the wake-up character; as a consequence, the DCE module UART is disabled when the timeout from last data received expires (2000 frames without data reception, as the default case).



**Figure 26: Wake-up via data reception without further communication**

Figure 27 shows the case where in addition to the wake-up character further (valid) characters are sent. The wake up character wakes-up the module UART. The other characters must be sent after the “wake up time” of ~20 ms. If this condition is satisfied, the module (DCE) recognizes characters. The module will disable the UART after 2000 GSM frames from the latest data reception.



**Figure 27: Wake-up via data reception with further communication**



The “wake-up via data reception” feature cannot be disabled.



In command mode<sup>10</sup>, if autobauding is enabled and the DTE does not implement HW flow control, the DTE must always send a character to the module before the “AT” prefix set at the beginning of each command line: the first character is ignored if the module is in active-mode, or it represents the wake-up character if the module is in idle-mode.



In command mode<sup>10</sup>, if autobauding is disabled, the DTE must always send a dummy “AT” before each command line: the first character is not ignored if the module is in active-mode (i.e. the module replies “OK”), or it represents the wake up character if the module is in low power idle-mode (i.e. the module does not reply).



No wake-up character or dummy “AT” is required from the DTE during a voice or data call since the module UART interface continues to be enabled and does not need to be woken-up. Furthermore in data mode<sup>10</sup> a dummy “AT” would affect the data communication.

### Additional considerations for SARA-U2 modules

SARA-U2 modules are forced to stay in active-mode if the USB is connected and not suspended, and therefore the AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 settings are overruled but they have effect on the UART behavior: they configure UART interface power saving, so that UART is enabled / disabled according to the AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 settings.

To set the AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 configuration over the USB interface of SARA-U2 modules, the autobauding must be previously disabled on the UART by the +IPR AT command over the used AT interface (the USB), and this +IPR AT command configuration must be saved in the module’ non-volatile memory (see u-blox AT Commands Manual [3]). Then, after the subsequent module re-boot, AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 can be issued over the used AT interface (the USB): all the AT profiles are updated accordingly.

<sup>10</sup> Refer to the u-blox AT Commands Manual [3] for the definition of the interface data mode, command mode and online command mode.

### 1.9.1.5 Multiplexer protocol (3GPP 27.010)

SARA-G3 and SARA-U2 series modules have a software layer with MUX functionality, the 3GPP TS 27.010 Multiplexer Protocol [13], available on the UART physical link. The auxiliary UART, the USB and the DDC (I<sup>2</sup>C) serial interfaces do not support the multiplexer protocol.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the used physical link (UART or SPI): the user can concurrently use AT command interface on one MUX channel and Packet-Switched / Circuit-Switched Data communication on another multiplexer channel. Each session consists of a stream of bytes transferring various kinds of data such as SMS, CBS, PSD, GNSS, AT commands in general. This permits, for example, SMS to be transferred to the DTE when a data connection is in progress.

The following virtual channels are defined:

- Channel 0: control channel
- Channel 1: AT and Data
- Channel 2: AT and Data
- Channel 3: AT and Data (not available on SARA-G300 / SARA-G310 modules)
- Channel 4: AT and Data (not available on SARA-G300 / SARA-G310 modules)
- Channel 5: AT and Data (not available on SARA-G300 / SARA-G310 modules)
- Channel 6: GNSS tunneling (not available on SARA-G300 / SARA-G310 modules)
- Channel 7: SIM Access Profile (not available on SARA-G3 series modules)

For more details, refer to Mux implementation Application Note [23].

### 1.9.2 Auxiliary asynchronous serial interface (UART AUX)



The auxiliary UART interface is not available on SARA-U2 series modules.

SARA-G3 modules provide the auxiliary UART interface: it is a 3-wire unbalanced 1.8 V asynchronous serial interface (only the **RXD\_AUX** data output and **TXD\_AUX** data input are provided), available for module FW upgrade by means of the u-blox EasyFlash tool and for diagnostic purpose.

The AT commands interface is not available on the auxiliary UART interface.

### 1.9.3 USB interface



The USB interface is not available on SARA-G3 series modules.

#### 1.9.3.1 USB features

SARA-U2 modules include a High-Speed USB 2.0 compliant interface with maximum data rate of 480 Mb/s between the module and a host processor.

The module itself acts as a USB device and can be connected to any USB host such as a Personal Computer or an embedded application microprocessor for AT commands, data communication, FW upgrade by means of the FOAT feature, FW upgrade by means of the u-blox EasyFlash tool and for diagnostic purpose.

The **USB\_D+/USB\_D-** pins carry USB serial data and signaling while the **VUSB\_DET** input pin senses the VBUS USB supply presence (nominally +5 V at the source) to detect the host connection and enable the interface.

The USB interface of the module is enabled only if a valid voltage is detected by the **VUSB\_DET** input (see the SARA-U2 series Data Sheet [2]). Neither the USB interface, nor the whole module is supplied by the **VUSB\_DET** input: the **VUSB\_DET** senses the USB supply voltage and absorbs few microamperes.

SARA-U2 modules provide by default the following USB profile with the listed set of available USB functions (USB CDCs, Communications Device Classes):

- USB1: AT and Data (AT command interface and packet-switched / circuit-switched data communication)
- USB2: AT and Data (AT command interface and packet-switched / circuit-switched data communication)
- USB3: AT and Data (AT command interface and packet-switched / circuit-switched data communication)
- USB4: GPS (tunneling communication with the u-blox GNSS receiver connected over I<sup>2</sup>C interface)
- USB5: Primary Log (diagnostic purpose)
- USB6: Secondary Log (diagnostic purpose)
- USB7: SAP (SIM Access Profile)

The user can concurrently use the AT command interface on one CDC, and packet-switched / circuit-switched data communication on another CDC.

The module firmware can be upgraded over the USB interface using the u-blox EasyFlash tool or by means of AT command (for more details see section 1.13.13 and Firmware update application note [25]).

Audio over USB capabilities can be enabled by specific AT command (refer to u-blox AT Commands Manual [3]): the Audio Device Class provides a streaming interface, which transfers audio data on isochronous pipes.



The USB Audio Device Class is not supported by initial firmware release.



For more details on the configuration of the USB interface of SARA-U2 modules, see the u-blox AT Commands Manual [3], +UUSBCONF AT command.

USB CDC/ACM drivers are available for the following operating system platforms:

- Windows 2000
- Windows XP
- Windows Vista
- Windows 7
- Windows 8
- Windows CE 5.0
- Windows Embedded CE 6.0
- Windows Embedded Compact 7
- Windows Embedded Automotive 7
- Windows Mobile 5
- Windows Mobile 6
- Windows Mobile 6.1
- Windows Mobile 6.5

SARA-U2 modules are compatible with standard Linux/Android USB kernel drivers.

The USB profile of SARA-U2 module identifies itself by its VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor according to the USB 2.0 specifications [14].

VID and PID of the SARA-U2 module USB profile with the set of USB functions described in details above (AT and Data, GNSS tunneling, Diagnostic, SAP) are the following:

- VID = 0x1546
- PID = 0x1102

If the USB interface of a SARA-U2 module is connected to the host before the module switch on, or if the module is reset with the USB interface connected to the host, the VID and PID are automatically updated runtime, after the USB detection. First, VID and PID are the following:

- VID = 0x058B
- PID = 0x0041

This VID and PID combination identifies a USB profile where the set of USB functions described in details above (AT and Data, GNSS tunneling, Diagnostic, SAP) are not available: AT commands must not be sent to the module over the USB profile identified by this VID and PID combination.

Then, after a time period (roughly 5 s, depending on the host / device enumeration timings), the VID and PID are updated to the following ones, which are related to the SARA-U2 module USB profile with the set of USB functions described in details above (AT and Data, GNSS tunneling, Diagnostic, SAP):

- VID = 0x1546
- PID = 0x1102

### 1.9.3.2 USB and power saving

If power saving is enabled by the AT+UPSV command, the modules automatically enter the USB suspended state when the device has observed no bus traffic for a specified time period (see the USB 2.0 specifications [14]). In suspended state, the module maintains any USB internal status as device. In addition, the module enters the suspended state when the hub port it is attached to is disabled. This is referred to as USB selective suspend.

The module exits suspend mode when there is bus activity. If the USB is connected and not suspended, the module is forced to stay in active-mode, therefore the AT+UPSV settings are overruled but they have effect on the power saving configuration of the other interfaces.

The modules are capable of USB remote wake-up signaling: i.e. it may request the host to exit suspend mode or selective suspend by using electrical signaling to indicate remote wake-up. This notifies the host that it should resume from its suspended mode, if necessary, and service the external event. Remote wake-up is accomplished using electrical signaling described in the USB 2.0 specifications [14].

For the module current consumption description with power saving enabled and USB suspended, or with power saving disabled and USB not suspended, see sections 1.5.1.4, 1.5.1.5 and SARA-U2 series Data Sheet [2].

## 1.9.4 DDC (I<sup>2</sup>C) interface



SARA-G300 and SARA-G310 modules do not support DDC (I<sup>2</sup>C) interface.

An I<sup>2</sup>C bus compatible Display Data Channel (DDC) interface for communication with u-blox GNSS receivers is available on **SDA** and **SCL** pins of SARA-G340, SARA-G350 and SARA-U2 modules. Only this interface provides the communication between the u-blox cellular module and u-blox positioning chips and modules.

SARA-U2 modules additionally support the communication with other external I<sup>2</sup>C devices as an audio codec.

The AT commands interface is not available on the DDC (I<sup>2</sup>C) interface.

DDC (I<sup>2</sup>C) slave-mode operation is not supported: the cellular module can act as master only, and the connected u-blox GNSS receiver or any other external I<sup>2</sup>C devices acts as slave in the DDC (I<sup>2</sup>C) communication.

Two lines, serial data (**SDA**) and serial clock (**SCL**), carry information on the bus. **SCL** is used to synchronize data transfers, and **SDA** is the data line. To be compliant to the I<sup>2</sup>C bus specifications, the module interface pins are open drain output and pull up resistors must be externally provided conforming to the I<sup>2</sup>C bus specifications [15].

u-blox has implemented special features in SARA-G340, SARA-G350 and SARA-U2 modules to ease the design effort required for the integration of a u-blox cellular module with a u-blox GNSS receiver.

Combining a u-blox cellular module with a u-blox GNSS receiver allows designers to have full access to the positioning receiver directly via the cellular module: it relays control messages to the GNSS receiver via a dedicated DDC (I<sup>2</sup>C) interface. A 2<sup>nd</sup> interface connected to the positioning receiver is not necessary: AT commands via the UART or USB serial interface of the cellular module allows a fully control of the GNSS receiver from any host processor.

SARA-G340, SARA-G350 and SARA-U2 modules feature embedded GNSS aiding that is a set of specific features developed by u-blox to enhance GNSS performance, decreasing the Time To First Fix (TTFF), thus allowing to calculate the position in a shorter time with higher accuracy.

SARA-G340, SARA-G350 and SARA-U2 modules support these GNSS aiding types:

- Local aiding
- AssistNow Online
- AssistNow Offline
- AssistNow Autonomous

The embedded GNSS aiding features can be used only if the DDC (I<sup>2</sup>C) interface of the cellular module is connected to the u-blox GNSS receivers.

SARA-G340, SARA-G350 and SARA-U2 cellular modules provide additional custom functions over GPIO pins to improve the integration with u-blox positioning chips and modules. GPIO pins can handle:

- GNSS receiver power-on/off: “GNSS supply enable” function provided by **GPIO2** improves the positioning receiver power consumption. When the GNSS functionality is not required, the positioning receiver can be completely switched off by the cellular module that is controlled by AT commands
- The wake up from idle-mode when the GNSS receiver is ready to send data: “GNSS data ready” function provided by **GPIO3** improves the cellular module power consumption. When power saving is enabled in the cellular module by the AT+UPSV command and the GNSS receiver does not send data by the DDC (I<sup>2</sup>C) interface, the module automatically enters idle-mode whenever possible. With the “GNSS data ready” function the GNSS receiver can indicate to the cellular module that it is ready to send data by the DDC (I<sup>2</sup>C) interface: the positioning receiver can wake up the cellular module if it is in idle-mode, so the cellular module does not lose the data sent by the GNSS receiver even if power saving is enabled
- The RTC synchronization signal to the GNSS receiver: “GNSS RTC sharing” function provided by **GPIO4** improves GNSS receiver performance, decreasing the Time To First Fix (TTFF), and thus allowing to calculate the position in a shorter time with higher accuracy. When GPS local aiding is enabled, the cellular module automatically uploads data such as position, time, ephemeris, almanac, health and ionospheric parameter from the positioning receiver into its local memory, and restores this to the GNSS receiver at the next power up of the positioning receiver



For more details regarding the handling of the DDC (I<sup>2</sup>C) interface, the GNSS aiding features and the GNSS related functions over GPIOs, see section 1.11, to the u-blox AT Commands Manual [3] (AT+UGPS, AT+UGPRF, AT+UGPIOC AT commands) and the GNSS Implementation Application Note [24].



“GNSS data ready” and “GNSS RTC sharing” functions are not supported by all u-blox GNSS receivers HW or ROM/FW versions. See the GNSS Implementation Application Note [24] or to the Hardware Integration Manual of the u-blox GNSS receivers for the supported features.

As additional improvement for the GNSS receiver performance, the **V\_BCKP** supply output of SARA-G340, SARA-G350 and SARA-U2 modules can be connected to the **V\_BCKP** supply input pin of u-blox positioning chips and modules to provide the supply for the GNSS real time clock and backup RAM when the **VCC** supply of the cellular module is within its operating range and the **VCC** supply of the GNSS receiver is disabled.

This enables the u-blox positioning receiver to recover from a power breakdown with either a hot start or a warm start (depending on the duration of the GNSS receiver **VCC** outage) and to maintain the configuration settings saved in the backup RAM.



## 1.10 Audio interface



SARA-G300 and SARA-G310 modules do not support audio interface.

The following audio interfaces are provided by SARA-G3 and SARA-U2 series modules:

- SARA-G340 and SARA-G350 modules provide one analog audio interface and one digital audio interface
- SARA-U2 modules provide one digital audio interface

The audio interfaces can be selected and set by the dedicated AT command +USPM (refer to the u-blox AT Commands Manual [3]): this command allows setting the audio path mode, composed by the uplink audio path and the downlink audio path.

Each uplink path mode defines the physical input (i.e. the analog or the digital audio input) and the set of parameters to process the uplink audio signal (uplink gains, uplink digital filters, echo canceller parameters). For example the “Headset microphone” uplink path uses the differential analog audio input with the default parameters for the headset profile.

Each downlink path mode defines the physical output (i.e. the analog or the digital audio output) and the set of parameters to process the downlink audio signal (downlink gains, downlink digital filters and sidetone). For example the “Mono headset” downlink path uses the differential analog audio output with the default parameters for the headset profile.

The set of parameters to process the uplink or the downlink audio signal can be changed with dedicated AT commands for each uplink or downlink path and then stored in two profiles in the non volatile memory (refer to u-blox AT Commands Manual [3] for Audio parameters tuning commands).

### 1.10.1 Analog audio interface



SARA-U2 modules do not provide analog audio interface.

#### 1.10.1.1 Uplink path

SARA-G340 / SARA-G350 pins related to the analog audio uplink path are:

- **MIC\_P / MIC\_N**: Differential analog audio signal inputs (positive/negative). These two pins are internally directly connected to the differential input of an integrated Low Noise Amplifier, without any internal series capacitor for DC blocking. The LNA output is internally connected to the digital processing system by an integrated sigma-delta analog-to-digital converter
- **MIC\_BIAS**: Supply output for an external microphone. The pin is internally connected to the output of a low noise LDO linear regulator provided with proper internal bypass capacitor to guarantee stable operation of the linear regulator
- **MIC\_GND**: Local ground for the external microphone. The pin is internally connected to ground as a sense line as the reference for the analog audio input

The analog audio input is selected when the parameter <main\_uplink> in AT+USPM command is set to “Headset microphone”, “Handset microphone” or “Hands-free microphone”: the uplink analog path profiles use the same physical input but have different sets of audio parameters (for more details, refer to u-blox AT Commands Manual [3], AT+USPM, AT+UMGC, AT+UUBF, AT+UHFP commands).

SARA-G3 series Data Sheet [1] provides the detailed electrical characteristics of the analog audio uplink path.



### 1.10.1.2 Downlink path

SARA-G340 / SARA-G350 pins related to the analog audio downlink path are:

- **SPK\_P / SPK\_N**: Differential analog audio signal output (positive/negative). These two pins are directly connected internally to the differential output of a low power audio amplifier, for which the input is connected internally to the digital processing system by to an integrated digital-to-analog converter.

The analog audio output is selected when the parameter `<main_downlink>` in `AT+USPM` command is set to "Normal earpiece", "Mono headset" or "Loudspeaker": the downlink analog path profiles use the same physical output but have different sets of audio parameters (for more details, refer to the u-blox AT Commands Manual [3], `AT+USPM`, `AT+USGC`, `AT+UDBF`, `AT+USTN` commands).

The differential analog audio output of SARA-G340 and SARA-G350 modules (**SPK\_P / SPK\_N**) is able to directly drive loads with resistance rating greater than 14  $\Omega$ : it can be directly connected to a headset earpiece or handset earpiece but cannot directly drive a 8  $\Omega$  or 4  $\Omega$  loudspeaker for the hands-free mode.

SARA-G3 series Data Sheet [1] provides the detailed electrical characteristics of the analog audio downlink path.



**Warning: excessive sound pressure from headphones can cause hearing loss.**

### 1.10.1.3 Headset mode

Headset mode is the default audio operating mode of the modules. The headset profile is configured when the uplink audio path is set to "Headset microphone" and the downlink audio path is set to "Mono headset" (refer to u-blox AT Commands Manual [3]: `AT+USPM` command: `<main_uplink>`, `<main_downlink>` parameters).

### 1.10.1.4 Handset mode

The handset profile is configured when the uplink audio path is set to "Handset microphone" and the downlink audio path is set to "Normal earpiece" (refer to u-blox AT commands manual [3]: `AT+USPM` command: `<main_uplink>`, `<main_downlink>` parameters).

### 1.10.1.5 Hands-free mode

The hands-free profile is configured when the uplink audio path is set to "Hands-free microphone" and the downlink audio path is set to "Loudspeaker" (refer to u-blox AT commands manual [3]: `AT+USPM` command: `<main_uplink>`, `<main_downlink>` parameters).

Hands-free functionality is implemented using appropriate digital signal processing algorithms for voice-band handling (echo canceller and automatic gain control), managed via software (refer to u-blox AT commands manual [3], `AT+UHFP` command).

### 1.10.2 Digital audio interface

SARA-G340, SARA-G350 and SARA-U2 modules provide one 1.8 V bidirectional 4-wire (**I2S\_TXD** data output, **I2S\_RXD** data input, **I2S\_CLK** clock, **I2S\_WA** world alignment) I<sup>2</sup>S digital audio interface that can be used for digital audio communication with external digital audio devices as an audio codec.

The I<sup>2</sup>S interface can be set to two modes, by the <I2S\_mode> parameter of the AT+UI2S command:

- PCM mode
- Normal I<sup>2</sup>S mode

The I<sup>2</sup>S interface can be set to two configurations, by the <I2S\_Master\_Slave> parameter of AT+UI2S:

- Master mode
- Slave mode



SARA-G340 and SARA-G350 modules do not support I<sup>2</sup>S slave mode: module acts as master only.

The sample rate of transmitted/received words can be set, by the <I2S\_sample\_rate> parameter of AT+UI2S, to:

- 8 kHz
- 11.025 kHz
- 12 kHz
- 16 kHz
- 22.05 kHz
- 24 kHz
- 32 kHz
- 44.1 kHz
- 48 kHz



SARA-G340 and SARA-G350 modules do not support the <I2S\_sample\_rate> parameter of AT+UI2S: the sample rate is fixed at 8 kHz only.

The <main\_uplink> and <main\_downlink> parameters of the AT+USPM command must be properly configured to select the I<sup>2</sup>S digital audio interfaces paths (for more details, refer to u-blox AT Commands Manual [3]):

- <main\_uplink> must be properly set to select:
  - the I<sup>2</sup>S interface (using **I2S\_RXD** module input)
- <main\_downlink> must be properly set to select:
  - the I<sup>2</sup>S interface (using **I2S\_TXD** module output)

Parameters of digital path can be configured and saved as described in the u-blox AT Commands Manual [3], +USGC, +UMGC, +USTN AT commands. Analog gain parameters are not used when digital path is selected.

The I<sup>2</sup>S receive data input and the I<sup>2</sup>S transmit data output signals are respectively connected in parallel to the analog microphone input and speaker output signals, so resources available for analog path can be shared:

- Digital filters and digital gains are available in both uplink and downlink direction
- Ringer tone and service tone are mixed on the TX path when active (downlink)
- The HF algorithm acts on I<sup>2</sup>S path



Refer to the u-blox AT Commands Manual [3]: AT+UI2S command for possible settings of I<sup>2</sup>S interface.

### 1.10.2.1 I<sup>2</sup>S interface – PCM mode

Main features of the I<sup>2</sup>S interface in PCM mode, which are configurable via a specific AT command (for further details see the related section in the u-blox AT Commands Manual [3], +UI2S AT command):

- I<sup>2</sup>S runs in PCM – short alignment mode
- I<sup>2</sup>S word alignment signal is configured by the <I2S\_sample\_rate> parameter
- I<sup>2</sup>S word alignment is set high for 1 or 2 clock cycles for the synchronization, and then is set low for 16 clock cycles of sample width. The frame length, according to the length of the high pulse for the synchronization, can be  $1 + 16 = 17$  bits or  $2 + 16 = 18$  bits
- I<sup>2</sup>S clock frequency depends on the frame length and the sample rate. It can be  $17 \times \text{<I2S\_sample\_rate>}$  or  $18 \times \text{<I2S\_sample\_rate>}$
- I<sup>2</sup>S transmit and I<sup>2</sup>S receive data are 16 bit words long with the same sampling rate as I<sup>2</sup>S word alignment, mono. Data is in 2's complement notation. MSB is transmitted first
- When I<sup>2</sup>S word alignment toggles high, the first synchronization bit is always low. Second synchronization bit (present only in case of 2 bit long I<sup>2</sup>S word alignment configuration) is MSB of the transmitted word (MSB is transmitted twice in this case)
- I<sup>2</sup>S transmit data changes on I<sup>2</sup>S clock rising edge, I<sup>2</sup>S receive data changes on I<sup>2</sup>S clock falling edge

### 1.10.2.2 I<sup>2</sup>S interface – Normal I<sup>2</sup>S mode

Normal I<sup>2</sup>S supports:

- 16 bits word
- Mono interface
- Sample rate: <I2S\_sample\_rate> parameter

Main features of I<sup>2</sup>S interface in normal I<sup>2</sup>S mode, which are configurable via a specific AT command (for further details see the related section in the u-blox AT Commands Manual [3], +UI2S AT command):

- I<sup>2</sup>S runs in normal I<sup>2</sup>S – long alignment mode
- I<sup>2</sup>S word alignment signal always runs at the <I2S\_sample\_rate> and synchronizes 2 channels (timeslots on word alignment high, word alignment low)
- I<sup>2</sup>S transmit data is composed of 16 bit words, dual mono (the words are written on both channels). Data are in 2's complement notation. MSB is transmitted first. The bits are written on I<sup>2</sup>S clock rising or falling edge (configurable)
- I<sup>2</sup>S receive data is read as 16 bit words, mono (words are read only on the timeslot with WA high). Data is read in 2's complement notation. MSB is read first. The bits are read on the I<sup>2</sup>S clock edge opposite to I<sup>2</sup>S transmit data writing edge (configurable)
- I<sup>2</sup>S clock frequency is  $16 \text{ bits} \times 2 \text{ channels} \times \text{<I2S\_sample\_rate>}$

Additionally, the following parameters can be set by means of the +UI2S AT command:

- MSB can be 1 bit delayed or non-delayed on I<sup>2</sup>S word alignment edge
- I<sup>2</sup>S transmit data can change on rising or falling edge of I<sup>2</sup>S clock signal
- I<sup>2</sup>S receive data are read on the opposite front of I<sup>2</sup>S clock signal

### 1.10.3 Voice-band processing system

#### 1.10.3.1 SARA-G340 / SARA-G350 modules audio processing

The voice-band processing on the SARA-G340 / SARA-G350 modules is implemented in the DSP core inside the baseband chipset. The analog audio front-end of the chipset is connected to the digital system through 16 bit ADC converters in the uplink path, and through 16 bit DAC converters in the downlink path. External digital audio devices can directly be interfaced to the DSP digital processing part via the I<sup>2</sup>S digital interface. The analog amplifiers are skipped in this case.

The voice-band processing system can be split up into three different blocks:

- Sample-based Voice-band Processing (single sample processed at 8 kHz, every 125  $\mu$ s)
- Frame-based Voice-band Processing (frames of 160 samples are processed every 20 ms)
- MIDI synthesizer running at 47.6 kHz

These three blocks are connected by buffers and sample rate converters (for 8 to 47.6 kHz conversion)

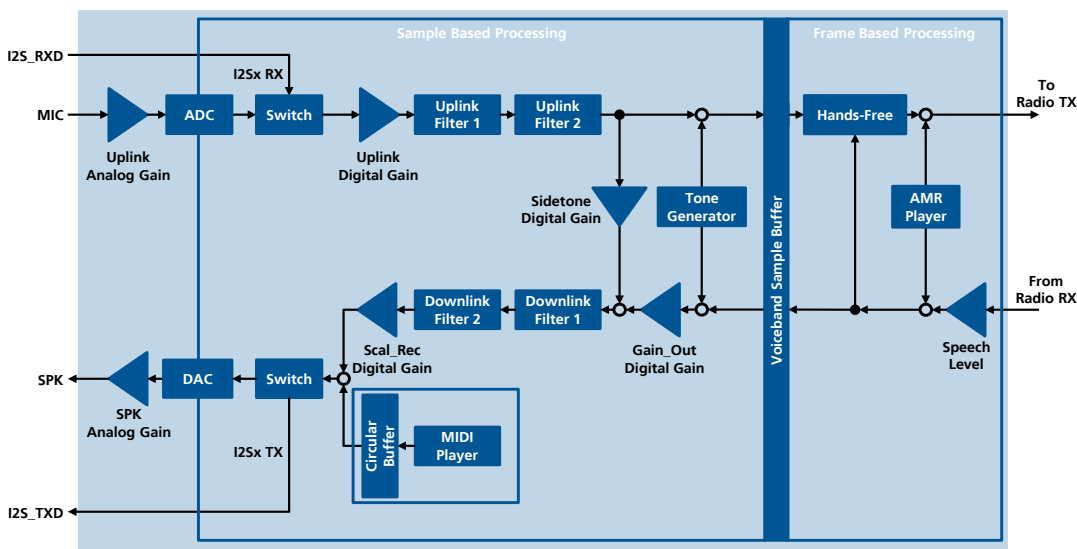


Figure 28: SARA-G340 / SARA-G350 modules audio processing system block diagram

The sample-based voice-band processing main task is to transfer the voice-band samples from either analog audio front-end uplink path or I2Sx RX path to the Voice-band Sample Buffer and from the Voice-band Sample Buffer to the analog audio front-end downlink path and/or I2Sx TX path. While doing this the samples are scaled by digital gains and processed by digital filters both in the uplink and downlink direction and the sidetone is generated mixing scaled uplink samples to the downlink samples (refer to the u-blox AT Commands Manual [3], +UUBF, +UDBF, +UMGC, +USGC, +USTN commands).

The frame-based voice-band processing implements the Hands-Free algorithm. This consists of the Echo Canceller, the Automatic Gain Control and the Noise Suppressor. Hands-Free algorithm acts on the uplink signal only. Algorithms are configurable with AT commands (refer to the u-blox AT Commands Manual [3], +UHFP command). The frame-based voice-band processing also implements an AMR player. The speech uplink path final block before radio transmission is the speech encoder. Symmetrically, on downlink path, the starting block is the speech decoder which extracts speech signal from the radio receiver.

The circular buffer is a 3000 word buffer to store and mix the voice-band samples from Midi synthesizer. The buffer has a circular structure, so that when the write pointer reaches the end of the buffer, it is wrapped to the begin address of the buffer.

Two different sample-based sample rate converters are used: an interpolator, required to convert the sample-based voice-band processing sampling rate of 8 kHz to the analog audio front-end output rate of 47.6 kHz; a decimator, required to convert the circular buffer sampling rate of 47.6 kHz to the I2Sx TX or the uplink path sample rate of 8 kHz.

The following speech codecs are supported by SARA-G340 / SARA-G350 firmware on the DSP:

- GSM Half Rate (TCH/HS)
- GSM Full Rate (TCH/FS)
- GSM Enhanced Full Rate (TCH/EFR)
- 3GPP Adaptive Multi Rate (AMR) (TCH/AFS+TCH/AHS)
  - In AMR Full Rate (AFS) the Active CODEC Set is selected from an overall set of 8 data rates: 12.2 – 10.2 – 7.95 – 7.40 – 6.70 – 5.90 – 5.15 – 4.75 kb/s
  - In AMR Half Rate (AHS) the overall set comprises 6 different data rates: 7.95 – 7.40 – 6.70 – 5.90 – 5.15 – 4.75 kb/s

### 1.10.3.2 SARA-U2 modules audio processing system

The voiceband processing on the SARA-U2 modules is implemented in the DSP core inside the baseband chipset. The external digital audio devices can be interfaced directly to the DSP digital processing part via the I<sup>2</sup>S digital interface. With exception of the speech encoder/decoder, audio processing can be controlled by AT commands.

The audio processing is implemented within the different blocks of the voiceband processing system:

- Sample-based Voice-band Processing (single sample processed at 16 kHz for Wide Band AMR codec or 8 kHz for all other speech codecs)
- Frame-based Voice-band Processing (frames of 320 samples for Wide Band AMR codec or 160 samples for all other speech codecs are processed every 20 ms)

These blocks are connected by buffers (circular buffer and voiceband sample buffer) and sample rate converters (for 8 / 16 to 47.6 kHz conversion).

The voiceband audio processing implemented in the DSP core of SARA-U2 modules is summarized in Figure 29.

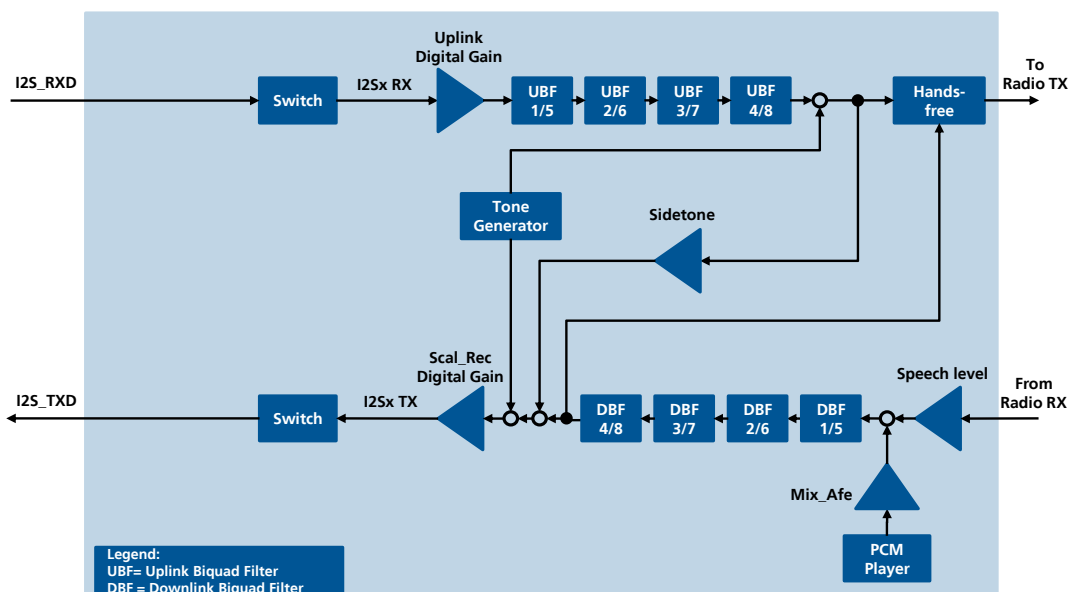


Figure 29: SARA-U2 modules audio processing system block diagram

SARA-U2 modules audio signal processing algorithms are:

- Speech encoding (uplink) and decoding (downlink). The following speech codecs are supported in firmware on the DSP for speech encoding and decoding:

GERAN GMSK codecs

- GSM HR (GSM Half Rate)
- GSM FR (GSM Full Rate)
- GSM EFR (GSM Enhanced Full Rate)
- HR AMR (GSM Half Rate Adaptive Multi Rate - Narrow Band)
- FR AMR (GSM Full Rate Adaptive Multi Rate - Narrow Band)
- FR AMR-WB (GSM Full Rate Adaptive Multi Rate - Wide Band)

UTRAN codecs:

- UMTS AMR2 (UMTS Adaptive Multi Rate version 2 – Narrow Band)
- UMTS AMR-WB (UMTS Adaptive Multi Rate – Wide Band)

- Mandatory sub-functions:
  - Discontinuous transmission, DTX (GSM 46.031, 46.041, 46.081 and 46.093 standards)
  - Voice activity detection, VAD (GSM 46.032, 46.042, 46.082 and 46.094 standards)
  - Background noise calculation (GSM 46.012, 46.022, 46.062 and 46.092 standards)
- Function configurable via specific AT commands (refer to the u-blox AT Commands Manual [3])
  - Signal routing: +USPM command
  - Analog amplification, digital amplification: +USGC, +CLVL, +CRSL, +CMUT command
  - Digital filtering: +UUBF, +UDBF commands
  - Hands-free algorithms (echo cancellation, Noise suppression, Automatic Gain control) +UHFP command
  - Sidetone generation (feedback of uplink speech signal to downlink path): +USTN command
  - Playing/mixing of alert tones:
    - Service tones: Tone generator with 3 sinus tones +UPAR command
    - User generated tones: Tone generator with a single sinus tone +UTGN command
  - PCM audio files (for prompting): The storage format of PCM audio files is 8 kHz sample rate, signed 16 bits, little endian, mono

## 1.11 General Purpose Input/Output (GPIO)



SARA-G300 and SARA-G310 modules do not support GPIOs.

SARA-G340, SARA-G350 and SARA-U2 modules provide pins which can be configured as general purpose input or output, or can be configured to provide special functions via u-blox AT commands (for further details refer to the u-blox AT Commands Manual [3], +UGPIOC, +UGPIOR, +UGPIOW, +UGPS, +UGPRF):

- SARA-G340 and SARA-G350 modules provide 4 configurable GPIO pins: **GPIO1, GPIO2, GPIO3, GPIO4**
- SARA-U2 modules provide 9 configurable GPIO pins: **GPIO1, GPIO2, GPIO3, GPIO4, I2S\_RXD, I2S\_TXD, I2S\_CLK, I2S\_WA, SIM\_DET**

The following functions are available:

- **Network status indication:**

The **GPIO1**, or the **GPIO2, GPIO3, GPIO4** and, on SARA-U2 series only, the **SIM\_DET**, alternatively from their default settings, can be configured to indicate network status (i.e. no service, registered home network, registered visitor network, voice or data call enabled), setting the parameter <gpio\_mode> of AT+UGPIOC command to 2.

No GPIO pin is by default configured to provide the “Network status indication” function.

The “Network status indication” mode can be provided only on one pin per time: it is not possible to simultaneously set the same mode on another pin.

The pin configured to provide the “Network status indication” function is set as

- Continuous Low, if no service (no network coverage or not registered)
- Cyclically High for 100 ms, Low for 2 s, if registered home 2G network
- Cyclically High for 50 ms, Low for 50 ms, High for 50 ms, Low for 2 s, if registered home 3G network
- Cyclically High for 100 ms, Low for 100 ms, High for 100 ms, Low for 2 s, if registered visitor 2G network (roaming)
- Cyclically High for 50 ms, Low for 50 ms, High for 50 ms, Low for 100 ms, if registered visitor 3G network (roaming)
- Continuous High, if voice or data 2G/3G call enabled

- **GSM Tx burst indication:**

**GPIO1** pin can be configured by AT+UGPIOC to indicate when a GSM Tx burst/slot occurs, setting the parameter <gpio\_mode> of AT+UGPIOC command to 9.

No GPIO pin is by default configured to provide the “GSM Tx burst indication” function.

The pin configured to provide the “GSM Tx burst indication” function is set as

- High, since ~10 μs before the start of first Tx slot, until ~5 μs after the end of last Tx slot
- Low, otherwise



SARA-U280 module does not support the “GSM Tx burst indication” function on **GPIO1**, as the module does not support 2G radio access technology.

- **GNSS supply enable:**

The **GPIO2** is by default configured by AT+UGPIOC command to enable or disable the supply of the u-blox GNSS receiver connected to the cellular module.

The **GPIO1**, **GPIO3**, **GPIO4** pins and, on SARA-U2 series only, also the **SIM\_DET** pin, can be configured to provide the “GNSS supply enable” function, alternatively to the default **GPIO2** pin, setting the parameter <gpio\_mode> of AT+UGPIOC command to 3. The “GNSS supply enable” mode can be provided only on one pin per time: it is not possible to simultaneously set the same mode on another pin.

The pin configured to provide the “GNSS supply enable” function is set as

- High, to switch on the u-blox GNSS receiver, if AT+UGPS parameter <mode> is set to 1
- Low, to switch off the u-blox GNSS receiver, if AT+UGPS parameter <mode> is set to 0 (default)

- **GNSS data ready:**

Only the **GPIO3** pin provides the “GNSS data ready” function, to sense when a u-blox GNSS receiver connected to the cellular module is ready to send data via the DDC (I<sup>2</sup>C) interface, setting the parameter <gpio\_mode> of AT+UGPIOC command to 4.

The pin configured to provide the “GNSS data ready” function is set as

- Input, to sense the line status, waking up the cellular module from idle-mode when the u-blox GNSS receiver is ready to send data via the DDC (I<sup>2</sup>C) interface, if the first AT+UGPS parameter is set to 1 and the first AT+UGPRF parameter is set to 16
- Tri-state with an internal active pull-down enabled, otherwise (default setting)

- **GNSS RTC sharing:**

Only the **GPIO4** pin provides the “GNSS RTC sharing” function, to provide an RTC (Real Time Clock) synchronization signal to the u-blox GNSS receiver connected to the cellular module, setting the parameter <gpio\_mode> of AT+UGPIOC command to 5.

The pin configured to provide the “GNSS RTC sharing” function is set as

- Output, to provide an RTC (Real Time Clock) synchronization signal to the u-blox GNSS receiver if the first AT+UGPS parameter is set to 1 and the first AT+UGPRF parameter is set to 32
- Low, otherwise (default setting)

- **SIM card detection:**

The **SIM\_DET** pin of SARA-G3 modules is by default configured to detect SIM card mechanical presence and this configuration cannot be changed by AT command.

The **SIM\_DET** pin of SARA-U2 modules is by default configured to detect SIM card mechanical presence as default setting of the AT+UGPIOC command: the “SIM card detection” function is enabled as the parameter <gpio\_mode> of AT+UGPIOC command is set to 7 (default setting).

The **SIM\_DET** pin configured to provide the “SIM card detection” function is set as

- Input with an internal active pull-down enabled, to sense SIM card mechanical presence

The **SIM\_DET** pin can sense the SIM card mechanical presence only if properly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **SIM\_DET** input pin is recognized as SIM card not present
- High logic level at **SIM\_DET** input pin is recognized as SIM card present

SARA-U2 modules provide the additional function “SIM card hot insertion/removal” on the **SIM\_DET** pin, which can be enabled using the AT+UDCONF=50 command if the “SIM card detection” function is enabled by AT+UGPIOC (for more details see u-blox AT Commands Manual [3]): in this case the SIM interface of the SARA-U2 modules is disabled when a Low logic level is recognized at **SIM\_DET** input pin (within 20 ms from the start of the Low level) and it is enabled when an High logic level at **SIM\_DET** input pin is recognized.



SARA-G3 series do not support the additional function “SIM card hot insertion/removal”



- **Module status indication:**

The **GPIO1** pin of SARA-U2 modules can be configured to indicate module status (power-off mode, i.e. module switched off, versus idle, active or connected mode, i.e. module switched on), by properly setting the parameter `<gpio_mode>` of AT+UGPIOC command to 10.

No GPIO pin is by default configured to provide the "Module status indication".

The pin configured to provide the "Module status indication" function is set as

- High, when the module is switched on (any operating mode during module normal operation)
- Low, when the module is switched off (power off mode)



SARA-G3 series do not support "Module status indication" function.

- **Module operating mode indication:**

The **SIM\_DET** pin of SARA-U2 modules can be configured to indicate module operating mode status (the low power idle-mode versus active or connected mode), by properly setting the parameter `<gpio_mode>` of AT+UGPIOC command to 11.

No GPIO pin is by default configured to provide the "Module operating mode indication".

The pin configured to provide the "Module operating mode indication" function is set as

- Output / High, when the module is in active or connected mode
- Output / Low, when the module is in idle-mode (that can be reached if power saving is enabled by +UPSV AT command: for further details see u-blox AT Commands Manual [3])



SARA-G3 series do not support "Module operating mode indication".

- **I<sup>2</sup>S digital audio interface:**

The **I2S\_RXD**, **I2S\_TXD**, **I2S\_CLK**, **I2S\_WA** pins of SARA-U2 modules are by default configured as the I<sup>2</sup>S digital audio interface.

Only these pins of SARA-U2 modules can be configured as the I<sup>2</sup>S digital audio interface, by correctly setting the parameter `<gpio_mode>` of AT+UGPIOC command to 12 (default setting).



SARA-G3 series do not support the I<sup>2</sup>S digital audio interface over GPIOs.

- **General purpose input:**

All the GPIOs can be configured as input to sense high or low digital level through AT+UGPIOR command, setting the parameter `<gpio_mode>` of AT+UGPIOC command to 1.

The "General purpose input" mode can be provided on more than one pin at a time.

No GPIO pin is by default configured as "General purpose input".

The pin configured to provide the "General purpose input" function is set as

- Input, to sense high or low digital level by AT+UGPIOR command.

- **General purpose output:**

All the GPIOs can be configured as output to set the high or the low digital level through AT+UGPIOW command, setting the parameter `<gpio_mode>` of +UGPIOC AT command to 0.

The "General purpose output" mode can be provided on more than one pin per time.

No GPIO pin is by default configured as "General purpose output".

The pin configured to provide the "General purpose output" function is set as

- Output / Low, if the parameter `<gpio_out_val>` of AT+UGPIOW command is set to 0
- Output / High, if the parameter `<gpio_out_val>` of AT+UGPIOW command is set to 1

- **Pin disabled:**

All the GPIOs can be configured in tri-state with an internal active pull-down enabled, as a not used pin, setting the parameter <gpio\_mode> of +UGPIOC AT command to 255.

The “Pin disabled” mode can be provided on more than one pin per time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

The pin configured to provide the “Pin disabled” function is set as

- Tri-state with an internal active pull-down enabled

Table 13 describes the configurations of all SARA-G340, SARA-G350 and SARA-U2 modules’ GPIO pins.

Pin	Module	Name	Description	Remarks
16	SARA-G340 SARA-G350	<b>GPIO1</b>	GPIO	By default, the pin is configured as Pin disabled. Can be alternatively configured by the AT+UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Network Status Indication</li> <li>• GNSS Supply Enable</li> <li>• GSM Tx Burst Indication</li> </ul>
	SARA-U260 SARA-U270	<b>GPIO1</b>	GPIO	By default, the pin is configured as Pin disabled. Can be alternatively configured by the AT+UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Network Status Indication</li> <li>• GNSS Supply Enable</li> <li>• GSM Tx Burst Indication</li> <li>• Module Status Indication</li> </ul>
	SARA-U280	<b>GPIO1</b>	GPIO	By default, the pin is configured as Pin disabled. Can be alternatively configured by the AT+UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Network Status Indication</li> <li>• GNSS Supply Enable</li> <li>• Module Status Indication</li> </ul>
23	SARA-G340 SARA-G350 SARA-U2 series	<b>GPIO2</b>	GPIO	By default, the pin is configured to provide GNSS Supply Enable function. Can be alternatively configured by the +UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Network Status Indication</li> <li>• Pin disabled</li> </ul>
24	SARA-G340 SARA-G350 SARA-U2 series	<b>GPIO3</b>	GPIO	By default, the pin is configured to provide GNSS Data Ready function. Can be alternatively configured by the +UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Network Status Indication</li> <li>• GNSS Supply Enable</li> <li>• Pin disabled</li> </ul>
25	SARA-G340 SARA-G350 SARA-U2 series	<b>GPIO4</b>	GPIO	By default, the pin is configured to provide GNSS RTC sharing function. Can be alternatively configured by the +UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Network Status Indication</li> <li>• GNSS Supply Enable</li> <li>• Pin disabled</li> </ul>

Pin	Module	Name	Description	Remarks
42	SARA-G340 SARA-G350	<b>SIM_DET</b>	SIM detection	By default, the pin is configured to provide SIM card detection function. The pin cannot be alternatively configured by the +UGPIOC command.
	SARA-U2 series	<b>SIM_DET</b>	GPIO	By default, the pin is configured to provide SIM card detection function. Can be alternatively configured by the +UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Network Status Indication</li> <li>• GNSS Supply Enable</li> <li>• Module Operating Mode Indication</li> <li>• Pin disabled</li> </ul>
34	SARA-U2 series	<b>I2S_WA</b>	GPIO	By default, the pin is configured to provide I <sup>2</sup> S word alignment function. Can be alternatively configured by the +UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Pin disabled</li> </ul>
35	SARA-U2 series	<b>I2S_TXD</b>	GPIO	By default, the pin is configured to provide I <sup>2</sup> S data output function. Can be alternatively configured by the +UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Pin disabled</li> </ul>
36	SARA-U2 series	<b>I2S_CLK</b>	GPIO	By default, the pin is configured to provide I <sup>2</sup> S clock function. Can be alternatively configured by the +UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Pin disabled</li> </ul>
37	SARA-U2 series	<b>I2S_RXD</b>	GPIO	By default, the pin is configured to provide I <sup>2</sup> S data input function. Can be alternatively configured by the +UGPIOC command as <ul style="list-style-type: none"> <li>• Output</li> <li>• Input</li> <li>• Pin disabled</li> </ul>

**Table 13: GPIO pins configurations**

## 1.12 Reserved pins (RSVD)

SARA-G3 and SARA-U2 series modules have pins reserved for future use: they can all be left unconnected on the application board, except the **RSVD** pin number **33** that must be externally connected to ground.

## 1.13 System features

### 1.13.1 Network indication

 Not supported by SARA-G300 and SARA-G310 modules.

The **GPIO1**, or the **GPIO2**, **GPIO3**, **GPIO4** and, on SARA-U2 series only, the **SIM\_DET**, alternatively from their default settings, can be configured to indicate network status (i.e. no service, registered home network, registered visitor network, voice or data call enabled), by means of the AT+UGPIOC command.

For the detailed description, see section 1.11 and to u-blox AT Commands Manual [3], GPIO commands.

### 1.13.2 Antenna detection

 Not supported by SARA-G300 and SARA-G310 modules.

**ANT\_DET** pin of SARA-G340, SARA-G350 and SARA-U2 series modules is an Analog to Digital Converter (ADC) provided to sense the presence of an external antenna when optionally set by the +UANTR AT command.

The external antenna assembly must be provided with a built-in resistor (diagnostic circuit) to be detected, and an antenna detection circuit must be implemented on the application board properly connecting the antenna detection input (**ANT\_DET**) to the antenna RF interface (**ANT**).

For more details regarding feature description and detection / diagnostic circuit design-in see sections 1.7.2 and 2.4.2, and to the u-blox AT Commands Manual [3].

### 1.13.3 Jamming detection

 Not supported by SARA-G300 and SARA-G310 modules.

In real network situations modules can experience various kind of out-of-coverage conditions: limited service conditions when roaming to networks not supporting the specific SIM, limited service in cells which are not suitable or barred due to operators' choices, no cell condition when moving to poorly served or highly interfered areas. In the latter case, interference can be artificially injected in the environment by a noise generator covering a given spectrum, thus obscuring the operator's carriers entitled to give access to the cellular service.

The Jamming Detection Feature detects such "artificial" interference and reports the start and stop of such conditions to the client, which can react appropriately by e.g. switching off the radio transceiver to reduce power consumption and monitoring the environment at constant periods.

The feature detects, at radio resource level, an anomalous source of interference and signals it to the client with an unsolicited indication when the detection is entered or released. The jamming condition occurs when:

- The module has lost synchronization with the serving cell and cannot select any other cell
- The band scan reveals at least n carriers with power level equal or higher than threshold
- On all such carriers, no synchronization is possible

The client can configure the number of minimum disturbing carriers and the power level threshold by using the AT+UCD command [3].

The jamming condition is cleared when any of the above mentioned statements does not hold.

The congestion (i.e. jamming) detection feature can be enabled and configured by the +UCD AT command (for more details see the u-blox AT Commands Manual [3]).

### 1.13.4 TCP/IP and UDP/IP

 Not supported by SARA-G300 and SARA-G310 modules.

Via the AT commands it is possible to access the embedded TCP/IP and UDP/IP stack functionalities over the Packet Switched data connection. For more details about AT commands see u-blox AT Commands Manual [3].

Direct Link mode for TCP and UDP sockets is supported. Sockets can be set in Direct Link mode to establish a transparent end-to-end communication with an already connected TCP or UDP socket via serial interface. In Direct Link mode, data sent to the serial interface from an external application processor is forwarded to the network and vice-versa.

To avoid data loss while using Direct Link, enable HW flow control on the serial interface.

### 1.13.5 FTP

 Not supported by SARA-G300 and SARA-G310 modules.

SARA-G340, SARA-G350 and SARA-U2 series modules support the File Transfer Protocol functionalities via AT commands. Files are read and stored in the local file system of the module.

SARA-U2 series modules support also Secure File Transfer Protocol functionalities providing SSL encryption.

For more details about AT commands see the u-blox AT Commands Manual [3].

### 1.13.6 HTTP


 Not supported by SARA-G300 and SARA-G310 modules.

SARA-G340, SARA-G350 and SARA-U2 modules support Hyper-Text Transfer Protocol functionalities as an HTTP client is implemented: HEAD, GET, POST, DELETE and PUT operations are available. The file size to be uploaded / downloaded depends on the free space available in the local file system (FFS) at the moment of the operation. Up to 4 HTTP client contexts can simultaneously be used.

SARA-U2 modules support also Secure Hyper-Text Transfer Protocol functionalities providing SSL encryption.

For more details about AT commands see the u-blox AT Commands Manual [3].

### 1.13.7 SMTP

 Not supported by SARA-G300, SARA-G310 and SARA-U2 modules.

SARA-G340 and SARA-G350 modules support SMTP client functionalities. It is possible to specify the common parameters (e.g. server data, authentication method, etc. can be specified), to send an email to a SMTP server. Emails can be sent with or without attachment. Attachments are stored in the module local file system.

For more details about AT commands see the u-blox AT Commands Manual [3].

### 1.13.8 SSL



Not supported by SARA-G300 and SARA-G310 modules.



Not supported by SARA-G340-00S and SARA-G350-00S / SARA-G350-00X modules.

The modules support the Secure Sockets Layer (SSL) / Transport Layer Security (TLS) with certificate key sizes up to 4096 bits to provide security over the FTP and HTTP protocols.



The modules:

- support the server authentication without the root certificate verification
- do not support the mutual authentication (use of client certificates)

SSL/TLS Version	SARA-U series	SARA-G series
SSL 2.0	NO	NO
SSL 3.0	YES	NO
TLS 1.0	YES	YES
TLS 1.1	NO	NO
TLS 1.2	NO	NO

**Table 14: SSL/TLS version support**

Algorithm	SARA-U series	SARA-G series
RSA	YES	YES
PSK	NO	YES

**Table 15: Authentication**

Algorithm	SARA-U series	SARA-G series
RC4	YES	YES
DES	NO	YES
3DES	NO	YES
AES128	YES	YES
AES256	NO	YES

**Table 16: Encryption**

Algorithm	SARA-U series	SARA-G series
MD5	YES	YES
SHA/SHA1	YES	YES
SHA256	NO	YES
SHA384	NO	YES

**Table 17: Message digest**

Description	Registry value	SARA-U series	SARA-G series
TLS_RSA_WITH_AES_128_CBC_SHA	0x00,0x2F	YES	YES
TLS_RSA_WITH_AES_128_CBC_SHA256	0x00,0x3C	NO	YES
TLS_RSA_WITH_AES_256_CBC_SHA	0x00,0x35	NO	YES
TLS_RSA_WITH_AES_256_CBC_SHA256	0x00,0x3D	NO	YES
TLS_RSA_WITH_3DES_EDE_CBC_SHA	0x00,0x0A	NO	YES
TLS_RSA_WITH_DES_CBC_SHA	0x00,0x09	NO	YES
TLS_RSA_WITH_RC4_128_MD5	0x00,0x04	YES	YES
TLS_RSA_WITH_RC4_128_SHA	0x00,0x05	YES	YES
TLS_PSK_WITH_AES_128_CBC_SHA	0x00,0x8C	NO	YES
TLS_PSK_WITH_AES_256_CBC_SHA	0x00,0x8D	NO	YES
TLS_PSK_WITH_3DES_EDE_CBC_SHA	0x00,0x8B	NO	YES
TLS_RSA_PSK_WITH_AES_128_CBC_SHA	0x00,0x94	NO	YES
TLS_RSA_PSK_WITH_AES_256_CBC_SHA	0x00,0x95	NO	YES
TLS_RSA_PSK_WITH_3DES_EDE_CBC_SHA	0x00,0x93	NO	YES
TLS_PSK_WITH_AES_128_CBC_SHA256	0x00,0xAE	NO	YES
TLS_PSK_WITH_AES_256_CBC_SHA384	0x00,0xAF	NO	YES
TLS_RSA_PSK_WITH_AES_128_CBC_SHA256	0x00,0xB6	NO	YES
TLS_RSA_PSK_WITH_AES_256_CBC_SHA384	0x00,0xB7	NO	YES

**Table 18: TLS cipher suite registry**

### 1.13.9 Dual stack IPv4/IPv6



Not supported by SARA-G3 modules.

SARA-U2 modules support both Internet Protocol version 4 and Internet Protocol version 6. For more details about dual stack IPv4/IPv6 see the u-blox AT Commands Manual [3].

### 1.13.10 Smart temperature management

Not supported by SARA-G300 and SARA-G310 modules.

Cellular modules – independent of the specific model – always have a well-defined operating temperature range. This range should be respected to guarantee full device functionality and long life span.

Nevertheless there are environmental conditions that can affect operating temperature, e.g. if the device is located near a heating/cooling source, if there is/is not air circulating, etc.

The module itself can also influence the environmental conditions; such as when it is transmitting at full power. In this case its temperature increases very quickly and can raise the temperature nearby.

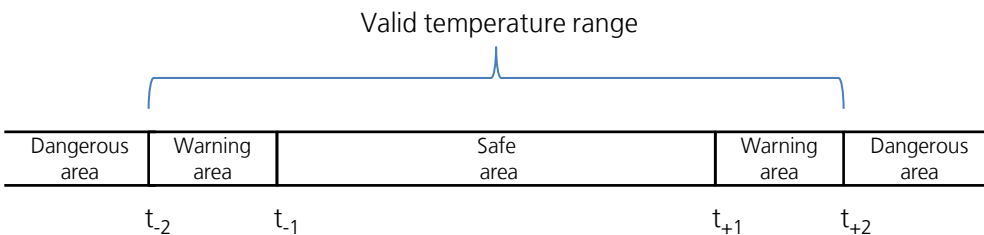
The best solution is always to properly design the system where the module is integrated. Nevertheless an extra check/security mechanism embedded into the module is a good solution to prevent operation of the device outside of the specified range.

#### Smart Temperature Supervisor (STS)

The Smart Temperature Supervisor is activated and configured by a dedicated AT+USTS command. See u-blox AT Commands Manual [3] for more details.

The cellular module measures the internal temperature (Ti) and its value is compared with predefined thresholds to identify the actual working temperature range.

Temperature measurement is done inside the module: the measured value could be different from the environmental temperature (Ta).



**Figure 30: Temperature range and limits**

The entire temperature range is divided into sub-regions by limits (see Figure 30) named  $t_{-2}$ ,  $t_{-1}$ ,  $t_{+1}$  and  $t_{+2}$ .

- Within the first limit, ( $t_{-1} < T_i < t_{+1}$ ), the cellular module is in the normal working range, the Safe Area
- In the Warning Area, ( $t_{-2} < T_i < t_{-1}$ ) or ( $t_{+1} < T_i < t_{+2}$ ), the cellular module is still inside the valid temperature range, but the measured temperature approaches the limit (upper or lower). The module sends a warning to the user (through the active AT communication interface), which can take, if possible, the necessary actions to return to a safer temperature range or simply ignore the indication. The module is still in a valid and good working condition
- Outside the valid temperature range, ( $T_i < t_{-2}$ ) or ( $T_i > t_{+2}$ ), the device is working outside the specified range and represents a dangerous working condition. This condition is indicated and the device shuts down to avoid damage

For security reasons the shutdown is suspended in case an emergency call in progress. In this case the device switches off at call termination.

The user can decide at anytime to enable/disable the Smart Temperature Supervisor feature. If the feature is disabled there is no embedded protection against disallowed temperature conditions.



Figure 31 shows the flow diagram implemented in the SARA-G340 and SARA-G350 modules for the Smart Temperature Supervisor.

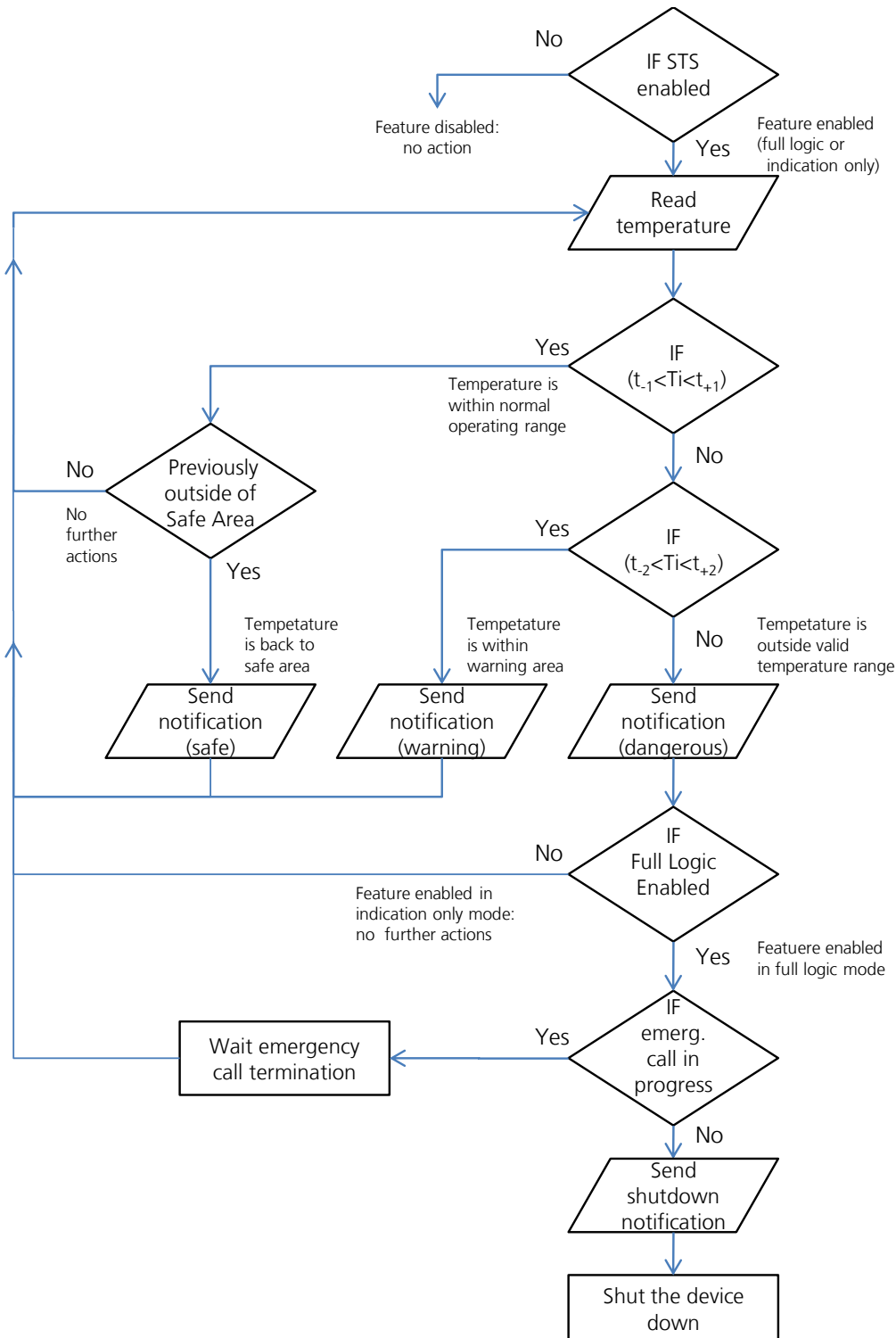


Figure 31: Smart Temperature Supervisor (STS) flow diagram

### Threshold definitions

When the module application operates at extreme temperatures with Smart Temperature Supervisor enabled, the user should note that outside the valid temperature range the device automatically shuts down as described above.

The input for the algorithm is always the temperature measured within the cellular module ( $T_i$ , internal). This value can be higher than the working ambient temperature ( $T_a$ , ambient), since (for example) during transmission at maximum power a significant fraction of DC input power is dissipated as heat. This behavior is partially compensated by the definition of the upper shutdown threshold ( $t_{+2}$ ) that is slightly higher than the declared environmental temperature limit.

Table 19 defines the temperature thresholds for SARA-G340 and SARA-G350 modules.

Symbol	Parameter	Temperature	Remarks
$t_{-2}$	Low temperature shutdown	-40 °C	Equal to the absolute minimum temperature rating for the cellular module (the lower limit of the extended temperature range)
$t_{-1}$	Low temperature warning	-30 °C	10 °C above $t_{-2}$
$t_{+1}$	High temperature warning	+85 °C	10 °C below $t_{+2}$ . The higher warning area for upper range ensures that any countermeasures used to limit the thermal heating will become effective, even considering some thermal inertia of the complete assembly.
$t_{+2}$	High temperature shutdown	+95 °C	Equal to the internal temperature $T_i$ measured in the worst case operating condition at typical supply voltage when the ambient temperature $T_a$ in the reference setup (*) equals the absolute maximum temperature rating (upper limit of the extended temperature range)

(\*) SARA-G340 / SARA-G350 module mounted on a 79 x 62 x 1.41 mm 4-Layers PCB with a high coverage of copper

**Table 19: Thresholds definition for Smart Temperature Supervisor on the SARA-G340 and SARA-G350 modules**

Table 20 defines the temperature thresholds for SARA-U2 modules.

Symbol	Parameter	Temperature	Remarks
$t_{-2}$	Low temperature shutdown	-40 °C	Equal to the absolute minimum temperature rating for the cellular module (the lower limit of the extended temperature range)
$t_{-1}$	Low temperature warning	-30 °C	10 °C above $t_{-2}$
$t_{+1}$	High temperature warning	+77 °C	20 °C below $t_{+2}$ . The higher warning area for upper range ensures that any countermeasures used to limit the thermal heating will become effective, even considering some thermal inertia of the complete assembly.
$t_{+2}$	High temperature shutdown	+97 °C	Equal to the internal temperature $T_i$ measured in the worst case operating condition at typical supply voltage when the ambient temperature $T_a$ in the reference setup (*) equals the absolute maximum temperature rating (upper limit of the extended temperature range)

(\*) SARA-U2 module mounted on a 79 x 62 x 1.41 mm 4-Layers PCB with a high coverage of copper

**Table 20: Thresholds definition for Smart Temperature Supervisor on the SARA-U2 modules**



The sensor measures board temperature inside the shields, which can differ from ambient temperature.

### 1.13.11 AssistNow clients and GNSS integration



Not supported by SARA-G300 and SARA-G310 modules.

For customers using u-blox GNSS receivers, SARA-G340, SARA-G350 and SARA-U2 modules feature embedded AssistNow clients. AssistNow A-GPS provides better GNSS performance and faster Time-To-First-Fix. The clients can be enabled and disabled with an AT command (see the u-blox AT Commands Manual [3]).

SARA-G340, SARA-G350 and SARA-U2 modules act as a stand-alone AssistNow client, making AssistNow available with no additional requirements for resources or software integration on an external host micro controller. Full access to u-blox positioning receivers is available via the cellular modules, through a dedicated DDC (I<sup>2</sup>C) interface, while the available GPIOs can handle the positioning chipset / module power-on/off. This means that the cellular module and the positioning chips and modules can be controlled through a single serial port from any host processor.

### 1.13.12 Hybrid positioning and CellLocate<sup>®</sup>



Not supported by SARA-G300 and SARA-G310 versions.

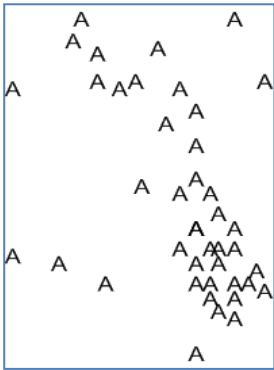
Although GNSS is a widespread technology, reliance on the visibility of extremely weak GNSS satellite signals means that positioning is not always possible, particularly in shielded environments such as indoors and enclosed park houses, or when a GNSS jamming signal is present. The situation can be improved by augmenting GNSS receiver data with network cell information to provide a level of redundancy that can benefit numerous applications.

#### Positioning through cellular information: CellLocate<sup>®</sup>

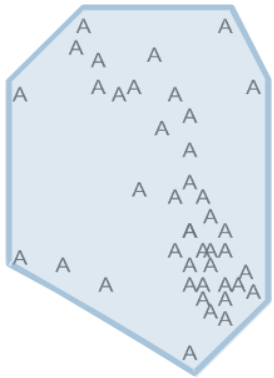
u-blox CellLocate<sup>®</sup> enables the device position estimation based on the parameters of the mobile network cells visible to the specific device. To estimate its position the module sends the CellLocate<sup>®</sup> server the parameters of network cells visible to it using a UDP connection. In return the server provides the estimated position based on the CellLocate<sup>®</sup> database. SARA-G340, SARA-G350 and SARA-U2 modules can either send the parameters of the visible home network cells only (normal scan) or the parameters of all surrounding cells of all mobile operators (deep scan).

The CellLocate<sup>®</sup> database is compiled from the position of devices which observed, in the past, a specific cell or set of cells (historical observations) as follows:

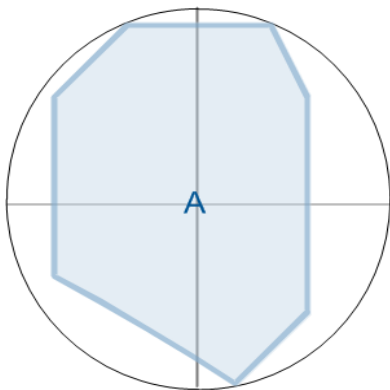
1. Several devices reported their position to the CellLocate<sup>®</sup> server when observing a specific cell (the As in the picture represent the position of the devices which observed the same cell A)



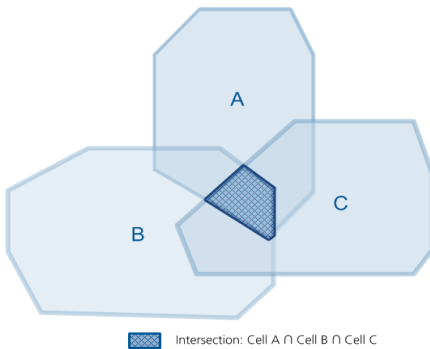
2. CellLocate<sup>®</sup> server defines the area of Cell A visibility



3. If a new device reports the observation of Cell A CellLocate<sup>®</sup> is able to provide the estimated position from the area of visibility



- The visibility of multiple cells provides increased accuracy based on the intersection of areas of visibility.



CellLocate<sup>®</sup> is implemented using a set of two AT commands that allow configuration of the CellLocate<sup>®</sup> service (AT+ULOCCELL) and requesting position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy.



The accuracy of the position estimated by CellLocate<sup>®</sup> depends on the availability of historical observations in the specific area.

### Hybrid positioning

With u-blox hybrid positioning technology, u-blox cellular modules can be triggered to provide their current position using either a u-blox GNSS receiver or the position estimated from CellLocate<sup>®</sup>. The choice depends on which positioning method provides the best and fastest solution according to the user configuration, exploiting the benefit of having multiple and complementary positioning methods.

Hybrid positioning is implemented through a set of three AT commands that allow GNSS receiver configuration (AT+ULOCGNSS), CellLocate<sup>®</sup> service configuration (AT+ULOCCELL), and requesting the position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy (if the position has been estimated by CellLocate<sup>®</sup>), and additional parameters if the position has been computed by the GNSS receiver.

The configuration of mobile network cells does not remain static (e.g. new cells are continuously added or existing cells are reconfigured by the network operators). For this reason, when a hybrid positioning method has been triggered and the GNSS receiver calculates the position, a database self-learning mechanism has been implemented so that these positions are sent to the server to update the database and maintain its accuracy.

The use of hybrid positioning requires a connection via the DDC (I<sup>2</sup>C) bus between the cellular modules and the u-blox GNSS receiver (see section 2.6.4).

See GNSS Implementation Application Note [24] for the complete description of the feature.



u-blox is extremely mindful of user privacy. When a position is sent to the CellLocate<sup>®</sup> server u-blox is unable to track the SIM used or the specific device.

### 1.13.13 Firmware upgrade Over AT (FOAT)

#### Overview

This feature allows upgrading the module Firmware over the AT interface of the module (the UART for SARA-G3 modules, the UART or the USB for SARA-U2 modules), using AT Commands.

- The AT+UFWUPD command triggers a reboot followed by the upgrade procedure at specified a baud rate (see u-blox AT Commands Manual [3] for more details)
- A special boot loader on the module performs firmware installation, security verifications and module reboot
- Firmware authenticity verification is performed via a security signature during the download. The firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader detects a fault at the next wake-up, and restarts the firmware download from the Xmodem-1k handshake. After completing the upgrade, the module is reset again and wakes-up in normal boot

#### FOAT procedure

The application processor must proceed in the following way:

- Send the AT+UFWUPD command through the AT interface, specifying file type and desired baud rate
- Reconfigure serial communication at selected baud rate, with the used protocol
- Send the new FW image via the used protocol

For more details, see the Firmware Update Application Note [25].

### 1.13.14 Firmware upgrade Over The Air (FOTA)



Not supported by SARA-G300 and SARA-G310 modules and SARA-U2 series.



Supported upon request on SARA-G340 and SARA-G350 modules.

This feature allows upgrading the module firmware over the air, i.e. over the cellular network. The main idea with updating firmware over the air is to reduce the amount of data required for transmission to the module. This is achieved by downloading only a “delta file” instead of the full firmware. The delta contains only the differences between the two firmware versions (old and new), and is compressed.

For more details, see the Firmware Update Application Note [25].

### 1.13.15 In-Band modem (eCall / ERA-GLONASS)

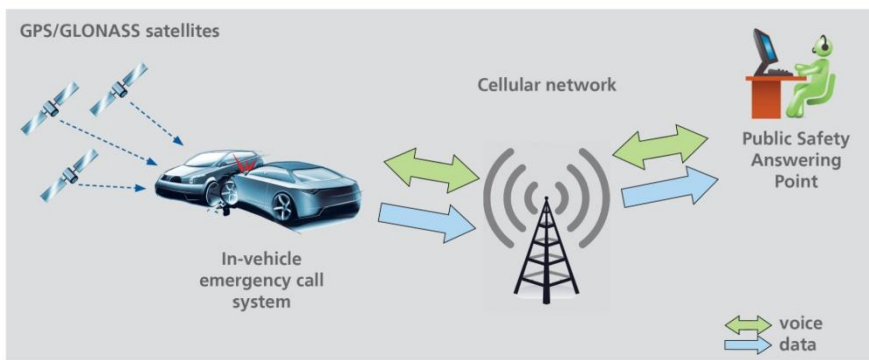


Not supported by SARA-G300 / SARA-G310 / SARA-U260 / SARA-U280 modules.

SARA-G340, SARA-G350 and SARA-U2 modules support an In-Band modem solution for the European eCall and the Russian ERA-GLONASS emergency call applications over cellular networks, implemented according to 3GPP TS 26.267 [22], BS EN 16062:2011 [30] and ETSI TS 122 101 [31] specifications.

eCall (European) and ERA-GLONASS (Russian) are initiatives to combine mobile communications and satellite positioning to provide rapid assistance to motorists in the event of a collision. The eCall automated emergency response system is based on GPS, and the ERA-GLONASS is based on the GLONASS positioning system.

When activated, the in-vehicle systems (IVS) automatically initiate an emergency call carrying both voice and data (including location data) directly to the nearest Public Safety Answering Point (PSAP) to determine whether rescue services should be dispatched to the known position.



**Figure 32: eCall and ERA-GLONASS automated emergency response systems diagram flow**

For more details regarding the In-Band modem solution for the European eCall and the Russian ERA-GLONASS emergency call applications see the u-blox eCall / ERA-GLONASS Application Note [29].

### 1.13.16 SIM Access Profile (SAP)



Not supported by SARA-G3 modules.

SIM access profile (SAP) feature allows SARA-U2 modules to access and use a remote (U)SIM card instead of the local SIM card directly connected to the module (U)SIM interface.

SARA-U2 modules provide a dedicated USB SAP channel and dedicated multiplexer SAP channel over UART for communication with the remote (U)SIM card.

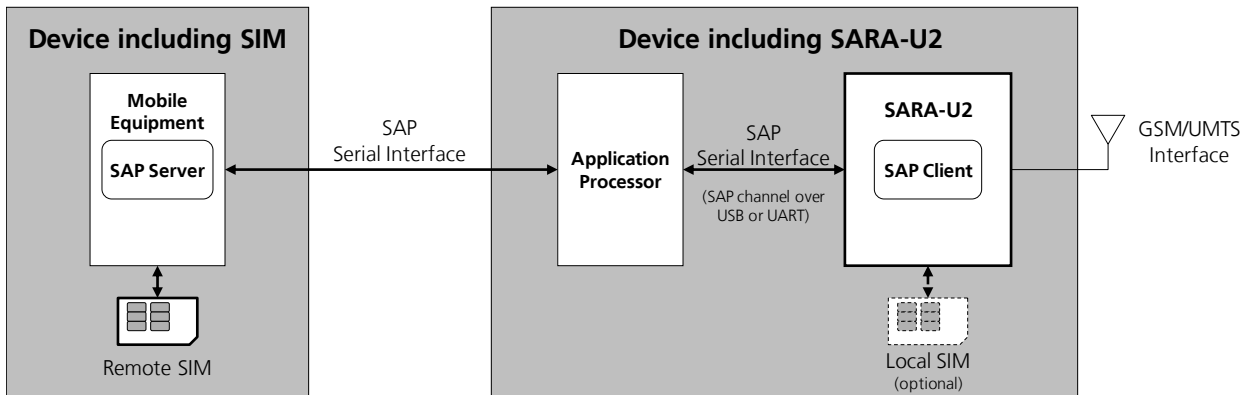
The communication between SARA-U2 modules and the remote SIM is conformed to client-server paradigm: the SARA-U2 module is the SAP client establishing a connection and performing data exchange to an SAP server directly connected to the remote SIM that is used by SARA-U2 module for GSM/UMTS network operations. The SAP communication protocol is based on the SIM Access Profile Interoperability Specification [28].



SARA-U2 modules do not support SAP server role: the module acts as SAP client only.

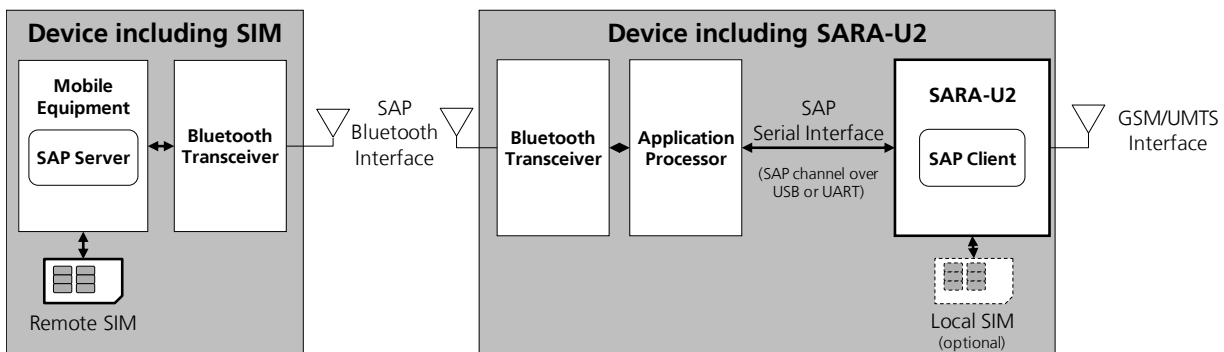
A typical application using the SAP feature is the scenario where a device such as an embedded car-phone with an integrated SARA-U2 module uses a remote SIM included in an external user device (e.g. a simple SIM card reader or a portable phone), which is brought into the car. The car-phone accesses the GSM/UMTS network using the remote SIM in the external device.

SARA-U2 modules, acting as an SAP client, can be connected to an SAP server by a completely wired connection, as shown in Figure 33.



**Figure 33: Remote SIM access via completely wired connection**

As stated in the SIM Access Profile Interoperability Specification [28], the SAP client can be connected to the SAP server by means of a Bluetooth wireless link, using additional Bluetooth transceivers. In this case, the application processor wired to SARA-U2 modules establishes and controls the Bluetooth connection using the SAP profile, and routes data received over a serial interface channel to data transferred over a Bluetooth interface and vice versa, as shown in Figure 34.



**Figure 34: Remote SIM access via Bluetooth and wired connection**

The application processor can start an SAP connection negotiation between SARA-U2 module SAP client and an SAP server using custom AT command (for more details refer to u-blox AT Commands Manual [3]).

While the connection with the SAP server is not fully established, the SARA-U2 module continues to operate with the attached (local) SIM, if present. Once the connection is established and negotiated, the SARA-U2 module performs a detach operation from the local SIM followed by an attach operation to the remote one. Then the remotely attached SIM is used for any GSM/UMTS network operation.

URC indications are provided to inform the user about the state of both the local and remote SIM. The insertion and the removal of the local SIM card are notified if a proper card presence detection circuit using the **SIM\_DET** pin of SARA-U2 modules is implemented as shown in the section 2.5, and if the related "SIM card detection" and "SIM hot insertion/removal" functions are enabled by AT commands (for more details see u-blox AT Commands Manual [3], +UGPIOC, +UDCONF=50 AT commands).

Upon SAP deactivation, the SARA-U2 modules perform a detach operation from the remote SIM followed by an attach operation to the local one, if present.



### 1.13.17 Power saving

The power saving configuration is by default disabled, but it can be enabled using the AT+UPSV command. When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption.

During low power idle-mode, the module is not ready to communicate with an external device by means of the application interfaces, since it is configured to reduce power consumption. It can be woken up from idle-mode to active-mode by the connected application processor, by the connected u-blox positioning receiver or by network activities, as described in Table 6.

During idle-mode, the module processor core runs with the RTC 32 kHz reference clock, which is generated by:

- The internal 32 kHz oscillator, in case of SARA-G340, SARA-G350 and SARA-U2 modules
- The 32 kHz signal provided at the **EXT32K** input pin, in case of SARA-G300 and SARA-G310 modules



SARA-G300 and SARA-G310 need a 32 kHz signal at **EXT32K** input to reach the low power idle-mode.

For the complete description of the AT+UPSV command, refer to the u-blox AT Commands Manual [3].

For the definition and the description of SARA-G3 and SARA-U2 series modules operating modes, including the events forcing transitions between the different operating modes, refer to section 1.4.

For the description of current consumption in idle and active operating modes, refer to sections 1.5.1.4, 1.5.1.5.

For the description of the UART settings related to module power saving configuration, refer to section 1.9.1.4.

For the description of the USB settings related to module power saving configuration, refer to section 1.9.3.2.

For the description of the **EXT32K** input and related application circuit design-in, refer to sections 1.6.4, 2.3.3.

## 2 Design-in

### 2.1 Overview

For an optimal integration of SARA-G3 and SARA-U2 series modules in the final application board follow the design guidelines stated in this section.

Every application circuit must be properly designed to guarantee the correct functionality of the related interface, however a number of points require higher attention during the design of the application device.

The following list provides a ranking of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT** and **ANT\_DET** pins. Antenna circuit directly affects the RF compliance of the device integrating a SARA-G3 and SARA-U2 series module with the applicable certification schemes. Very carefully follow the suggestions provided in section 2.4 for schematic and layout design.
2. Module supply: **VCC** and **GND** pins. The supply circuit affects the RF compliance of the device integrating a SARA-G3 and SARA-U2 series module with applicable certification schemes as well as antenna circuit design. Very carefully follow the suggestions provided in section 2.2.1 for schematic and layout design.
3. USB interface: **USB\_D+**, **USB\_D-** and **VUSB\_DET** pins. Accurate design is required to guarantee USB 2.0 high-speed interface functionality. Carefully follow the suggestions provided in the related section 2.6.1 for schematic and layout design.
4. SIM interface: **VSIM**, **SIM\_CLK**, **SIM\_IO**, **SIM\_RST**, **SIM\_DET** pins. Accurate design is required to guarantee SIM card functionality and compliance with applicable conformance standards, reducing also the risk of RF coupling. Carefully follow the suggestions provided in section 2.5 for schematic and layout design.
5. System functions: **RESET\_N**, **PWR\_ON** pins. Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in section 2.3 for schematic and layout design.
6. Analog audio interface: **MIC\_BIAS**, **MIC\_GND**, **MIC\_P**, **MIC\_N** uplink and **SPK\_P**, **SPK\_N** downlink pins. Accurate design is required to obtain clear and high quality audio reducing the risk of noise from audio lines due to both supply burst noise coupling and RF detection. Carefully follow the suggestions provided in section 2.7.1 for schematic and layout design.
7. Other digital interfaces: UART and auxiliary UART interfaces, DDC I<sup>2</sup>C-compatible interface, digital audio interface and GPIOs. Accurate design is required to guarantee proper functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6.1, 2.6.2, 2.6.4, 2.7.2 and 2.8 for schematic and layout design.
8. 32 kHz signal: the **EXT32K** input pin and the **32K\_OUT** output pin of SARA-G300 and SARA-G310 modules require accurate layout design as it may affect the stability of the RTC reference. Follow the suggestions provided in section 2.3.3 for schematic and layout design.
9. Other supplies: the **V\_BCKP** RTC supply input/output and the **V\_INT** digital interfaces supply output. Accurate design is required to guarantee proper functionality. Follow the suggestions provided in sections 2.2.2 and 2.2.3 for schematic and layout design.

## 2.2 Supply interfaces

### 2.2.1 Module supply (VCC)

#### 2.2.1.1 General guidelines for VCC supply circuit selection and design

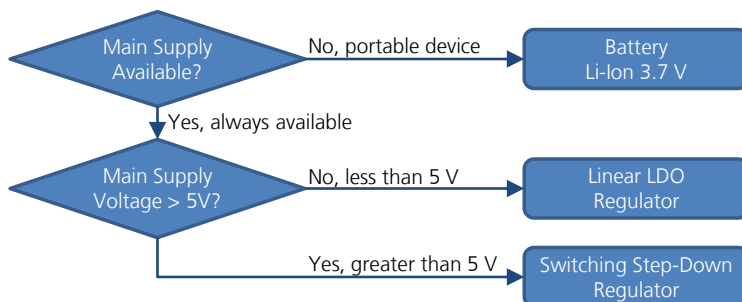
**VCC** pins are internally connected, but connect all the available pins to the external supply to minimize the power loss due to series resistance.

**GND** pins are internally connected but connect all the available pins to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

SARA-G3 and SARA-U2 series modules must be supplied through the **VCC** pins by a proper DC power supply that should comply with the module **VCC** requirements summarized in Table 7.

The proper DC power supply can be selected according to the application requirements (see Figure 35) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery



**Figure 35: VCC supply concept selection**

The DC/DC switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the modules **VCC** operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. Refer to sections 2.2.1.2 and 2.2.1.6, 2.2.1.9, 2.2.1.10 for specific design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less than 5 V). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. Refer to sections 2.2.1.3 and 2.2.1.6, 2.2.1.9, 2.2.1.10 for specific design-in.

If the modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. Refer to sections 2.2.1.4 and 2.2.1.6, 2.2.1.9, 2.2.1.10 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit which is not included in SARA-G3 and SARA-U2 series modules. The charger circuit has to be designed to prevent over-voltage on **VCC** pins of the module, and it should be selected according to the application requirements: a DC/DC switching charger is the typical choice when the charging source has an high nominal

voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time in the application as possible supply source, then a proper charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. Refer to sections 2.2.1.7, 2.2.1.8, 2.2.1.6, 2.2.1.9, and 2.2.1.10 for specific design-in.

The use of a primary (not rechargeable) battery is in general uncommon, but appropriate parts can be selected given that the most cells available are seldom capable of delivering the burst peak current for a GSM call due to high internal resistance. Refer to sections 2.2.1.5, 2.2.1.6, 2.2.1.9, and 2.2.1.10 for specific design-in.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The usage of a regulator or a battery not able to support the highest peak of **VCC** current consumption specified in the SARA-G3 series Data Sheet [1] and in the SARA-U2 series Data Sheet [2] is generally not recommended. However, if the selected regulator or battery is not able to support the highest peak current of the module, it must be able to support at least the highest averaged current consumption value specified in the SARA-G3 series Data Sheet [1] and in the SARA-U2 series Data Sheet [2]. The additional energy required by the module during a 2G Tx slot can be provided by an appropriate bypass tank capacitor or supercapacitor with very large capacitance and very low ESR placed close to the module **VCC** pins. Depending on the actual capability of the selected regulator or battery, the required capacitance can be considerably larger than 1 mF and the required ESR can be in the range of few tens of mΩ. Carefully evaluate the implementation of this solution since aging and temperature conditions significantly affect the actual capacitor characteristics.

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 7.



For the additional specific guidelines for SARA-G350 ATEX modules integration in potentially explosive atmospheres applications, refer to section 2.14.

### 2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail to the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- **Power capability:** the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the specified maximum peak / pulse current with 1/8 duty cycle (refer to the SARA-G3 series Data Sheet [1] or the SARA-U2 series Data Sheet [2]).
- **Low output ripple:** the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **High switching frequency:** for best performance and for smaller applications select a switching frequency  $\geq 600$  kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** voltage profile and therefore negatively impact GSM modulation spectrum performance. An additional L-C low-pass filter between the switching regulator output to **VCC** supply pins can mitigate the ripple on **VCC**, but adds extra voltage drop due to resistive losses on series inductors.

- PWM mode operation:** it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected-mode Pulse Frequency Modulation (PFM) mode and PFM/PWM mode, transitions must be avoided to reduce the noise on the **VCC** voltage profile. Switching regulators that are able to switch between low ripple PWM mode and high efficiency burst or PFM mode can be used, provided the mode transition occurs when the module changes status from idle/active-mode to connected-mode (where current consumption increases to a value greater than 100 mA): it is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold (e.g. 60 mA).
- Output voltage slope:** the use of the soft start function provided by some voltage regulators should be carefully evaluated, since the **VCC** pins voltage must ramp from 2.5 V to 3.2 V in less than 1 ms to switch on the SARA-U2 modules or in less than 4 ms to switch on the SARA-G3 modules by applying **VCC** supply, that otherwise can be switched on by forcing a low level on the **RESET\_N** pin during the **VCC** rising edge and then releasing the **RESET\_N** pin when the **VCC** supply voltage stabilizes at its proper nominal value.

Figure 36 and the components listed in Table 21 show an example of a high reliability power supply circuit, where the module **VCC** is supplied by a step-down switching regulator capable of delivering to **VCC** pins the specified maximum peak / pulse current, with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

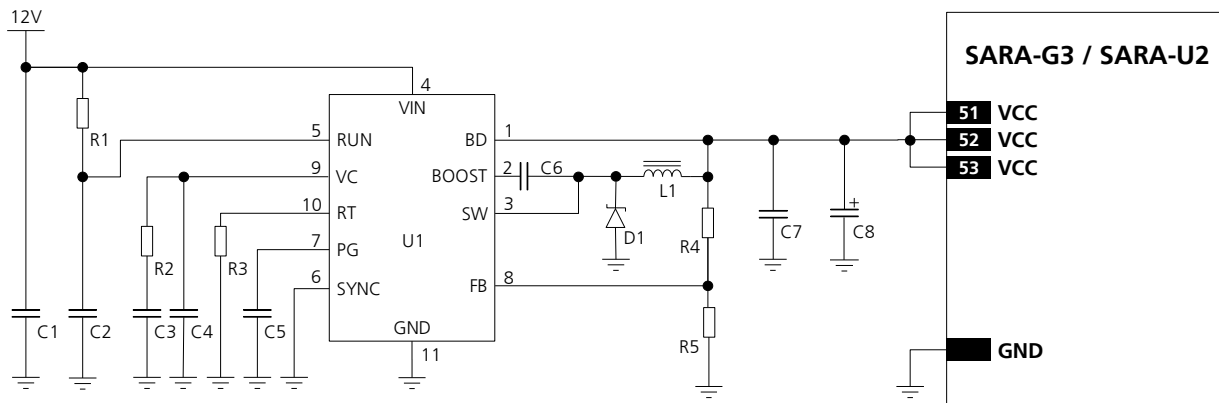


Figure 36: Suggested schematic design for the VCC voltage supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	10 $\mu$ F Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 - Murata
C4	22 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H220JZ01 - Murata
C5	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	470 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E474KA12 - Murata
C7	22 $\mu$ F Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C8	330 $\mu$ F Capacitor Tantalum D_SIZE 6.3 V 45 m $\Omega$	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 $\mu$ H Inductor 744066100 30% 3.6 A	744066100 - Würth Electronics
R1	470 k $\Omega$ Resistor 0402 5% 0.1 W	2322-705-87474-L - Yageo
R2	15 k $\Omega$ Resistor 0402 5% 0.1 W	2322-705-87153-L - Yageo
R3	22 k $\Omega$ Resistor 0402 5% 0.1 W	2322-705-87223-L - Yageo
R4	390 k $\Omega$ Resistor 0402 1% 0.063 W	RC0402FR-07390KL - Yageo
R5	100 k $\Omega$ Resistor 0402 5% 0.1 W	2322-705-70104-L - Yageo
U1	Step-Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 21: Suggested components for the VCC voltage supply application circuit using a step-down regulator

Figure 37 and the components listed in Table 22 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by a step-down switching regulator capable of delivering to **VCC** pins the specified maximum peak / pulse current, transforming a 12 V supply input.

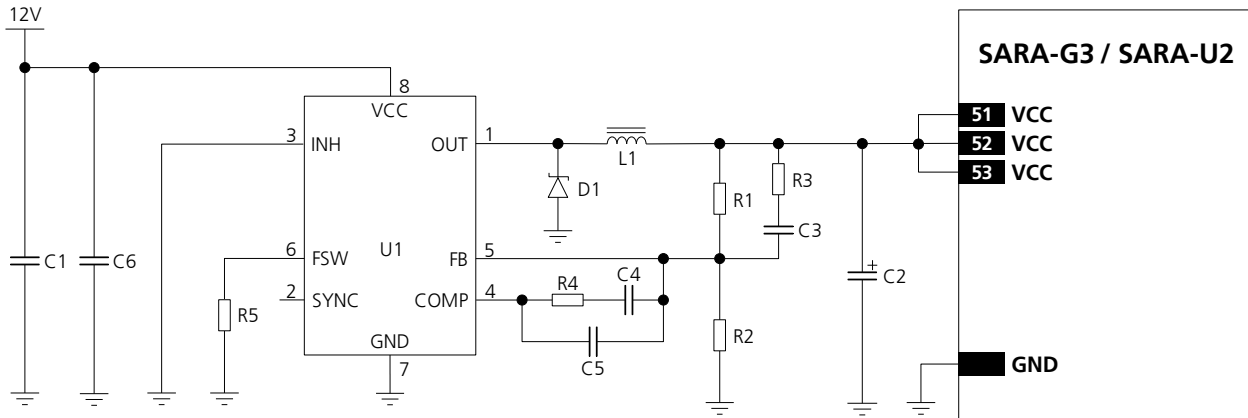


Figure 37: Suggested low cost solution for the VCC voltage supply application circuit using step-down regulator

Reference	Description	Part Number - Manufacturer
C1	22 $\mu$ F Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 – Murata
C2	100 $\mu$ F Capacitor Tantalum B_SIZE 20% 6.3V 15m $\Omega$	T520B107M006ATE015 – Kemet
C3	5.6 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H562KA88 – Murata
C4	6.8 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H682KA88 – Murata
C5	56 pF Capacitor Ceramic COG 0402 5% 50 V	GRM1555C1H560JA01 – Murata
C6	220 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E224KA88 – Murata
D1	Schottky Diode 25V 2 A	STPS2L25 – STMicroelectronics
L1	5.2 $\mu$ H Inductor 30% 5.28A 22 m $\Omega$	MSS1038-522NL – Coilcraft
R1	4.7 k $\Omega$ Resistor 0402 1% 0.063 W	RC0402FR-074K7L – Yageo
R2	910 $\Omega$ Resistor 0402 1% 0.063 W	RC0402FR-07910RL – Yageo
R3	82 $\Omega$ Resistor 0402 5% 0.063 W	RC0402JR-0782RL – Yageo
R4	8.2 k $\Omega$ Resistor 0402 5% 0.063 W	RC0402JR-078K2L – Yageo
R5	39 k $\Omega$ Resistor 0402 5% 0.063 W	RC0402JR-0739KL – Yageo
U1	Step-Down Regulator 8-VFQFPN 3 A 1 MHz	L5987TR – ST Microelectronics

Table 22: Suggested components for low cost solution VCC voltage supply application circuit using a step-down regulator

### 2.2.1.3 Guidelines for VCC supply circuit design using a Low Drop-Out (LDO) linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the **VCC** value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module **VCC** normal operating range.

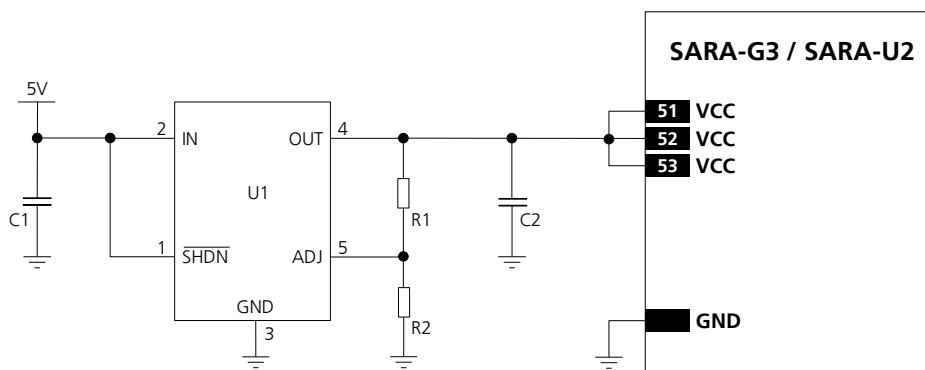
The characteristics of the LDO linear regulator connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- **Power capabilities:** the LDO linear regulator with its output circuit must be capable of providing a proper voltage value to the **VCC** pins and of delivering to **VCC** pins the specified maximum peak / pulse current with 1/8 duty cycle (refer to the SARA-G3 series Data Sheet [1] or the SARA-U2 series Data Sheet [2]).
- **Power dissipation:** the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the max input voltage to the min output voltage to evaluate the power dissipation of the regulator).

- Output voltage slope:** the use of the soft start function provided by some voltage regulator should be carefully evaluated, since the **VCC** pins voltage must ramp from 2.5 V to 3.2 V in less than 1 ms to switch on the SARA-U2 modules or in less than 4 ms to switch on the SARA-G3 modules by applying **VCC** supply, that otherwise can be switched on by forcing a low level on the **RESET\_N** pin during the **VCC** rising edge and then releasing the **RESET\_N** pin when the **VCC** supply voltage stabilizes at its proper nominal value.

Figure 38 and the components listed in Table 23 show an example of a high reliability power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified highest peak / pulse current, with proper power handling capability. The regulator described in this example supports a wide input voltage range, and it includes internal circuitry for reverse battery protection, current limiting, thermal limiting and reverse current protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V as in the circuit described in Figure 38 and Table 23). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.



**Figure 38: Suggested schematic design for the VCC voltage supply application circuit using an LDO linear regulator**

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	9.1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-079K1L - Yageo Phycomp
R2	3.9 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K9L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

**Table 23: Suggested components for VCC voltage supply application circuit using an LDO linear regulator**

Figure 39 and the components listed in Table 24 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified highest peak / pulse current, with proper power handling capability. The regulator described in this example supports a limited input voltage range and it includes internal circuitry for current and thermal protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V as in the circuit described in Figure 39 and Table 24). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.



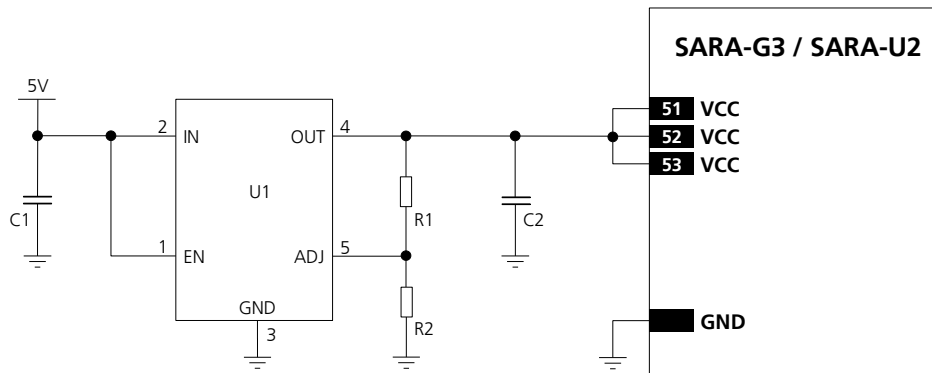


Figure 39: Suggested schematic design for the VCC voltage supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 $\mu$ F Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	27 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-0727KL - Yageo Phycomp
R2	4.7 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LP38501ATJ-ADJ/NOPB - Texas Instrument

Table 24: Suggested components for VCC voltage supply application circuit using an LDO linear regulator

#### 2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable Li-Ion or Li-Pol battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- Maximum pulse and DC discharge current:** the rechargeable Li-Ion battery with its output circuit must be capable of delivering to **VCC** pins the specified maximum peak / pulse current with 1/8 duty cycle, and a DC current greater than the module maximum average current consumption (refer to the SARA-G3 series Data Sheet [1] or the SARA-U2 series Data Sheet [2]). The maximum pulse discharge current and the maximum DC discharge current are not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- DC series resistance:** the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 400 mV during transmit bursts.

#### 2.2.1.5 Guidelines for VCC supply circuit design using a primary (disposable) battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- Maximum pulse and DC discharge current:** the non-rechargeable battery with its output circuit must be capable of delivering to **VCC** pins the specified maximum peak / pulse current with 1/8 duty cycle, and a DC current greater than the module maximum average current consumption (refer to the SARA-G3 series Data Sheet [1] or the SARA-U2 series Data Sheet [2]). The maximum pulse and the maximum DC discharge current is not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- DC series resistance:** the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 400 mV during transmit bursts.



### 2.2.1.6 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The resistance of the power supply lines (connected to the **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize power losses.

Three pins are allocated for **VCC** supply. Another twenty pins are designated for **GND** connection. Even if all the **VCC** pins and all the **GND** pins are internally connected within the module, it is recommended to properly connect all of them to supply the module to minimize series resistance losses.

To avoid voltage drop undershoot and overshoot at the start and end of a transmit burst during a single-slot 2G voice/data call (when current consumption on the **VCC** supply can rise up to the maximum peak / pulse current specified in the SARA-G3 series Data Sheet [1] or in the SARA-U2 series Data Sheet [2]), place a bypass capacitor with large capacitance (more than 100  $\mu\text{F}$ ) and low ESR near the **VCC** pins, for example:

- 330  $\mu\text{F}$  capacitance, 45 m $\Omega$  ESR (e.g. KEMET T520D337M006ATE045, Tantalum Capacitor)

The use of very large capacitors (i.e. greater than 1000  $\mu\text{F}$ ) on the **VCC** line should be carefully evaluated, since the voltage at the **VCC** pins voltage must ramp from 2.5 V to 3.2 V in less than 1 ms to switch on the SARA-U2 modules or in less than 4 ms to switch on the SARA-G3 modules by applying **VCC** supply, that otherwise can be switched on by forcing a low level on the **RESET\_N** pin during the **VCC** rising edge and then releasing the **RESET\_N** pin when the **VCC** supply voltage stabilizes at its proper nominal value.

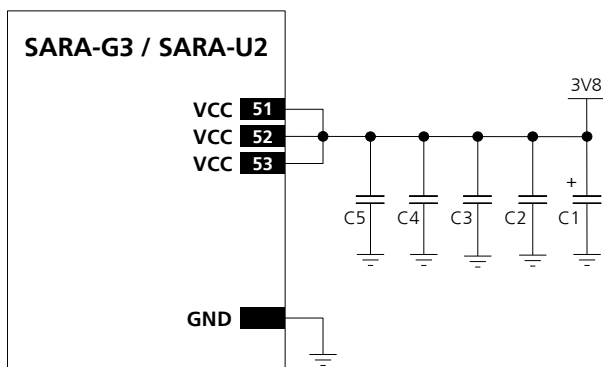
To reduce voltage ripple and noise, especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 100 nF capacitor (e.g. Murata GRM155R61C104K) to filter digital logic noise from clocks and data sources
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noise from clocks and data sources
- 56 pF capacitor with Self-Resonant Frequency in 800/900 MHz range (e.g. Murata GRM1555C1E560J) to filter transmission EMI in the GSM/EGSM bands
- 15 pF capacitor with Self-Resonant Frequency in 1800/1900 MHz range (e.g. Murata GRM1555C1E150J) to filter transmission EMI in the DCS/PCS bands

A series ferrite bead for GHz band noise (e.g. Murata BLM18EG221SN1) can be placed close to the **VCC** pins of the module for additional noise filtering, but in general it is not strictly required.



Figure 40 shows the complete configuration but the mounting of each single component depends on the application design: it is recommended to provide all the **VCC** bypass capacitors as described in Figure 40 and Table 25 if the application device integrates an internal antenna.



**Figure 40: Suggested schematic and layout design for the VCC bypass capacitors to reduce ripple / noise on VCC voltage profile and to avoid undershoot / overshoot on VCC voltage drops**

Reference	Description	Part Number - Manufacturer
C1	330 $\mu$ F Capacitor Tantalum D_SIZE 6.3 V 45 m $\Omega$	T520D337M006ATE045 - KEMET
C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C3	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	56 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C5	15 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1E150JA01 - Murata

**Table 25: Suggested components to reduce ripple / noise on VCC and to avoid undershoot/ overshoot on VCC voltage drops**



ESD sensitivity rating of the **VCC** supply pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to **VCC** pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

### 2.2.1.7 Guidelines for external battery charging circuit

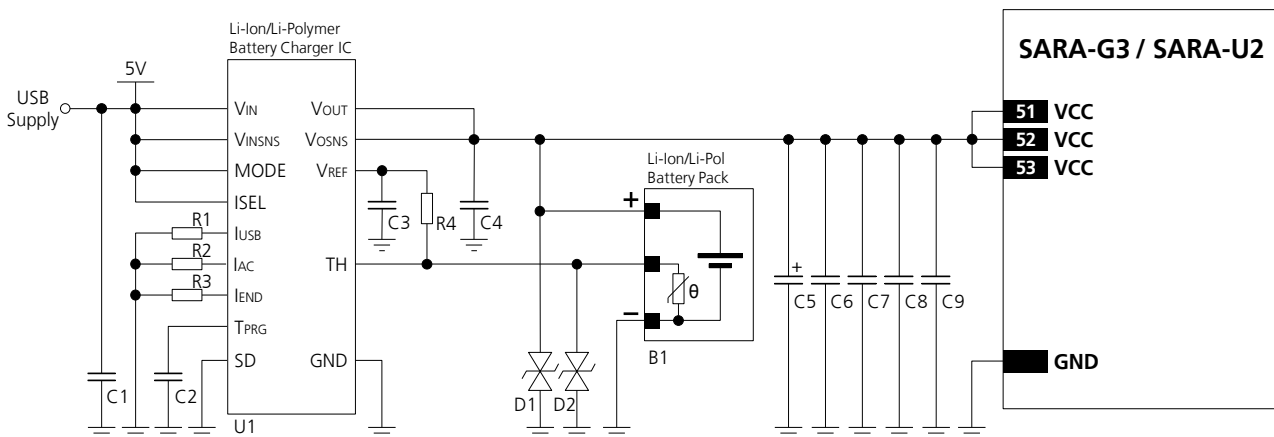
Application devices that are powered by a Li-Ion (or Li-Polymer) battery pack should implement a suitable battery charger design as SARA-G3 and SARA-U2 series modules do not have an on-board charging circuit.

In the application circuit example described in Figure 41, a rechargeable Li-Ion (or Li-Polymer) battery pack, that features proper pulse and DC discharge current capabilities and proper DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is fully managed by the STMicroelectronics L6924U Battery Charger IC that, from a USB source (5.0 V typ.), charges as a linear charger the battery, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for USB power source (~500 mA)
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the L6924U starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor to ~15 mA or when the charging timer reaches the value configured by an external capacitor to ~9800 s

Using a battery pack with an internal NTC resistor, the L6924U can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The L6924U, as linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, refer to the following section 2.2.1.8 for specific design-in), even if the L6924U can also charge from an AC wall adapter as its input voltage range is tolerant up to 12 V: when a current-limited adapter is used, it can operate in quasi-pulse mode, reducing power dissipation.


**Figure 41: Li-Ion (or Li-Polymer) battery charging application circuit**

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 $\Omega$ NTC	Various manufacturer
C1, C4	1 $\mu$ F Capacitor Ceramic X7R 0603 10% 16 V	GRM188R71C105KA12 - Murata
C2, C6	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	1 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H102KA01 - Murata
C5	330 $\mu$ F Capacitor Tantalum D_SIZE 6.3 V 45 m $\Omega$	T520D337M006ATE045 - KEMET
C7	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C8	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C9	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1, R2	24 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-0724KL - Yageo Phycomp
R3	3.3 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-073K3L - Yageo Phycomp
R4	1.0 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
U1	Single Cell Li-Ion (or Li-Polymer) Battery Charger IC for USB port and AC Adapter	L6924U - STMicroelectronics

**Table 26: Suggested components for Li-Ion (or Li-Polymer) battery charging application circuit**

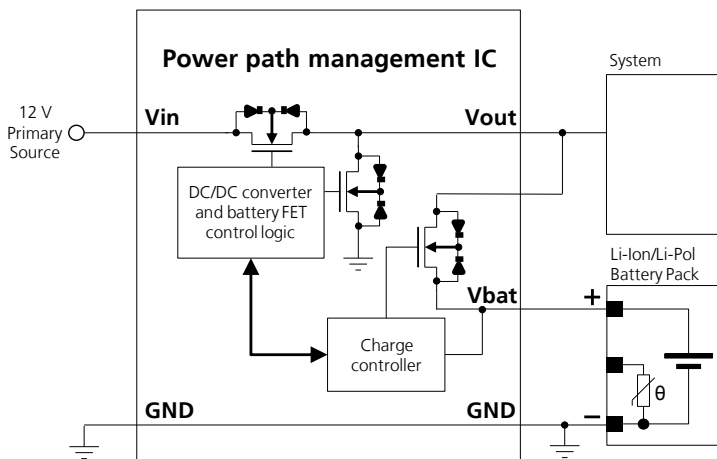
### 2.2.1.8 Guidelines for external battery charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g.  $\sim 12$  V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 42 reports a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g.  $\sim 12$  V) using the integrated regulator which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system: the power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- High efficiency internal step down converter, compliant with the performances specified in section 2.2.1.2
- Low internal resistance in the active path  $V_{out} - V_{bat}$ , typically lower than 50 m $\Omega$
- High efficiency switch mode charger with separate power path control



**Figure 42: Charger / regulator with integrated power path management circuit block diagram**

Figure 43 and the components listed in Table 27 provide an application circuit example where the MPS MP2617 switching charger / regulator with integrated power path management function provides the supply to the cellular module while concurrently and autonomously charging a suitable Li-Ion (or Li-Polymer) battery with proper pulse and DC discharge current capabilities and proper DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617 IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as supply source for the module, and starts a charging phase accordingly.

The MP2617 IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

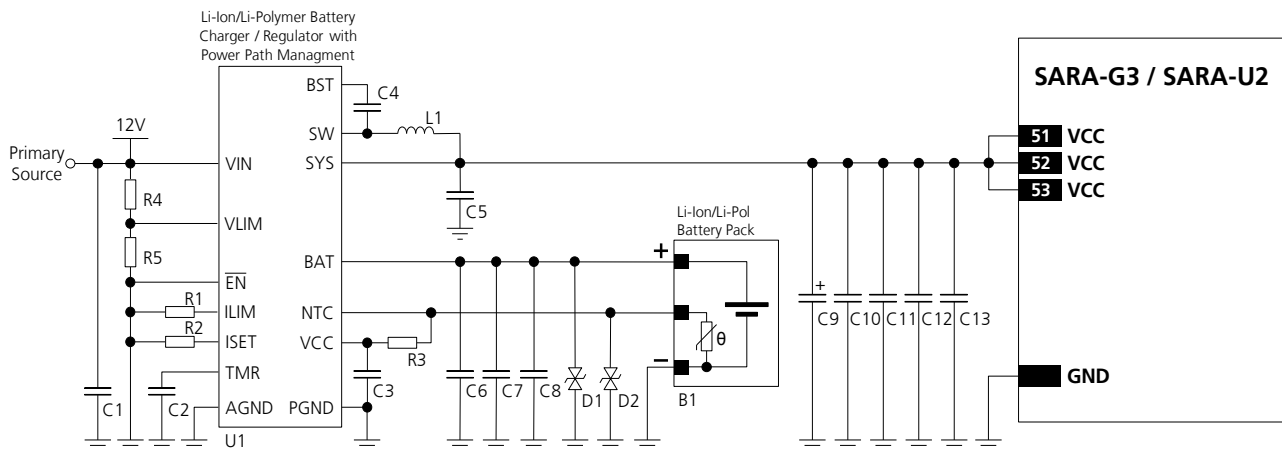
Additionally, the power path control allows an internal connection from battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor

Using a battery pack with an internal NTC resistor, the MP2617 can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, the system output voltage can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: proper resistors or capacitors have to be accordingly connected to the related pins of the IC.



**Figure 43: Li-Ion (or Li-Polymer) battery charging and power path management application circuit**

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 10 k $\Omega$ NTC	Various manufacturer
C1, C5, C6	22 $\mu$ F Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C2, C4, C10	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	1 $\mu$ F Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C7, C12	56 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C8, C13	15 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C9	330 $\mu$ F Capacitor Tantalum D_SIZE 6.3 V 45 m $\Omega$	T520D337M006ATE045 - KEMET
C11	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1, R3, R5	10 k $\Omega$ Resistor 0402 5% 1/16 W	RC0402JR-0710KL - Yageo Phycomp
R2	1.0 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
R4	22 k $\Omega$ Resistor 0402 5% 1/16 W	RC0402JR-0722KL - Yageo Phycomp
L1	1.2 $\mu$ H Inductor 6 A 21 m $\Omega$ 20%	7447745012 - Würth
U1	Li-Ion/Li-Polymer Battery DC/DC Charger / Regulator with integrated Power Path Management function	MP2617 - Monolithic Power Systems (MPS)

**Table 27: Suggested components for Li-Ion (or Li-Polymer) battery charging and power path management application circuit**

### 2.2.1.9 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- **VCC** connection must be as wide as possible and as short as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between **VCC** track and other signal routing.
- Coupling between **VCC** and audio lines (especially microphone inputs) must be avoided, because the typical GSM burst has a periodic nature of approx. 217 Hz, which lies in the audible audio range.
- The tank bypass capacitor with low ESR for current spikes smoothing described in Figure 40 and Table 25 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and cellular module tank capacitor.
- The bypass capacitors in the pF range described in Figure 40 and Table 25 should be placed as close as possible to the **VCC** pins. This is highly recommended if the application device integrates an internal antenna.
- Since **VCC** is directly connected to RF Power Amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the SARA-G3 and SARA-U2 series modules in the worst case.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the cellular module, preferably closer to the DC source (otherwise protection functionality may be compromised).

### 2.2.1.10 Guidelines for grounding layout design

Good connection of the module **GND** pins with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pin surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.
- It is recommended to implement one layer of the application board as ground plane as wide as possible.
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board.
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs.
- Good grounding of **GND** pins also ensures thermal heat sink. This is critical during call connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating.

## 2.2.2 RTC supply (V\_BCKP)

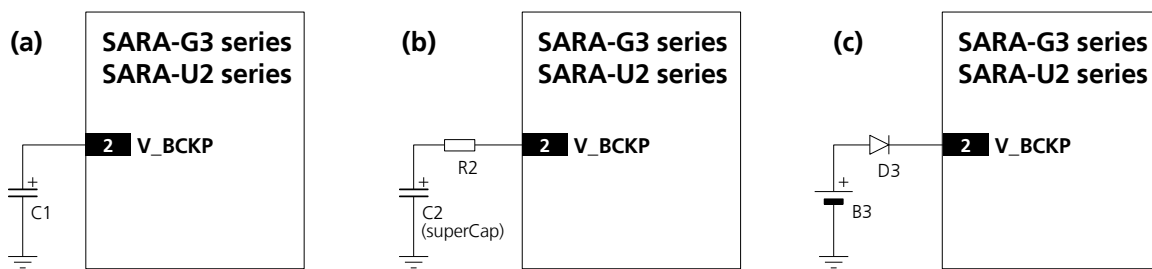
### 2.2.2.1 Guidelines for V\_BCKP circuit design

If RTC timing is required to run for a time interval of  $T$  [s] at 25 °C when **VCC** supply is removed, place a capacitor with a nominal capacitance of  $C$  [ $\mu$ F] at the **V\_BCKP** pin. Choose the capacitor using the following formula:

$$\begin{aligned} C [\mu\text{F}] &= (\text{Current\_Consumption} [\mu\text{A}] \times T [\text{s}]) / \text{Voltage\_Drop} [\text{V}] \\ &= 1.5 \times T [\text{s}] \text{ for SARA-G3 series} \\ &= 2.5 \times T [\text{s}] \text{ for SARA-U2 series} \end{aligned}$$

For example, a 100  $\mu$ F capacitor (such as the Murata GRM43SR60J107M) can be placed at **V\_BCKP** to provide a long buffering time. This capacitor holds **V\_BCKP** voltage within its valid range for around 70 s (SARA-G3 series) or for around 40 s (SARA-U2 series) at 25 °C, after the **VCC** supply is removed.

If a very long buffering time is required, a 70 mF super-capacitor (e.g. Seiko Instruments XH414H-IV01E) can be placed at **V\_BCKP**, with a 4.7 k $\Omega$  series resistor to hold the **V\_BCKP** voltage within its valid range for ~13 hours (SARA-G3 series) or for ~8 hours (SARA-U2 series) at 25 °C, after the **VCC** supply is removed. The purpose of the series resistor is to limit the capacitor charging current due to the large capacitor specifications, and also to let a fast rise time of the voltage value at the **V\_BCKP** pin after **VCC** supply has been provided. These capacitors allow the time reference to run during battery disconnection.



**Figure 44: Real time clock supply (V\_BCKP) application circuits: (a) using a 100  $\mu$ F capacitor to let the RTC run for ~1 minute after VCC removal; (b) using a 70 mF capacitor to let RTC run for ~10 hours after VCC removal; (c) using a non-rechargeable battery**

Reference	Description	Part Number - Manufacturer
C1	100 $\mu$ F Tantalum Capacitor	GRM43SR60J107M - Murata
R2	4.7 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
C2	70 mF Capacitor	XH414H-IV01E - Seiko Instruments

**Table 28: Example of components for V\_BCKP buffering**

If longer buffering time is required to allow the RTC time reference to run during a disconnection of the **VCC** supply, then an external battery can be connected to **V\_BCKP** pin. The battery should be able to provide a proper nominal voltage and must never exceed the maximum operating voltage for **V\_BCKP** (specified in the Input characteristics of Supply/Power pins table in the SARA-G3 series Data Sheet [1] or in the SARA-U2 series Data Sheet [2]). The connection of the battery to **V\_BCKP** should be done with a suitable series resistor for a rechargeable battery, or with an appropriate series diode for a non-rechargeable battery. The purpose of the series resistor is to limit the battery charging current due to the battery specifications, and also to allow a fast rise time of the voltage value at the **V\_BCKP** pin after the **VCC** supply has been provided. The purpose of the series diode is to avoid a current flow from the module **V\_BCKP** pin to the non-rechargeable battery.



If the RTC timing is not required when the **VCC** supply is removed, it is not needed to connect the **V\_BCKP** pin to an external capacitor or battery. In this case the date and time are not updated when **VCC**

is disconnected. If **VCC** is always supplied, then the internal regulator is supplied from the main supply and there is no need for an external component on **V\_BCKP**.

Combining a SARA-G3 or a SARA-U2 cellular module with a u-blox GNSS positioning receiver, the positioning receiver **VCC** supply is controlled by the cellular module by means of the “GNSS supply enable” function provided by the **GPIO2** of the cellular module. In this case the **V\_BCKP** supply output of the cellular module can be connected to the **V\_BCKP** backup supply input pin of the GNSS receiver to provide the supply for the positioning real time clock and backup RAM when the **VCC** supply of the cellular module is within its operating range and the **VCC** supply of the GNSS receiver is disabled. This enables the u-blox GNSS receiver to recover from a power breakdown with either a hot start or a warm start (depending on the duration of the positioning **VCC** outage) and to maintain the configuration settings saved in the backup RAM. Refer to section 2.6.4 for more details regarding the application circuit with a u-blox GNSS receiver.

On SARA-G300 and SARA-G310 modules, the **V\_BCKP** supply output can be used to supply an external 32 kHz oscillator which provides a 32 kHz signal to the **EXT32K** input pin as reference clock for the RTC timing, so that the modules can enter the low power idle-mode and can make available the RTC functions.



The internal regulator for **V\_BCKP** is optimized for low leakage current and very light loads. Do not apply loads which might exceed the limit for maximum available current from **V\_BCKP** supply, as this can cause malfunctions in the module. SARA-G3 series Data Sheet [1] and SARA-U2 series Data Sheet [2] describe the detailed electrical characteristics.

**V\_BCKP** supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.



ESD sensitivity rating of the **V\_BCKP** supply pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible back-up battery connector is directly connected to **V\_BCKP** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4514THSG varistor array) close to the accessible point.

#### 2.2.2.2 Guidelines for **V\_BCKP** layout design

RTC supply (**V\_BCKP**) requires careful layout: avoid injecting noise on this voltage domain as it may affect the stability of the 32 kHz oscillator.



## 2.2.3 Interface supply (V\_INT)

### 2.2.3.1 Guidelines for V\_INT circuit design

The **V\_INT** digital interfaces 1.8 V supply output can be mainly used to:

- Pull-up DDC (I<sup>2</sup>C) interface signals (see section 2.6.4 for more details)
- Pull-up SIM detection signal (see section 2.5 for more details)
- Supply voltage translators to connect digital interfaces of the module to a 3.0 V device (see section 2.6.1)
- Supply a 1.8 V u-blox 6 or subsequent GNSS receiver (see section 2.6.4 for more details)
- Indicate when the module is switched on (see sections 1.6.1, 1.6.2 for more details)



Do not apply loads which might exceed the limit for maximum available current from **V\_INT** supply, as this can cause malfunctions in internal circuitry supplies to the same domain. The SARA-G3 series Data Sheet [1] and the SARA-U2 series Data Sheet [2] describe the detailed electrical characteristics.



**V\_INT** can only be used as an output; do not connect any external regulator on **V\_INT**.

Since the **V\_INT** supply is generated by an internal switching step-down regulator, the **V\_INT** voltage ripple can range from 15 mVpp during active-mode or connected-mode (when the switching regulator operates in PWM mode), to 90 mVpp (SARA-G3 series) or 70 mVpp (SARA-U2 series) in low power idle-mode (when the switching regulator operates in PFM mode).



It is not recommended to supply sensitive analog circuitry without adequate filtering for digital noise.

**V\_INT** supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.



ESD sensitivity rating of the **V\_INT** supply pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.



If the **V\_INT** supply output is not required by the customer application, since DDC (I<sup>2</sup>C) interface and SIM detection functions are not used, voltage translations of digital interfaces are not needed and sensing when the module is switched on is not needed, the **V\_INT** pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of accessible testpoint directly connected to the **V\_INT** pin.

### 2.2.3.2 Guidelines for V\_INT layout design

**V\_INT** digital interfaces supply output is generated by an integrated switching step-down converter, used internally to supply the digital interfaces. Because of this, it can be a source of noise: avoid coupling with sensitive signals.

## 2.3 System functions interfaces

### 2.3.1 Module power-on (PWR\_ON)

#### 2.3.1.1 Guidelines for PWR\_ON circuit design

Connecting the **PWR\_ON** input to a push button that shorts the **PWR\_ON** pin to ground, provide an external pull-up resistor (e.g. 100 k $\Omega$ ) biased by the **V\_BCKP** supply pin of the module, as described in Figure 45 and Table 29. Connecting the **PWR\_ON** input to a push button, the pin will be externally accessible on the application device: according to EMC/ESD requirements of the application, provide an additional ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point.



The **PWR\_ON** pin has high input impedance and is weakly pulled to the high level on the module. Avoid keeping it floating in a noisy environment. To hold the high logic level stable, the **PWR\_ON** pin must be connected to a pull-up resistor (e.g. 100 k $\Omega$ ) biased by the **V\_BCKP** supply pin of the module.



ESD sensitivity rating of the **PWR\_ON** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **PWR\_ON** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

When connecting the **PWR\_ON** input to an external device (e.g. application processor), use an open drain output on the external device with an external pull-up resistor (e.g. 100 k $\Omega$ ) biased by the **V\_BCKP** supply pin of the module, as described in Figure 45 and Table 29.

A compatible push-pull output of an application processor can also be used: in this case the pull-up can be provided to pull the **PWR\_ON** level high when the application processor is switched off. If the high-level voltage of the push-pull output pin of the application processor is greater than the maximum input voltage operating range of the **V\_BCKP** pin (refer to the SARA-G3 series Data Sheet [1] and the SARA-U2 series Data Sheet [2]), the **V\_BCKP** supply cannot be used to bias the pull-up resistor: the supply rail of the application processor or the module **VCC** supply could be used, but this increases the **V\_BCKP** (RTC supply) current consumption when the module is in not-powered mode (**VCC** supply not present). Using a push-pull output of the external device, take care to fix the proper level in all the possible scenarios to avoid an inappropriate module switch-on.

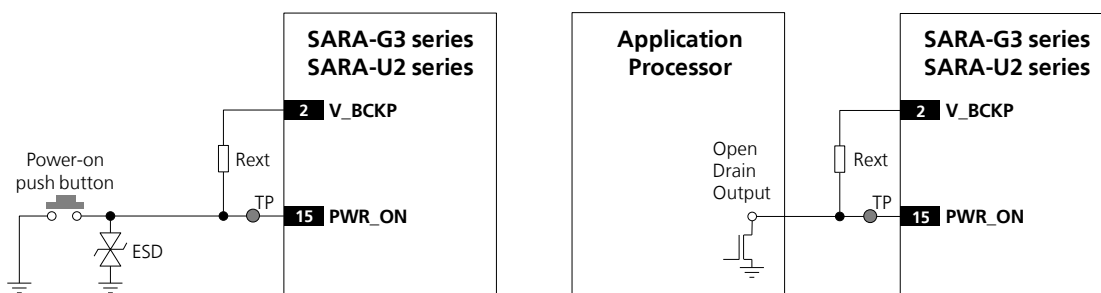


Figure 45: PWR\_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
Rext	100 k $\Omega$ Resistor 0402 5% 0.1 W	External pull-up resistor
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 29: Example of pull-up resistor and ESD protection for the PWR\_ON application circuit



It is recommended to provide direct access to the **PWR\_ON** pin on the application board by means of accessible testpoint directly connected to the **PWR\_ON** pin.

### 2.3.1.2 Guidelines for PWR\_ON layout design

The power-on circuit (**PWR\_ON**) requires careful layout since it is the sensitive input available to switch on the SARA-G3 and SARA-U2 series modules until a valid **VCC** supply is provided after that the module has been switched off by the AT+CPWROFF command: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

## 2.3.2 Module reset (RESET\_N)

### 2.3.2.1 Guidelines for RESET\_N circuit design

As described in Figure 21, the module has an internal pull-up resistor on the reset input line: an external pull-up is not required on the application board.

Connecting the **RESET\_N** input to a push button that shorts the **RESET\_N** pin to ground, the pin will be externally accessible on the application device: according to EMC/ESD requirements of the application, provide an additional ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point, as described in Figure 46 and Table 30.



ESD sensitivity rating of the **RESET\_N** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **RESET\_N** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

Connecting the **RESET\_N** input to an external device (e.g. application processor), an open drain output can be directly connected without any external pull-up, as described in Figure 46 and Table 30: the internal pull-up resistor provided by the module pulls the line to the high logic level when the **RESET\_N** pin is not forced low by the application processor. A compatible push-pull output of an application processor can be used too.

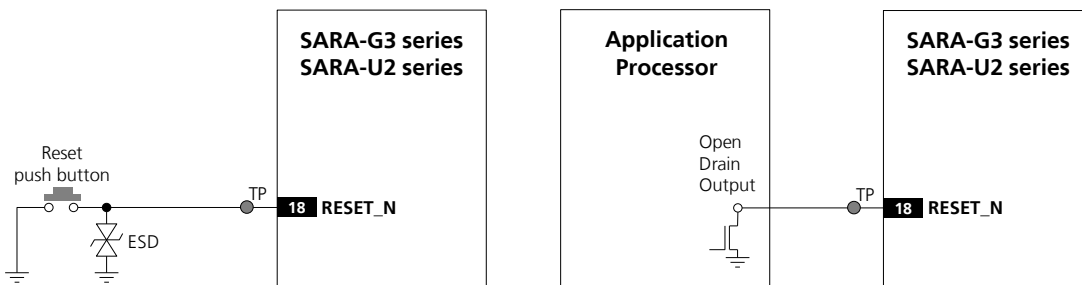


Figure 46: RESET\_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 30: Example of ESD protection component for the RESET\_N application circuit



If the external reset function is not required by the customer application, the **RESET\_N** input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of accessible testpoint directly connected to the **RESET\_N** pin.

### 2.3.2.2 Guidelines for RESET\_N layout design

The reset circuit (**RESET\_N**) requires careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to **RESET\_N** as short as possible.

### 2.3.3 32 kHz signal (EXT32K and 32K\_OUT)



The **EXT32K** and **32K\_OUT** pins are not available on SARA-G340, SARA-G350 and SARA-U2 modules.

#### 2.3.3.1 Guidelines for EXT32K and 32K\_OUT circuit design

The application circuit of Figure 47 describes how the **32K\_OUT** output pin of SARA-G300 / SARA-G310 modules can be connected to the **EXT32K** input pin, providing the 32 kHz signal which constitutes the Real Time Clock (RTC) reference clock, so that the modules can enter the low power idle-mode, reaching low current consumption figures (refer to the section 1.5.1.4 and to the SARA-G3 series Data Sheet [1]), and can provide the RTC functions when the module is switched on.

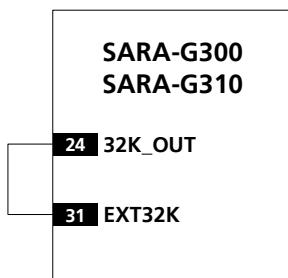


Figure 47: EXT32K application circuit using the 32 kHz signal provided by the 32K\_OUT output

The application circuit of Figure 48 and Table 31 describe how an external oscillator can be connected to the **EXT32K** input pin of SARA-G300 / SARA-G310 modules, providing the external 32 kHz signal which constitutes the RTC reference clock, so that the modules can enter the very low power idle-mode, reaching very low current consumption figures (refer to the section 1.5.1.4 and to the SARA-G3 series Data Sheet [1]), and can provide the RTC functions when the RTC block is switched on since **V\_BCKP** voltage is within the valid range.

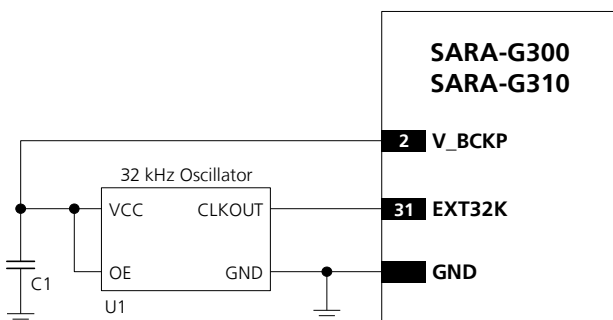


Figure 48: EXT32K application circuit using an external 32 kHz oscillator

Reference	Description	Remarks
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Low Power Clock Oscillator 32.768 kHz	OV-7604-C7 - Micro Crystal or SG-3040LC - EPSON TOYOCOM

Table 31: Example of components for the EXT32K application circuit

The two different solutions described in Figure 47 and Figure 48 are alternative and mutually exclusive: only one of the two proposed solutions must be implemented according to the required current consumption figures for the idle-mode (for the detailed characteristics see the SARA-G3 series Data Sheet [1]).

As additional solution, alternative and mutually exclusive to the two described in Figure 47 and Figure 48, a proper 32 kHz signal can be provided to the **EXT32K** input by the used application processor, if capable.

The **EXT32K** input and the **32K\_OUT** output are not available on SARA-G340 and SARA-G350 modules since the internal oscillator generates the 32 kHz RTC reference clock.



ESD sensitivity rating of the **EXT32K** input pin and the **32K\_OUT** output pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.



If the customer application does not require the low power idle-mode and the RTC functions, the **EXT32K** input pin and the **32K\_OUT** output pin can be left not connected.

### 2.3.3.2 Guidelines for EXT32K and 32K\_OUT layout design

The **EXT32K** input pin and the **32K\_OUT** output pin require accurate layout design: avoid injecting noise on these pins as it may affect the stability of the RTC timing reference.

## 2.4 Antenna interface

The **ANT** pin, provided by all the SARA-G3 and SARA-U2 series modules, represents the RF input/output used to transmit and receive the 2G/3G RF cellular signals: the antenna must be connected to this pin. The **ANT** pin has a nominal characteristic impedance of  $50\ \Omega$  and must be connected to the antenna through a  $50\ \Omega$  transmission line to allow transmission and reception of radio frequency (RF) signals in the 2G and 3G operating bands.

### 2.4.1 Antenna RF interface (ANT)

#### 2.4.1.1 General guidelines for antenna selection and design

The cellular antenna is the most critical component to be evaluated: care must be taken about it at the start of the design development, when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating a SARA-G3 and SARA-U2 series module with all the applicable required certification schemes depends from antenna radiating performance.

Cellular antennas are typically available as:

- External antenna (e.g. linear monopole):
  - External antenna usage basically does not imply physical restrictions on the design of the PCB where the SARA-G3 and SARA-U2 series module is mounted.
  - The radiation performance mainly depends on the antenna: select the antenna with optimal radiating performance in the operating bands.
  - If antenna detection functionality is required, select an antenna assembly provided with a proper built-in diagnostic circuit with a resistor connected to ground: see guidelines in section 2.4.2.
  - Select an RF cable with minimum insertion loss: additional insertion loss due to low quality or long cable reduces radiation performance.
  - Select a suitable  $50\ \Omega$  connector providing proper PCB-to-RF-cable transition: it is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antenna (PCB antennas such as patches or ceramic SMT elements):
  - Internal integrated antenna implies physical restriction to the design of the PCB: the ground plane can be reduced down to a minimum size that must be similar to the quarter of the wavelength of the minimum frequency that has to be radiated. As numerical example:  
 Frequency = 824 MHz → Wavelength = 36.4 cm → Minimum GND plane size = 9.1 cm
  - The radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage: select the antenna with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
  - Select a complete custom antenna designed by an antenna manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide): the antenna design process should begin at the start of the whole product design process.
  - Select an integrated antenna solution provided by an antenna manufacturer if the required ground plane dimensions are large enough according to the related integrated antenna solution specifications: the antenna selection and the definition of its placement in the product layout should begin at the start of the product design process.
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
  - Further to the custom PCB and product restrictions, the antenna may require tuning to obtain the required performance for compliance with the applicable certification schemes. It is recommended to ask the antenna manufacturer for the design-in guidelines related to the custom application.

In both cases, selecting an external or an internal antenna, observe these recommendations:

- Select an antenna providing optimal return loss (or V.S.W.R.) figure over all the operating frequencies.
- Select an antenna providing optimal efficiency figure over all the operating frequencies.
- Select an antenna providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States, as reported in section 4.2.2).



For the additional specific guidelines for SARA-G350 ATEX modules integration in potentially explosive atmospheres applications, see section 2.14.

### 2.4.1.2 Guidelines for antenna RF interface design

#### Guidelines for ANT pin RF connection design

Proper transition between the **ANT** pin and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the pad designed for the **ANT** pin:

- On a multi layer board, the whole layer stack below the RF connection should be free of digital lines
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT** pad, on the top layer of the application PCB, to at least 250  $\mu\text{m}$  up to adjacent pads metal definition and up to 400  $\mu\text{m}$  on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 49
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** pad if the top-layer to buried layer dielectric thickness is below 200  $\mu\text{m}$ , to reduce parasitic capacitance to ground, as described in the right picture in Figure 49

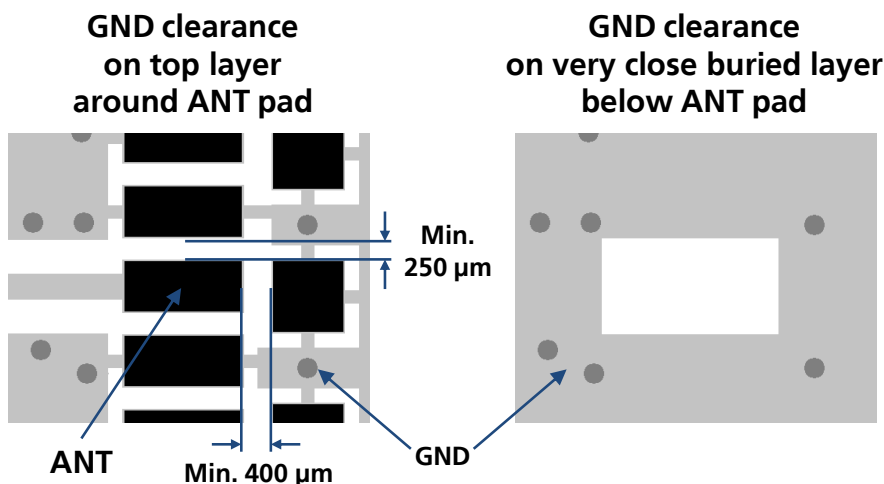


Figure 49: GND keep-out area on the top layer around ANT pad and on the very close buried layer below ANT pad

#### Guidelines for RF transmission line design

The transmission line from the **ANT** pad up to antenna connector or up to the internal antenna pad must be designed so that the characteristic impedance is as close as possible to 50  $\Omega$ .

The transmission line can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 50 and Figure 51 provide two examples of proper  $50\ \Omega$  coplanar waveguide designs. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

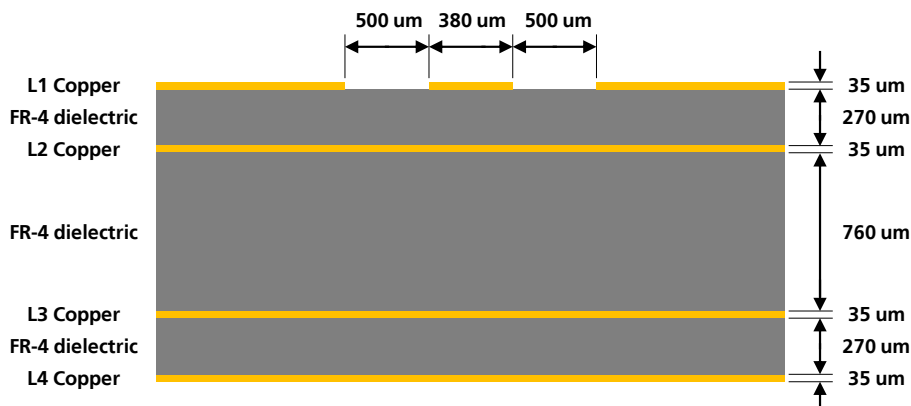


Figure 50: Example of  $50\ \Omega$  coplanar waveguide transmission line design for the described 4-layer board layout

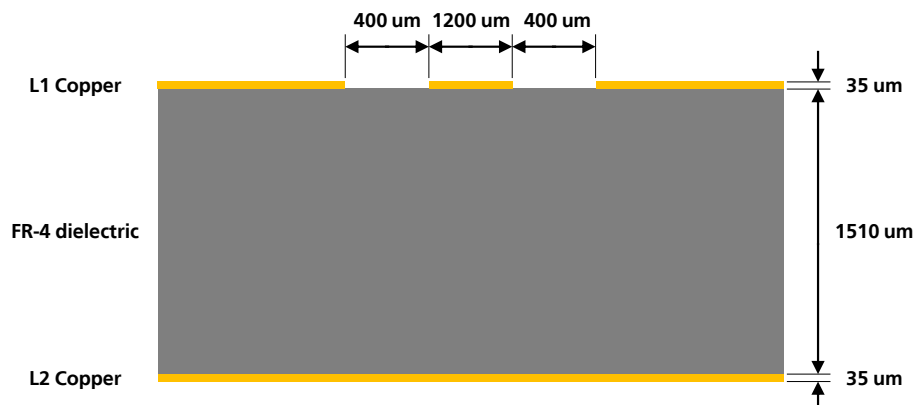


Figure 51: Example of  $50\ \Omega$  coplanar waveguide transmission line design for the described 2-layer board layout

If the two examples do not match the application PCB layout, the  $50\ \Omega$  characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like AppCAD from Agilent ([www.agilent.com](http://www.agilent.com)) or TXLine from Applied Wave Research ([www.mwoffice.com](http://www.mwoffice.com)), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a  $50\ \Omega$  characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35  $\mu\text{m}$  in the example of Figure 50 and Figure 51)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270  $\mu\text{m}$  in Figure 50, 1510  $\mu\text{m}$  in Figure 51)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 50 and Figure 51)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500  $\mu\text{m}$  in Figure 50, 400  $\mu\text{m}$  in Figure 51)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for the  $50\ \Omega$  calculation.



Additionally to the 50  $\Omega$  impedance, the following guidelines are recommended for the transmission line design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission line, if top-layer to buried layer dielectric thickness is below 200  $\mu\text{m}$ , to reduce parasitic capacitance to ground.
- The transmission line width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND.
- Add GND vias around transmission line, as described in Figure 52.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough on the adjacent metal layer, as described in Figure 52.
- Route RF transmission line far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as analog audio lines).
- Avoid stubs on the transmission line.
- Avoid signal routing in parallel to transmission line or crossing the transmission line on buried metal layer.
- Do not route microstrip line below discrete component or other mechanics placed on top layer.

Two examples of proper RF circuit design are reported in the Figure 52, where the antenna detection circuit is not implemented (if the antenna detection function is required by the application, follow the guidelines for circuit and layout implementation reported in section 2.4.2):

- In the first example described on the left, the **ANT** pin is directly connected to an SMA connector by means of a proper 50  $\Omega$  transmission line, designed with proper layout.
- In the second example described on the right, the **ANT** pin is connected to an SMA connector by means of a proper 50  $\Omega$  transmission line, designed with proper layout, with an additional high pass filter (consisting of a proper series capacitor and a proper shunt inductor) to improve the ESD immunity at the antenna port of SARA-U2 modules as described in section 2.13 (a series 0  $\Omega$  jumper can be mounted for SARA-G3 modules instead of the high pass filter as no further precaution to ESD immunity test is needed).

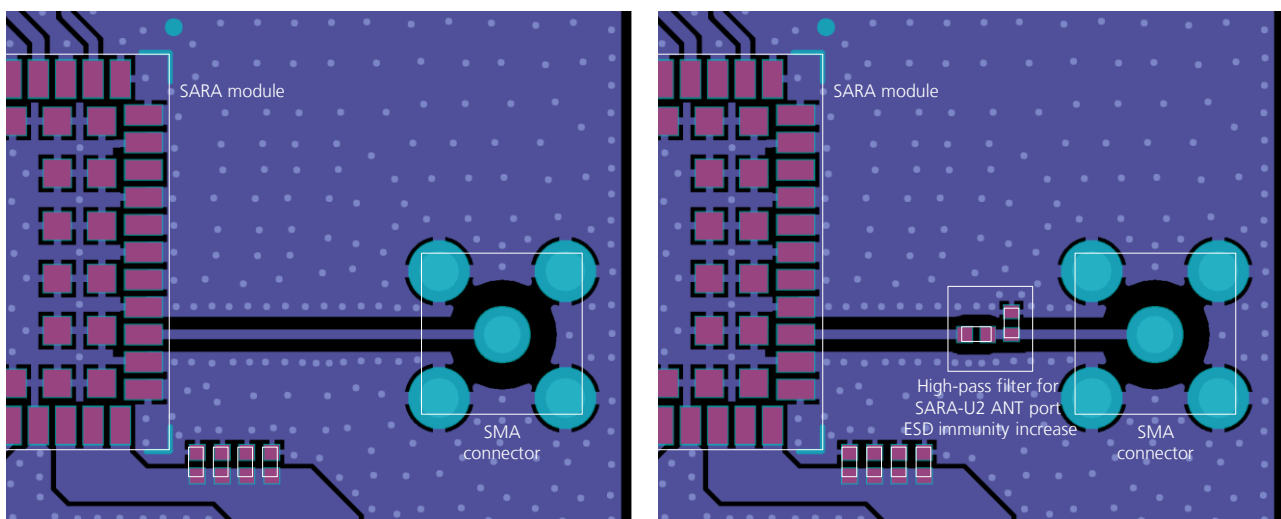


Figure 52: Suggested circuit and layout for antenna RF circuit on application board, if antenna detection is not required

### Guidelines for RF termination design

The RF termination must provide a characteristic impedance of  $50\ \Omega$  as well as the RF transmission line up to the RF termination itself, to match the characteristic impedance of the **ANT** pin of the module.

However, real antennas do not have perfect  $50\ \Omega$  load on all the supported frequency bands. Therefore, to reduce as much as possible performance degradation due to antenna mismatch, the RF termination must provide optimal return loss (or V.S.W.R.) figure over all the operating frequencies, as summarized in Table 10.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use a suitable  $50\ \Omega$  connector providing proper PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts, as shown in Figure 52.
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads.
- Cut out the GND layer under RF connectors and close to buried vias, to remove stray capacitance and thus keep the RF line  $50\ \Omega$ : e.g. the active pad of U.FL connectors needs to have a GND keep-out (i.e. clearance, a void area) at least on first inner layer to reduce parasitic capacitance to ground

If an integrated antenna is used, the RF termination is represented by the integrated antenna itself:

- Use an antenna designed by an antenna manufacturer, providing the best possible return loss (or V.S.W.R.).
- Provide a ground plane large enough according to the related integrated antenna requirements: the ground plane of the application PCB can be reduced to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated. As numerical example:  
 Frequency = 824 MHz → Wavelength = 36.4 cm → Minimum GND plane size = 9.1 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for the antenna related to the custom application.

Additionally, these recommendations regarding the antenna system must be followed:

- Do not include antenna within closed metal case.
- Do not place the antenna in close vicinity to end users, since the emitted radiation in human tissue is limited by regulatory requirements.
- Place the antenna far from sensitive analog systems or employ countermeasures to reduce electromagnetic compatibility issues.
- Take care of interaction between co-located RF systems since the GSM / UMTS transmitted RF power may interact or disturb the performance of companion systems.
- The antenna shall provide optimal efficiency figure over all the operating frequencies.
- The antenna shall provide appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity does not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States, as reported in section 4.2.2).

## Examples of antennas

Table 32 lists some examples of possible internal on-board surface-mount antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	PA.25.A	Anam	GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 36.0 x 6.0 x 5.0 mm
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PCS.06.A	Havok	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2500..2690 MHz 42.0 x 10.0 x 3.0 mm
Antenova	A10340	Calvus	GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 28.0 x 8.0 x 3.2 mm
Ethertronics	P522304	Prestta	GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 35.0 x 9.0 x 3.2 mm
2J	2JE04		GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 24.0 x 5.5 x 4.4 mm
Yaego	ANT3505B000TWPENA		GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 35.0 x 5.0 x 6.0 mm

**Table 32: Examples of internal surface-mount antennas**

Table 33 lists some examples of possible internal off-board PCB-type antennas with cable and connector.

Manufacturer	Part Number	Product Name	Description
Taoglas	FXP14.A.07.0100A		GSM / WCDMA PCB Antenna with cable and U.FL connector 824..960 MHz, 1710..2170 MHz 70.4 x 20.4 mm
Taoglas	FXP14R.A.07.0100A		GSM / WCDMA PCB Antenna with cable and U.FL connector Integrated 10k shunt diagnostic resistor 824..960 MHz, 1710..2170 MHz 80.0 x 20.8 mm
Taoglas	PC29.09.0100A	TheStripe	GSM / WCDMA PCB Antenna with cable and MMCX(M)RA connector 824..960 MHz, 1710..2170 MHz 80.4 x 29.4 mm
Taoglas	FXUB63.07.0150C		GSM / WCDMA / LTE PCB Antenna with cable and U.FL connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Ethertronics	P522310	Prestta	GSM / WCDMA PCB Antenna with cable and U.FL connector 824..960 MHz, 1710..2170 MHz 41.0 x 15.0 mm
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE PCB Antenna with cable and U.FL connector 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm
Yaego	ANTX100P001BWPEN3		GSM / WCDMA PCB Antenna with cable and I-PEX connector 824..960 MHz, 1710..2170 MHz 50.0 x 20.0 mm

**Table 33: Examples of internal antennas with cable and connector**

Table 34 lists some examples of possible external antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	GSA.8827.A.101111	Phoenix	GSM / WCDMA / LTE low-profile adhesive-mount Antenna with cable and SMA(M) connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2490..2690 MHz 105 x 30 x 7.7 mm
Taoglas	GSA.8821.A.301721	I-Bar	GSM / WCDMA low-profile adhesive-mount Antenna with cable and Fakra (code-D) connector 824..960 MHz, 1710..2170 MHz 106.7 x 14.7 x 5.8 mm
Taoglas	TG.30.8112		GSM / WCDMA / LTE swivel dipole Antenna with SMA(M) connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz 148.6 x 49 x 10 mm
Taoglas	OMB.8912.03F21		GSM / WCDMA pole-mount Antenna with N-type (F) connector 824..960 MHz, 1710..2170 MHz 527 x Ø 26 mm
Taoglas	FW.92.RNT.M		GSM / WCDMA whip monopole Antenna with RP-N-type(M) connector 824..960 MHz, 1710..2170 MHz 274 x Ø 20 mm
Nearson	T6150AM		GSM / WCDMA swivel monopole Antenna with SMA(M) connector 824..960 MHz, 1710..2170 MHz 179.3 x 22 x 6.5 mm
Laird Tech.	MAF94300	HEPTA-SM	GSM / WCDMA swivel monopole Antenna with SMA(M) connector 824..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2500 MHz 161 x 9.3 mm
Laird Tech.	TRA806/171033P		GSM / WCDMA screw-mount Antenna with N-type(F) connector 824..960 MHz, 1710..2170 MHz 69.8 x Ø 38.1 mm
Laird Tech.	CMS69273		GSM / WCDMA / LTE ceiling-mount Antenna with N-type(F) connector 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount Antenna with N-type(M) connector 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Abracon	APAMS-102		GSM / WCDMA low-profile adhesive-mount Antenna with cable and SMA(M) connector 824..960 MHz, 1710..2170 MHz 138 x 21 x 6 mm

**Table 34: Examples of external antennas**

## 2.4.2 Antenna detection interface (ANT\_DET)



Antenna detection interface (**ANT\_DET**) is not supported by SARA-G300 and SARA-G310 modules.

### 2.4.2.1 Guidelines for ANT\_DET circuit design

Figure 53 and Table 35 describe the recommended schematic and components for the antenna detection circuit to be provided on the application board for the diagnostic circuit that must be provided on the antenna assembly to achieve antenna detection functionality.

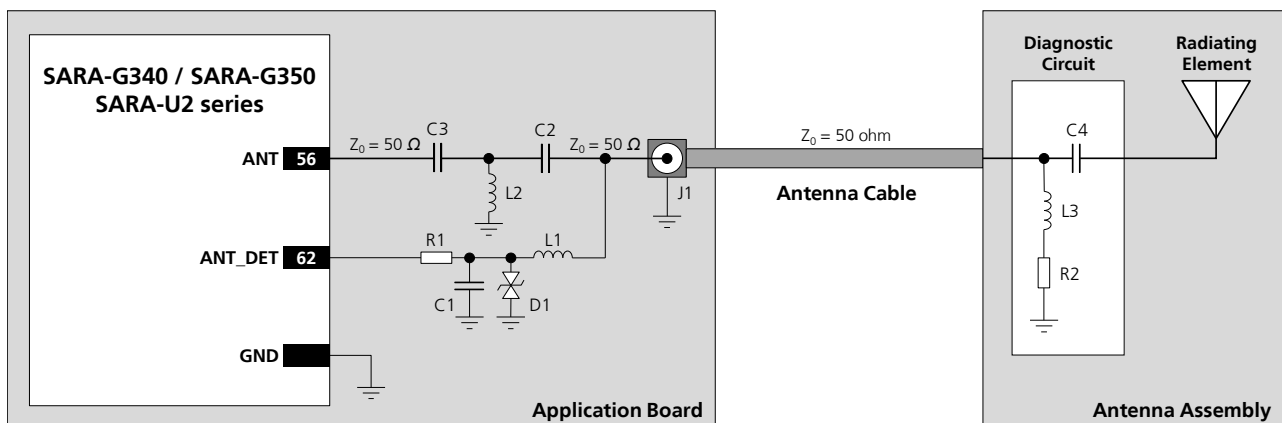


Figure 53: Suggested schematic for antenna detection circuit on application board and diagnostic circuit on antenna assembly

Reference	Description	Part Number - Manufacturer
C1	27 pF Capacitor Ceramic COG 0402 5% 50 V	GRM1555C1H270J - Murata
C2	33 pF Capacitor Ceramic COG 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
L1	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ Resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1	SMA Connector 50 Ω Through Hole Jack	SMA6251A1-3GT50G-50 - Amphenol
C3	SARA:U2: 15 pF Capacitor Ceramic COG 0402 5% 50 V SARA-G3: 0 Ω jumper 0402	GRM1555C1H150J - Murata Various Manufacturers
L2	SARA:U2: 39 nH Multilayer Inductor 0402 (SRF ~1 GHz) SARA-G3: Do not install	LQG15HN39NJ02 - Murata
C4	22 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H220J - Murata
L3	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2	15 kΩ Resistor for Diagnostic	Various Manufacturers

Table 35: Suggested components for antenna detection circuit on application board and diagnostic circuit on antenna assembly

The antenna detection circuit and diagnostic circuit suggested in Figure 53 and Table 35 are here explained:

- When antenna detection is forced by the +UANTR AT command, the **ANT\_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C3) to decouple the DC current generated by the **ANT\_DET** pin.
- Choke inductors with a Self Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT\_DET** pin (L1) and in series at the diagnostic resistor (L2), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Additional components (R1, C1 and D1 in Figure 53) are needed at the **ANT\_DET** pin as ESD protection.

- Additional high pass filter (C3 and L2 in Figure 53) is provided at the **ANT** pin as ESD immunity improvement for SARA-U2 modules (a series 0  $\Omega$  jumper can be mounted for SARA-G340 and SARA-G350 modules instead of the high pass filter, as no further precaution to ESD immunity test is needed).
- The **ANT** pin must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50  $\Omega$ .

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 53, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.



It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 k $\Omega$  to 30 k $\Omega$  to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with built-in DC load resistor of 15 k $\Omega$ . Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

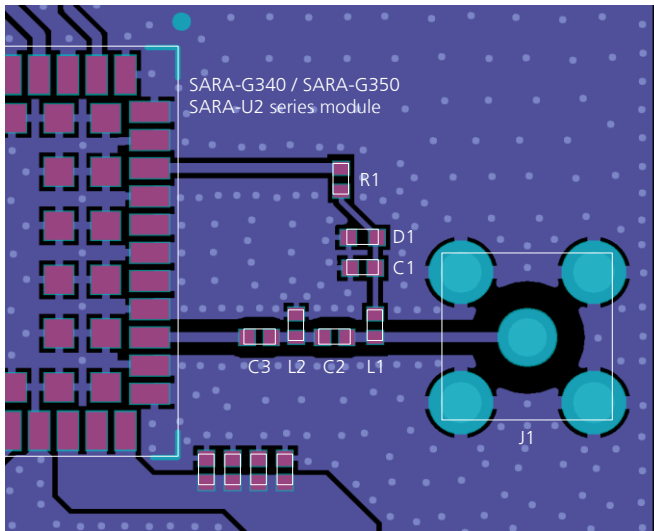
- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 k $\Omega$  to 17 k $\Omega$  if a 15 k $\Omega$  diagnostic resistor is used) indicate that the antenna is properly connected.
- Values close to the measurement range maximum limit (approximately 50 k $\Omega$ ) or an open-circuit "over range" report (see u-blox AT Commands Manual [3]) means that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 k $\Omega$ ) highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostic.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.



If the antenna detection function is not required by the customer application, the **ANT\_DET** pin can be left not connected and the **ANT** pin can be directly connected to the antenna connector by means of a 50  $\Omega$  transmission line as described in Figure 52.

### 2.4.2.2 Guidelines for ANT\_DET layout design

Figure 54 describes the recommended layout for the antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in the previous Figure 53 and Table 35.



**Figure 54: Suggested layout for antenna detection circuit on application board**

The antenna detection circuit layout suggested in Figure 54 is here explained:

- The **ANT** pin is connected to the antenna connector by means of a 50  $\Omega$  transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at the **ANT** pin (C2) is placed in series to the 50  $\Omega$  transmission line.
- The **ANT\_DET** pin is connected to the 50  $\Omega$  transmission line by means of a sense line.
- Choke inductor in series at the **ANT\_DET** pin (L1) is placed so that one pad is on the 50  $\Omega$  transmission line and the other pad represents the start of the sense line to the **ANT\_DET** pin.
- The additional components (R1, C1 and D1) on the **ANT\_DET** line are placed as ESD protection.
- The additional high pass filter (C3 and L2) on the **ANT** line are placed as ESD immunity improvement for SARA-U2 modules (a series 0  $\Omega$  jumper can be mounted for SARA-G340 and SARA-G350 modules instead of the high pass filter, as no further precaution to ESD immunity test is needed).

## 2.5 SIM interface

### 2.5.1.1 Guidelines for SIM circuit design

#### Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC) which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the cellular network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM\_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM\_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It must be connected to **VSIM**
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM\_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1 = VCC, C2 = RST, C3 = CLK, C5 = GND, C6 = VPP, C7 = I/O) or 8 contacts, providing also the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses. Only 6 contacts are required and must be connected to the module SIM card interface as described above, since the modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Removable SIM card are suitable for applications where the SIM changing is required during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins related to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided: select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Solderable UICC / SIM chip contacts mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as follows:

- Package Pin 8 = UICC Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Package Pin 7 = UICC Contact C2 = RST (Reset) → It must be connected to **SIM\_RST**
- Package Pin 6 = UICC Contact C3 = CLK (Clock) → It must be connected to **SIM\_CLK**
- Package Pin 5 = UICC Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Package Pin 1 = UICC Contact C5 = GND (Ground) → It must be connected to **GND**
- Package Pin 2 = UICC Contact C6 = VPP (Programming supply) → It must be connected to **VSIM**
- Package Pin 3 = UICC Contact C7 = I/O (Data input/output) → It must be connected to **SIM\_IO**
- Package Pin 4 = UICC Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A solderable SIM chip has 8 contacts and can provide also the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above, since SARA-G3 and SARA-U2 modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.



### Guidelines for single SIM card connection without detection

An application circuit for the connection to a single removable SIM card placed in a SIM card holder is described in Figure 55, where the optional SIM detection feature is not implemented (see the circuit described in Figure 57 if the SIM detection feature is required).

Follow these guidelines connecting the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) and C6 (VPP) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM\_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM\_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM\_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM\_CLK**, **SIM\_IO**, **SIM\_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector: ESD sensitivity rating of the SIM interface pins is 1 kV (Human Body Model according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal (**SIM\_CLK**, **SIM\_IO**, **SIM\_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM\_CLK** line, 1.0  $\mu$ s is the maximum allowed rise time on the **SIM\_IO** and **SIM\_RST** lines).

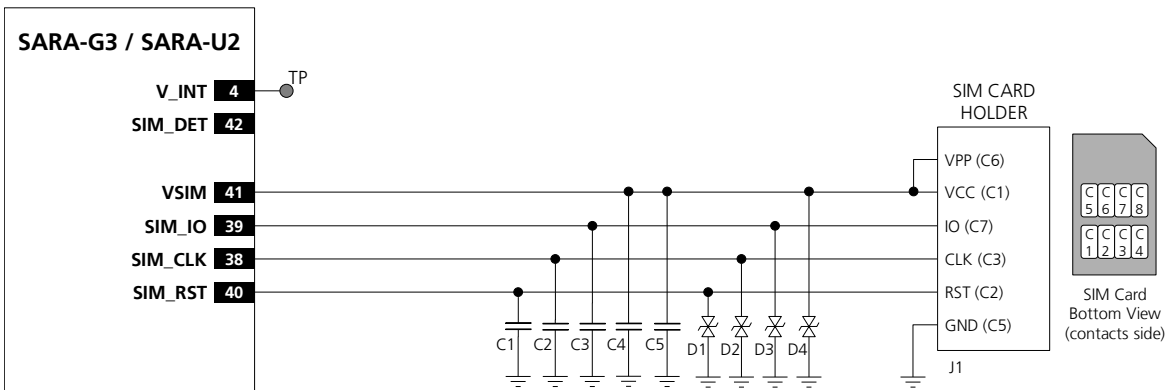


Figure 55: Application circuit for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
J1	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, C707 10M006 136 2 - Amphenol

Table 36: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

### Guidelines for single SIM chip connection

An application circuit for the connection to a single solderable SIM chip (M2M UICC Form Factor) is described in Figure 56, where the optional SIM detection feature is not implemented (see the circuit described in Figure 57 if the SIM detection feature is required).

Follow these guidelines connecting the module to a solderable SIM chip without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) and C6 (VPP) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM\_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM\_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM\_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**) close to the related pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM\_CLK**, **SIM\_IO**, **SIM\_RST**), to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Limit capacitance and series resistance on each SIM signal (**SIM\_CLK**, **SIM\_IO**, **SIM\_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM\_CLK** line, 1.0  $\mu$ s is the maximum allowed rise time on the **SIM\_IO** and **SIM\_RST** lines).

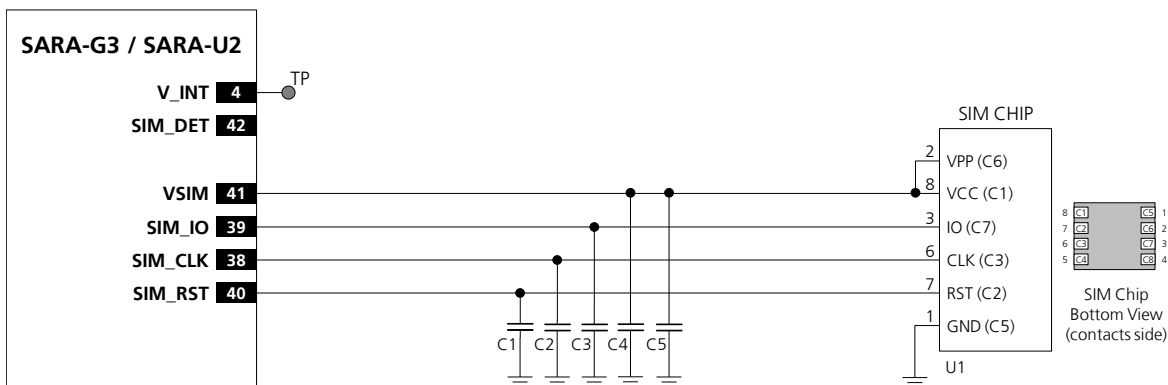


Figure 56: Application circuit for the connection to a single solderable SIM chip, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic COG 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 37: Example of components for the connection to a single solderable SIM chip, with SIM detection not implemented

## Guidelines for single SIM card connection with detection



SIM card detection is not supported by SARA-G300-00S and SARA-G310-00S modules.

An application circuit for the connection to a single removable SIM card placed in a SIM card holder is described in Figure 57, where the optional SIM card detection feature is implemented.

Follow these guidelines connecting the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) and C6 (VPP) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM\_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM\_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM\_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Connect one pin of the mechanical switch integrated in the SIM connector (as the SW2 pin in Figure 57) to the **SIM\_DET** input pin, providing a weak pull-down resistor (e.g. 470 k $\Omega$ , as R2 in Figure 57).
- Connect the other pin of the mechanical switch integrated in the SIM connector (as SW1 pin in Figure 57) to the **V\_INT** 1.8 V supply output by means of a strong pull-up resistor (e.g. 1 k $\Omega$ , as R1 in Figure 57).
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM\_CLK**, **SIM\_IO**, **SIM\_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector: ESD sensitivity rating of SIM interface pins is 1 kV (HBM according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface (27.7 ns = max allowed rise time on **SIM\_CLK**, 1.0  $\mu$ s = max allowed rise time on **SIM\_IO** and **SIM\_RST**).

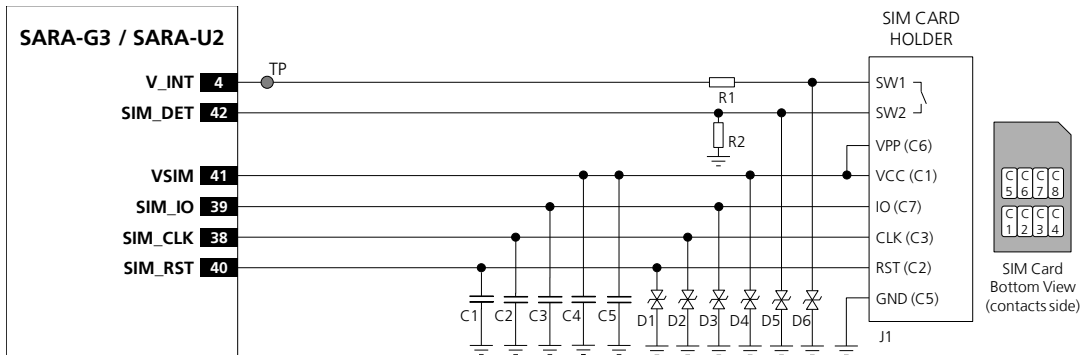


Figure 57: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic COG 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D6	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	1 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-07470KL - Yageo Phycomp
J1	SIM Card Holder 6 + 2 positions, with card presence switch	Various Manufacturers, CCM03-3013LFT R102 - C&K Components

Table 38: Example of components for the connection to a single removable SIM card, with SIM detection implemented

### Guidelines for dual SIM card / chip connection

Two SIM card / chip can be connected to the modules' SIM interface as described in the circuit of Figure 58.

SARA-G3 and SARA-U2 modules do not support the usage of two SIM at the same time, but two SIM can be populated on the application board providing a proper switch to connect only the first SIM or only the second SIM per time to the SIM interface of the SARA-G3 and SARA-U2 modules as described in Figure 58.

SARA-G3 modules do not support SIM hot insertion / removal: the module is able to properly use a SIM only if the SIM / module physical connection is provided before the module boot and then held for normal operation. Switching from one SIM to another one can only be properly done within one of these two time periods:

- after module switch-off by the AT+CPWROFF and before module switch-on by **PWR\_ON**
- after network deregistration by AT+COPS=2 and before module reset by AT+CFUN=16 or **RESET\_N**

SARA-U2 modules support SIM hot insertion / removal on the **SIM\_DET** pin: if the feature is enabled using the specific AT commands (refer to sections 1.8.2 and 1.11, and to the u-blox AT Commands Manual [3], +UGPIOC, +UDCONF commands), the switch from first SIM to the second SIM can be properly done when a Low logic level is present on the **SIM\_DET** pin ('SIM not inserted' = SIM interface not enabled), without the necessity of a module re-boot, so that the SIM interface will be re-enabled by the module to use the second SIM when an High logic level will be re-applied on the **SIM\_DET** pin.

In the application circuit example represented in Figure 58, the application processor will drive the SIM switch using its own GPIO to properly select the SIM that is used by the module. Another GPIO may be used to handle the SIM hot insertion / removal function of SARA-U2 modules, which can also be handled by other external circuits or by the cellular module GPIO according to the application requirements.

The dual SIM connection circuit described in Figure 58 can be implemented for SIM chips as well, providing proper connection between SIM switch and SIM chip as described in Figure 56.

If it is required to switch between more than two SIMs, a circuit similar to the one described in Figure 58 can be implemented: for example, in case of four SIM circuit, using a proper 4-pole 4-throw switch (or, alternatively, four 1-pole 4-throw switches) instead of the suggested 4-pole 2-throw switch.

Follow these guidelines connecting the module to two SIM connectors:

- Use a proper low on resistance (i.e. few ohms) and low on capacitance (i.e. few pF) 2-throw analog switch (e.g. Fairchild FSA2567) as SIM switch to ensure high-speed data transfer according to SIM requirements.
- Connect the contacts C1 (VCC) and C6 (VPP) of the two UICC / SIM to the **VSIM** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C7 (I/O) of the two UICC / SIM to the **SIM\_IO** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C3 (CLK) of the two UICC / SIM to the **SIM\_CLK** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C2 (RST) of the two UICC / SIM to the **SIM\_RST** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C5 (GND) of the two UICC / SIM to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the two SIM connectors, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM\_CLK**, **SIM\_IO**, **SIM\_RST**), very close to each related pad of the two SIM connectors, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holders.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the two SIM connectors, according to the EMC/ESD requirements of the custom application.
- Limit capacitance and series resistance on each SIM signal (**SIM\_CLK**, **SIM\_IO**, **SIM\_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM\_CLK** line, 1.0 μs is the maximum allowed rise time on the **SIM\_IO** and **SIM\_RST** lines).

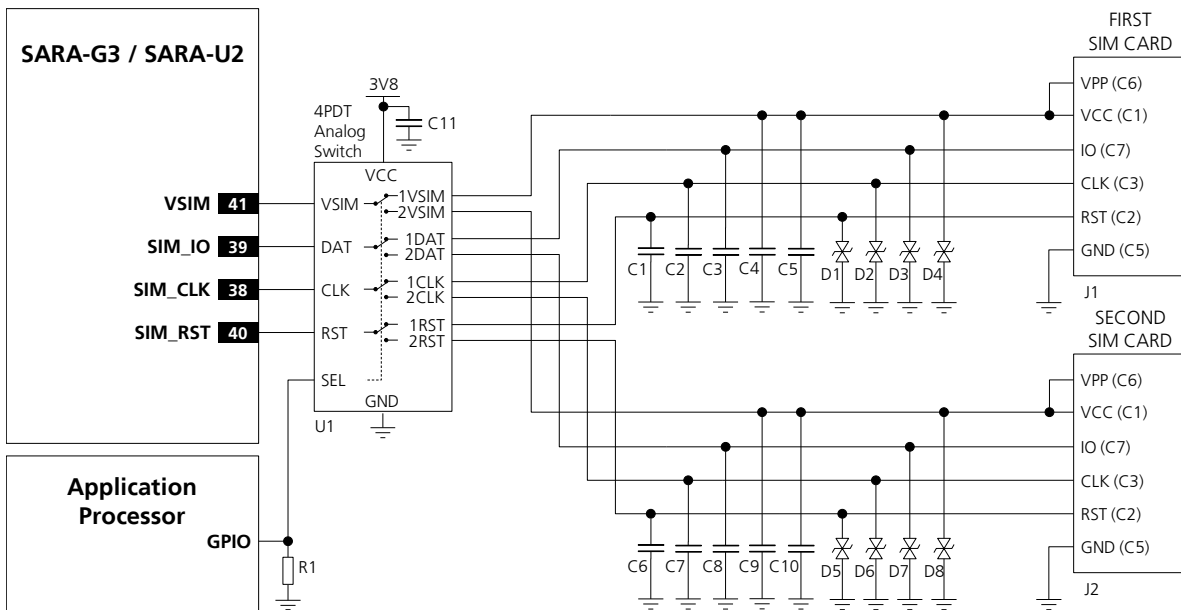


Figure 58: Application circuit for the connection to two removable SIM cards, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1 – C4, C6 – C9	33 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H330JZ01 - Murata
C5, C10, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D8	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL- Yageo Phycomp
J1, J2	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, C707 10M006 136 2 - Amphenol
U1	4PDT Analog Switch, with Low On-Capacitance and Low On-Resistance	FSA2567 - Fairchild Semiconductor

Table 39: Example of components for the connection to two removable SIM cards, with SIM detection not implemented

### 2.5.1.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM\_CLK**, **SIM\_IO**, **SIM\_RST**) may be critical if the SIM card is placed far away from the SARA-G3 and SARA-U2 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface: keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of GSM / UMTS receiver channels whose carrier frequency is coincidental with harmonic frequencies: placing the RF bypass capacitors suggested in Figure 57 near the SIM connector will mitigate the problem.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges: add adequate ESD protection as suggested in Figure 57 to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications: the connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

## 2.6 Serial interfaces

### 2.6.1 Asynchronous serial interface (UART)

#### 2.6.1.1 Guidelines for UART circuit design

##### Providing the full RS-232 functionality (using the complete V.24 link)

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC8T245PW) can be used to provide full RS-232 (9 lines) functionality. The Texas Instruments chip provides the translation from 1.8 V to 3.3 V and vice versa, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level and vice versa.

If a 1.8 V Application Processor (DTE) is used and complete RS-232 functionality as per ITU Recommendation [10] is required in the DTE/DCE serial communication, then the complete 1.8 V UART interface of the module (DCE) must be connected to a 1.8 V DTE as described in Figure 59.

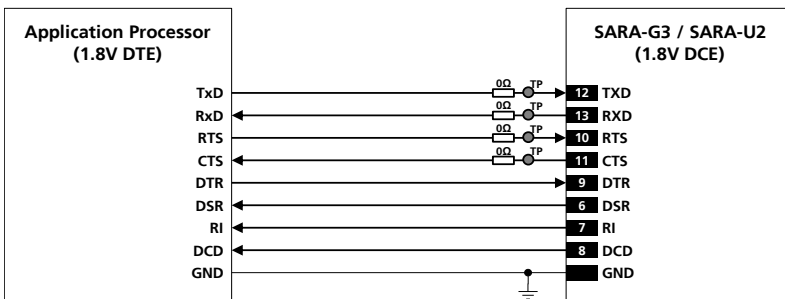


Figure 59: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V\_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 60.

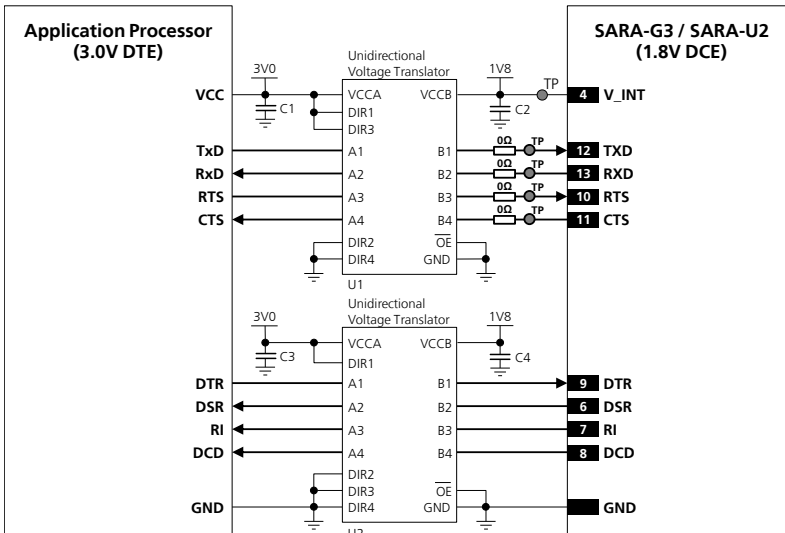


Figure 60: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1, U2	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments

Table 40: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

### Providing the TXD, RXD, RTS, CTS and DTR lines only (not using the complete V.24 link)

If the functionality of the **DSR**, **DCD** and **RI** lines is not required, or the lines are not available:

- Leave **DSR**, **DCD** and **RI** lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

Figure 61 describes the circuit that should be implemented as if a 1.8 V Application Processor (DTE) is used, given that the DTE will behave properly regardless **DSR** input setting.

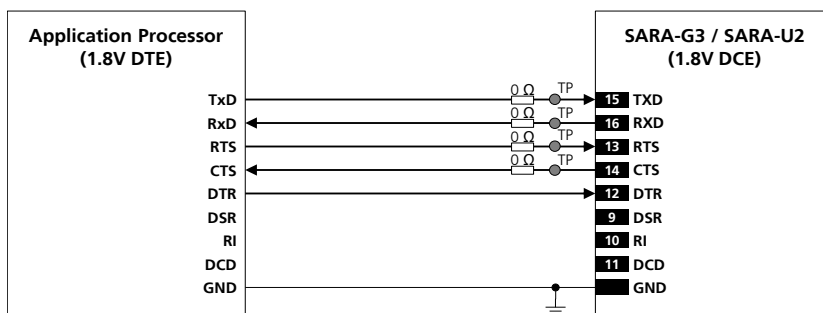


Figure 61: UART interface application circuit with partial V.24 link (6-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V\_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 62, given that the DTE will behave properly regardless **DSR** input setting.

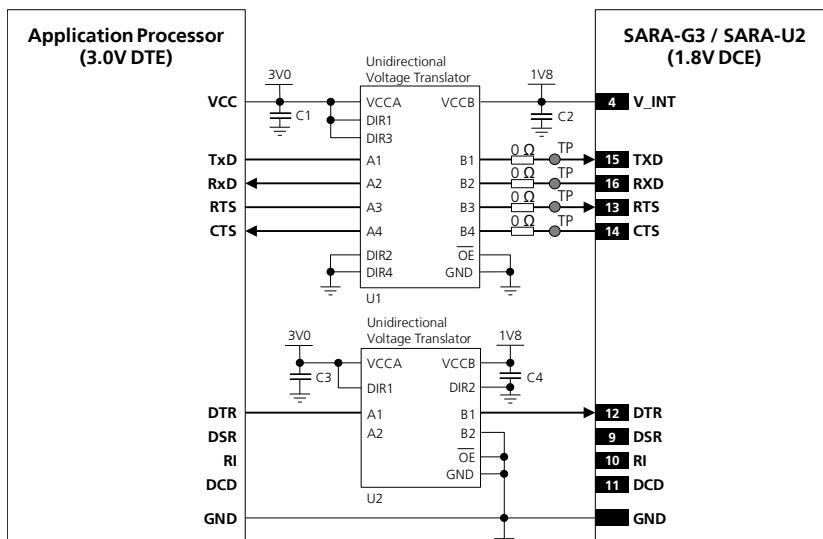


Figure 62: UART interface application circuit with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments
U2	Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 41: Component for UART application circuit with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)



If only **TXD**, **RxD**, **RTS**, **CTS** and **DTR** lines are provided (as implemented in Figure 61 and in Figure 62) and if HW flow-control is enabled (AT&K3, default setting), the power saving can be activated as it can be done when the complete UART link is provided (9-wire, as implemented in Figure 59 and in Figure 60), i.e. in these ways:

- AT+UPSV=1: the module automatically enters the low power idle-mode whenever possible and the UART interface is periodically enabled, as described in section 1.9.1.4, reaching low current consumption.  
With this configuration, when the module is in idle-mode, the data transmitted by the DTE will be buffered by the DTE and will be correctly received by the module when active-mode is entered.
- AT+UPSV=3: the module automatically enters the low power idle-mode whenever possible and the UART interface is enabled by the **DTR** line, as described in section 1.9.1.4, reaching very low current consumption.  
With this configuration, not supported only by SARA-G3 modules, when the module is in idle-mode, the UART is re-enabled 20 ms after **DTR** has been set ON, and the recognition of subsequent characters is guaranteed until the module is in active-mode.

If the HW flow-control is disabled (AT&K0), it is recommended to enable the power saving in one of these ways:

- AT+UPSV=2: the module automatically enters the low power idle-mode whenever possible and the UART interface is enabled by the **RTS** line, as described in section 1.9.1.4, reaching very low current consumption.  
With this configuration, when the module is in idle-mode, the UART is re-enabled 20 ms after **RTS** has been set ON, and the recognition of subsequent characters is guaranteed until the module is in active-mode.
- AT+UPSV=3: the module automatically enters the low power idle-mode whenever possible and the UART interface is enabled by the **DTR** line, as described in section 1.9.1.4, reaching very low current consumption.  
With this configuration, not supported only by SARA-G3 modules, when the module is in idle-mode, the UART is re-enabled 20 ms after **DTR** has been set ON, and the recognition of subsequent characters is guaranteed until the module is in active-mode.

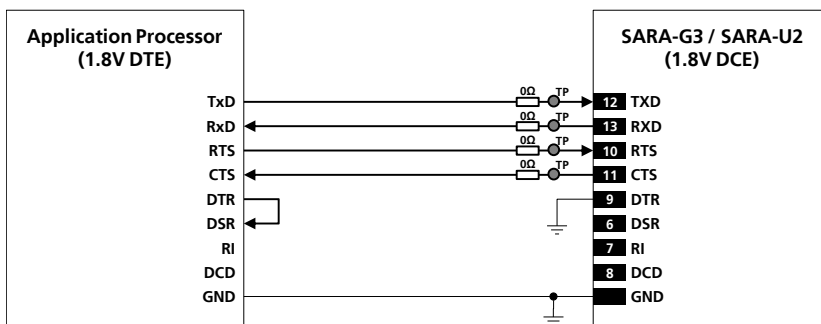
**Providing the TXD, RxD, RTS and CTS lines only (not using the complete V.24 link)**

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required in, or the lines are not available:

- Connect the module **DTR** input line to GND, since the module requires **DTR** active (low electrical level)
- Leave **DSR**, **DCD** and **RI** lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, the Maxim 13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

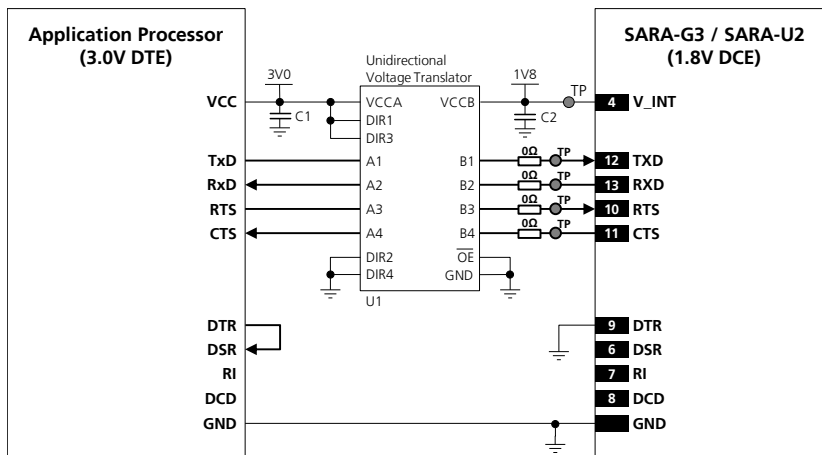
If a 1.8 V Application Processor (DTE) is used, the circuit should be implemented as described in Figure 63.



**Figure 63: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication (1.8 V DTE)**



If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V\_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 64.



**Figure 64: UART interface application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)**

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments

**Table 42: Component for UART application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)**

If only **TXD**, **RXD**, **RTS** and **CTS** lines are provided, as implemented in Figure 63 and in Figure 64, and if HW flow-control is enabled (AT&K3, default setting), the power saving can be activated in this way:

- AT+UPSV=1: the module automatically enters the low power idle-mode whenever possible and the UART interface is periodically enabled, as described in section 1.9.1.4, reaching low current consumption.

With this configuration, when the module is in idle-mode, data transmitted by the DTE will be buffered by the DTE and will be correctly received by the module when active-mode is entered.

If the HW flow-control is disabled (AT&K0), it is recommended to enable the power saving in this way:

- AT+UPSV=2: the module automatically enters the low power idle-mode whenever possible and the UART interface is enabled by the **RTS** line, as described in section 1.9.1.4, reaching very low current consumption.

With this configuration, when the module is in idle-mode, the UART is re-enabled 20 ms after **RTS** has been set ON, and the recognition of subsequent characters is guaranteed until the module is in active-mode.

### Providing the TXD and RXD lines only (not using the complete V24 link)

If the functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available:

- Connect the module **RTS** input line to GND or to the **CTS** output line of the module: since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, that is the default setting), the pin can be connected using a 0 Ω series resistor to GND or to the active-module **CTS** (low electrical level) when the module is in active-mode, the UART interface is enabled and the HW flow-control is enabled.
- Connect the module **DTR** input line to GND, since the module requires **DTR** active (low electrical level).
- Leave **DSR**, **DCD** and **RI** lines of the module unconnected and floating.

If RS-232 compatible signal levels are needed, the Maxim 13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor (DTE) is used, the circuit that should be implemented as described in Figure 65:

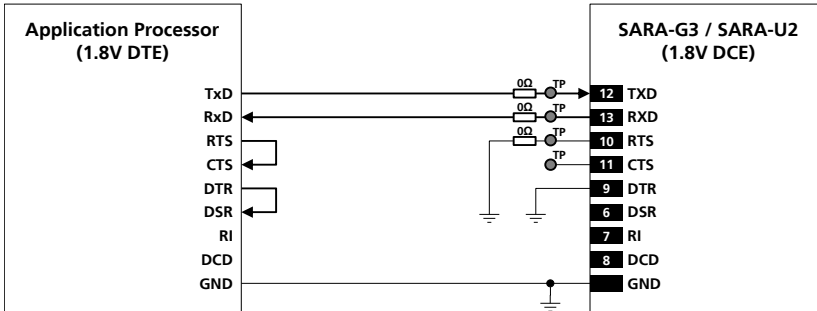


Figure 65: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V\_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 66.

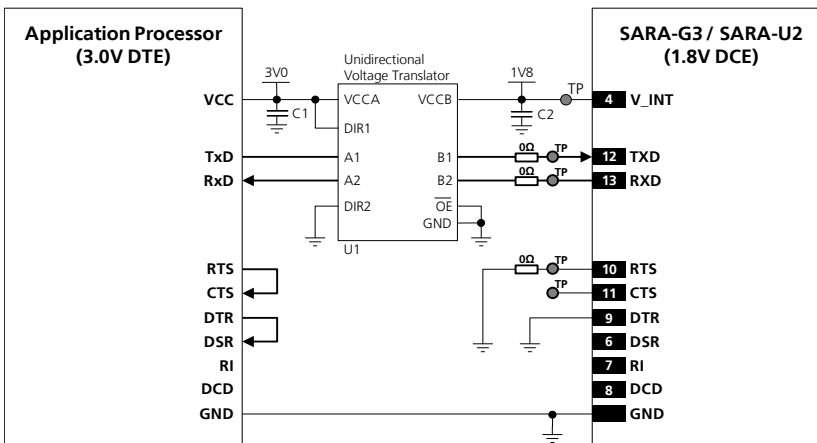


Figure 66: UART interface application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 43: Component for UART application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

If only **TXD** and **RXD** lines are provided, as described in Figure 65 or in Figure 66, and HW flow-control is disabled (AT&K0), the power saving must be enabled in this way:

- AT+UPSV=1: the module automatically enters the low power idle-mode whenever possible and the UART interface is periodically enabled, as described in section 1.9.1.4, reaching low current consumption. With this configuration, when the module is in idle-mode, the UART is re-enabled 20 ms after the first data reception, and the recognition of subsequent characters is guaranteed until the module is in active-mode.



If only **TXD** and **RXD** lines are provided, data delivered by the DTE can be lost with these settings:

- HW flow-control enabled in the module (AT&K3, that is the default setting)
- Module power saving enabled by AT+UPSV=1
- HW flow-control disabled in the DTE



In this case the first character sent when the module is in idle-mode will be a wake-up character and will not be a valid communication character (see section 1.9.1.4 for the complete description).



If power saving is enabled the application circuit with the **TXD** and **RXD** lines only is not recommended. During command mode the DTE must send to the module a wake-up character or a dummy "AT" before each command line (see section 1.9.1.4 for the complete description), but during data mode the wake-up character or the dummy "AT" would affect the data communication.

### Additional considerations

If a 3.0 V Application Processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the opposite 1.8 V input of the module (DCE) can be implemented, as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values and mind that any DTE signal connected to the module has to be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V\_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the opposite 3.0 V input of the Application Processor (DTE) can be implemented by means of an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V\_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.



If the USB interface of SARA-U2 modules is connected to the host application processor, the UART can be left unconnected as not required for AT and data communication, but it is anyway highly recommended to provide direct access to the **TXD**, **RXD**, **RTS**, **CTS** pins of SARA-U2 modules for the execution of firmware upgrade over UART using the u-blox EasyFlash tool and for diagnostic purpose: provide a testpoint on each line to accommodate the access and provide a 0  $\Omega$  series resistor on each line to detach the module pin from any other connected device.



Any external signal connected to the UART interface must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V\_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode and during the module power-on sequence.



ESD sensitivity rating of UART interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

#### 2.6.1.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

## 2.6.2 Auxiliary asynchronous serial interface (UART AUX)



Auxiliary UART interface is not supported by SARA-U2 modules.

### 2.6.2.1 Guidelines for UART AUX circuit design

The auxiliary UART interface can be connected to an application processor if it can be set in pass-through mode so that the auxiliary UART interface can be accessed for SARA-G3 modules' firmware upgrade by means of the u-blox EasyFlash tool and for diagnostic purpose.



It is highly recommended to provide direct access to the **TXD\_AUX**, **RXD\_AUX** pins of SARA-G3 modules for execution of firmware upgrade over auxiliary UART using the u-blox EasyFlash tool and for diagnostic purpose: provide a testpoint on each line to accommodate the access and provide a  $0\ \Omega$  series resistor on each line to detach the module pin from any other connected device.

The circuit with a 1.8 V application processor should be implemented as described in Figure 67.

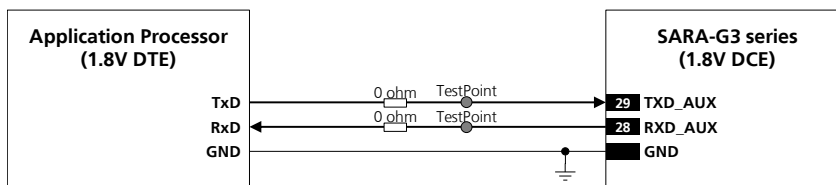


Figure 67: UART AUX interface application circuit connecting a 1.8 V application processor

If a 3.0 V application processor is used, then it is recommended to connect the 1.8 V auxiliary UART interface of the module by means of appropriate unidirectional voltage translators using the module **V\_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 68.

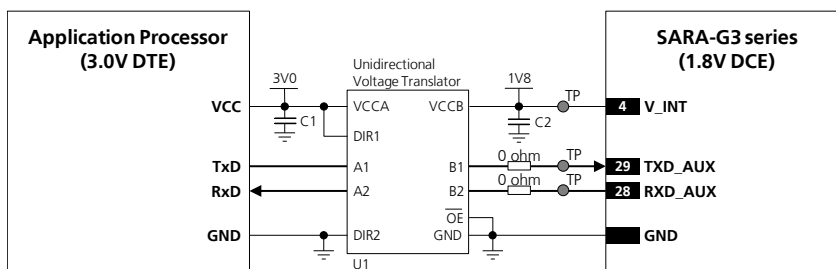


Figure 68: UART AUX interface application circuit connecting a 3.0 V application processor

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 44: Component for UART AUX interface application circuit connecting a 3.0 V application processor

See Firmware Update Application Note [25] for additional guidelines regarding the procedure for SARA-G3 modules' firmware upgrade over the auxiliary UART interface using the u-blox EasyFlash tool.



Any external signal connected to the auxiliary UART interface must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V\_INT** output), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode and during the module power-on sequence.



ESD sensitivity rating of auxiliary UART pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

### 2.6.2.2 Guidelines for UART AUX layout design

The auxiliary UART serial interface is not critical for the layout design since it is not used during normal operation of SARA-G3 modules. Ensure accessibility to the **TXD\_AUX** and **RXD\_AUX** pins providing test points on the application board.

## 2.6.3 Universal Serial Bus (USB)

USB interface is not supported by SARA-G3 modules.

### 2.6.3.1 Guidelines for USB circuit design

The **USB\_D+** and **USB\_D-** lines carry the USB serial data and signaling. The lines are used in single ended mode for full speed signaling handshake, as well as in differential mode for high speed signaling and data transfer.

USB pull-up or pull-down resistors on **USB\_D+** and **USB\_D-** as required by the Universal Serial Bus Revision 2.0 specification [14] are part of the USB pin driver and do not need to be externally provided.

Series resistors on **USB\_D+** and **USB\_D-** as required by Universal Serial Bus Revision 2.0 specification [14] are also integrated and do not need to be externally provided.

Since the module acts as a USB device, the VBUS USB supply (5.0 V typ.) generated by the USB host must be connected to the **VUSB\_DET** input, which absorbs few microamperes to sense the host connection and enable the USB interface of the module.

If connecting the **USB\_D+** and **USB\_D-** pins to a USB device connector, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device with very low capacitance should be provided close to accessible point on the line connected to this pin, as described in Figure 69 and Table 45.

The USB interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140 ESD protection device) on the lines connected to these pins, close to accessible points.

The USB pins of the modules can be directly connected to the USB host application processor without additional ESD protections if they are not externally accessible or according to EMC/ESD requirements.

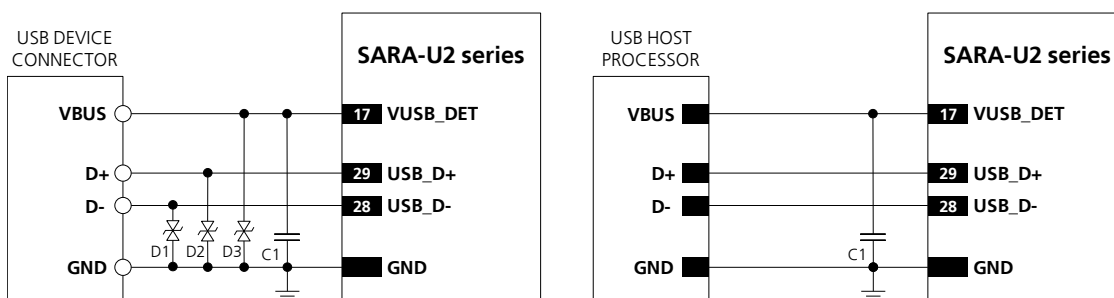


Figure 69: USB Interface application circuits

Reference	Description	Part Number - Manufacturer
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics

Table 45: Component for USB application circuits

If the USB interface is not required by the customer application, as the UART interface is used for AT and data communication with the host application processor, the USB pins can be left unconnected, but it is highly recommended providing direct access on the application board by means of accessible testpoint directly connected to the **VUSB\_DET**, **USB\_D+**, **USB\_D-** pins of SARA-U2 modules.

### 2.6.3.2 Guidelines for USB layout design

The **USB\_D+** / **USB\_D-** lines require accurate layout design to achieve reliable signaling at the high speed data rate (up to 480 Mb/s) supported by the USB serial interface.

The characteristic impedance of the **USB\_D+** / **USB\_D-** lines is specified by the Universal Serial Bus Revision 2.0 specification [14]. The most important parameter is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential. Signal integrity may be degraded if PCB layout is not optimal, especially when the USB signaling lines are very long.

Use the following general routing guidelines to minimize signal quality problems:

- Route **USB\_D+** / **USB\_D-** lines as a differential pair.
- Route **USB\_D+** / **USB\_D-** lines as short as possible.
- Ensure the differential characteristic impedance ( $Z_o$ ) is as close as possible to 90 Ω.
- Ensure the common mode characteristic impedance ( $Z_{CM}$ ) is as close as possible to 30 Ω.
- Consider design rules for **USB\_D+** / **USB\_D-** similar to RF transmission lines, being them coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area.
- Avoid coupling with any RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Figure 70 and Figure 71 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

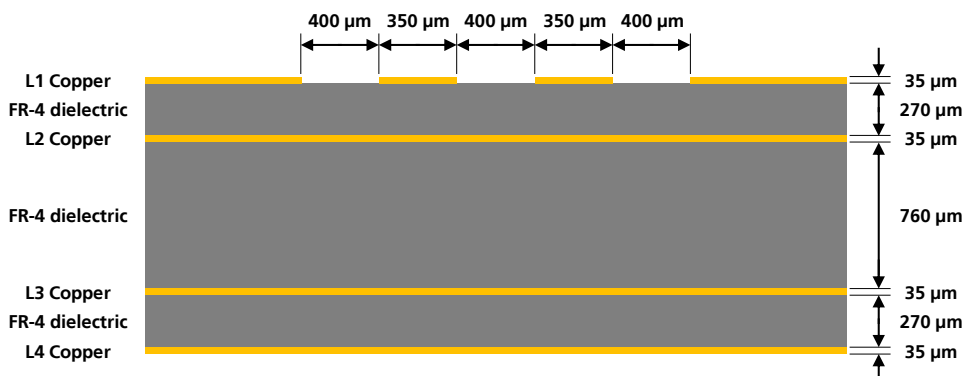


Figure 70: Example of USB line design, with  $Z_o$  close to 90 Ω and  $Z_{CM}$  close to 30 Ω, for the described 4-layer board layout

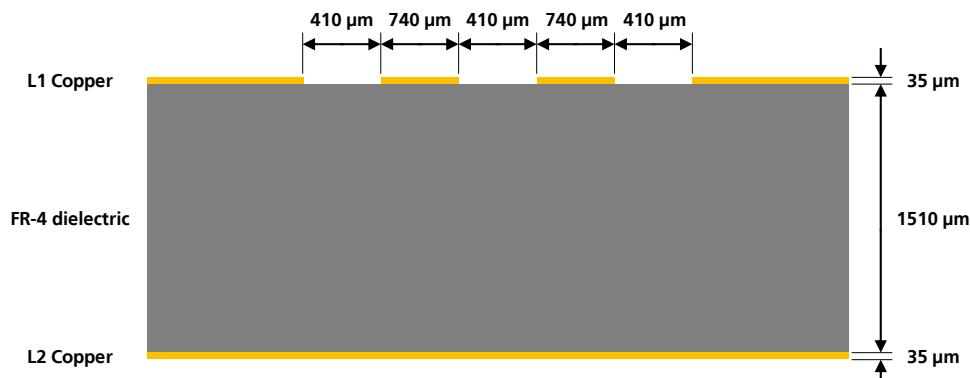


Figure 71: Example of USB line design, with  $Z_o$  close to 90 Ω and  $Z_{CM}$  close to 30 Ω, for the described 2-layer board layout

## 2.6.4 DDC (I<sup>2</sup>C) interface



DDC (I<sup>2</sup>C) interface is not supported by SARA-G300 and SARA-G310 modules.

### 2.6.4.1 Guidelines for DDC (I<sup>2</sup>C) circuit design

#### General considerations

The DDC I<sup>2</sup>C-bus master interface of SARA-G340, SARA-G350 and SARA-U2 cellular modules can be used to communicate with u-blox GNSS receivers and, on SARA-U2 modules only, it can be also used to communicate with other external I<sup>2</sup>C-bus slaves as an audio codec. Beside the general considerations reported below, see:

- the following parts of this section for specific guidelines for the connection to u-blox GNSS receivers.
- the section 2.7.2 for an application circuit example with an external audio codec I<sup>2</sup>C-bus slave.

To be compliant to the I<sup>2</sup>C-bus specifications, the module bus interface pins are open drain output and pull up resistors must be mounted externally. Resistor values must conform to I<sup>2</sup>C bus specifications [15]: for example, 4.7 k $\Omega$  resistors can be commonly used.



Connect the external DDC (I<sup>2</sup>C) pull-ups to the **V\_INT** 1.8 V supply source, or another supply source enabled after **V\_INT** (e.g., as the GNSS 1.8 V supply present in Figure 72 application circuit), as any external signal connected to the DDC (I<sup>2</sup>C) interface must not be set high before the switch-on of the **V\_INT** supply of the DDC (I<sup>2</sup>C) pins, to avoid latch-up of circuits and let a proper boot of the module.

The signal shape is defined by the values of the pull-up resistors and the bus capacitance. Long wires on the bus increase the capacitance. If the bus capacitance is increased, use pull-up resistors with nominal resistance value lower than 4.7 k $\Omega$ , to match the I<sup>2</sup>C bus specifications [15] regarding rise and fall times of the signals.



Capacitance and series resistance must be limited on the bus to match the I<sup>2</sup>C specifications (1.0  $\mu$ s is the maximum allowed rise time on the **SCL** and **SDA** lines): route connections as short as possible.



ESD sensitivity rating of the DDC (I<sup>2</sup>C) pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.



If the pins are not used as DDC bus interface, they can be left unconnected.



### Connection with u-blox 1.8 V GNSS receivers

Figure 72 shows an application circuit example for connecting a SARA-G340, SARA-G350 or SARA-U2 cellular module to a u-blox 1.8 V GNSS receiver:

- The **SDA** and **SCL** pins of the cellular module are directly connected to the related pins of the u-blox 1.8 V GNSS receiver, with appropriate pull-up resistors connected to the 1.8 V GNSS supply enabled after the **V\_INT** supply of the I<sup>2</sup>C pins of the cellular module.
- The **GPIO2** pin is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 1.8 V GNSS receiver providing the “GNSS supply enable” function. A pull-down resistor is provided to avoid a switch on of the positioning receiver when the cellular module is switched off or in the reset state.
- The **GPIO3** and **GPIO4** pins are directly connected respectively to **TXD1** and **EXTINT0** pins of the u-blox 1.8 V GNSS receiver providing “GNSS data ready” and “GNSS RTC sharing” functions.
- The **V\_BCKP** supply output of the cellular module is connected to the **V\_BCKP** backup supply input pin of the GNSS receiver to provide the supply for the GNSS real time clock and backup RAM when the **VCC** supply of the cellular module is within its operating range and the **VCC** supply of the GNSS receiver is disabled. This enables the u-blox GNSS receiver to recover from a power breakdown with either a hot start or a warm start (depending on the actual duration of the GNSS **VCC** outage) and to maintain the configuration settings saved in the backup RAM.

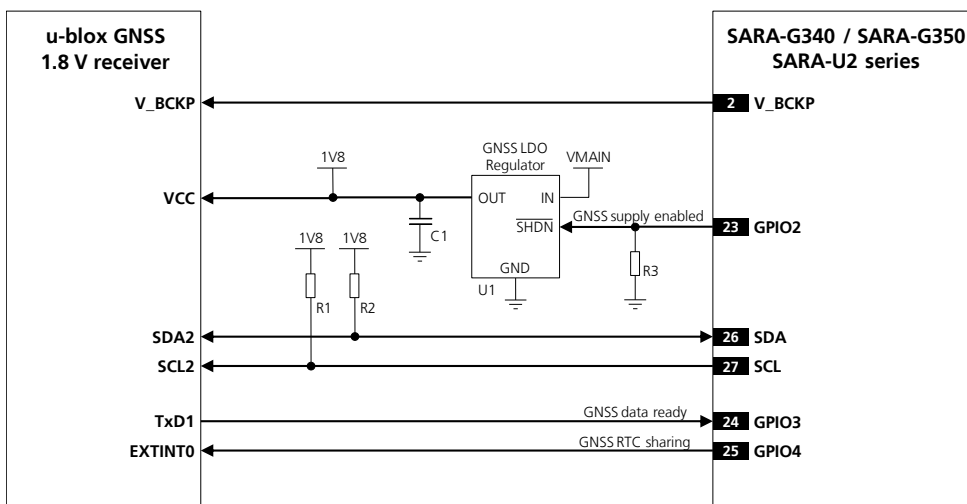


Figure 72: Application circuit for connecting SARA-G3 / SARA-U2 modules to u-blox 1.8 V GNSS receivers

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
U1	Voltage Regulator for GNSS receiver	See GNSS receiver Hardware Integration Manual

Table 46: Components for connecting SARA-G3 / SARA-U2 modules to u-blox 1.8 V GNSS receivers

Figure 73 illustrates an alternative solution as supply for u-blox 1.8 V GNSS receivers: the **V\_INT** 1.8 V regulated supply output of SARA-G340 / SARA-G350 / SARA-U2 cellular modules can be used to supply a u-blox 1.8 V GNSS receiver of the u-blox 6 generation (or any newer u-blox GNSS receiver generation) instead of using an external voltage regulator as shown in the previous Figure 72. The **V\_INT** supply is able to support the maximum current consumption of these positioning receivers.

The internal switching step-down regulator that generates the **V\_INT** supply is set to 1.8 V (typical) when the cellular module is switched on and it is disabled when the module is switched off.

The supply of the u-blox 1.8 V GNSS receiver can be switched off using an external p-channel MOSFET controlled by the **GPIO2** pin by means of a proper inverting transistor as shown in Figure 73, implementing the “GNSS supply enable” function. If this feature is not required, the **V\_INT** supply output can be directly connected to the u-blox 1.8 V GNSS receiver, so that it will be switched on when **V\_INT** output is enabled.

The **V\_INT** supply output provides low voltage ripple (up to 15 mVpp) when the module is in active-mode or in connected-mode, but it provides higher voltage ripple (up to 90 mVpp on SARA-G3 series, or up to 70 mVpp on SARA-U2 series) when the module is in the low power idle-mode with power saving configuration enabled by the AT+UPSV (see u-blox AT Commands Manual [3]).

According to the voltage ripple characteristic of the **V\_INT** supply output:

- The power saving configuration cannot be enabled to use **V\_INT** output to properly supply any 1.8 V GNSS receiver of the u-blox 6 generation and any 1.8 V GNSS receiver of the u-blox 7 generation or any newer u-blox GNSS receiver generation with TCXO.
- The power saving configuration can be enabled to use **V\_INT** output to properly supply any 1.8 V GNSS receiver of the u-blox 7 generation or any newer u-blox GNSS receiver generation without TCXO.
- Additional filtering may be needed to properly supply an external LNA, depending on the characteristics of the used LNA, adding a series ferrite bead and a bypass capacitor (e.g. the Murata BLM15HD182SN1 ferrite bead and the Murata GRM1555C1H220J 22 pF capacitor) at the input of the external LNA supply line.

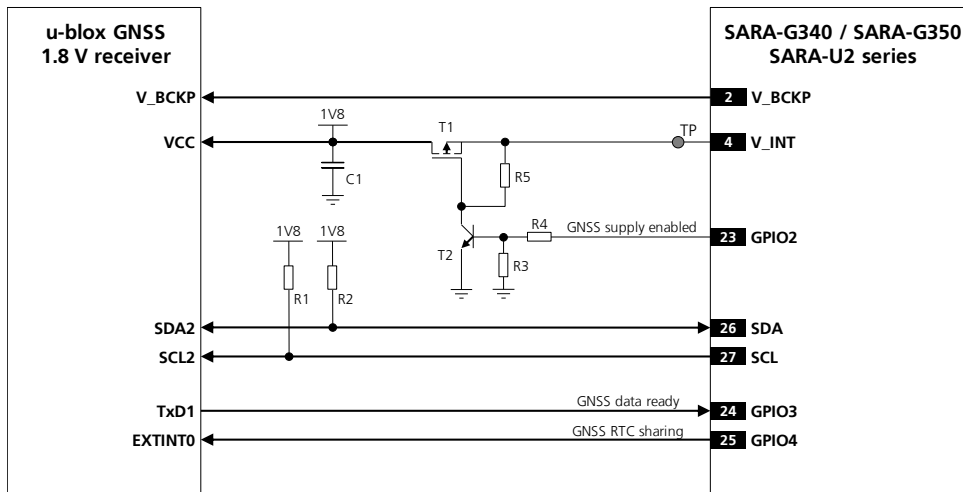


Figure 73: Application circuit for connecting SARA-G3 / SARA-U2 modules to u-blox 1.8 V GNSS receivers using **V\_INT** as supply

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R4	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R5	100 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07100KL - Yageo Phycomp
T1	P-Channel MOSFET Low On-Resistance	IRLML6401 - International Rectifier or NTZS3151P - ON Semi
T2	NPN BJT Transistor	BC847 - Infineon
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata

Table 47: Components for connecting SARA-G3 / SARA-U2 modules to u-blox 1.8 V GNSS receivers using **V\_INT** as supply

For additional guidelines regarding the design of applications with u-blox 1.8 V GNSS receivers see the GNSS Implementation Application Note [24] and to the Hardware Integration Manual of the u-blox GNSS receivers.

### Connection with u-blox 3.0 V GNSS receivers

Figure 74 shows an application circuit example for connecting a SARA-G340 or a SARA-G350 cellular module to a u-blox 3.0 V GNSS receiver:

- The **SDA** and **SCL** pins of SARA-G340 / SARA-G350 are directly connected to the related pins of the u-blox 3.0 V GNSS receiver, with appropriate pull-up resistors connected to the 3.0 V GNSS supply enabled after the **V\_INT** supply of the I<sup>2</sup>C pins of the cellular module. An I<sup>2</sup>C-bus Voltage Translator is not needed because the SARA-G340 / SARA-G350 DDC (I<sup>2</sup>C) pins are capable up to 3.3 V.
- The **GPIO2** is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 3.0 V GNSS receiver providing the “GNSS supply enable” function. A pull-down resistor is provided to avoid a switch on of the positioning receiver when the cellular module is switched off or in the reset state.
- As the **GPIO3** and **GPIO4** pins of SARA-G340 / SARA-G350 cellular modules are not tolerant up to 3.0 V, the connection to the related pins of the u-blox 3.0 V GNSS receiver must be provided using a proper Unidirectional General Purpose Voltage Translator (e.g. TI SN74AVC2T245, which additionally provides the partial power down feature so that the 3.0 V GNSS supply can be also ramped up before the **V\_INT** 1.8 V cellular supply).
- The **V\_BCKP** supply output of SARA-G340 / SARA-G350 is directly connected to the **V\_BCKP** backup supply input pin of the u-blox 3.0 V GNSS receiver as in the application circuit for a u-blox 1.8 V GNSS receiver.

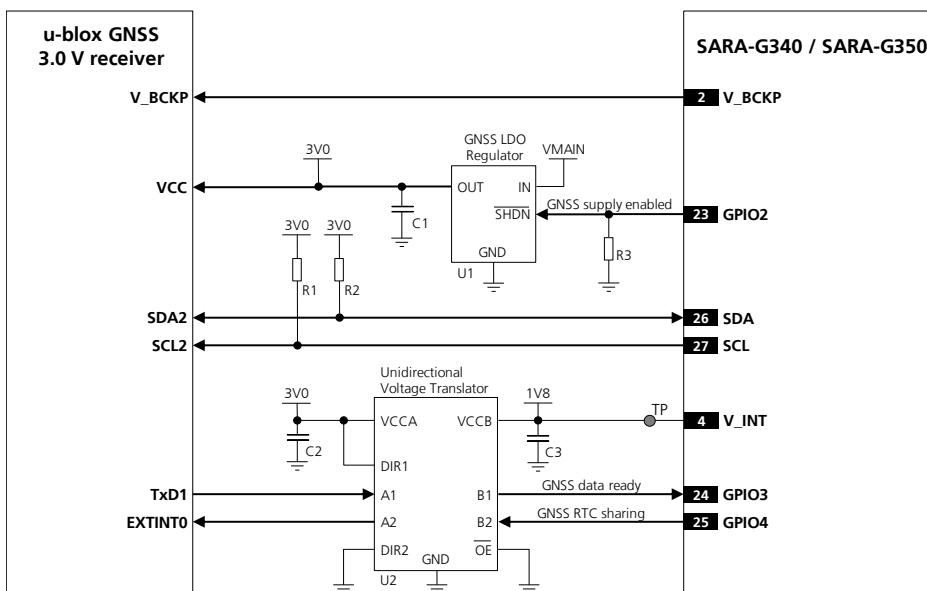


Figure 74: Application circuit for connecting SARA-G3 modules to u-blox 3.0 V GNSS receivers

Reference	Description	Part Number – Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
C2, C3	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 - Murata
U1	Voltage Regulator for GNSS receiver	See GNSS receiver Hardware Integration Manual
U2	Generic Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 48: Components for connecting SARA-G3 modules to u-blox 3.0 V GNSS receivers

Figure 75 shows an application circuit example for connecting a SARA-U2 cellular module to a u-blox 3.0 V GNSS receiver:

- As the **SDA** and **SCL** pins of the SARA-U2 cellular module are not tolerant up to 3.0 V, the connection to the related I<sup>2</sup>C pins of the u-blox 3.0 V GNSS receiver must be provided using a proper I<sup>2</sup>C-bus Bidirectional Voltage Translator (e.g. TI TCA9406, which additionally provides the partial power down feature so that the GNSS 3.0 V supply can be ramped up before the **V\_INT** 1.8 V cellular supply), with proper pull-up resistors.
- The **GPIO2** is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 3.0 V GNSS receiver providing the “GNSS supply enable” function. A pull-down resistor is provided to avoid a switch on of the positioning receiver when the cellular module is switched off or in the reset state.
- As the **GPIO3** and **GPIO4** pins of the SARA-U2 cellular modules are not tolerant up to 3.0 V, the connection to the related pins of the u-blox 3.0 V GNSS receiver must be provided using a proper Unidirectional General Purpose Voltage Translator (e.g. TI SN74AVC2T245, which additionally provides the partial power down feature so that the 3.0 V GNSS supply can be also ramped up before the **V\_INT** 1.8 V cellular supply).
- The **V\_BCKP** supply output of the cellular module can be directly connected to the **V\_BCKP** backup supply input pin of the GNSS receiver as in the application circuit for a u-blox 1.8 V GNSS receiver.

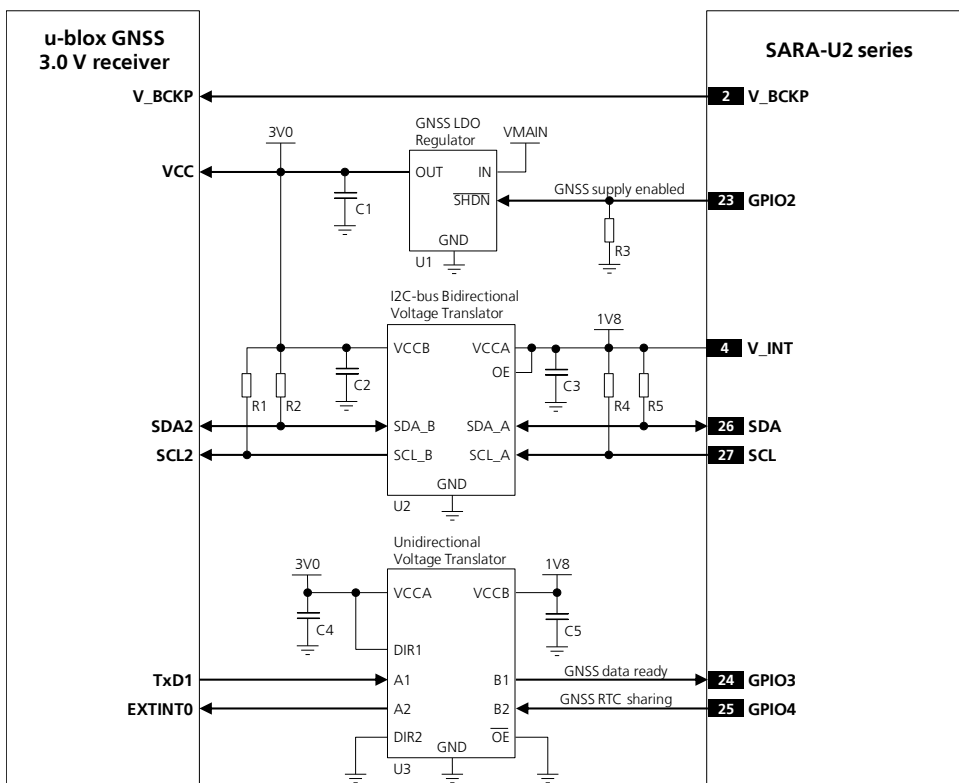


Figure 75: Application circuit for connecting SARA-U2 modules to u-blox 3.0 V GNSS receivers

Reference	Description	Part Number - Manufacturer
R1, R2, R4, R5	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
C2, C3, C4, C5	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM1155R71C104KA01 - Murata
U1, C1	Voltage Regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver Hardware Integration Manual
U2	I2C-bus Bidirectional Voltage Translator	TCA9406DCUR - Texas Instruments
U3	Generic Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 49: Components for connecting SARA-U2 modules to u-blox 3.0 V GNSS receivers

For additional guidelines regarding the design of applications with u-blox 3.0 V GNSS receivers see the GNSS Implementation Application Note [24] and to the Hardware Integration Manual of the u-blox GNSS receivers.

#### **2.6.4.2 Guidelines for DDC (I<sup>2</sup>C) layout design**

The DDC (I<sup>2</sup>C) serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

## 2.7 Audio interface

### 2.7.1 Analog audio interface



SARA-G300, SARA-G310 and SARA-U2 modules do not provide analog audio interface.

#### 2.7.1.1 Guidelines for microphone and speaker connection circuit design (headset / handset modes)

SARA-G340 and SARA-G350 modules provide one analog audio input path and one analog audio output path: the same paths are used for both headset and handset modes, so that basically the same application circuit can be implemented for both headset and handset modes.

Figure 76 shows an application circuit for the analog audio interface in headset and handset modes, connecting a 2.2 k $\Omega$  electret microphone and a 16  $\Omega$  receiver / speaker:

- External microphone can be connected to the uplink path of the module, since the module provides supply and reference as well as differential signal input for the external microphone.
- A 16  $\Omega$  receiver / speaker can be directly connected to the balanced output of the module, since the differential analog audio output of the module is able to directly drive loads with resistance rating greater than 14  $\Omega$ .

As in the example circuit in Figure 76, follow the general guidelines for the design of an analog audio circuit for both headset and handset modes:

- Provide proper supply to the used electret microphone, providing a proper connection from the MIC\_BIAS supply output to the microphone. It is suggested to implement a bridge structure:
  - The electret microphone, with its nominal intrinsic resistance value, represents one resistor of the bridge.
  - To achieve good supply noise rejection, the ratio of the two resistance in one leg (R2/R3) should be equal to the ratio of the two resistance in the other leg (R4/MIC), i.e. R2 has to be equal to R4 (e.g. 2.2 k $\Omega$ ) and R3 has to be equal to the microphone nominal intrinsic resistance value (e.g. 2.2 k $\Omega$ ).
- Provide a proper series resistor at the **MIC\_BIAS** supply output and then mount a proper large bypass capacitor to provide additional supply noise filtering. See the R1 series resistor (2.2 k $\Omega$ ) and the C1 bypass capacitor (10  $\mu$ F).
- Do not place a bypass capacitor directly at the **MIC\_BIAS** supply output, since proper internal bypass capacitor is already provided to guarantee stable operation of the internal regulator.
- Connect the reference of the microphone circuit to the **MIC\_GND** pin of the module as a sense line.
- Provide a proper series capacitor at both **MIC\_P** and **MIC\_N** analog uplink inputs for DC blocking (as the C2 and C3 100 nF Murata GRM155R71C104K capacitors in Figure 76). This provides a high-pass filter for the microphone DC bias with proper cut-off frequency according to the value of the resistors of the microphone supply circuit. Then connect the signal lines to the microphone.
- Provide proper parts on each line connected to the external microphone as noise and EMI improvements, to minimize RF coupling and TDMA noise, according to the custom application requirements.
  - Mount an 82 nH series inductor with a Self Resonance Frequency  $\sim$ 1 GHz (e.g. the Murata LQG15HS82NJ02) on each microphone line (L1 and L2 inductors in Figure 76).
  - Mount a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each microphone line to solid ground plane (C4 and C5 capacitors in Figure 76).
- Use a microphone designed for GSM applications, which typically has an internal built-in bypass capacitor.
- Connect the **SPK\_P** and **SPK\_N** analog downlink outputs directly to the receiver / speaker (which resistance rating must be greater than 14  $\Omega$ ).

- Provide proper parts on each line connected to the receiver / speaker as noise and EMI improvements, to minimize RF coupling, according to EMC requirements of the custom application.
  - Mount a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each speaker line to solid ground plane (C6 and C7 capacitors in Figure 76).
- Provide additional ESD protection (e.g. Bourns CG0402MLE-18G varistor) if the analog audio lines will be externally accessible on the application device, according to the EMC/ESD requirements of the custom application. Mount the protection close to an accessible point of the line (D1-D4 in Figure 76).

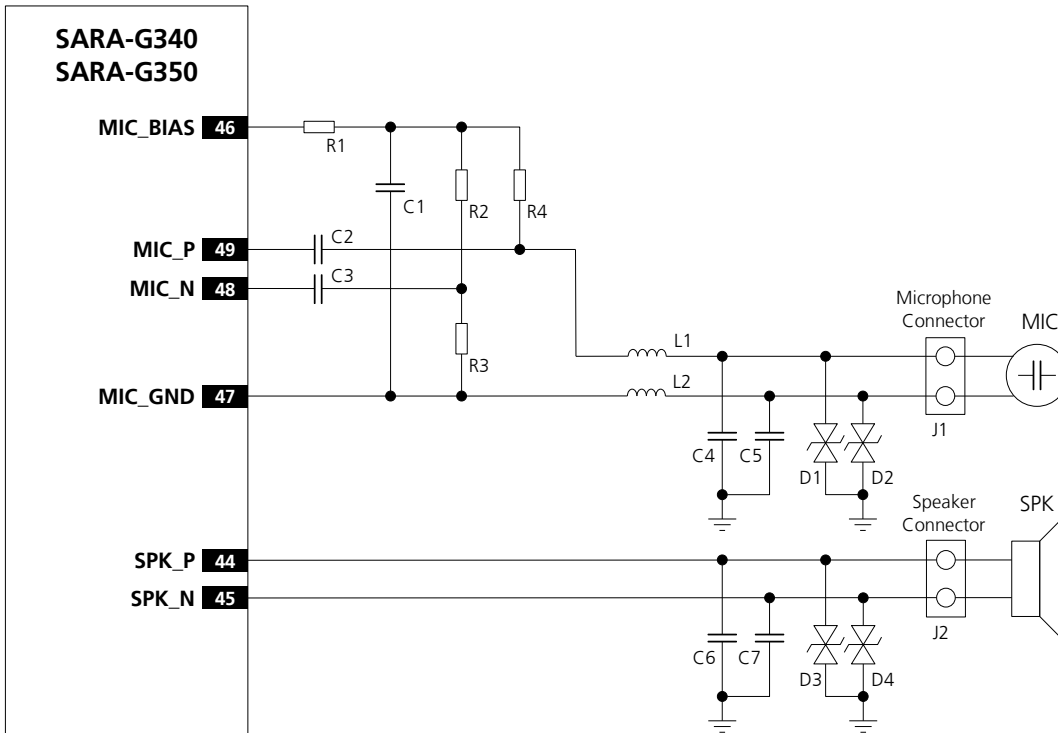


Figure 76: Analog audio interface headset and handset mode application circuit

Reference	Description	Part Number – Manufacturer
C1	10 $\mu$ F Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C2, C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA88 – Murata
C4, C5, C6, C7	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JA01 – Murata
D1, D2, D3, D4	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
J1	Microphone Connector	Various Manufacturers
J2	Speaker Connector	Various Manufacturers
L1, L2	82 nH Multilayer inductor 0402 (self resonance frequency $\sim$ 1 GHz)	LQG15HS82NJ02 – Murata
MIC	2.2 k $\Omega$ Electret Microphone	Various Manufacturers
R1, R2, R3, R4	2.2 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
SPK	16 $\Omega$ Speaker	Various Manufacturers

Table 50: Example of components for analog audio interface headset and handset mode application circuit



If the analog audio interface is not used, the analog audio pins (**MIC\_BIAS**, **MIC\_GND**, **MIC\_P**, **MIC\_N**, **SPK\_P**, **SPK\_N**) can be left unconnected on the application board.

### 2.7.1.2 Guidelines for microphone and loudspeaker connection circuit design (hands-free mode)

Figure 77 shows an application circuit for the analog audio interface in hands-free mode, connecting a 2.2 k $\Omega$  electret microphone and an 8  $\Omega$  or 4  $\Omega$  loudspeaker:

- External microphone can be connected to the uplink path of the module, since the module provides supply and reference as well as differential signal input for the external microphone.
- Using a 8  $\Omega$  or 4  $\Omega$  loudspeaker for the hands-free mode, an external audio amplifier must be provided on the application board to amplify the low power audio signal provided by the downlink path of the module, so that the external audio amplifier will drive the 8  $\Omega$  or 4  $\Omega$  loudspeaker, since differential analog audio output of the module is able to directly drive loads with resistance rating greater than 14  $\Omega$ .

As in the example circuit in Figure 77, follow the general guidelines for the design of an analog audio circuit for hands-free mode:

- Provide proper supply to the used electret microphone, providing a proper connection from the MIC\_BIAS supply output to the microphone. It is suggested to implement a bridge:
  - The electret microphone, with its nominal intrinsic resistance value, represents one resistor of the bridge.
  - To achieve good supply noise rejection, the ratio of the two resistance in one leg (R2/R3) should be equal to the ratio of the two resistance in the other leg (R4/MIC), i.e. R2 has to be equal to R4 (e.g. 2.2 k $\Omega$ ) and R3 must be equal to the microphone nominal intrinsic resistance value (e.g. 2.2 k $\Omega$ ).
- Provide a series resistor at the **MIC\_BIAS** supply output and then mount a good bypass capacitor to provide additional supply noise filtering, as the R1 series resistor (2.2 k $\Omega$ ) and the C1 bypass capacitor (10  $\mu$ F).
- Do not place a bypass capacitor directly at the **MIC\_BIAS** supply output, since proper internal bypass capacitor is already provided to guarantee stable operation of the internal regulator.
- Connect the reference of the microphone circuit to the **MIC\_GND** pin of the module as a sense line.
- Provide a proper series capacitor at both **MIC\_P** and **MIC\_N** analog uplink inputs for DC blocking (C2 and C3 100 nF Murata GRM155R71C104K capacitors in Figure 77). This provides a high-pass filter for the microphone DC bias with proper cut-off frequency according to the value of the resistors of the microphone supply circuit. Then connect the signal lines to the microphone.
- Provide proper parts on each line connected to the external microphone as noise and EMI improvements, to minimize RF coupling and TDMA noise, according to the custom application requirements.
  - Mount an 82 nH series inductor with a Self Resonance Frequency  $\sim$ 1 GHz (e.g. the Murata LQG15HS82NJ02) on each microphone line (L1 and L2 inductors in Figure 77).
  - Mount a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each microphone line to solid ground plane (C4 and C5 capacitors in Figure 77).
- Use a microphone designed for GSM applications, which typically have internal built-in bypass capacitor.
- Provide a 47 nF series capacitor at both **SPK\_P** and **SPK\_N** analog downlink outputs for DC blocking (C8 and C9 Murata GRM155R71C473K capacitors in Figure 77). Then connect the lines to the differential input of a proper external audio amplifier, differential output which must be connected to the 8  $\Omega$  or 4  $\Omega$  loudspeaker. (See the Analog Devices SSM2305CPZ filter-less mono 2.8 W class-D Audio Amplifier in the circuit described in Figure 77.)
- Provide proper parts on each line connected to the external loudspeaker as noise and EMI improvements, to minimize RF coupling, according to EMC requirements of the custom application.
  - Mount a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each loudspeaker line to solid ground plane (C6 and C7 capacitors in Figure 77).
- Provide additional ESD protection (e.g. Bourns CG0402MLE-18G varistor) if the analog audio lines will be externally accessible on the application device, according to the EMC/ESD requirements of the custom application. The protection should be mounted close to an accessible point of the line (D1-D4 parts in the circuit described in Figure 77).



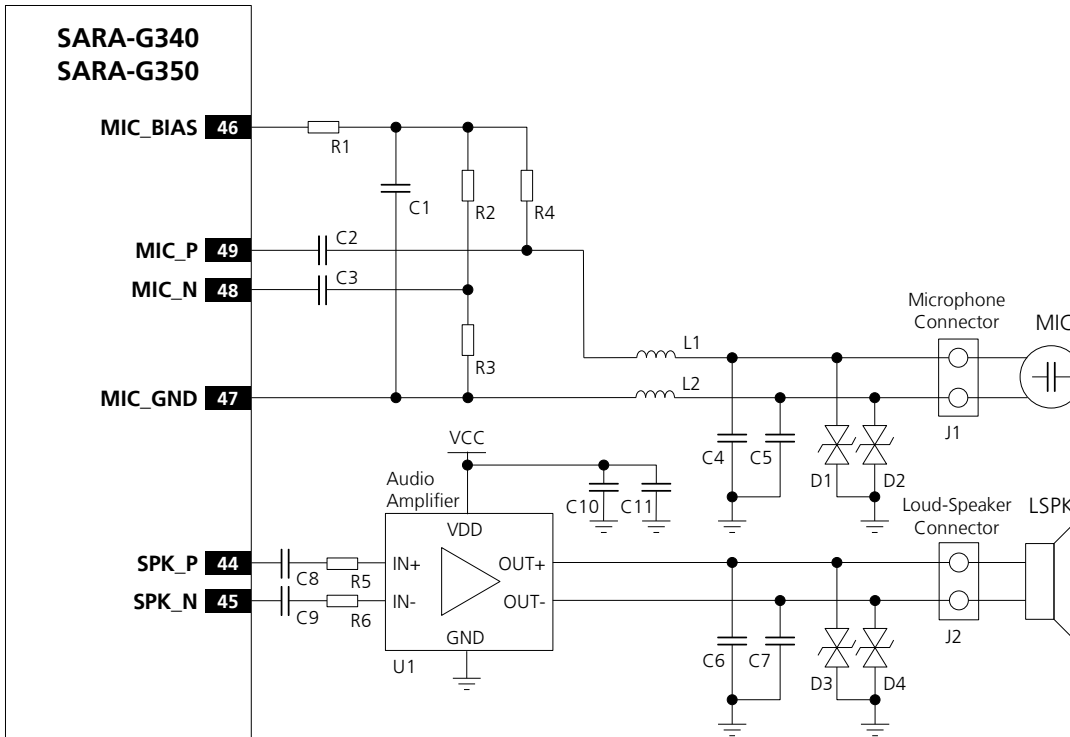


Figure 77: Analog audio interface hands-free mode application circuit

Reference	Description	Part Number – Manufacturer
C1, C10	10 $\mu$ F Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C2, C3, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA88 – Murata
C4, C5, C6, C7	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JA01 – Murata
C8, C9	47 nF Capacitor Ceramic X7R 0402 10% 16V	GRM155R71C473KA01 – Murata
D1, D2, D3, D4	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
J1	Microphone Connector	Various Manufacturers
J2	Speaker Connector	Various Manufacturers
L1, L2	82 nH Multilayer inductor 0402 (self resonance frequency $\sim$ 1 GHz)	LQG15HS82NJ02 – Murata
LSPK	8 $\Omega$ Loud-Speaker	Various Manufacturers
MIC	2.2 k $\Omega$ Electret Microphone	Various Manufacturers
R1, R2, R3, R4	2.2 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
R5, R6	0 $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-070RL – Yageo Phycomp
U1	Filter-less Mono 2.8 W Class-D Audio Amplifier	SSM2305CPZ – Analog Devices

Table 51: Example of components for analog audio interface hands-free mode application circuit



If the analog audio interface is not used, the analog audio pins (**MIC\_BIAS**, **MIC\_GND**, **MIC\_P**, **MIC\_N**, **SPK\_P**, **SPK\_N**) can be left unconnected on the application board.

### 2.7.1.3 Guidelines for external analog audio device connection circuit design

The differential analog audio I/O can be used to connect the module to an external analog audio device. Audio devices with a differential analog I/O are preferable, as they are more immune to external disturbances.

Figure 78 and Table 52 describe the application circuits, following the suggested circuit design-in.

Guidelines for the connection to a differential analog audio input:

- The **SPK\_P / SPK\_N** balanced output of the module must be connected to the differential input of the external audio device by means of series capacitors for DC blocking (e.g. 10  $\mu\text{F}$ ) to decouple the bias present at the module output, as described in the left side of Figure 78.

Guidelines for the connection to a single ended analog audio input:

- A proper differential to single ended circuit must be inserted from the **SPK\_P / SPK\_N** balanced output of the module to the single ended input of the external audio device, as described in the Figure 78 right side: 10  $\mu\text{F}$  series capacitors are provided to decouple the bias present at the module output, and a voltage divider is provided to properly adapt the signal level from module output to external audio device input.

Guidelines for the connection to a differential analog audio output:

- The **MIC\_P / MIC\_N** balanced input of the module must be connected to the differential output of the external audio device by means of series capacitors for DC blocking (e.g. 10  $\mu\text{F}$ ) to decouple the bias present at the module input, as described in the Figure 78 left side.

Guidelines for the connection to a single ended analog audio output:

- A proper single ended to differential circuit has to be inserted from the single ended output of the external audio device to the **MIC\_P / MIC\_N** balanced input of the module, as described in the Figure 78 right side: 10  $\mu\text{F}$  series capacitors are provided to decouple the bias present at the module input, and a voltage divider is provided to properly adapt the signal level from the external device output to the module input.

Additional guidelines for any connection:

- The DC-block series capacitor acts as high-pass filter for audio signals, with cut-off frequency depending on both the values of capacitor and on the input impedance of the device. For example: in case of differential input impedance of 600  $\Omega$ , the two 10  $\mu\text{F}$  capacitors will set the -3 dB cut-off frequency to 53 Hz, while for single ended connection to 600  $\Omega$  external device, the cut-off frequency with just the single 10  $\mu\text{F}$  capacitor will be 103 Hz. In both cases the high-pass filter has a low enough cut-off for proper frequency response.
- Use a suitable power-on sequence to avoid audio bump due to charging of the capacitor: the final audio stage should be always enabled as last one.
- The signal levels can be adapted by setting gain using AT commands (see u-blox AT Commands Manual [3], +USGC, +UMGC), but additional circuitry must be inserted if **SPK\_P / SPK\_N** output level of the module is too high for the audio device input or if the audio device output level is too high for **MIC\_P / MIC\_N**, as the voltage dividers present in the circuits described in Figure 78 right side to properly adapt the signal level.

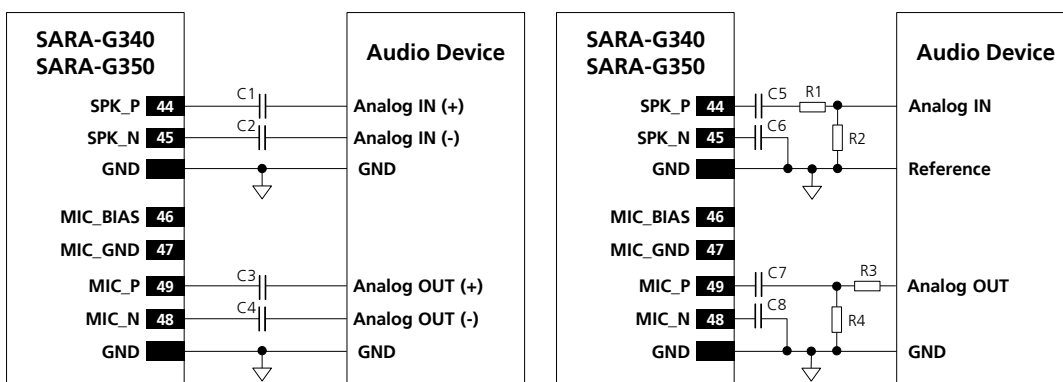


Figure 78: Application circuits to connect the module to audio devices with proper differential or single-ended input/output

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8	10 $\mu$ F Capacitor X5R 0603 5% 6.3 V	GRM188R60J106M – Murata
R1, R3	0 $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-070RL – Yageo Phycomp
R2, R4	Not populated	

**Table 52: Connection to an analog audio device**

#### 2.7.1.4 Guidelines for analog audio layout design

Accurate analog audio design is very important to obtain clear and high quality audio. The GSM signal burst has a repetition rate of 217 Hz that lies in the audible range. A careful layout is required to reduce the risk of noise from audio lines due to both **VCC** burst noise coupling and RF detection.

Guidelines for the uplink path, which is the most sensitive since the analog input signals are in the microVolts range, are the following:

- Avoid coupling of any noisy signal to microphone lines: it is strongly recommended to route microphone lines away from module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Keep ground separation from microphone lines to other noisy signals. Use an intermediate ground layer or vias wall for coplanar signals.
- Route microphone signal lines as a differential pair embedded in ground to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Route microphone reference as a signal line since the **MIC\_GND** pin is internally connected to ground as a sense line as the reference for the analog audio input.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place bypass capacitor for RF very close to active microphone. The preferred microphone should be designed for GSM applications which typically have internal built-in bypass capacitor for RF very close to active device. If the integrated FET detects the RF burst, the resulting DC level will be in the pass-band of the audio circuitry and cannot be filtered by any other device.

Guidelines for the downlink path are the following:

- The physical width of the audio output lines on the application board must be wide enough to minimize series resistance since the lines are connected to low impedance speaker transducer.
- Avoid coupling of any noisy signal to speaker lines: it is recommended to route speaker lines away from module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Route speaker signal lines as a differential pair embedded in ground up to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place bypass capacitor for RF close to the speaker.

## 2.7.2 Digital audio interface



SARA-G300 and SARA-G310 modules do not provide digital audio interface.

### 2.7.2.1 Guidelines for digital audio circuit design

The I<sup>2</sup>S digital audio interface of SARA-G3 and SARA-U2 series modules can be connected to an external digital audio device for voice applications.

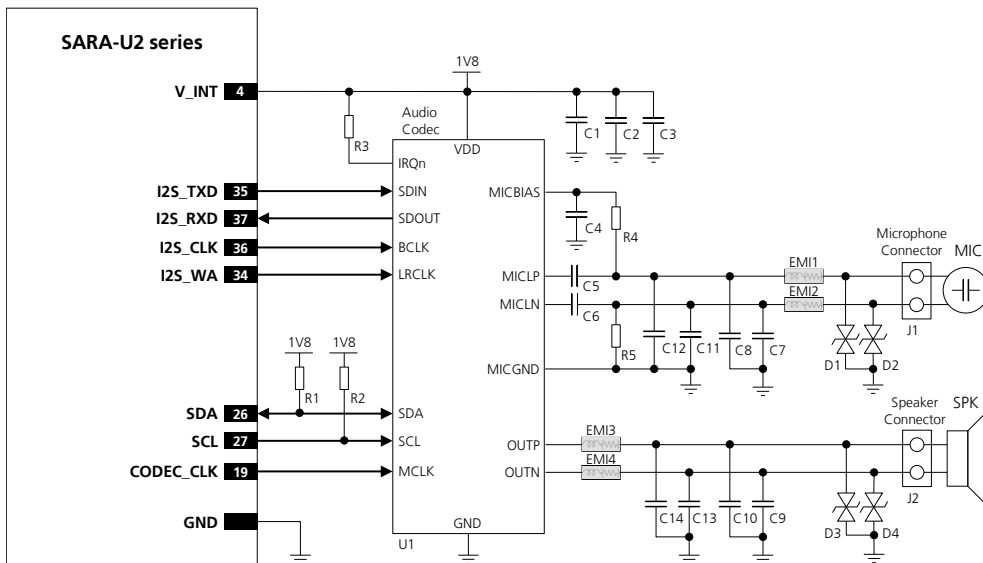
Any external digital audio device compliant to the configuration of the digital audio interface of the cellular module can be used, given that the external digital audio device has to provide:

- The opposite role: slave for SARA-G3 modules that act as master only; slave or master for SARA-U2 modules that may act as master or slave
- The same mode and frame format: PCM / short alignment or Normal I<sup>2</sup>S mode / long alignment mode with
  - data in 2's complement notation
  - MSB transmitted first
  - word length = 16-bit
  - frame length = 17-bit or 18-bit in PCM / short alignment mode (16 + 1 or 16 + 2 clock cycles, with Word Alignment / Synchronization signal set high for 1 clock cycle or 2 clock cycles), or
  - frame length = 32-bit in Normal I<sup>2</sup>S mode / long alignment mode (16 x 2 clock cycles)
- The same sample rate and serial clock frequency: as the clock frequency depends on the frame length and the sample rate, the clock frequency can be
  - 17 x <I2S\_sample\_rate> or 18 x <I2S\_sample\_rate> in PCM / short alignment mode, or
  - 16 x 2 x <I2S\_sample\_rate> in Normal I<sup>2</sup>S mode / long alignment mode
- Compatible voltage levels (1.80 V typ.), otherwise it is recommended to connect the 1.8 V digital audio interface of the module to the external 3.0 V (or similar) digital audio device by means of appropriate unidirectional voltage translators (e.g. Texas Instruments SN74AVC4T774 or SN74AVC2T245), using the module **V\_INT** output as 1.8 V supply for the voltage translators on the module side

For the appropriate selection of a compliant external digital audio device, see the section 1.10.2 including subsections 1.10.2.1 and 1.10.2.2. See the +UI2S AT command description in the u-blox AT Commands Manual [3] for further details regarding the capabilities and the possible settings of I<sup>2</sup>S digital audio interface of SARA-G3 and SARA-U2 series modules.

Figure 79 and Table 53 describe an application circuit example for the I<sup>2</sup>S digital audio interface of SARA-U2 modules providing voice capability using an external audio voice codec. DAC and ADC integrated in the external audio codec respectively converts an incoming digital data stream to analog audio output through a mono amplifier and converts the microphone input signal to the digital bit stream over the digital audio interface.

- The module's I<sup>2</sup>S interface (I<sup>2</sup>S master) is connected to the related pins of the external audio codec (I<sup>2</sup>S slave).
- The **V\_INT** output supplies the external audio codec, defining proper digital interfaces voltage level.
- The external audio codec is controlled by the SARA-U2 module using the DDC (I<sup>2</sup>C) interface: this interface can be concurrently used to communicate with u-blox GNSS receivers and with an external audio codec.
- The **CODEC\_CLK** pin of the SARA-U2 module (that provides a suitable digital output clock) is connected to the clock input of the external audio codec to provide clock reference.
- Additional components are provided for EMC and ESD immunity conformity: a 10 nF bypass capacitor and a series chip ferrite bead noise/EMI suppression filter provided on each microphone line input and speaker line output of the external codec as described in Figure 79 and Table 53. The necessity of these or other additional parts for EMC improvement may depend on the specific application board design.



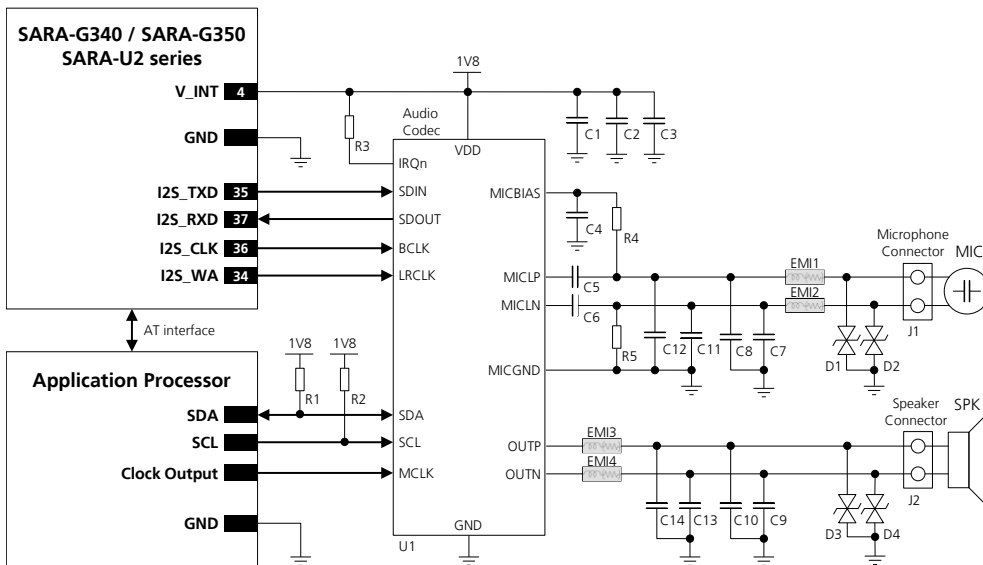
**Figure 79: Application circuit for connecting SARA-U2 modules with an external audio codec to provide voice capability**

Reference	Description	Part Number – Manufacturer
C1	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
C2, C4, C5, C6	1 $\mu$ F Capacitor Ceramic X5R 0402 10% 6.3 V	GRM155R60J105KE19 – Murata
C3	10 $\mu$ F Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C7, C8, C9, C10	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JZ01 – Murata
C11, C12, C13, C14	10 nF Capacitor Ceramic X5R 0402 10% 50V	GRM155R71C103KA88 – Murata
D1, D2, D3, D4	Low Capacitance ESD Protection	CG0402MLE-18G – Bourns
EMI1, EMI2, EMI3, EMI4	Chip Ferrite Bead Noise/EMI Suppression Filter 1800 Ohm at 100 MHz, 2700 Ohm at 1 GHz	BLM15HD182SN1 – Murata
J1	Microphone Connector	Various manufacturers
J2	Speaker Connector	Various manufacturers
MIC	2.2 k $\Omega$ Electret Microphone	Various manufacturers
R1, R2	4.7 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	10 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R4, R5	2.2 k $\Omega$ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
SPK	32 $\Omega$ Speaker	Various manufacturers
U1	16-Bit Mono Audio Voice Codec	MAX9860ETG+ - Maxim

**Table 53: Example of components for connecting SARA-U2 modules with an external audio codec to provide voice capability**

Figure 80 describes an application circuit example for connecting the I<sup>2</sup>S digital audio interface of SARA-G340, SARA-G350 and SARA-U2 modules to an external audio voice codec, using the same parts listed in Table 53.

- The module's I<sup>2</sup>S interface (I<sup>2</sup>S master) is connected to the related pins of the external audio codec (I<sup>2</sup>S slave).
- The **V\_INT** output supplies the external audio codec, defining proper digital interfaces voltage level.
- The external audio codec is controlled by the application processor using the DDC (I<sup>2</sup>C) interface.
- The clock output of the application processor is connected to the clock input of the external audio codec to provide clock reference.
- Additional components are provided for EMC and ESD immunity conformity: a 10 nF bypass capacitor and a series chip ferrite bead noise/EMI suppression filter provided on each microphone line input and speaker line output of the external codec as described in Figure 80 and Table 53. The necessity of these or other additional parts for EMC improvement may depend on the specific application board design.



**Figure 80: Application circuit for connecting SARA-G3 / SARA-U2 modules with an external audio codec**

As in general any external digital audio device compliant to the configuration of the digital audio interface of the cellular module can be used, various external audio codecs other than the one described in Figure 79, Figure 80 and Table 53 can be used to provide voice capability. For example the Maxim MAX9867 audio codec, the Maxim MAX9880A audio codec as well as many other parts produced by the same or other various manufacturers (including Texas Instruments, Wolfson / Cirrus Logic, Freescale, etc) can be used instead of the Maxim MAX9860 audio codec described above, implementing and configuring an appropriate application circuit according to the specific device and application requirements.



Any external signal connected to the digital audio interface must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V\_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode and during the module power-on sequence.



ESD sensitivity rating of I<sup>2</sup>S interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.



If the I<sup>2</sup>S digital audio pins are not used, they can be left unconnected on the application board.

### 2.7.2.2 Guidelines for digital audio layout design

The I<sup>2</sup>S interfaces lines (**I2S\_CLK**, **I2S\_RX**, **I2S\_TX**, **I2S\_WA**) require the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

## 2.8 General Purpose Input/Output (GPIO)

### 2.8.1.1 Guidelines for GPIO circuit design

The following application circuits are suggested as a general guideline for the usage of the GPIO pins available with the SARA-G340 / SARA-G350 and SARA-U2 series modules, according to the related custom function.

Figure 81 describes an application circuit for a typical usage of some GPIO functions of the modules:

- Network indication function provided by the **GPIO1** pin
- GNSS supply enable function provided by the **GPIO2** pin
- GNSS data ready function provided by the **GPIO3** pin
- GNSS RTC sharing function provided by the **GPIO4** pin

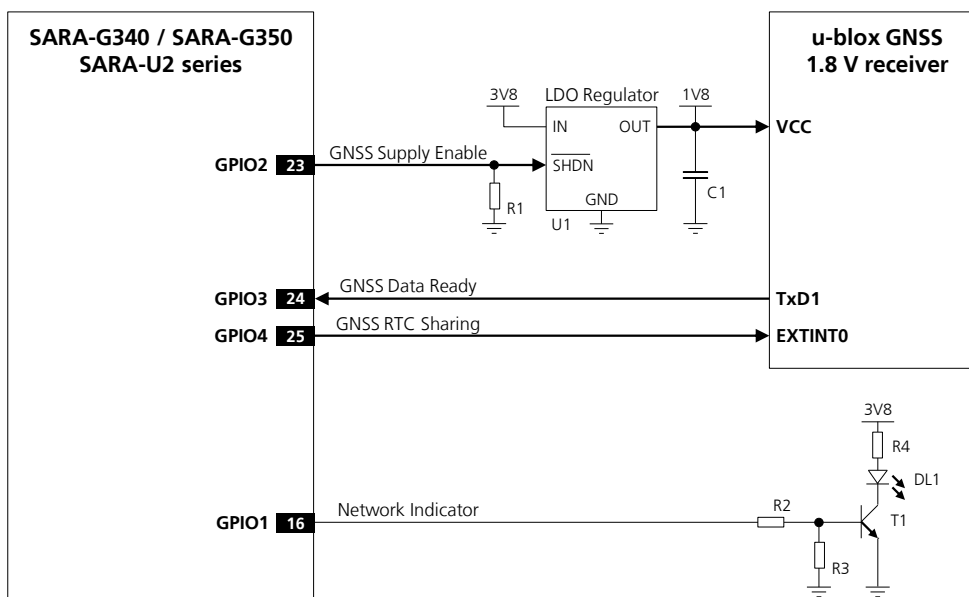


Figure 81: GPIO application circuit

Reference	Description	Part Number - Manufacturer
R1	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
U1	Voltage Regulator for GNSS receiver	See GNSS module Hardware Integration Manual
R2	10 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R4	820 Ω Resistor 0402 5% 0.1 W	Various manufacturers
DL1	LED Red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT Transistor	BC847 - Infineon

Table 54: Components for GPIO application circuit



Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO.



ESD sensitivity rating of the GPIO pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

Any external signal connected to the GPIOs must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V\_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode and during the module power-on sequence.

If the GPIO pins are not used, they can be left unconnected on the application board.

### 2.8.1.2 Guidelines for GPIO layout design

The general purpose input/output pins are generally not critical for layout.

## 2.9 Reserved pins (RSVD)

SARA-G3 and SARA-U2 series modules have pins reserved for future use. All the **RSVD** pins, except pin number 33, can be left unconnected on the application board. Figure 82 illustrates the application circuit.

Pin 33 (**RSVD**) must be connected to GND.

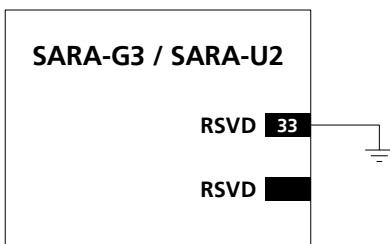


Figure 82: Application circuit for the reserved pins (RSVD)

## 2.10 Module placement

Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.

Make sure that the module, RF and analog parts / circuits are clearly separated from any possible source of radiated energy, including digital circuits that can radiate some digital frequency harmonics, which can produce Electro-Magnetic Interference affecting module, RF and analog parts / circuits' performance or implement proper countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Make sure that the module, RF and analog parts / circuits, high speed digital circuits are clearly separated from any sensitive part / circuit which may be affected by Electro-Magnetic Interference or employ countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Provide enough clearance between the module and any external part.

The heat dissipation during transmission at maximum power can raise the temperature of the module and its environment, as the application board locations near and below the SARA-G3 series modules and, more significantly, the locations near and below the SARA-U2 series modules: avoid placing temperature sensitive devices close to the module.



## 2.11 Module footprint and paste mask

Figure 83 and Table 55 describe the suggested footprint (i.e. copper mask) and paste mask layout for SARA modules: the proposed land pattern layout reflects the modules' pins layout, while the proposed stencil apertures layout is slightly different (see the  $F''$ ,  $H''$ ,  $I''$ ,  $J''$ ,  $O''$  parameters compared to the  $F'$ ,  $H'$ ,  $I'$ ,  $J'$ ,  $O'$  ones).

The Non Solder Mask Defined (NSMD) pad type is recommended over the Solder Mask Defined (SMD) pad type, implementing the solder mask opening 50  $\mu\text{m}$  larger per side than the corresponding copper pad.

The recommended solder paste thickness is 150  $\mu\text{m}$ , according to application production process requirements.

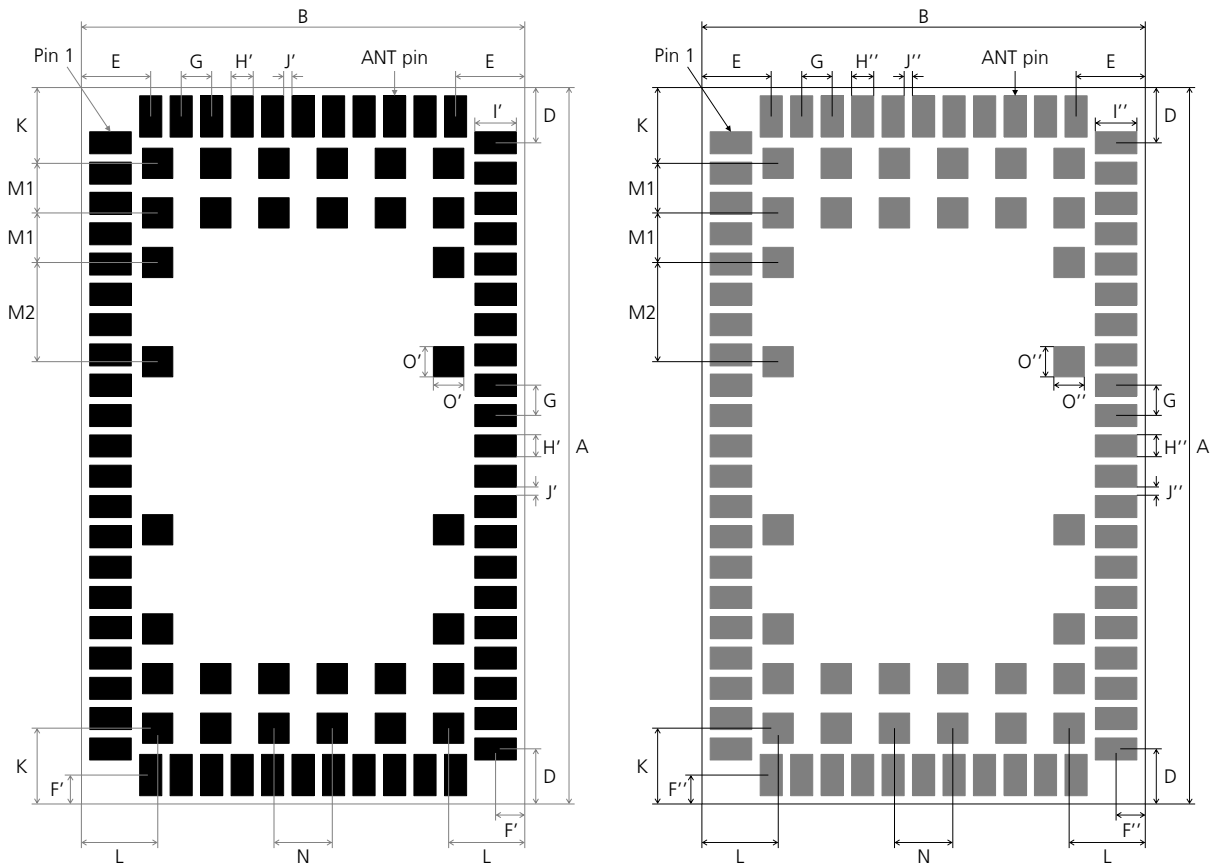


Figure 83: SARA-G3 and SARA-U2 series modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	G	1.10 mm	K	2.75 mm
B	16.0 mm	H'	0.80 mm	L	2.75 mm
C	3.00 mm	H''	0.75 mm	M1	1.80 mm
D	2.00 mm	I'	1.50 mm	M2	3.60 mm
E	2.50 mm	I''	1.55 mm	N	2.10 mm
F'	1.05 mm	J'	0.30 mm	O'	1.10 mm
F''	1.00 mm	J''	0.35 mm	O''	1.05 mm

Table 55: SARA-G3 and SARA-U2 series modules suggested footprint and paste mask dimensions



These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

## 2.12 Thermal guidelines



SARA-G3 and SARA-U2 series module operating temperature range and module thermal resistance are specified in the SARA-G3 series Data Sheet [1] or the SARA-U2 series Data Sheet [2].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload or voice call in connected-mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks; however the application should be correctly designed to cope with it.

During transmission at maximum RF power the SARA-G3 modules generate thermal power that can exceed 1 W, whereas the SARA-U2 modules generate thermal power that can exceed 2 W: these are indicative values since the exact generated power strictly depends on operating condition such as the cellular radio access technology, the number of allocated TX slot, the transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application, in particular for SARA-U2 modules when operating in the 3G cellular radio access technology.



SARA-U2 modules implement an integrated self protection algorithm when operating in the 3G cellular radio access technology: the module reduces the transmitted power when the temperature internally sensed in the integrated 3G Power Amplifier approaches the maximum allowed internal temperature, to guarantee device functionality and long life span.

The spreading of the Module-to-Ambient thermal resistance ( $R_{th,M-A}$ ) depends on module operating condition: the overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

Mounting a SARA-G3 module on a 79 mm x 62 mm x 1.41 mm 4-Layers PCB with a high coverage of copper in still air conditions<sup>11</sup>, the increase of the module temperature<sup>12</sup> in different modes of operation, referred to idle state initial condition<sup>13</sup>, can be summarized as following:

- ~8 °C during a GSM voice call (1 TX slot, 1 RX slot) at max TX power
- ~12 °C during a GPRS data transfer (2 TX slots, 3 RX slots) at max TX power



The Module-to-Ambient thermal resistance value and the relative increase of module temperature are application dependent, according to the specific mechanical deployment of the module, e.g. application PCB dimensions and characteristics, mechanical shells enclosure and air flow conditions.

The increase of thermal dissipation, i.e. the Module-to-Ambient thermal resistance reduction, will decrease the temperature for internal circuitry of the SARA-G3 and SARA-U2 series modules for a given operating ambient temperature. This improves device long-term reliability for applications operating at high ambient temperature.

A few hardware techniques may be used to reduce the Module-to-Ambient thermal resistance in the application:

- Connect each **GND** pin with solid ground layer of the application board and connect each ground area of the multilayer application board with complete via stack down to main ground layer
- Provide a ground plane as wide as possible on the application board
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power

<sup>11</sup> Refer to SARA-G3 and SARA-U2 series Data Sheet [1] for the  $R_{th,M-A}$  value in this application condition

<sup>12</sup> Temperature is measured by internal sensor of cellular module

<sup>13</sup> Steady state thermal equilibrium is assumed. The module's temperature in idle state can be considered equal to ambient temperature

- Optimize the thermal design of any high-power component included in the application, as linear regulators and amplifiers, to optimize overall temperature distribution in the application device
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure of the application device that integrates the module) so that it provides good thermal dissipation
- Force ventilation air-flow within mechanical enclosure
- Provide a heat sink component attached to the module top side, with electrically insulated / high thermal conductivity adhesive, or on the backside of the application board, below the cellular module, as a large part of the heat is transported through the GND pads and dissipated over the backside of the application board

For example, after the installation of a robust aluminum heat-sink with forced air ventilation on the back of the same application board described above, the Module-to-Ambient thermal resistance ( $R_{th,M-A}$ ) is reduced up to the Module-to-Case thermal resistance ( $R_{th,M-C}$ ) defined in the SARA-G3 series Data Sheet [1] or the SARA-U2 series Data Sheet [2].

The effect of lower  $R_{th,M-A}$  due to the installation of a robust heat-sink on the backside of the application board with forced air ventilation can be seen from the module temperature increase, which now can be summarized as following for SARA-G3 modules:

- ~1 °C during a GSM voice call (1 TX slot, 1 RX slot) at the maximum TX power
- ~2 °C during a GPRS data transfer (2 TX slots, 3 RX slots) at the maximum TX power

Beside the reduction of the Module-to-Ambient thermal resistance implemented by the hardware design of the application device integrating a SARA-G3 and SARA-U2 series module, the increase of module temperature can be moderated by the software implementation of the application.

Since the most critical condition concerning module thermal power occurs when module connected-mode is enabled, the actual module thermal power depends, as module current consumption, on the radio access mode, the operating band and the average TX power.

A few software techniques may be implemented to reduce the module temperature increase in the application:

- Select the radio access mode which provides lower temperature increase by means of AT command (see the u-blox AT Commands Manual [3])
- Select by means of AT command the GPRS multi-slot class which provides lower current consumption (see current consumption values reported in SARA-G3 series Data Sheet [1] or SARA-U2 series Data Sheet [2], and u-blox AT Commands Manual [3], +UCLASS command)
- Select by means of AT command the operating band which provides lower current consumption (see current consumption values reported in SARA-G3 series Data Sheet [1] or SARA-U2 series Data Sheet [2], and u-blox AT Commands Manual [3], +UBANDSEL command)
- Enable module connected-mode for a given time period and then disable it for a time period enough long to properly mitigate temperature increase

## 2.13 ESD guidelines

The sections 2.13.1 and 2.13.2 are related to EMC / ESD immunity, herein described in section 2.13.1. The modules are ESD sensitive devices and the ESD sensitivity for each pin (as Human Body Model according to JESD22-A114F) is specified in SARA-G3 series Data Sheet [1] or SARA-U2 series Data Sheet [2], requiring special precautions when handling: for ESD handling guidelines see section 3.2.

### 2.13.1 ESD immunity test overview

The immunity of devices integrating SARA-G3 and SARA-U2 series modules to Electro-Static Discharge (ESD) is part of the Electro-Magnetic Compatibility (EMC) conformity, which is required for products bearing the CE marking, compliant with the R&TTE Directive (99/5/EC), the EMC Directive (89/336/EEC) and the Low Voltage Directive (73/23/EEC) issued by the Commission of the European Community.

Compliance with these directives implies conformity to the following European Norms for device ESD immunity: ESD testing standard CENELEC EN 61000-4-2 [18] and the radio equipment standards ETSI EN 301 489-1 [19], ETSI EN 301 489-7 [20], ETSI EN 301 489-24 [21], which requirements are summarized in Table 56.

The ESD immunity test is performed at the enclosure port, defined by ETSI EN 301 489-1 [19] as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is defined as all insulating and conductive surfaces housing the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

The applicability of the ESD immunity test to the whole device depends on the device classification as defined by ETSI EN 301 489-1 [19]. Applicability of the ESD immunity test to the relative device ports or the relative interconnecting cables to auxiliary equipments, depends on device accessible interfaces and manufacturer requirements, as defined by ETSI EN 301 489-1 [19].

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in CENELEC EN 61000-4-2 [18].



For the definition of integral antenna, removable antenna, antenna port, device classification see ETSI EN 301 489-1 [19], whereas for contact and air discharges definitions see CENELEC EN 61000-4-2 [18]

Application	Category	Immunity Level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration	Contact Discharge	4 kV
	Air Discharge	8 kV

**Table 56: EMC / ESD immunity requirements as defined by CENELEC EN 61000-4-2, ETSI EN 301 489-1, 301 489-7, 301 489-24**

### 2.13.2 ESD immunity test of u-blox SARA-G3 and SARA-U2 reference designs

EMC certification tests (including ESD immunity) have been successfully performed on the u-blox SARA-G3 and SARA-U2 reference designs according to applicable European Norms (see Table 56), as required for customized devices integrating the modules for R&TTED and European Conformance CE mark.

The EMC / ESD approved u-blox reference designs consist of a SARA-G3 or a SARA-U2 module soldered onto a motherboard which provides supply interface, SIM card, headset and communication port. An external cellular antenna is connected to an SMA connector provided on the motherboard.

Since an external antenna is used, the antenna port can be separated from the enclosure port. The reference design is not enclosed in a box so that the enclosure port is not identified with physical surfaces. Therefore, some test cases cannot be applied. Only the antenna port is identified as accessible for direct ESD exposure.

Table 57 reports the u-blox SARA-G3 and SARA-U2 reference designs ESD immunity test results, according to the CENELEC EN 61000-4-2 [18], ETSI EN 301 489-1 [19], 301 489-7 [20], 301 489-24 [21] test requirements.

Category	Application	Immunity Level	Remarks
Contact Discharge to coupling planes (indirect contact discharge)	Enclosure	+4 kV / -4 kV	
Contact Discharges to conducted surfaces (direct contact discharge)	Enclosure port	Not Applicable	Test not applicable to u-blox reference design because it does not provide enclosure surface. The test is applicable only to equipments providing conductive enclosure surface.
	Antenna port	+4 kV / -4 kV	Test applicable to u-blox reference design because it provides antenna with conductive & insulating surfaces. The test is applicable only to equipments providing antenna with conductive surface.
Air Discharge at insulating surfaces	Enclosure port	Not Applicable	Test not applicable to the u-blox reference design because it does not provide an enclosure surface. The test is applicable only to equipments providing insulating enclosure surface.
	Antenna port	+8 kV / -8 kV	Test applicable to u-blox reference design because it provides antenna with conductive & insulating surfaces. The test is applicable only to equipments providing antenna with insulating surface.

**Table 57: Enclosure ESD immunity level of u-blox SARA-G3 and SARA-U2 reference designs**



SARA-G3 and SARA-U2 reference designs implement all the ESD precautions described in section 2.13.3.

### 2.13.3 ESD application circuits

The application circuits described in this section are recommended and should be implemented in any device that integrates a SARA-G3 and SARA-U2 series module, according to the application board classification (see ETSI EN 301 489-1 [19]), to satisfy the requirements for ESD immunity test summarized in Table 56.

#### Antenna interface

The **ANT** pin of SARA-G3 modules provides ESD immunity up to  $\pm 4$  kV for direct Contact Discharge and up to  $\pm 8$  kV for Air Discharge according to IEC 61000-4-2: no further precaution to ESD immunity test is needed, as implemented in the EMC / ESD approved reference design of SARA-G3 modules.

The **ANT** pin of SARA-U2 modules provides ESD immunity up to  $\pm 2$  kV for direct Contact Discharge and up to  $\pm 4$  kV for Air Discharge according to IEC 61000-4-2: higher protection level is required if the line is externally accessible on the device (i.e. the application board where the SARA-U2 module is mounted).

The following precautions are suggested for satisfying ESD immunity test requirements using SARA-U2 modules:

- If the device implements an embedded antenna, the device insulating enclosure should provide protection to direct contact discharge up to  $\pm 4$  kV and protection to air discharge up to  $\pm 8$  kV to the antenna interface
- If the device implements an external antenna, the antenna and its connecting cable should provide a completely insulated enclosure able to provide protection to direct contact discharge up to  $\pm 4$  kV and protection to air discharge up to  $\pm 8$  kV to the whole antenna and cable surfaces
- If the device implements an external antenna, and the antenna and its connecting cable do not provide a completely insulated enclosure able to provide protection to direct contact discharge up to  $\pm 4$  kV and protection to air discharge up to  $\pm 8$  kV to the whole antenna and cable surfaces, an external high pass filter, consisting of a series 15 pF capacitor (Murata GRM1555C1H150JA01) and a shunt 39 nH coil (Murata

LQG15HN39NJ02) should be implemented at the antenna port as described in the Figure 52, Figure 53 and Figure 54, as implemented in the EMC / ESD approved reference design of SARA-U2 modules

The antenna interface application circuit implemented in the EMC / ESD approved reference designs of SARA-G3 and SARA-U2 series modules is described in Figure 52 in case of antenna detection circuit not implemented, and is described in Figure 53 and Table 35 in case of antenna detection circuit implemented (section 2.4).

### RESET\_N pin

The following precautions are suggested for the **RESET\_N** line of SARA-G3 and SARA-U2 series modules, depending on the application board handling, to satisfy ESD immunity test requirements:

- It is recommended to keep the connection line to **RESET\_N** as short as possible

Maximum ESD sensitivity rating of the **RESET\_N** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the **RESET\_N** pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG varistor array or EPCOS CT0402S14AHSG varistor) should be mounted on the **RESET\_N** line, close to accessible point

The **RESET\_N** application circuit implemented in the EMC / ESD approved reference design of SARA-G3 modules is described in Figure 46 and Table 30 (section 2.3.2).

### SIM interface

The following precautions are suggested for SARA-G3 and SARA-U2 modules SIM interface (**VSIM**, **SIM\_RST**, **SIM\_IO**, **SIM\_CLK**), depending on the application board handling, to satisfy ESD immunity test requirements:

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470J) must be mounted on the lines connected to **VSIM**, **SIM\_RST**, **SIM\_IO** and **SIM\_CLK** pins to assure SIM interface functionality when an electrostatic discharge is applied to the application board enclosure
- It is suggested to use as short as possible connection lines at SIM pins

Maximum ESD sensitivity rating of SIM interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if SIM interface pins are externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A low capacitance (i.e. less than 10 pF) ESD protection device (e.g. Tyco Electronics PESD0402-140) should be mounted on each SIM interface line, close to accessible points (i.e. close to the SIM card holder)

The SIM interface application circuit implemented in the EMC / ESD approved reference design of SARA-G3 modules is described in Figure 57 and Table 38 (section 2.5).

### Other pins and interfaces

All the module pins that are externally accessible on the device integrating SARA-G3 and SARA-U2 series module should be included in the ESD immunity test since they are considered to be a port as defined in ETSI EN 301 489-1 [19]. Depending on applicability, to satisfy ESD immunity test requirements according to ESD category level, all the module pins that are externally accessible should be protected up to  $\pm 4$  kV for direct Contact Discharge and up to  $\pm 8$  kV for Air Discharge applied to the enclosure surface.

The maximum ESD sensitivity rating of all the other pins of the module is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the related pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A very low capacitance (i.e. less or equal to 1 pF) ESD protection device (e.g. Tyco Electronics PESD0402-140) should be mounted on each high speed USB line, close to accessible points (i.e. close to the USB connector)
- A general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG or EPCOS CT0402S14AHSG varistor) should be mounted on each generic interface line, close to accessible point

## 2.14 SARA-G350 ATEX integration in explosive atmospheres applications

### 2.14.1 General guidelines

SARA-G350 ATEX modules are certified as components intended for use in potentially explosive atmospheres (see section 4.5 and see the 'Approvals' section of the SARA-G3 series Data Sheet [1] for further details), with the following marking:

- Ex II 1G, Ex ia IIC/IIB

According to the marking stated above, the SARA-G350 ATEX modules are certified as electrical equipment of:

- group 'II': intended for use in areas with explosive gas atmosphere other than mines susceptible to firedamp
- category '1G': intended for use in zone 0 hazardous areas, in which explosive atmospheres caused by mixtures of air and gases, vapours or mists are continuously present, for long periods or frequently, so that the modules are also suitable for applications intended for use in zone 1 and zone 2 hazardous areas
- level of protection 'ia': intrinsically safe apparatus with very high level of protection, not capable of causing ignition in normal operation and with the application of one countable fault or a combination of any two countable fault plus those non-countable faults which give the most onerous condition
- subdivision 'IIC/IIB': intended for use in areas where the nature of the explosive gas atmosphere is considered very dangerous based on the Maximum Experimental Safe Gap or the Minimum Ignition Current ratio of the explosive gas atmosphere in which the equipment may be installed (typical gases are hydrogen, acetylene, carbon disulphide), so that the modules are also suitable for applications intended for use in subdivision IIB (typical gases are ethylene, coke oven gas and other industrial gases) and subdivision IIA (typical gases are industrial methane, propane, petrol and the majority of industrial gases)

The temperature range of use of SARA-G350 ATEX modules is defined in the 'Operating temperature range' section of the SARA-G3 series Data Sheet [1].

Even if the SARA-G350 ATEX modules are certified as components intended for use in potentially explosive atmospheres as described above, the application device that integrates the module must be approved under all the certification schemes required by the specific application device to be deployed in the market as apparatus intended for use in potentially explosive atmospheres.

The certification scheme approvals required for the application device integrating SARA-G350 ATEX modules, intended for use in potentially explosive atmospheres, may differ depending on the following topics:

- the country or the region where the application device must be deployed
- the classification of the application device in relation to the use in potentially explosive atmospheres
- the classification of the hazardous areas in which the application device is intended for use



Any specific applicable requirement for the implementation of the apparatus integrating SARA-G350 ATEX modules, intended for use in potentially explosive atmospheres, must be fulfilled according to the exact applicable standards: check the detailed requisites on the pertinent normatives for the application, as for example the IEC 60079-0 [32], IEC 60079-11 [33], IEC 60079-26 [34] standards.



The certification of the application device that integrates a SARA-G350 ATEX module and the compliance of the application device with all the applicable certification schemes, directives and standards required for use in potentially explosive atmospheres are the sole responsibility of the application device manufacturer.

The application device integrating a SARA-G350 ATEX module for use in potentially explosive atmospheres must be designed so that any circuit/part of the apparatus shall not invalidate the specific characteristics of the type of protection of the SARA-G350 ATEX module electrical equipment.

The intrinsic safety 'i' type of protection of SARA-G350 ATEX modules is based on the restriction of electrical energy within equipment and of interconnecting wiring exposed to the explosive atmosphere to a level below that which can cause ignition by either sparking or heating effects.



The following input and equivalent parameters must be considered integrating a SARA-G350 ATEX module in an application device intended for use in potentially explosive atmospheres:

- Total internal capacitance,  $C_i = 103 \mu\text{F}$
- Total internal inductance,  $L_i = 4.1 \mu\text{H}$
- The module does not contain blocks which increase the voltage (e.g. like step-up, duplicators, boosters, etc.)

The nameplate of SARA-G350 ATEX modules is described in the 'Product labeling' section of the SARA-G3 series Data Sheet [1]. Additional information can be found on the SARA-G350 ATEX modules' certificate of compliancy for use in potentially explosive atmospheres available on our website ([www.u-blox.com](http://www.u-blox.com)).



The final enclosure of the application device integrating SARA-G350 ATEX modules, intended for use in potentially explosive atmospheres, must guarantee a minimum degree of ingress protection of IP20.

### 2.14.2 Guidelines for VCC supply circuit design

The power supply ratings, average and pulse, must be considered in the design of the **VCC** supply circuit on the application device integrating SARA-G350 ATEX module, implementing proper circuits providing adequate maximum voltage and current to the **VCC** supply input of SARA-G350 ATEX modules, according to the specific potentially explosive gas atmosphere category subdivision where the apparatus is intended for use.

The following maximum input and equivalent parameters must be considered in gas sub-division IIC:

- $U_i = 3.8 \text{ V}$
- $I_i = 1.6 \text{ A (burst)}$
- $P_i = 2.5 \text{ W}$
- $C_i = 103 \mu\text{F}$
- $L_i = 4.1 \mu\text{H}$

The following maximum input and equivalent parameters must be considered in gas sub-divisions IIB, IIA:

- $U_i = 4.2 \text{ V}$
- $I_i = 2.5 \text{ A (burst)}$
- $P_i = 2.5 \text{ W}$
- $C_i = 103 \mu\text{F}$
- $L_i = 4.1 \mu\text{H}$

#### Primary and secondary cells and batteries

Cells and batteries incorporated into equipment with intrinsic safety 'i' protection to potentially explosive gas atmosphere shall conform to the requirements of the IEC 60079-0 [32] and IEC 60079-11 ATEX standards [33].

#### Shunt voltage limiters

For Level of Protection 'ia', the application of controllable semiconductor components as shunt voltage limiting devices, for example transistors, thyristors, voltage/current regulators, etc., may be permitted if both the input and output circuits are intrinsically safe circuits or where it can be shown that they cannot be subjected to transients from the power supply network. In circuits complying with the above, two devices are considered to be an infallible assembly.

For Level of Protection 'ia', three independent active voltage limitation semiconductor circuits may be used in associated apparatus provided the transient conditions of the clause 7.5.1 of IEC 60079-11 standard are met. These circuits shall also be tested in accordance with the clause 10.1.5.3 of the IEC 60079-11 standard [33].



### Series current limiters

The use of three series blocking diodes in circuits of Level of Protection 'ia' is permitted, however, other semiconductors and controllable semiconductor devices shall be used as series current-limiting devices only in Level of Protection 'ib' or 'ic' apparatus. However, for power limitation purposes, Level of Protection 'ia' apparatus may use series current limiters consisting of controllable and non-controllable semiconductor devices.

The use of semiconductors and controllable semiconductor devices as current-limiting devices for spark ignition limitation is not permitted for Level of Protection 'ia' apparatus because of their possible use in areas in which a continuous or frequent presence of an explosive atmosphere may coincide with the possibility of a brief transient which could cause ignition. The maximum current that may be delivered may have a brief transient but will not be taken as  $I_o$ , because the compliance with the spark ignition test of the clause 10.1 of IEC 60079-11 standard [33] would have established the successful limitation of the energy in this transient.

### Protection against polarity reversal

Protection against polarity reversal shall be provided within intrinsically safe apparatus to prevent invalidation of the type of protection as a result of reversal of the polarity of supplies to that intrinsically safe apparatus or at connections between cells of a battery where this could occur. For this purpose, single diode shall be acceptable.

### Other considerations

All the recommendations reported in the section 2.14.1 must be considered for the implementation of the **VCC** supply circuit on application integrating SARA-G350 ATEX modules intended for use in potentially explosive atmospheres. Any specific applicable requirement for the **VCC** supply circuit design must be fulfilled according to all the exact applicable standards for the apparatus.



Check the detailed requisites on the pertinent normatives for the application apparatus, as for example the IEC 60079-0 [32], IEC 60079-11 [33], IEC 60079-26 [34] standards.

## 2.14.3 Guidelines for antenna RF interface design

The RF output power of the SARA-G350 ATEX modules transmitter is compliant to all the applicable 3GPP / ETSI standards, with a maximum output of 2 W RF pulse power and 1.15 mJ RF pulse energy in 850/900 MHz bands and with a maximum output of 1 W RF pulse power and 0.58 mJ RF pulse energy in the 1800/1900 MHz bands according to the GSM/GPRS power classes stated in Table 3.

The RF threshold power of the application device integrating a SARA-G350 ATEX module is defined, according to the IEC 60079-0 ATEX standard [32], as the product of the effective output power of the transmitter (the SARA-G350 ATEX module) multiplied by the antenna gain (implemented/used on the application device).

The RF threshold power of the application device integrating a SARA-G350 ATEX module transmitter, according to the IEC 60079-0 ATEX standard [32], must not exceed the limits shown in Table 58.

Gas group II subdivision	RF threshold power limits according to the IEC 60079-0 ATEX standard
IIA (a typical gas is propane)	6.0 W
IIB (a typical gas is ethylene)	3.5 W
IIC (a typical gas is hydrogen)	2.0 W

**Table 58: RF threshold power limits for the different gas group II subdivisions according to the IEC 60079-0 ATEX standard [32]**



The system antenna(s) implemented/used on the application device for SARA-G350 ATEX modules must be designed/selected so that the antenna gain (i.e. the combined transmission line, connector, cable losses and radiating element gain) multiplied by the output power of the transmitter (SARA-G350 ATEX module) does not exceed the limits shown in Table 58.

## 2.15 Schematic for SARA-G3 and SARA-U2 series module integration

### 2.15.1 Schematic for SARA-G300 / SARA-G310 modules integration

Figure 84 is an example of a schematic diagram where a SARA-G300 / SARA-G310 module is integrated into an application board, using all the available interfaces and functions of the module.

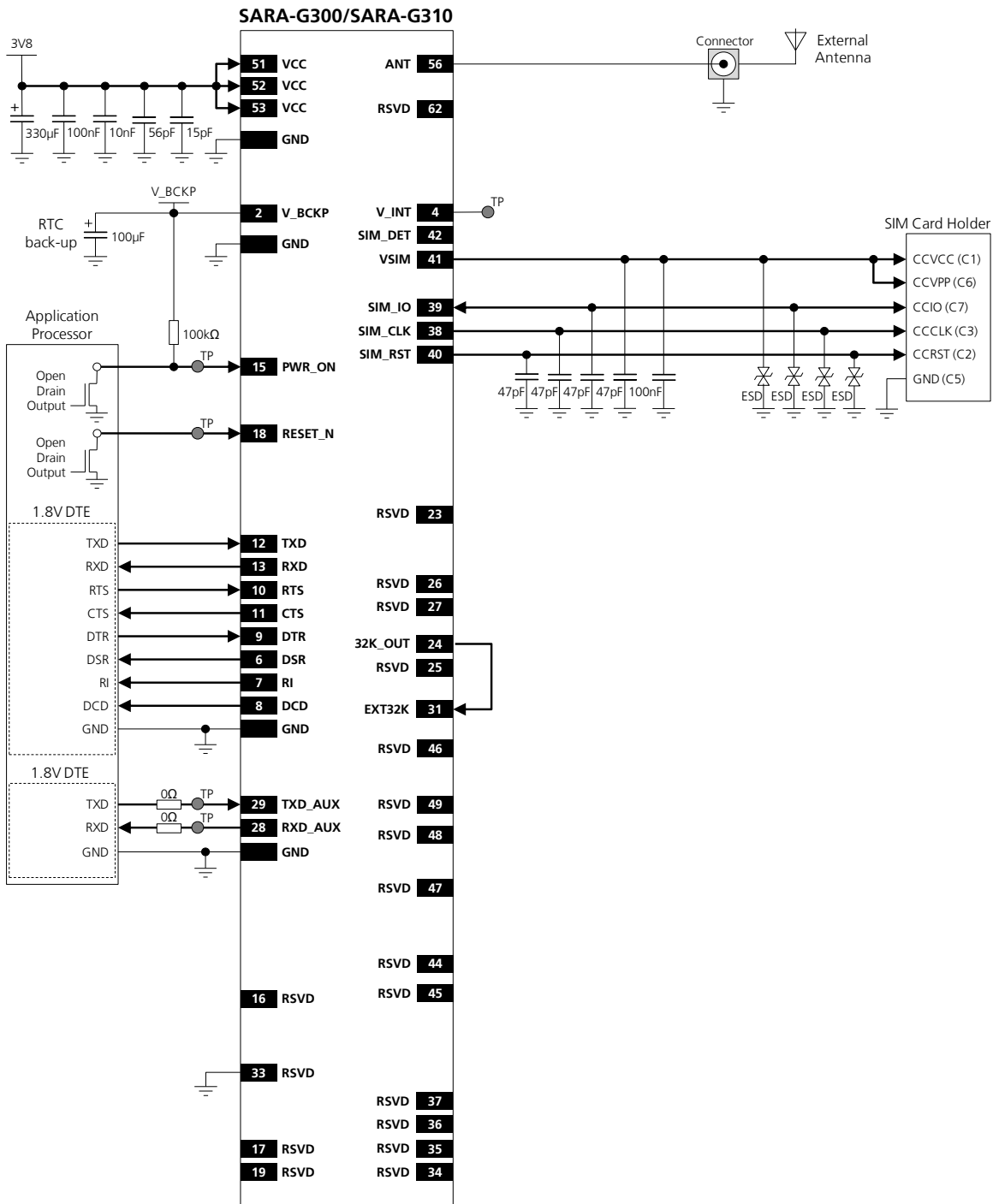


Figure 84: Example of schematic diagram to integrate SARA-G300/G310 modules in an application board, using all the interfaces

### 2.15.2 Schematic for SARA-G340 / SARA-G350 modules integration

Figure 85 is an example of a schematic diagram where a SARA-G340 / SARA-G350 module is integrated into an application board, using all the available interfaces and functions of the module.

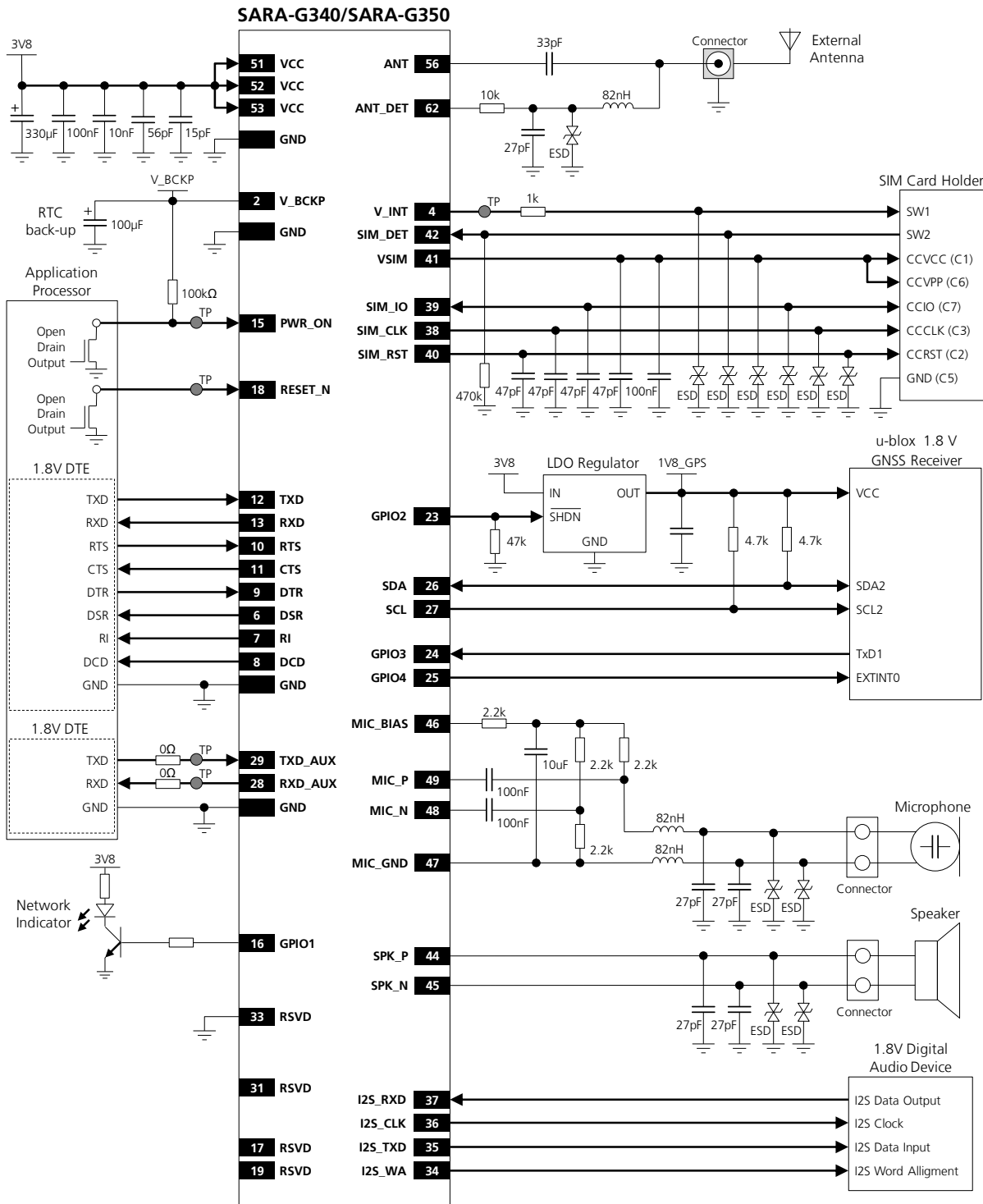


Figure 85: Example of schematic diagram to integrate SARA-G340/G350 module in an application board, using all the interfaces

### 2.15.3 Schematic for SARA-U2 series modules integration

Figure 86 is an example of a schematic diagram where a SARA-U2 module is integrated into an application board, using all the available interfaces and functions of the module.

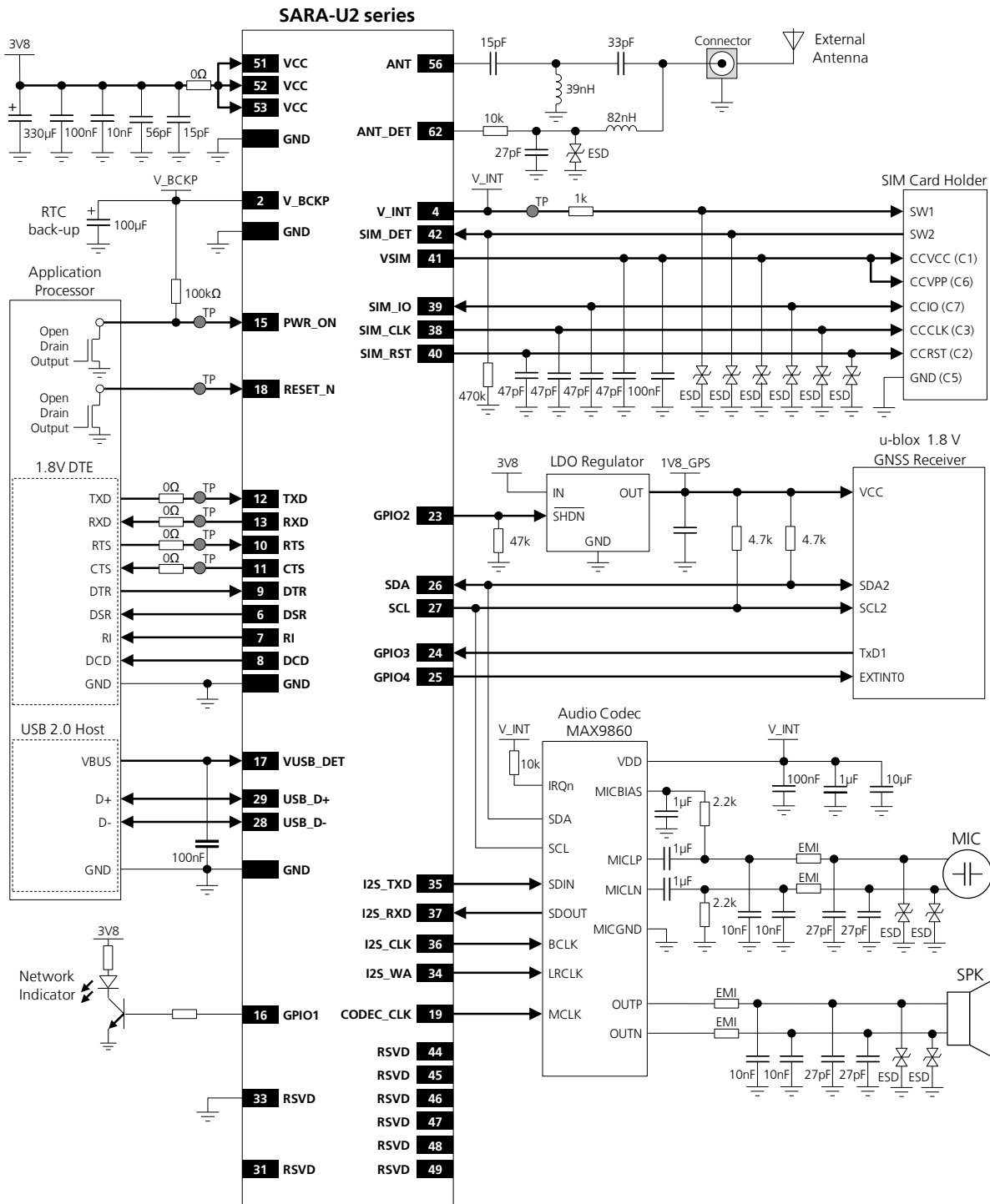


Figure 86: Example of schematic diagram to integrate SARA-U2 module in an application board, using all the interfaces



For a complete schematic example including all SARA-G3 and SARA-U2 series modules see Figure 94.

## 2.16 Design-in checklist

This section provides a design-in checklist.

### 2.16.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin above the minimum operating range limit.
- ☑ DC supply must be capable of providing 1.9 A current pulses, providing a voltage at **VCC** pin above the minimum operating range limit and with a maximum 400 mV voltage drop from the nominal value.
- ☑ **VCC** supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ **VCC** voltage must ramp from 2.5 V to 3.2 V within 4 ms to allow a proper switch-on of the module.
- ☑ Do not leave **PWR\_ON** floating: fix properly the level, e.g. adding a proper pull-up resistor to **V\_BCKP**.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V\_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, since the signal names follow the ITU-T V.24 Recommendation [10].
- ☑ Provide accessible testpoints directly connected to the following pins of the SARA-G3 series modules: **TXD\_AUX** and **RXD\_AUX** pins, **V\_INT** pin, **RESET\_N** and/or **PWR\_ON** pins, for module FW upgrade by the u-blox EasyFlash tool and for diagnostic purpose.
- ☑ Provide accessible testpoints directly connected to the following pins of the SARA-U2 series modules: **VUSB\_DET**, **USB\_D+**, **USB\_D-** and/or **RXD**, **TXD**, **CTS**, **RTS** pins, **V\_INT** pin, **RESET\_N** and/or **PWR\_ON** pins, for module FW upgrade by the u-blox EasyFlash tool and for diagnostic purpose.
- ☑ Add a proper pull-up resistor (e.g. 4.7 k $\Omega$ ) to **V\_INT** or another proper 1.8 V supply on each DDC (I<sup>2</sup>C) interface line, if the interface is used.
- ☑ Capacitance and series resistance must be limited on each high speed line of the USB interface.
- ☑ Capacitance and series resistance must be limited on each line of the DDC (I<sup>2</sup>C) interface.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 k $\Omega$  resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Connect the pin number 33 (**RSVD**) to ground.
- ☑ Insert the suggested passive filtering parts on each used analog audio line.
- ☑ Check the digital audio interface specifications to connect a proper device.
- ☑ Capacitance and series resistance must be limited on **CODEC\_CLK** line and each I<sup>2</sup>S interface line.
- ☑ Provide proper precautions for ESD immunity as required on the application board.
- ☑ Any external signal connected to any generic digital interface pin must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V\_INT** output of the module), to avoid latch-up of circuits and let a proper boot of the module.
- ☑ All unused pins can be left unconnected except the **PWR\_ON** pin (its level must be properly fixed, e.g. adding a 100 k $\Omega$  pull-up to **V\_BCKP**) and the **RSVD** pin number 33 (it must be connected to GND).

## 2.16.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50  $\Omega$  nominal characteristic impedance of the RF transmission line connected to the **ANT** pad (antenna RF input/output interface).
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (primarily analog audio input/output signals, SIM signals, high-speed digital lines).
- ☑ **VCC** line should be wide and short.
- ☑ Route **VCC** supply line away from sensitive analog signals.
- ☑ Ensure proper grounding.
- ☑ Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.
- ☑ Design **USB\_D+** / **USB\_D-** connection as 90  $\Omega$  differential pair, with 30  $\Omega$  common mode impedance.
- ☑ Route analog audio signals away from noisy sources (primarily RF interface, **VCC**, switching supplies).
- ☑ The audio outputs lines on the application board must be wide enough to minimize series resistance.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ Ensure optimal thermal dissipation from the module to the ambient, in particular for SARA-U2 modules.

## 2.16.3 Antenna checklist

- ☑ Antenna termination should provide 50  $\Omega$  characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Follow the additional guidelines for products marked with the FCC logo (United States only) reported in section 4.2.2
- ☑ Follow the guidelines in section 2.4.2 to get proper antenna detection functionality, if required.

## 3 Handling and soldering



No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

### 3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the SARA-G3 series Data Sheet [1] or the SARA-U2 series Data Sheet [2] and the u-blox Package Information Guide [27].

### 3.2 Handling

The SARA-G3 and SARA-U2 series modules are Electro-Static Discharge (ESD) sensitive devices.



**Ensure ESD precautions are implemented during handling of the module.**



Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of SARA-G3 and SARA-U2 series modules (as Human Body Model according to JESD22-A114F) is specified in the SARA-G3 series Data Sheet [1] or the SARA-U2 series Data Sheet [2].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the SARA-G3 and SARA-U2 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron,...).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD safe soldering iron.

For more robust designs, employ additional ESD protection measures on the application device integrating the SARA-G3 and SARA-U2 series modules, as described in section 2.13.3.

## 3.3 Soldering

### 3.3.1 Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste: OM338 SAC405 / Nr.143714 (Cookson Electronics)  
 Alloy specification: 95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)  
 95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)  
 Melting Temperature: 217 °C  
 Stencil Thickness: 150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.11



The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

### 3.3.2 Reflow soldering

**A convection type-soldering oven is strongly recommended** over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Reflow profiles are to be selected according to the following recommendations.



**Failure to observe these recommendations can result in severe damage to the device!**

#### Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s      If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 to 120 s      If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 to 200 °C      If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

#### Heating/ reflow phase

The temperature rises above the liquidus temperature of 217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 217 °C liquidus temperature: 40 to 60 s
- Peak reflow temperature: 245 °C

#### Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

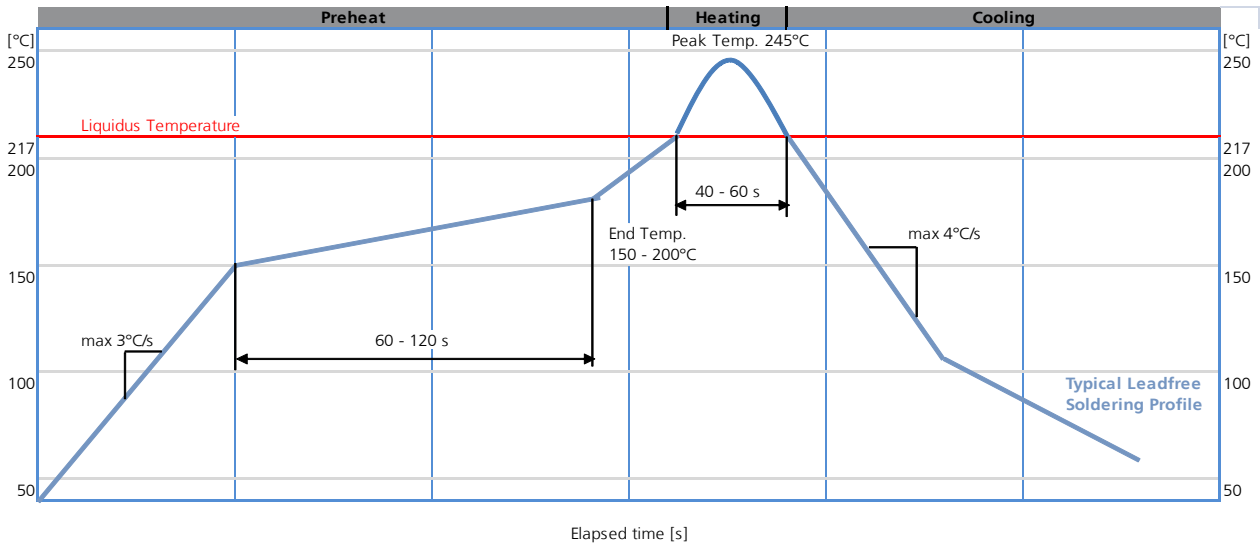
- Temperature fall rate: max 4 °C/s



To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

**Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.**



**Figure 87: Recommended soldering profile**

SARA-G3 and SARA-U2 series modules must not be soldered with a damp heat process.

### 3.3.3 Optical inspection

After soldering the SARA-G3 and SARA-U2 series modules, inspect the modules optically to verify that the module is properly aligned and centered.

### 3.3.4 Cleaning

Cleaning the soldered modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

### 3.3.5 Repeated reflow soldering

Only a single reflow soldering process is encouraged for boards with a SARA-G3 and SARA-U2 series module populated on it.

### 3.3.6 Wave soldering

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with SARA-G3 and SARA-U2 series modules.

### 3.3.7 Hand soldering

Hand soldering is not recommended.

### 3.3.8 Rework

Rework is not recommended.



Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

### 3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products. These materials affect the RF properties of the SARA-G3 and SARA-U2 series modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.



Conformal Coating of the module will void the warranty.

### 3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the SARA-G3 and SARA-U2 series modules before implementing this in the production.



Casting will void the warranty.

### 3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.



u-blox gives no warranty for damages to the SARA-G3 and SARA-U2 series modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

### 3.3.12 Use of ultrasonic processes

SARA-G3 and SARA-U2 series modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the module.



u-blox gives no warranty against damages to the SARA-G3 and SARA-U2 series modules caused by any Ultrasonic Processes.

## 4 Approvals



For the complete list of all the certification schemes approvals of SARA-G3 and SARA-U2 series modules and the corresponding declarations of conformity, see the u-blox web-site (<http://www.u-blox.com>).

### 4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called “certification schemes” that can be divided into three distinct categories:

- Regulatory certification
  - Country specific approval required by local government in most regions and countries, as:
    - CE (Conformité Européenne) marking for European Union
    - FCC (Federal Communications Commission) approval for United States
- Industry certification
  - Telecom industry specific approval verifying the interoperability between devices and networks:
    - GCF (Global Certification Forum), partnership between European device manufacturers and network operators to ensure and verify global interoperability between devices and networks
    - PTCRB (PCS Type Certification Review Board), created by United States network operators to ensure and verify interoperability between devices and North America networks
- Operator certification
  - Operator specific approval required by some mobile network operator, as:
    - AT&T network operator in United States

Even if the SARA-G3 and SARA-U2 series modules are approved under all major certification schemes, the application device that integrates the modules must be approved under all the certification schemes required by the specific application device to be deployed in the market.

The required certification scheme approvals and relative testing specifications differ depending on the country or the region where the device that integrates SARA-G3 and SARA-U2 series modules must be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device must operate.



The certification of the application device that integrates a SARA-G3 and SARA-U2 series module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

SARA-G3 and SARA-U2 series modules are certified according to all capabilities and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to 3GPP TS 51.010-2 [16] and 3GPP TS 34.121-2 [17], is a statement of the device capabilities and options.



The PICS document of the application device integrating a SARA-G3 and SARA-U2 series module must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the application device. For more details regarding the AT commands settings that affect the PICS, see the u-blox AT Commands Manual [3].



Check the specific settings required for mobile network operators approvals as they may differ from the AT commands settings defined in the module as integrated in the application device.

## 4.2 Federal Communications Commission and Industry Canada notice

Federal Communications Commission (FCC) ID:

- For SARA-G310 modules: XPYSARAG350
- For SARA-G350 modules: XPYSARAG350
- For SARA-U260 modules: XPYSARAU260
- For SARA-U280 modules: to be defined

Industry Canada (IC) Certification Numbers:

- For SARA-G310 modules: 8595A-SARAG350
- For SARA-G350 modules: 8595A-SARAG350
- For SARA-U260 modules: 8595A-SARAU260
- For SARA-U280 modules: to be defined


### 4.2.1 Safety warnings review the structure


- Equipment for building-in. The requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed


### 4.2.2 Declaration of conformity

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation


 **Radiofrequency radiation exposure Information: this equipment complies with FCC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.**

 **The gain of the system antenna(s) used for SARA-G310 / SARA-G350 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 8.39 dBi (850 MHz) and 3.11 dBi (1900 MHz) for mobile and fixed or mobile operating configurations.**

 **The gain of the system antenna(s) used for SARA-U260 / SARA-U280 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 3.5 dBi (850 MHz) and 2.0 dBi (1900 MHz) for mobile and fixed or mobile operating configurations.**

### 4.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

 **Manufacturers of mobile or fixed devices incorporating SARA-G310 / SARA-G350 / SARA-U260 / SARA-U280 modules are authorized to use the FCC Grants and Industry Canada Certificates of the SARA-G310 / SARA-G350 / SARA-U260 / SARA-U280 modules for their own final products according to the conditions referenced in the certificates.**

 **The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:**

**For SARA-G310 and SARA-G350 modules: "Contains FCC ID: XPYSARAG350" resp.**

**For SARA-U260 modules: "Contains FCC ID: XPYSARAU260" resp.**

**For SARA-U280 modules: to be defined.**

 **The IC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:**

**For SARA-G310 and SARA-G350 modules: "Contains IC: 8595A-SARAG350" resp.**

**For SARA-U260 modules: "Contains IC: 8595A-SARAU260" resp.**

**For SARA-U280 modules: to be defined.**

 **Canada, Industry Canada (IC) Notices**

**This Class B digital apparatus complies with Canadian CAN ICES-3 (B)/NMB-3(B) and RSS-210.**

**Operation is subject to the following two conditions:**

- **this device may not cause interference**
- **this device must accept any interference, including interference that may cause undesired operation of the device**

#### **Radio Frequency (RF) Exposure Information**

**The radiated output power of the u-blox Cellular Module is below the Industry Canada (IC) radio frequency exposure limits. The u-blox Cellular Module should be used in such a manner such that the potential for human contact during normal operation is minimized.**

**This device has been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions (antennas are greater than 20 cm from a person's body).**

**This device has been certified for use in Canada. Status of the listing in the Industry Canada's REL (Radio Equipment List) can be found at the following web address:**

**<http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng>**

**Additional Canadian information on RF exposure also can be found at the following web address: <http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html>**

 **IMPORTANT: Manufacturers of portable applications incorporating the SARA-G310 / SARA-G350 / SARA-U260 / SARA-U280 modules are required to have their final product certified and apply for their own FCC Grant and Industry Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.**

**Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.**

 **Canada, avis d'Industrie Canada (IC)**

**Cet appareil numérique de classe B est conforme aux normes canadiennes CAN ICES-3 (B)/NMB-3(B) et RSS-210.**

**Son fonctionnement est soumis aux deux conditions suivantes:**

- **cet appareil ne doit pas causer d'interférence**

- **cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement**

#### **Informations concernant l'exposition aux fréquences radio (RF)**

La puissance de sortie émise par l'appareil de sans fil u-blox Cellular Module est inférieure à la limite d'exposition aux fréquences radio d'Industrie Canada (IC). Utilisez l'appareil de sans fil u-blox Cellular Module de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).

Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL - Radio Equipment List) d'Industrie Canada rendez-vous sur:

<http://www.ic.gc.ca/app/sitt/reletel/srch/nwRdSrch.do?lang=fra>

Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur: <http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html>



**IMPORTANT:** les fabricants d'applications portables contenant les modules SARA-G310 / SARA-G350 / SARA-U260 / SARA-U280 doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat Industrie Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.

Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

## **4.3 R&TTED and European conformance CE mark**

SARA-G3 series, SARA-U270 modules have been evaluated against the essential requirements of the 1999/5/EC Directive.

In order to satisfy the essential requirements of the 1999/5/EC Directive, the modules are compliant with the following standards:

- Radio Frequency spectrum use (R&TTE art. 3.2):
  - EN 301 511 V9.0.2
- Electromagnetic Compatibility (R&TTE art. 3.1b):
  - EN 301 489-1 V1.9.2
  - EN 301 489-7 V1.4.1
- Health and Safety (R&TTE art. 3.1a)
  - EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2011 + AC:2011
  - EN 62311:2008

The conformity assessment procedure for SARA-G300-00S/SARA-G310-00S/SARA-G340-00S/SARA-G350-00S/SARA-G350-01S modules, referred to in Article 10 and detailed in Annex IV of Directive 1999/5/EC, has been followed with the involvement of the following Notified Body number: 1909

Thus, the following marking is included in the product:

# **CE 1909**

The conformity assessment procedure for SARA-G350 ATEX modules, referred to in Article 10 and detailed in Annex IV of Directive 1999/5/EC, has been followed with the involvement of the following Notified Body number: 1304

Thus, the following marking is included in the product:

# CE 1304

The conformity assessment procedure for SARA-G340-01S and SARA-U270 modules, referred to in Article 10 and detailed in Annex IV of Directive 1999/5/EC, has been followed with the involvement of the following Notified Body number: 1588

Thus, the following marking is included in the product:

# CE 1588

There is no restriction for the commercialization of the SARA-G3 series and SARA-U270 modules in all the countries of the European Union.

## 4.4 Anatel certification

SARA-G310 and SARA-G350 modules are certified by the Brazilian Agency of Telecommunications (Agência Nacional de Telecomunicações in Portuguese) (Anatel).



Anatel IDs for the SARA-G310 modules:

- EAN barcode: (01)0 789 8941 57509 0
- Homologation number 3419-13-5903

Anatel IDs for the SARA-G350 modules:

- EAN barcode: (01)0 789 8941 57510 6
- Homologation number 3420-13-5903

## 4.5 CCC mark

SARA-G350 modules are certificated for China compulsory product certification (CCC mark).



## 4.6 SARA-G350 ATEX conformance for use in explosive atmospheres

SARA-G350 ATEX modules are certified as components intended for use in potentially explosive atmospheres compliant to the following standards:

- IEC 60079-0: 2011
- IEC 60079-11: 2011
- IEC 60079-26: 2006

The certification number of SARA-G350 ATEX modules according to the ATEX directive 94/9/EC is:

- SIQ 13 ATEX 032 U

The certification number of SARA-G350 ATEX modules according to the IECEx conformity assessment system is:

- IECEx SIQ 13.0004U

According to the standards listed above, the SARA-G350 ATEX modules are certified with the following marking:

- Ex II 1G, Ex ia IIC/IIB

The temperature range for using SARA-G350 ATEX modules is defined in the 'Operating temperature range' section of the SARA-G3 series Data Sheet [1].

The RF radiating profile of SARA-G350 ATEX modules is compliant to all the applicable 3GPP / ETSI standards, with a maximum of 2 W RF pulse power and 1.15 mJ RF pulse energy according to the GSM/GPRS power class stated in Table 3.

The nameplate of SARA-G350 ATEX modules is described in the 'Product labeling' section of the SARA-G3 series Data Sheet [1].

The following maximum input and equivalent parameters must be considered in sub-division IIC:

- $U_i = 3.8 \text{ V}$
- $I_i = 1.6 \text{ A (burst)}$
- $P_i = 2.5 \text{ W}$
- $C_i = 103 \text{ } \mu\text{F}$
- $L_i = 4.1 \text{ } \mu\text{H}$

The following maximum input and equivalent parameters must be considered in sub-divisions IIB, IIA:

- $U_i = 4.2 \text{ V}$
- $I_i = 2.5 \text{ A (burst)}$
- $P_i = 2.5 \text{ W}$
- $C_i = 103 \text{ } \mu\text{F}$
- $L_i = 4.1 \text{ } \mu\text{H}$



## 5 Product testing

### 5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (Serial interface communication, analog audio interface, real time clock, temperature sensor, antenna detection, SIM card communication)
- Digital tests (GPIOs, digital interfaces)
- Measurement and calibration of RF characteristics in all supported bands (Receiver S/N verification, frequency tuning of reference clock, calibration of transmitter and receiver power levels)
- Verification of RF characteristics after calibration (modulation accuracy, power levels and spectrum performance are checked to be within tolerances when calibration parameters are applied)

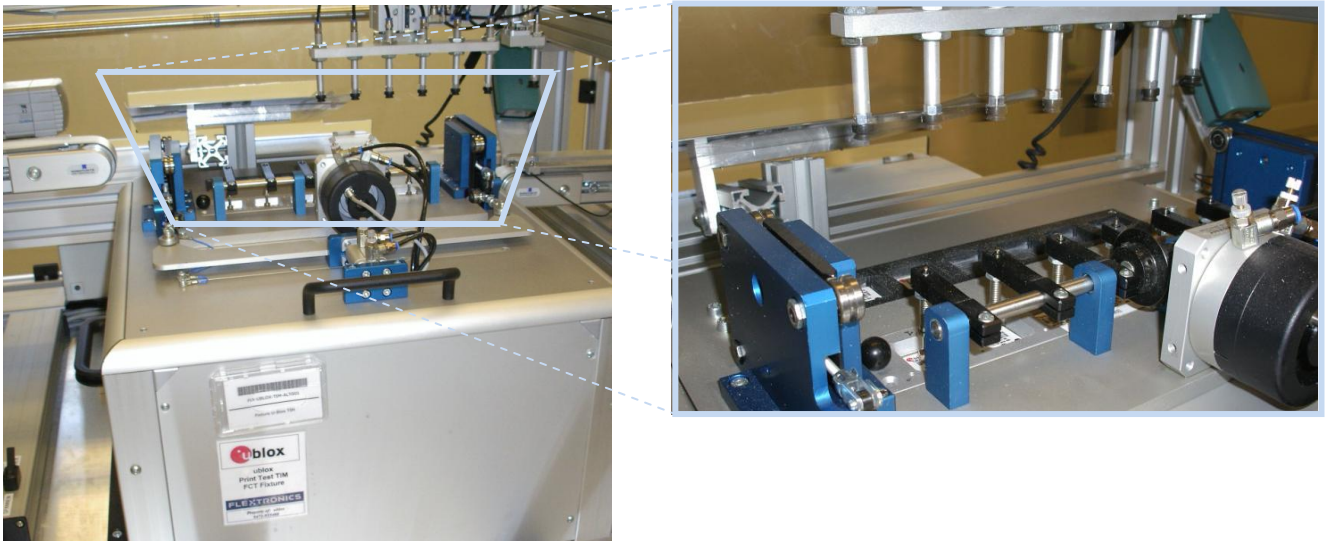


Figure 88: Automatic test equipment for module tests

### 5.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

An OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damaged the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins

- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified status can detect a short circuit if compared with a “Golden Device” result. Module AT commands are used to perform functional tests (communication with host controller, check SIM card interface, check communication between module and GNSS, GPIOs, etc.) and to perform RF performance tests.

### 5.2.1 “Go/No go” tests for integrated devices

A ‘Go/No go’ test is to compare the signal quality with a “Golden Device” in a position with excellent network coverage and after having dialed a call (see u-blox AT Commands Manual [3], AT+CSQ command: <rsqi>, <ber> parameters).



These kinds of test may be useful as a ‘go/no go’ test but not for RF performance measurements.

This test is suitable to check the communication with host controller and SIM card, the audio and power supply functionality and verify if components at antenna interface are well soldered.

### 5.2.2 Functional tests providing RF operation

Overall RF performance test of the device including antenna can be performed with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator using AT+UTEST command over AT interface.

The AT+UTEST command gives a simple interface to set the module to Rx and Tx test modes ignoring 2G/3G signaling protocol. The command can set the module:

- In transmitting mode in a specified channel and power level in all the supported modulation schemes (single slot GMSK, single slot 8PSK, WCDMA) and bands 2G, 3G
- In receiving mode in a specified channel to returns the measured power level in all 2G/3G supported bands



See the u-blox AT Commands Manual [3], for AT+UTEST command syntax description.



See the End user test Application Note [26], for AT+UTEST command user guide, limitations and examples of use.

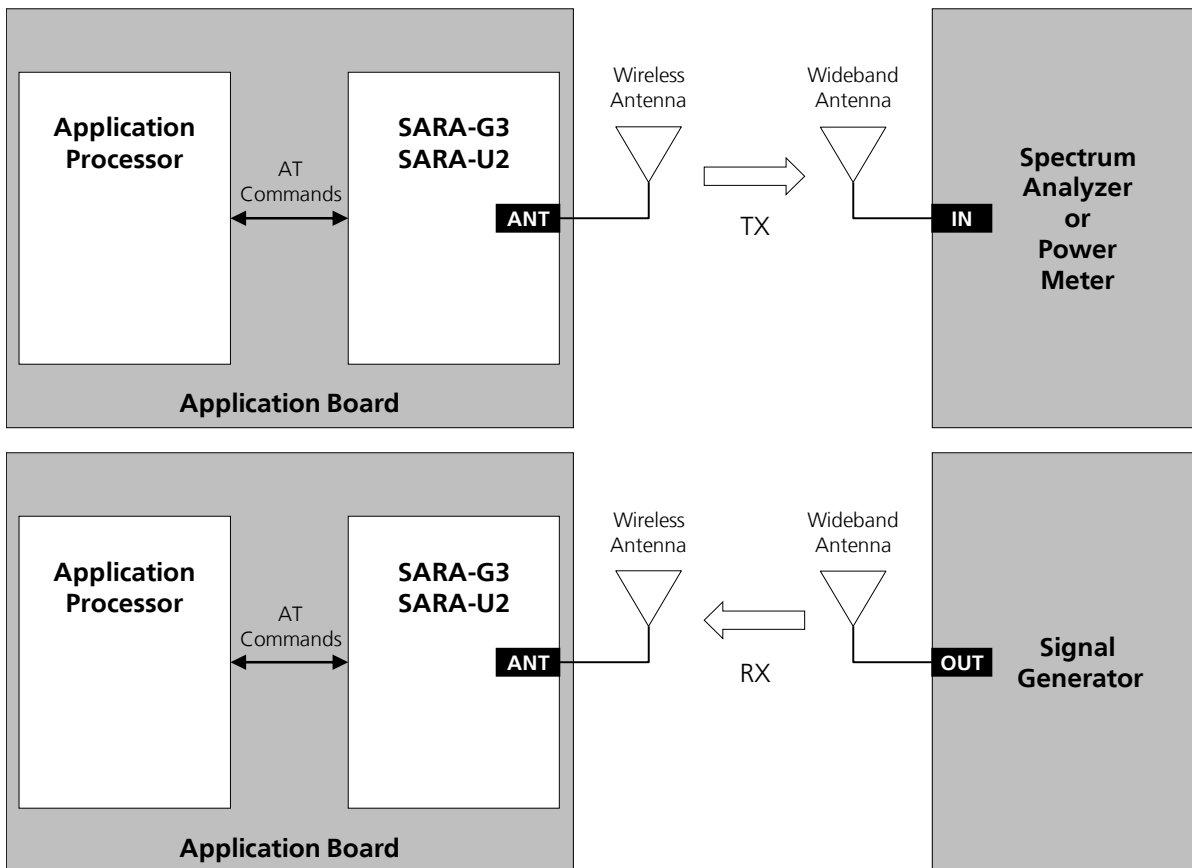





Figure 89: Setup with spectrum analyzer and signal generator for radiated measurement

This feature allows the measurement of the transmitter and receiver power levels to check component assembly related to the module antenna interface and to check other device interfaces from which depends the RF performance.


 **To avoid module damage during transmitter test, a proper antenna according to module specifications or a 50  $\Omega$  termination must be connected to ANT pin.**

 **To avoid module damage during receiver test the maximum power level received at ANT pin must meet module specifications.**

 The AT+UTEST command sets the module to emit RF power ignoring the 2G/3G signalling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purpose in controlled environments by qualified user and must not be used during the normal module operation. Follow instructions suggested in u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Example of production tests for OEM manufacturer:

1. Trigger TX GMSK burst at low Power Control Level (lower than 15) or a RX measure reporting to check:
  - If **ANT** pin is soldered
  - If **ANT** pin is in short circuit
  - If the module was damaged during soldering process or during handling (ESD, mechanical shock...)
  - If antenna matching components on application board are soldered
  - If integrated antenna is correctly connected

 **To avoid module damage during transmitter test when good antenna termination is not guaranteed, use a low Power Control Level (i.e. PCL lower or equal to 15). u-blox assumes no responsibilities for module damaging caused by an inappropriate use of this feature.**

2. Trigger TX GMSK burst at maximum PCL:
  - To check if the power supply is correctly assembled and is able to deliver the required current
3. Trigger TX GMSK burst, TX 8PSK burst and TX WCDMA signal:
  - To measure current consumption
  - To check if module components were damaged during soldering process or during handling (ESD, mechanical shock...)
4. Trigger RX measurement:
  - To test receiver signal level. Assuming that there are no losses between **ANT** pin and input power source, be aware that the power level estimated by the module can vary approximately within 3GPP tolerances for the average value
  - To check if module was damaged during soldering process or during handling (ESD, mechanical shock...)
5. Trigger TX GMSK, TX 8PSK burst and TX WCDMA signal and RX measurement to check:
  - Overall RF performance of the device including antenna measuring TX and RX power levels

# Appendix

## A Migration between LISA and SARA-G3 modules

### A.1 Overview

Migrating between LISA-U1, LISA-U2, LISA-C2 series and SARA-G3 series module designs is a straight-forward procedure that allows customers to take maximum advantage of their hardware and software investments.

The SARA cellular modules (26.0 x 16.0 mm LGA) have a different form factor than the LISA cellular modules (33.2 x 22.4 mm LCC), but the footprint of SARA and LISA modules has been developed to provide pin-to-pin compatibility on the lateral edge of the antenna pin so that each SARA / LISA pin can share the same pad on the application board, due to the same pitch and nearly the same functions provided, as described in Figure 90.

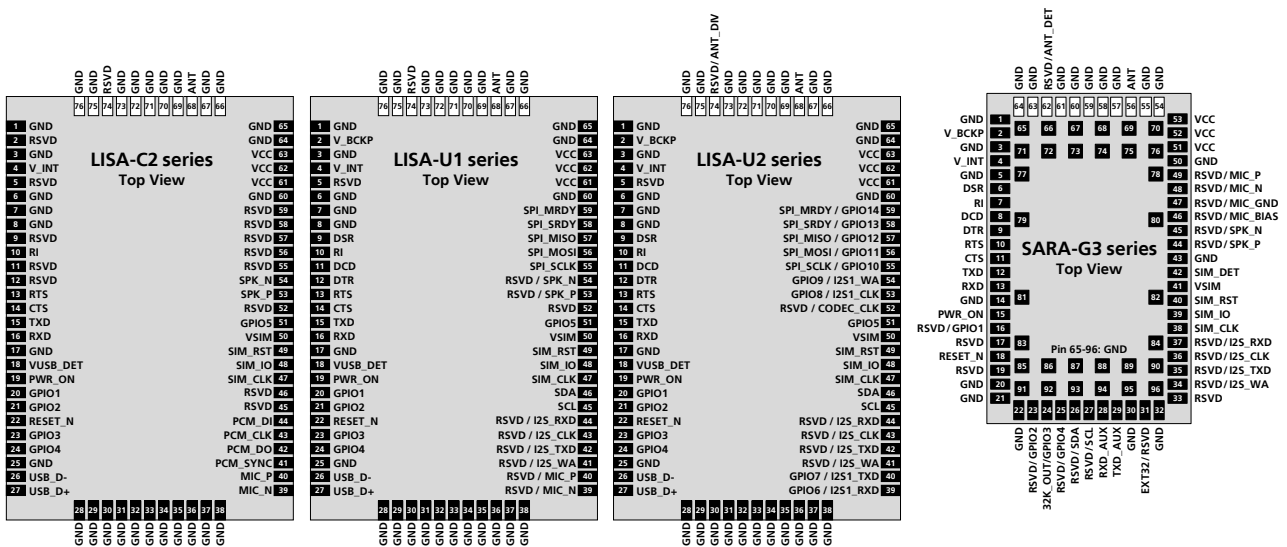


Figure 90: LISA series vs. SARA-G3 series modules pin assignment: highlighted pads that can be shared on the application board

This is the basis of the Nested Design concept: any SARA-G3, LISA-U1, LISA-U2, or LISA-C2 module can be mounted on the same nested board as shown in Figure 91, enabling straightforward development of products supporting either GSM/GPRS, W-CDMA or CDMA cellular technology with the same application board.

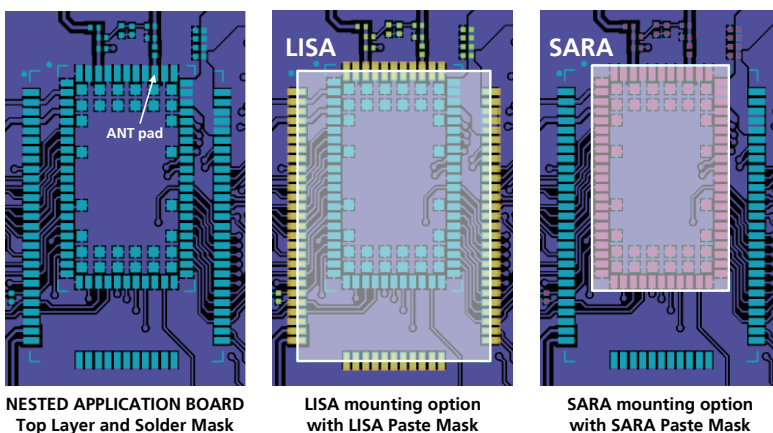


Figure 91: Nested Design concept description: LISA and SARA modules alternatively mounted on the same application board

The voltage level of all the digital interfaces of SARA and LISA modules is 1.8 V: this allows the direct connection from a 1.8 V external device (e.g. application processor) to all the modules.

The following sections explain in detail all the points to consider during the migration between LISA and SARA designs, implementing or not a nested design

For further details regarding SARA-G3 and LISA characteristics, usage, or settings, see the related module datasheet [1], [4], [5], [6], System Integration Manual [7], [8], and AT commands manual [3], [9].

## A.2 Checklist for migration

### Have you chosen the optimal SARA-G3 module?

- For quad-band GSM/GPRS, full feature set, select the SARA-G350 module.
- For dual-band GSM/GPRS, full feature set, select the SARA-G340 module.
- For quad-band GSM/GPRS, reduced feature set, select the SARA-G310 module.
- For dual-band GSM/GPRS, reduced feature set, select the SARA-G300 module.

### Check SARA-G3 modules hardware requirements

- Check power capabilities of the external supply circuit: SARA-G3 modules require large current pulses in connected-mode as well as LISA-U series modules when a 2G call is enabled. LISA-C2 series modules do not require large current pulses due to the CDMA channel access technology.
- Check supported bands for proper antenna circuit development: SARA-G3 modules frequency ranges are within LISA-U modules ranges, but LISA-C2 modules range is quite different.
- Check antenna detection requirements: SARA-G340 and SARA-G350 modules provide the antenna detection function implementing an external application circuit between **ANT\_DET** and **ANT** pins.
- Check the module power-on requirements: Table 59 and relative section summarize differences between SARA-G3 and LISA modules.
- Check the module requirements to enter low power idle-mode: SARA-G300 and SARA-G310 modules require a 32 kHz signal at **EXT32K** input, which for example can be provided by the **32K\_OUT** output.
- Check serial interfaces requirements: SARA-G3 modules provide UART interface for AT command, data communication, multiplexer functionality, FW upgrade over AT and provide auxiliary UART interface for FW upgrade using the u-blox EasyFlash tool and for diagnostic purpose.
- Check analog audio requirements: SARA-G340 and SARA-G350 modules do not provide DC blocking capacitors at the **MIC\_P** / **MIC\_N** input pins and provide supply output and local ground for an external microphone at the **MIC\_BIAS** / **MIC\_GND** pins.
- Check digital audio requirements: SARA-G340 and SARA-G350 modules provide a 4-wire 1.8 V interface supporting PCM and Normal I2S modes, master role and fixed sample rate.
- Check internal active pull-up / down values at digital interface input pins and the current capability of digital interface output pins, since they are slightly different between SARA-G3 and LISA modules.

### Check SARA-G3 modules software requirements

- Not all of the functionalities available with LISA modules are supported by all the SARA-G3 modules versions. SARA-G300 and SARA-G310 modules do not support:
  - o Audio interfaces, DDC (I<sup>2</sup>C) interface, Antenna detection interface, GPIOs
  - o Low power idle-mode, if a 32 kHz signal at **EXT32K** input pin is not provided
  - o TCP/IP, UDP/IP, FTP, HTTP
  - o GNSS via Modem, AssistNow clients, Hybrid positioning and CellLocate<sup>®</sup> functionalities
  - o Jamming detection

## A.3 Software migration

Software migration between SARA-G3 and LISA cellular modules is a straightforward procedure. Nevertheless there are some differences to be considered with firmware version. Each cellular module supports AT commands according to 3GPP standards: TS 27.007 [11], TS 27.005 [12], TS 27.010 [13] and the u-blox AT command extension. Backward compatibility has been maintained as far as possible.



For the complete list of supported AT commands and their syntax see the relevant AT commands manual of the module [3], [9].

## A.4 Hardware migration

SARA modules have been designed with backward compatibility to LISA series modules in mind but some minor differences were unavoidable. These minor differences are however not relevant for the majority of the designs.

The following subsections describe the hardware differences between the interfaces of SARA-G3 modules and LISA modules while Table 60 summarizes the detailed differences between the pins.

### A.4.1 Supply interfaces

#### Module supply input (VCC)

The same compatible external circuit can be implemented for SARA and LISA modules even if there are minor differences in the **VCC** input voltage ranges and some differences in the current consumption figures.

The voltage provided must be within the normal operating range limits to allow module switch-on and must be above the minimum limit of the extended operating range to avoid module switch-off. For the detailed **VCC** input voltage ranges values see Table 60 or to the relative datasheet of the module [1], [4], [5], [6].

The SARA-G3 maximum average current consumption is lower than the LISA one due to the lower data rate or the different channel access technology. SARA-G3 modules require large current pulses in connected-mode as well as LISA-U series when a 2G call is enabled. LISA-C2 series do not require large current pulses due to the CDMA channel access technology. For the detailed current consumption values see the related module datasheet [1], [4], [5], [6].

Detailed supply circuit design-in guidelines are reported in section 2.2.1 and in the corresponding System Integration Manual of the module [7], [8].

#### RTC supply input/output (V\_BCKP)

The same compatible external circuit can be implemented for SARA and LISA-U series even if there are minor differences in the **V\_BCKP** typical output voltage and input voltage range as reported in Table 60 or in the relative datasheet of the module [1], [4], [5], [6]. LISA-C2 series do not provide **V\_BCKP** RTC supply input/output as well as the whole RTC functionality.

#### Interfaces supply output (V\_INT)

The same compatible external circuit can be implemented for SARA and LISA series: there are no differences in the **V\_INT** output characteristics.



## A.4.2 System functions interfaces

### Module power-on

SARA-G3 and LISA series power-on sequence is initiated in one of the ways summarized in Table 59. For more details, see section 1.6.1 or to the relative System Integration Manual of the module [7], [8].

SARA-G3 series	LISA-C2 series	LISA-U1 series	LISA-U2 series
Rising edge on the <b>VCC</b> pins to a valid voltage as module supply	Rising edge on the <b>VCC</b> pins to a valid voltage as module supply with <b>PWR_ON</b> pin permanently low when <b>VCC</b> is applied	Rising edge on the <b>VCC</b> pins to a valid voltage as module supply	Rising edge on the <b>VCC</b> pins to a valid voltage as module supply
Low level on the <b>PWR_ON</b> pin for appropriate time period	Low pulse on the <b>PWR_ON</b> pin for appropriate time period	Low pulse on the <b>PWR_ON</b> pin for appropriate time period	Low pulse on the <b>PWR_ON</b> pin for appropriate time period
Pre-programmed RTC alarm (not supported by SARA-G300/G310)		Pre-programmed RTC alarm	Pre-programmed RTC alarm
		<b>RESET_N</b> input pin released from the low level	<b>RESET_N</b> input pin released from the low level

**Table 59: Summary of power on events among modules**

The same compatible external power-on circuit can be implemented for SARA and LISA modules even if there are minor differences in the **PWR\_ON** input voltage levels ranges and in the low level time or low pulse time to switch-on the module, as reported in Table 60 or in the relative datasheet of the module [1], [4], [5], [6]. **PWR\_ON** falling edge (i.e. low pulse) is required for LISA series, but it is not required for SARA. External pull-up is not needed for LISA-C2 series since internal pull-up is provided.

### Module power-off

SARA and LISA modules can all be properly switched off by means of the AT+CPWROFF command.

Additionally, all LISA-U2 modules, except LISA-U200-00S, can be properly switched off by low pulse on the **PWR\_ON** pin, as reported in Table 60 or in the relative datasheet of the module [6].

### Module reset

SARA and LISA modules reset can be performed in one of the following ways:

- Forcing a low level on the **RESET\_N** pin, causing an “external” or “hardware” reset
- By means of the AT+CFUN command, causing an “internal” or “software” reset

The same compatible external reset circuit can be implemented for SARA and LISA modules even if there are minor differences in the **RESET\_N** input voltage levels ranges and in the low level time, as reported in Table 60 or in the relative datasheet of the module [1], [4], [5], [6].

Additional precautions are suggested for the **RESET\_N** line of LISA-U series modules, depending on the application board handling, to satisfy ESD immunity test requirements as described in the LISA-U Series System Integration Manual [8].

### External 32 kHz input and internal 32 kHz output

The **EXT32K** input and the **32K\_OUT** output are available only on the SARA-G300 and SARA-G310 modules to provide the 32 kHz reference clock for the Real Time Clock (RTC) timing, used by the module processor to reach the low power idle-mode and provide the RTC functions.

SARA-G340, SARA-G350 and LISA-U modules are equipped with internal 32 kHz oscillator to provide the same functions.

LISA-C2 series do not provide RTC and the relative functions.



### A.4.3 Antenna interface

#### RF interface for Tx/Rx antenna

The same compatible external circuit can be implemented for SARA and LISA series **ANT** pin even if there are some differences in the operating bands frequency ranges, as summarized in Figure 92.

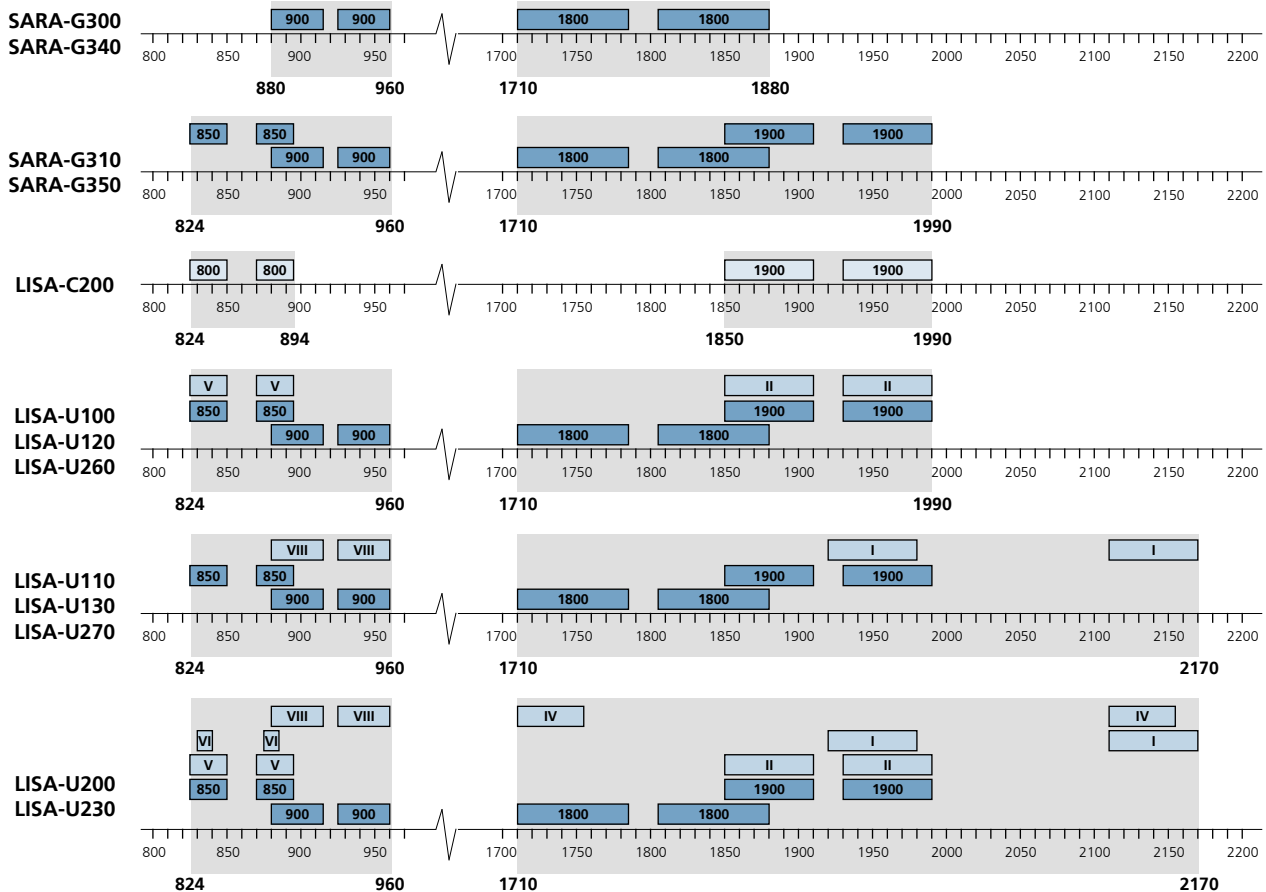


Figure 92: Summary of operating bands frequency ranges among modules

An external circuit can be implemented on the application device integrating SARA-U2 and LISA-U2 modules to satisfy ESD immunity test requirements at the antenna port, as described in sections 2.13 and 2.4, and in the LISA-U Series System Integration Manual [8]. The same external circuit is not required for SARA-G3, LISA-U1 and LISA-C2 modules.

#### RF interface for Rx diversity antenna

Only the LISA-U230 modules provide the RF input for Rx diversity antenna (**ANT\_DIV**).

SARA-G3, LISA-C2, LISA-U1 and the other LISA-U2 series modules do not support Rx diversity.

#### Antenna detection interface

An external application circuit can be implemented on the application device integrating SARA-G340 / SARA-G350 modules to provide antenna detection functionality, with a proper connection between the **ANT\_DET** pin and the **ANT** pin, as described in section 2.4.2.

LISA-U modules are equipped with internal circuit for antenna detection support.

SARA-G300, SARA-G310 and LISA-C2 series modules do not support antenna detection.

## A.4.4 SIM interface

### SIM interface

The same compatible external circuit can be implemented for SARA and LISA modules: 1.8 V and 3.0 V SIM are supported. LISA-C2 modules do not need an external SIM for Sprint and Verizon mobile operators. LISA-C2 series SIM interface is hardware ready but the support of external SIM card / IC will be provided by the upcoming firmware releases.

### SIM detection interface

The same compatible external circuit can be implemented for SARA and LISA modules: SIM detection function is provided by the **SIM\_DET** pin on SARA-G3 modules and by the **GPIO5** pin on LISA-U modules. SIM card hot insertion/removal is additionally supported by all LISA-U2 series except LISA-U200-00S.

LISA-C2 modules do not support SIM detection.

## A.4.5 Serial interfaces

### UART interface

The same compatible external circuit can be implemented for SARA and LISA modules: a 1.8 V unbalanced asynchronous serial port with RS-232 functionality is provided on SARA-G3 modules (for AT command, data communication, MUX functionality, FW upgrade over AT), LISA-C2 modules (for AT command, data communication, MUX functionality), LISA-U modules (for AT command, data communication, MUX functionality, FW upgrade over AT or using the u-blox EasyFlash tool).

LISA-C2 modules do not support **DSR**, **DCD** and **DTR** functions.

Table 60 and the module's datasheet [1], [4], [5], [6] report minor differences in the internal pull-ups and drivers strengths.

These are the default settings of the UART interfaces:

- SARA-G3 modules: automatic baud rate and frame format detection
- LISA-U2 except LISA-U200-00S modules: one-shot automatic baud rate and frame format detection
- LISA-C2, LISA-U1 and LISA-U200-00S modules: 115200 b/s baud rate and 8N1 frame format

For further details regarding UART interface settings see the module's datasheet [1], [4], [5], [6] and to the related AT commands manual of the module [3], [9].

### UART AUX interface

Only the SARA-G3 modules provide an auxiliary UART interface for FW upgrade using the u-blox EasyFlash tool and for diagnostic purpose.

LISA modules do not provide an auxiliary UART interface.

### USB interface

SARA-G3 modules do not provide a USB interface such as is available on LISA-U modules (High-Speed USB 2.0 for AT command, data communication, FW upgrade over AT or using the u-blox EasyFlash tool, and for Trace log capture) and on LISA-C2 modules (Full-Speed USB 2.0 for AT command, Data communication, FW upgrade).

### SPI interface

SARA-G3 and LISA-C2 modules do not provide an SPI interface such as is available on LISA-U modules (5-wire IPC interface for AT command, data communication, MUX functionality, FW upgrade over AT).

### DDC (I<sup>2</sup>C) interface

The same compatible external circuit can be implemented for SARA-G340 / SARA-G350 and LISA series: A 1.8 V DDC (I<sup>2</sup>C bus compatible) interface is provided to communicate with u-blox GNSS receivers.

SARA-G300, SARA-G310 and LISA-U200-00S modules do not support the DDC (I<sup>2</sup>C) interface.

LISA-C2 modules will support the DDC (I<sup>2</sup>C) interface in the upcoming firmware releases.

All LISA-U2 modules, except LISA-U200-00S, additionally support the communication with I<sup>2</sup>C slaves by means of dedicated AT commands, other than u-blox positioning receivers over the same DDC (I<sup>2</sup>C) interface.

## A.4.6 Audio interfaces

### Analog audio interfaces

Differential analog audio input is provided on the **MIC\_P / MIC\_N** pins of SARA-G340 / SARA-G350 modules (without internal DC blocking capacitor) and LISA-C2 series, LISA-U120, and LISA-U130 modules (with an internal DC blocking capacitor).

Supply output and local ground for an external microphone is provided on the **MIC\_BIAS / MIC\_GND** pins of SARA-G340 / SARA-G350 modules only: the supply for an external microphone has to be provided by an external LDO linear regulator with the other modules.

Differential analog audio output is provided on the **SPK\_P / SPK\_N** pins of SARA-G340, SARA-G350, LISA-U120, LISA-U130 modules (16 ohm load capable) and LISA-C2 series modules (32 ohm load capable).

SARA-G300/SARA-G310, LISA-U100/U110, LISA-U200-00S modules do not provide analog audio interfaces.

LISA-U2 series modules do not provide analog audio interfaces, but analog audio can be provided with external audio codec connected to a digital audio interface of all LISA-U2 series modules except LISA-U200-00S (e.g. the 4-wire I<sup>2</sup>S digital audio interface provided instead of the 4 analog audio pins). The modules provide control of the external codec by means of the I<sup>2</sup>C interface and clock reference by means of the **CODEC\_CLK** pin.

For further details regarding analog audio interfaces characteristics, usage, and settings, see the related module datasheet [1], [4], [5], [6], System Integration Manual 1.10.1, 2.7.1, [7], [8], and AT commands manual [3], [9].

### Digital audio interfaces

The digital audio interface is provided on the **I2S\_TXD, I2S\_RXD, I2S\_CLK, I2S\_WA** pins of SARA-G340 / SARA-G350 modules (1.8 V, PCM & Normal I2S modes, master, fixed sample rate) and LISA-U120/U130 and all LISA-U2 series modules except LISA-U200-00S (1.8 V, PCM & Normal I2S modes, master & slave, configurable sample rate). It is provided on the **PCM\_DO, PCM\_DI, PCM\_CLK, PCM\_SYNC** pins of LISA-C2 series modules (1.8 V, PCM). The same compatible external circuit can be implemented according to external digital audio device capabilities.

An additional digital audio interface is provided on **I2S1\_TXD, I2S1\_RXD, I2S1\_CLK, I2S1\_WA** pins of all LISA-U2 series except LISA-U200-00S (1.8 V, PCM & Normal I2S modes, master & slave, configurable sample rate).

SARA-G300/SARA-G310, LISA-U100/LISA-U110, LISA-U200-00S modules do not provide digital audio interfaces.

For further details regarding digital audio interfaces characteristics, usage, and settings, see the related module datasheet [1], [4], [5], [6], System Integration Manual 1.10.2, 2.7.2, [7], [8], and AT commands manual [3], [9].

## A.4.7 GPIO pins

The same compatible external circuit can be implemented for SARA-G340 / SARA-G350 and LISA series: four 1.8 V GPIOs are provided by SARA-G340 / SARA-G350 modules, providing the same functionalities as LISA series modules except Module Status and Operating Mode Indications. The **SIM\_DET** pin provides the SIM detection function on SARA modules rather than the **GPIO5** pin as on LISA-U series modules.

SARA-G300 and SARA-G310 modules do not provide GPIOs.

## A.4.8 Reserved pins

SARA modules **RSVD** pin 33 must be connected to ground, as does the **RSVD** pin 5 on LISA modules.

## A.4.9 Pin-out comparison between LISA and SARA-G3

Table 60 summarizes the pin electrical differences between LISA and SARA-G3 cellular modules.

Pin Name	N°	SARA-G3 series	N°	LISA-C2 series	LISA-U1 series	LISA-U2 series
<b>Power</b>						
VCC	51-53	Normal op. range: 3.35 V – 4.5 V Extended op. range: 3.00 V – 4.5 V High pulse current due to GSM TDMA	61-63	Normal op. range: 3.3 V – 4.4 V Extended op. range: Not applicable No high pulse current due to CDMA	Normal op. range: 3.4 V – 4.2 V Extended op. range: 3.1 V – 4.2 V High pulse current due to GSM TDMA	Normal op. range: 3.3 V – 4.4 V Extended op. range: 3.1 V – 4.5 V High pulse current due to GSM TDMA
V_BCKP	2	Output characteristics: 2.3 V typ, 2 mA max Input op. range: 1.0 V – 2.4 V	2	Not Available	Output characteristics: 2.3 V typ, 3 mA max Input op. range: 1.0 V – 2.5 V	Output characteristics: 1.8 V typ, 3 mA max Input op. range: 1.0 V – 1.9 V
V_INT	4	Output characteristics: 1.8 V typ, 50 mA max	4	Output characteristics: 1.8 V typ, 50 mA max	Output characteristics: 1.8 V typ, 50 mA max	Output characteristics: 1.8 V typ, 50 mA max
<b>Antenna</b>						
ANT	56	RF input/output for Tx/Rx antenna	68	RF input/output for Tx/Rx antenna	RF input/output for Tx/Rx antenna	RF input/output for main Tx/Rx antenna
ANT_DIV		Not Available	74	Not Available	Not Available	LISA-U230 only: RF input for Rx diversity antenna
ANT_DET	62	SARA-G340/SARA-G350: Input for antenna detection circuit		Not Available	Internal antenna detection circuit	Internal antenna detection circuit
<b>System</b>						
PWR_ON	15	No internal pull-up L-level: -0.10 V – 0.65 V H-level: 2.00 V – 4.50 V ON L-level time: 5 ms min OFF L-level pulse time: Not Available	19	180 k $\Omega$ internal pull-up L-level: -0.30 V – 0.30 V H-level: 2.00 V – 4.70 V ON L-level pulse time: 150 ms min OFF L-level pulse time: Not Available	No internal pull-up L-level: -0.30 V – 0.65 V H-level: 2.00 V – 4.50 V ON L-level pulse time: 5 ms min OFF L-level pulse time: Not Available	No internal pull-up L-level: -0.30 V – 0.65 V H-level: 1.50 V – 4.40 V ON L-level pulse time: 50 $\mu$ s min / 80 $\mu$ s max OFF L-level pulse time: 1 s min
RESET_N	18	Internal diode & pull-up L-level: -0.30 V – 0.30 V H-level: 2.00 V – 4.70 V Reset L-level pulse time: SARA-G340/SARA-G350: 50 ms min SARA-G300/SARA-G310: 3 s min	22	550 $\Omega$ internal pull-up L-level: -0.30 V – 0.63 V H-level: 1.32 V – 2.10 V Reset L-level pulse time: 300 ms min	10 k $\Omega$ internal pull-up L-level: -0.30 V – 0.65 V H-level: 1.69 V – 2.48 V Reset L-level pulse time: 50 ms min	10 k $\Omega$ internal pull-up L-level: -0.30 V – 0.51 V H-level: 1.32 V – 2.01 V Reset L-level pulse time: 50 ms min
EXT32K	31	SARA-G300/SARA-G310: 32 kHz input for RTC & low power idle mode SARA-G340/SARA-G350: Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal reference for low power idle mode	Not Available: Internal 32 kHz for RTC & low power idle mode	Not Available: Internal 32 kHz for RTC & low power idle mode
32K_OUT	24	SARA-G300/SARA-G310: 32 kHz output, only to feed the EXT32K input SARA-G340/SARA-G350: Not Available		Not Available	Not Available	Not Available

Pin Name	N°	SARA-G3 series	N°	LISA-C2 series	LISA-U1 series	LISA-U2 series
<b>SIM</b>						
SIM_CLK	38	1.8V / 3V SIM clock	47	1.8V / 3V SIM clock (upcoming FW releases)	1.8V / 3V SIM clock	1.8V / 3V SIM clock
SIM_IO	39	1.8V / 3V SIM data Internal 4.7k pull-up	48	1.8V / 3V SIM data (upcoming FW releases) Internal 10k pull-up	1.8V / 3V SIM data Internal 4.7k pull-up	1.8V / 3V SIM data Internal 4.7k pull-up
SIM_RST	40	1.8V / 3V SIM reset	49	1.8V / 3V SIM reset (upcoming FW releases)	1.8V / 3V SIM reset	1.8V / 3V SIM reset
VSIM	41	1.8V / 3V SIM supply	50	1.8V / 3V SIM supply (upcoming FW releases)	1.8V / 3V SIM supply	1.8V / 3V SIM supply
SIM_DET	42	1.8 V, SIM detect input Inner pull-down: 103 µA		Not Available	Provided by GPIO5: 1.8 V, SIM detect input Inner pull-down: 55 µA	Provided by GPIO5: 1.8 V, SIM detect input Inner pull-down: 200 µA
<b>UART</b>						
DSR	6	1.8 V, DSR output Driver strength: 6 mA	9	Not Available	1.8 V, DSR output Driver strength: 4 mA	1.8 V, DSR output Driver strength: 1 mA
RI	7	1.8 V, RI output Driver strength: 6 mA	10	1.8 V, RI output Driver strength: 6 mA	1.8 V, RI output Driver strength: 4 mA	1.8 V, RI output Driver strength: 2 mA
DCD	8	1.8 V, DCD output Driver strength: 6 mA	11	Not Available	1.8 V, DCD output Driver strength: 4 mA	1.8 V, DCD output Driver strength: 2 mA
DTR	9	1.8 V, DTR input Internal pull-up: -55 µA	12	Not Available	1.8 V, DTR input Internal pull-up: -110 µA	1.8 V, DTR input Internal pull-up: -125 µA
RTS	10	1.8 V, Flow ctrl input Internal pull-up: -31 µA	13	1.8 V, Flow ctrl input Internal pull-up: -30 µA	1.8 V, Flow ctrl input Internal pull-up: -60 µA	1.8 V, Flow ctrl input Internal pull-up: -240 µA
CTS	11	1.8 V, Flow ctrl output Driver strength: 6 mA	14	1.8 V, Flow ctrl output Driver strength: 4 mA	1.8 V, Flow ctrl output Driver strength: 4 mA	1.8 V, Flow ctrl output Driver strength: 6 mA
TXD	12	1.8 V, Data input Internal pull-up: -102 µA	15	1.8 V, Data input Internal pull-up: -30 µA	1.8 V, Data input Internal pull-up: -60 µA	1.8 V, Data input Internal pull-up: -240 µA
RXD	13	1.8 V, Data output Driver strength: 5 mA	16	1.8 V, Data output Driver strength: 4 mA	1.8 V, Data output Driver strength: 4 mA	1.8 V, Data output Driver strength: 6 mA
<b>UART AUX</b>						
TXD_AUX	29	1.8 V, Data input Internal pull-up: -102 µA		Not Available	Not Available	Not Available
RXD_AUX	28	1.8 V, Data output Driver strength: 5 mA		Not Available	Not Available	Not Available
<b>USB</b>						
VUSB_DET		Not Available	18	5 V, Supply detection	5 V, Supply detection	5 V, Supply detection
USB_D-		Not Available	26	Full-Speed USB 2.0	High-Speed USB 2.0	High-Speed USB 2.0
USB_D+		Not Available	27	Full-Speed USB 2.0	High-Speed USB 2.0	High-Speed USB 2.0
<b>SPI</b>						
SPI_SCLK		Not Available	55	Not Available	1.8 V, Clock input Inner pull-down: 100 µA	1.8 V, Clock input Inner pull-down: 200 µA
SPI_MOSI		Not Available	56	Not Available	1.8 V, Data input Internal pull-up: -220 µA	1.8 V, Data input Internal pull-up: -240 µA
SPI_MISO		Not Available	57	Not Available	1.8 V, Data output Driver strength: 2.5 mA	1.8 V, Data output Driver strength: 6 mA
SPI_SRDY		Not Available	58	Not Available	1.8 V, Flow ctrl output Driver strength: 4 mA	1.8 V, Flow ctrl output Driver strength: 6 mA
SPI_MRDY		Not Available	59	Not Available	1.8 V, Flow ctrl input Inner pull-down: 55 µA	1.8 V, Flow ctrl input Inner pull-down: 200 µA
<b>DDC (I<sup>2</sup>C)</b>						
SCL	27	SARA-G340/SARA-G350: 1.8 V, open drain Driver strength: 3 mA	45	1.8 V, open drain (upcoming FW releases)	1.8 V, open drain Driver strength: 1 mA	1.8 V, open drain Driver strength: 1 mA LISA-U200-00S: N.A.
SDA	26	SARA-G340/SARA-G350: 1.8 V, open drain Driver strength: 3 mA	46	1.8 V, open drain (upcoming FW releases)	1.8 V, open drain Driver strength: 1 mA	1.8 V, open drain Driver strength: 1 mA LISA-U200-00S: N.A.

Pin Name	N°	SARA-G3 series	N°	LISA-C2 series	LISA-U1 series	LISA-U2 series
<b>Audio</b>						
Analog						
MIC_BIAS	46	SARA-G340/SARA-G350: 2.2 V supply output for external microphone		Not Available	Not Available	Not Available
MIC_GND	47	SARA-G340/SARA-G350: Local ground sense for external microphone		Not Available	Not Available	Not Available
MIC_P	49	SARA-G340/SARA-G350: Differential input (+) No internal capacitor for DC blocking	40	Differential input (+) 100 nF internal capacitor for DC blocking	LISA-U120/U130 only: Differential input (+) 100 nF internal capacitor for DC blocking	Not Available
MIC_N	48	SARA-G340/SARA-G350: Differential input (-) No internal capacitor for DC blocking	39	Differential input (-) 100 nF internal capacitor for DC blocking	LISA-U120/U130 only: Differential input (-) 100 nF internal capacitor for DC blocking	Not Available
SPK_P	44	SARA-G340/SARA-G350: Differential output (+) 16 ohm load capable	53	Differential output (+) 32 ohm load capable	LISA-U120/U130 only: Differential output (+) 16 ohm load capable	Not Available
SPK_N	45	SARA-G340/SARA-G350: Differential output (-) 16 ohm load capable	54	Differential output (-) 32 ohm load capable	LISA-U120/U130 only: Differential output (-) 16 ohm load capable	Not Available
Digital						
I2S_TXD	35	SARA-G340/SARA-G350: 1.8 V, Data Out PCM / Normal I2S mode Driver strength: 5 mA	42	PCM_DO: 1.8 V, PCM Data Out	LISA-U120/U130 only: 1.8 V, Data Out PCM / Normal I2S mode Driver strength: 2.5 mA	1.8 V, Data Out PCM / Normal I2S mode Driver strength: 2 mA LISA-U200-00S: N.A.
I2S_RXD	37	SARA-G340/SARA-G350: 1.8 V, Data In PCM / Normal I2S mode Inner pull-down: 103 µA	44	PCM_DI: 1.8 V, PCM Data In	LISA-U120/U130 only: 1.8 V, Data In PCM / Normal I2S mode Inner pull-down: 100 µA	1.8 V, Data In PCM / Normal I2S mode Inner pull-down: 200 µA LISA-U200-00S: N.A.
I2S_WA	34	SARA-G340/SARA-G350: 1.8 V, Word align. Out Fixed frequency Driver strength: 6 mA	41	PCM_SYNC: 1.8 V, PCM Sync Out	LISA-U120/U130 only: 1.8 V, Word align. In/Out Configurable frequency Inner pull-down: 100 µA Driver strength: 2.5 mA	1.8 V, Word align. In/Out Configurable frequency Inner pull-down: 200 µA Driver strength: 2 mA LISA-U200-00S: N.A.
I2S_CLK	36	SARA-G340/SARA-G350: 1.8 V, Clock Out Fixed frequency Driver strength: 5 mA	43	PCM_CLK: 1.8 V, PCM Clock Out	LISA-U120/U130 only: 1.8 V, Clock In/Out Configurable frequency Inner pull-down: 100 µA Driver strength: 2.5 mA	1.8 V, Clock In/Out Configurable frequency Inner pull-down: 200 µA Driver strength: 2 mA LISA-U200-00S: N.A.
I2S1_WA		Not Available	54	Not Available	Not Available	1.8 V, Data Out PCM / Normal I2S mode Driver strength: 1 mA LISA-U200-00S: N.A.
I2S1_TXD		Not Available	40	Not Available	Not Available	1.8 V, Data In PCM / Normal I2S mode Inner pull-down: 150 µA LISA-U200-00S: N.A.
I2S1_CLK		Not Available	53	Not Available	Not Available	1.8 V, Word align. In/Out Configurable frequency Inner pull-down: 150 µA Driver strength: 1 mA LISA-U200-00S: N.A.
I2S1_RXD		Not Available	39	Not Available	Not Available	1.8 V, Clock In/Out Configurable frequency Inner pull-down: 150 µA Driver strength: 1 mA LISA-U200-00S: N.A.

Pin Name	N°	SARA-G3 series	N°	LISA-C2 series	LISA-U1 series	LISA-U2 series
Other						
CODEC_CLK		Not Available	52	Not Available	Not Available	1.8 V, 13/26 MHz Out Driver strength: 4 mA LISA-U200-00S: N.A.
<b>GPIO</b>						
GPIO1	16	SARA-G340/SARA-G350: 1.8 V, configurable GPIO Default: Pin disabled Driver strength: 6 mA Inner pull-down: 51 µA	20	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 1 mA Inner pull-down: 100 µA	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 6 mA Inner pull-down: 200 µA
GPIO2	23	SARA-G340/SARA-G350: 1.8 V, configurable GPIO Default: GNSS supply ena. Driver strength: 6 mA Inner pull-down: 51 µA	21	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: GNSS supply en. Driver strength: 1 mA Inner pull-down: 85 µA	1.8 V, configurable GPIO Default: GNSS supply en. Driver strength: 1 mA Inner pull-down: 150 µA
GPIO3	24	SARA-G340/SARA-G350: 1.8 V, configurable GPIO Default: GNSS data ready Driver strength: 5 mA Inner pull-down: 27 µA	23	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: GNSS data ready Driver strength: 4 mA Inner pull-down: 55 µA	1.8 V, configurable GPIO Default: GNSS data ready Driver strength: 6 mA Inner pull-down: 200 µA
GPIO4	25	SARA-G340/SARA-G350: 1.8 V, configurable GPIO Default: GNSS RTC shar. Driver strength: 6 mA Inner pull-down: 51 µA	24	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: GNSS RTC sharing (4.7 k external pull-down required for RTC sharing) Driver strength: 4 mA Inner pull-down: 55 µA	1.8 V, configurable GPIO Default: GNSS RTC sharing Driver strength: 6 mA Inner pull-down: 200 µA
GPIO5		Not Available	51	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: SIM detection Driver strength: 2.5 mA Inner pull-down: 55 µA	1.8 V, configurable GPIO Default: SIM detection Driver strength: 6 mA Inner pull-down: 200 µA
GPIO6		Not Available	39	Not Available	Not Available	1.8 V, configurable GPIO Default: I2S1_RXD Driver strength: 1 mA Inner pull-down: 150 µA
GPIO7		Not Available	40	Not Available	Not Available	1.8 V, configurable GPIO Default: I2S1_TXD Driver strength: 1 mA Inner pull-down: 150 µA
GPIO8		Not Available	53	Not Available	Not Available	1.8 V, configurable GPIO Default: I2S1_CLK Driver strength: 1 mA Inner pull-down: 150 µA
GPIO9		Not Available	54	Not Available	Not Available	1.8 V, configurable GPIO Default: I2S1_WA Driver strength: 1 mA Inner pull-down: 150 µA
GPIO10		Not Available	55	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_SCLK Driver strength: 6 mA Inner pull-down: 200 µA
GPIO11		Not Available	56	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_MOSI Driver strength: 6 mA Inner pull-down: 200 µA
GPIO12		Not Available	57	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_MISO Driver strength: 6 mA Inner pull-down: 200 µA

Pin Name	N°	SARA-G3 series	N°	LISA-C2 series	LISA-U1 series	LISA-U2 series
GPIO13		Not Available	58	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_SRDY Driver strength: 6 mA Inner pull-down: 200 $\mu$ A
GPIO14		Not Available	59	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_MRDY Driver strength: 6 mA Inner pull-down: 200 $\mu$ A

**Table 60: Summary of pin differences and compatibility level among modules**



# B Migration between SARA-G3 and SARA-U2

## B.1 Overview

SARA-G3 and SARA-U2 series cellular modules have exactly the same SARA form factor (26.0 x 16.0 mm LGA) with exactly the same 96-pin layout as described in Figure 90, so that the modules can be alternatively mounted on a single application board using exactly the same copper mask, solder mask and paste mask.

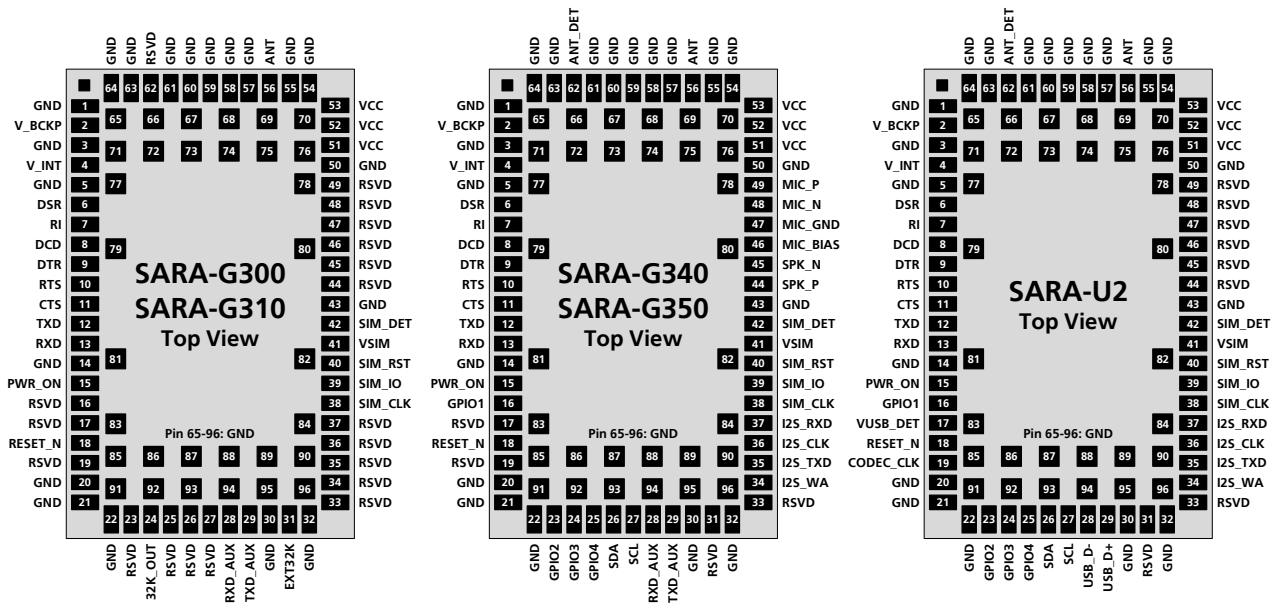


Figure 93: SARA-G3 and SARA-U2 series modules pin layout and pin assignment

Table 61 summarizes the interfaces provided by SARA-G3 and SARA-U2 series modules: all the interfaces provided by different modules are electrically compatible, so that the same compatible external circuit can be implemented on the application board.

Modules	Power	Antenna	System	SIM	Serial	Audio	Other
	Module supply input RTC supply I/O 1.8 V supply Output	Antenna RF I/O Rx diversity input Antenna detection	Power-on input Reset input 32 kHz input 32 kHz output	1.8 V / 3.0 V SIM SIM detection	1.8 V UART 1.8 V UART AUX 1.8 V SPI USB 2.0 1.8 V DDC	Analog audio I/O 1.8 V digital audio 13/26 MHz output	1.8 V GPIOs Network indication GNSS supply enable GNSS Tx data ready GNSS RTC sharing
<b>SARA-G300/G310 series</b>	• • •	•	• • • •	• •	• •		
<b>SARA-G340/G350 series</b>	• • •	• •	• •	• •	• •	• •	• • • • •
<b>SARA-U2 series</b>	• • •	• •	• •	• •	• •	• •	• • • • •

Table 61: Summary of SARA-G3 and SARA-U2 series modules interfaces

## B.2 Pin-out comparison between SARA-G3 and SARA-U2

Pin No	SARA-G3		SARA-U2		Remarks for migration
	Pin Name	Description	Pin Name	Description	
1	GND	Ground	GND	Ground	
2	V_BCKP	RTC Supply I/O Output characteristics: 2.3 V typ, 2 mA max Input op. range: 1.0 V – 2.4 V	V_BCKP	RTC Supply I/O Output characteristics: 1.8 V typ, 3 mA max Input op. range: 1.0 V – 1.9 V	No functional difference
3	GND	Ground	GND	Ground	
4	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 50 mA max	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 50 mA max	No functional difference
5	GND	Ground	GND	Ground	
6	DSR	UART DSR Output 1.8 V, Driver strength: 6 mA	DSR	UART DSR Output 1.8 V, Driver strength: 1 mA	No functional difference
7	RI	UART RI Output 1.8 V, Driver strength: 6 mA	RI	UART RI Output 1.8 V, Driver strength: 2 mA	No functional difference
8	DCD	UART DCD Output 1.8 V, Driver strength: 6 mA	DCD	UART DCD Output 1.8 V, Driver strength: 2 mA	No functional difference
9	DTR	UART DTR Input 1.8 V, Internal pull-up: ~33k	DTR	UART DTR Input 1.8 V, Internal pull-up: ~14 k	No functional difference
10	RTS	UART RTS Input 1.8 V, Internal pull-up: ~58 k	RTS	UART RTS Input 1.8 V, Internal pull-up: ~8 k	No functional difference
11	CTS	UART CTS Output 1.8 V, Driver strength: 6 mA	CTS	UART CTS Output 1.8 V, Driver strength: 6 mA	No functional difference
12	TXD	UART Data Input 1.8 V, Internal pull-up: ~18 k	TXD	UART Data Input 1.8 V, Internal pull-up: ~8 k	No functional difference
13	RXD	UART Data Output 1.8 V, Driver strength: 6 mA	RXD	UART Data Output 1.8 V, Driver strength: 6 mA	No functional difference
14	GND	Ground	GND	Ground	
15	PWR_ON	Power-on Input No internal pull-up L-level: -0.10 V – 0.65 V H-level: 2.00 V – 4.50 V ON L-level time: 5 ms min OFF L-level pulse time: Not Available	PWR_ON	Power-on Input No internal pull-up L-level: -0.30 V – 0.65 V H-level: 1.50 V – 4.40 V ON L-level pulse time: 50 µs min / 80 µs max OFF L-level pulse time: 1 s min	No functional difference
16	GPIO1 / RSVD	1.8 V GPIO / Reserved Default: Pin disabled Driver strength: 6 mA Internal pull-down: ~35 k	GPIO1	1.8 V GPIO Default: Pin disabled Driver strength: 6 mA Internal pull-down: ~9 k	No functional difference
17	RSVD	Reserved	VUSB_DET	USB Detect Input 5 V, Supply detection	USB detection instead of Reserved
18	RESET_N	Reset signal Internal diode & pull-up L-level: -0.30 V – 0.30 V H-level: 2.00 V – 4.70 V Reset L-level pulse time: 50 ms min (SARA-G350/G340) 3 s min (SARA-G300/G310)	RESET_N	Reset signal 10 kΩ internal pull-up L-level: -0.30 V – 0.51 V H-level: 1.32 V – 2.01 V Reset L-level pulse time: 50 ms min	No functional difference
19	RSVD	Reserved	CODEC_CLK	13 or 26 MHz Output Driver strength: 4 mA	Clock output instead of Reserved
20-22	GND	Ground	GND	Ground	
23	GPIO2 / RSVD	1.8 V GPIO / Reserved Default: GNSS supply enable Driver strength: 6 mA Internal pull-down: ~35 k	GPIO2	1.8 V GPIO Default: GNSS supply enable Driver strength: 1 mA Internal pull-down: ~14 k	No functional difference
24	GPIO3 / 32K_OUT	1.8 V GPIO / 32 kHz Output Default: GNSS data ready Driver strength: 5 mA Inner pull-down: ~67 k	GPIO3	1.8 V GPIO Default: GNSS data ready Driver strength: 6 mA Internal pull-down: ~9 k	No functional difference

SARA-G3			SARA-U2		Remarks for migration
Pin No	Pin Name	Description	Pin Name	Description	
25	GPIO4 / RSVD	1.8 V GPIO / Reserved Default: GNSS RTC sharing Driver strength: 6 mA Internal pull-down: ~35 k	GPIO4	1.8 V GPIO Default: GNSS RTC sharing Driver strength: 6 mA Internal pull-down: ~9 k	No functional difference
26	SDA / RSVD	I <sup>2</sup> C Data I/O / Reserved 1.8 V, open drain Driver strength: 3 mA	SDA	I <sup>2</sup> C Data I/O 1.8 V, open drain Driver strength: 1 mA	No functional difference
27	SCL / RSVD	I <sup>2</sup> C Clock Output / Reserved 1.8 V, open drain Driver strength: 3 mA	SCL	I <sup>2</sup> C Clock Output 1.8 V, open drain Driver strength: 1 mA	No functional difference
28	RXD_AUX	Aux UART Data Out 1.8 V, Driver strength: 5 mA	USB_D-	USB Data I/O (D-) High-Speed USB 2.0	USB instead of Auxiliary UART
29	TXD_AUX	Aux UART Data In 1.8 V, Internal pull-up:~18 k	USB_D+	USB Data I/O (D+) High-Speed USB 2.0	USB instead of Auxiliary UART
30	GND	Ground	GND	Ground	
31	RSVD / EXT32K	Reserved / 32 kHz Input	RSVD	Reserved	No functional difference
32	GND	Ground	GND	Ground	
33	RSVD	Reserved	RSVD	Reserved	No functional difference
34	I2S_WA / RSVD	I <sup>2</sup> S Word Alignment / Reserved 1.8 V, Driver strength: 6 mA	I2S_WA	I <sup>2</sup> S Word Alignment 1.8 V, Driver strength: 2 mA	No functional difference
35	I2S_TXD / RSVD	I <sup>2</sup> S Data Output / Reserved 1.8 V, Driver strength: 5 mA	I2S_TXD	I <sup>2</sup> S Data Output 1.8 V, Driver strength: 2 mA	No functional difference
36	I2S_CLK / RSVD	I <sup>2</sup> S Clock / Reserved 1.8 V, Driver strength: 5 mA	I2S_CLK	I <sup>2</sup> S Clock 1.8 V, Driver strength: 2 mA	No functional difference
37	I2S_RXD / RSVD	I <sup>2</sup> S Data Input / Reserved 1.8 V, Internal pull-down:~18 k	I2S_RXD	I <sup>2</sup> S Data Input 1.8 V, Inner pull-down: ~9 k	No functional difference
38	SIM_CLK	SIM Clock Output	SIM_CLK	SIM Clock Output	No functional difference
39	SIM_IO	SIM Data I/O	SIM_IO	SIM Data I/O	No functional difference
40	SIM_RST	SIM Reset Output	SIM_RST	SIM Reset Output	No functional difference
41	VSIM	SIM Supply Output	VSIM	SIM Supply Output	No functional difference
42	SIM_DET	SIM Detection Input 1.8 V, Internal pull-down:~18 k	SIM_DET	SIM Detection Input 1.8 V, Inner pull-down: ~9 k	No functional difference
43	GND	Ground	GND	Ground	
44	SPK_P / RSVD	Analog Audio Out (+) / Reserved	RSVD	Reserved	Analog audio not supported
45	SPK_N / RSVD	Analog Audio Out (-) / Reserved	RSVD	Reserved	Analog audio not supported
46	MIC_BIAS / RSVD	Microphone Supply Out / Reserved	RSVD	Reserved	Analog audio not supported
47	MIC_GND / RSVD	Microphone Ground / Reserved	RSVD	Reserved	Analog audio not supported
48	MIC_N / RSVD	Analog Audio In (-) / Reserved	RSVD	Reserved	Analog audio not supported
49	MIC_P / RSVD	Analog Audio In (+) / Reserved	RSVD	Reserved	Analog audio not supported
50	GND	Ground	GND	Ground	
51-53	VCC	Module Supply Input Normal op. range: 3.35 V – 4.5 V Extended op. range: 3.00 V – 4.5 V	VCC	Module Supply Input Normal op. range: 3.3 V – 4.4 V Extended op. range: 3.1 V – 4.5 V	No functional difference
54-55	GND	Ground	GND	Ground	
56	ANT	RF Antenna I/O ESD immunity (IEC 61000-4-2): ±4 kV contact / ±8 kV air ESD	ANT	RF Antenna I/O ESD immunity (IEC 61000-4-2): ±2 kV contact / ±4 kV air ESD	No functional difference
57-61	GND	Ground	GND	Ground	
62	ANT_DET / RSVD	Antenna Detection Input / Reserved	ANT_DET	Antenna Detection Input	No functional difference
63-96	GND	Ground	GND	Ground	

**Table 62: SARA-G3 and SARA-U2 pin assignment with remarks for migration**

For the detailed functional description of each interface of SARA-G3 and SARA-U2 series modules see the related section in the section 1, whereas for detailed design-in see the related section in the chapter 2.

For the detailed electrical characteristics of each interface of SARA-G3 and SARA-U2 series modules see the SARA-G3 series Data Sheet [1] and the SARA-U2 series Data Sheet [2].

### B.3 Schematic for SARA-G3 and SARA-U2 integration

Figure 94 shows an example of schematic diagram where a SARA-G3 or SARA-U2 series module can be integrated into the same application board, using all the available interfaces and functions of the modules. The different mounting options for the external parts are highlighted in different colors as described in the legend, according to the interfaces supported by the relative modules.

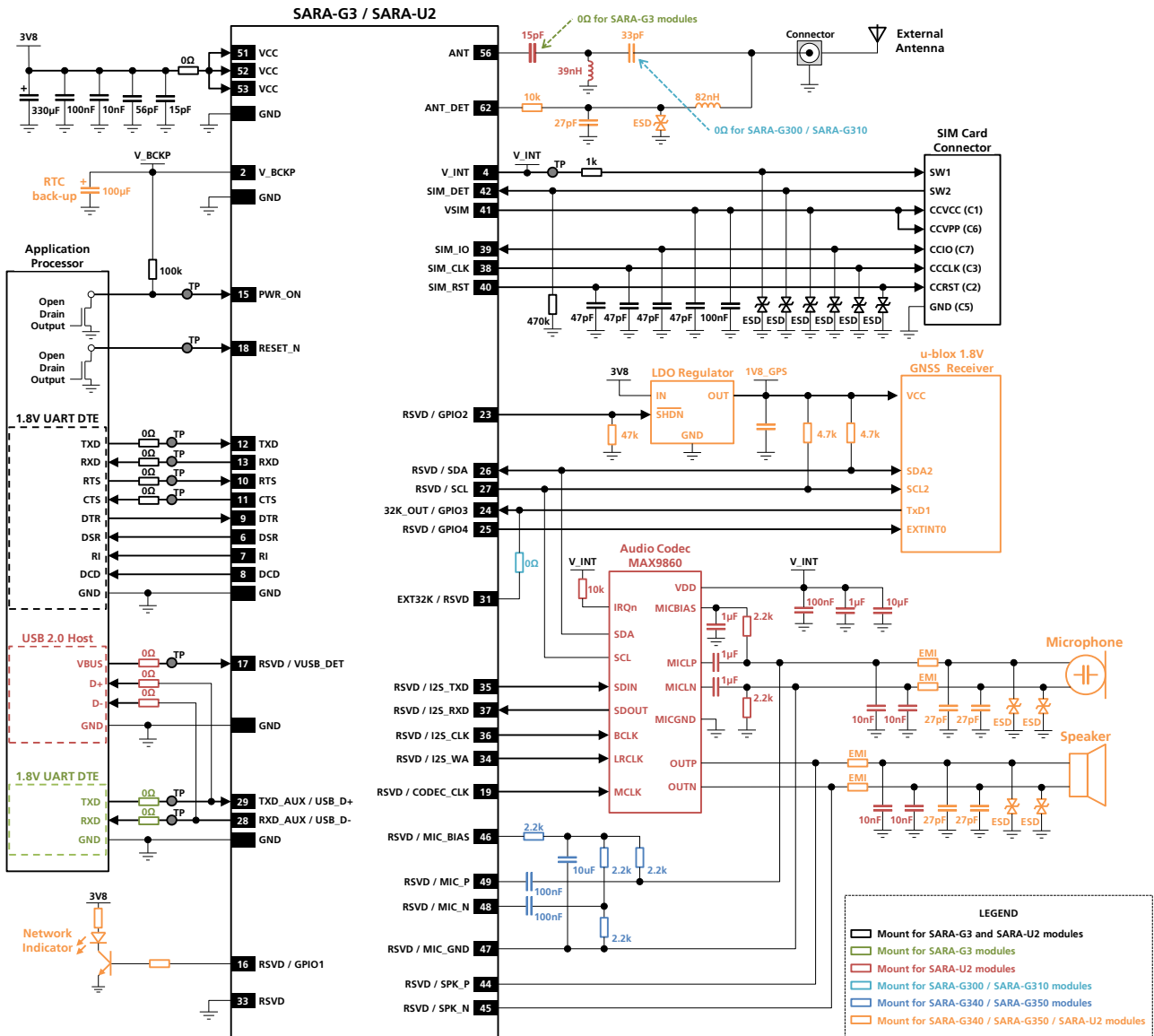


Figure 94: Example of complete schematic diagram to integrate SARA-G3 and SARA-U2 modules on the same application board

## C Glossary

3GPP	3rd Generation Partnership Project
ADC	Analog to Digital Converter
AP	Application Processor
AT	AT Command Interpreter Software Subsystem, or attention
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DDC	Display Data Channel interface
DL	Down-link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTM	Dual Transfer Mode
DTR	Data Terminal Ready
EMC	Electro-magnetic Compatibility
EMI	Electro-magnetic Interference
ESD	Electro-static Discharge
ESR	Equivalent Series Resistance
FEM	Front End Module
FOAT	Firmware Over AT commands
FTP	File Transfer Protocol
FTPS	FTP Secure
FW	Firmware
GMSK	Gaussian Minimum Shift Keying modulation
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HF	Hands-free
HTTP	HyperText Transfer Protocol
HTTPS	Hypertext Transfer Protocol over Secure Socket Layer
HW	Hardware
I/Q	In phase and Quadrature

I <sup>2</sup> C	Inter-Integrated Circuit interface
I <sup>2</sup> S	Inter IC Sound interface
IP	Internet Protocol
LCC	Leadless Chip Carrier
LDO	Low-Dropout
LGA	Land Grid Array
LNA	Low Noise Amplifier
M2M	Machine-to-Machine
MCS	Modulation Coding Scheme
N/A	Not Applicable
N.A.	Not Available
PA	Power Amplifier
PCM	Pulse Code Modulation
PCS	Personal Communications Service
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
PSRAM	Pseudo-Static RAM
PWM	Pulse Width Modulation
RF	Radio Frequency
RI	Ring Indicator
RTC	Real Time Clock
RTS	Request To Send
SAW	Surface Acoustic Wave
SDN / IN / PCN	Sample Delivery Note / Information Note / Product Change Notification
SIM	Subscriber Identification Module
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SPI	Serial Peripheral Interface
SRF	Self Resonant Frequency
TBD	To Be Defined
TCP	Transmission Control Protocol
TDMA	Time Division Multiple Access
TP	Test-Point
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
UL	Up-link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
UTRA	UMTS Terrestrial Radio Access
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio

## Related documents

- [1] u-blox SARA-G3 series Data Sheet, Docu No UBX-13000993
- [2] u-blox SARA-U2 series Data Sheet, Docu No UBX-13005287
- [3] u-blox AT Commands Manual, Docu No UBX-13002752
- [4] u-blox LISA-C200 series Data Sheet, Docu No UBX-13000623
- [5] u-blox LISA-U1 series Data Sheet, Docu No UBX-13002048
- [6] u-blox LISA-U2 series Data Sheet, Docu No UBX-13001734
- [7] u-blox LISA-C200 & FW75-C200/D200 System Integration Manual, Docu No UBX-13000620
- [8] u-blox LISA-U series System Integration Manual, Docu No UBX-13001118
- [9] u-blox C200 AT Commands Manual, Docu No UBX-13000621
- [10] ITU-T Recommendation V.24 - 02-2000 - List of definitions for interchange circuits between the Data Terminal Equipment (DTE) and the Data Circuit-terminating Equipment (DCE).  
<http://www.itu.int/rec/T-REC-V.24-200002-I/en>
- [11] 3GPP TS 27.007 – AT command set for User Equipment (UE) (Release 1999)
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- [13] 3GPP TS 27.010 – Terminal Equipment to User Equipment (TE-UE) multiplexer protocol (Release 1999)
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Some of the above documents can be downloaded from u-blox web-site (<http://www.u-blox.com>).

## Revision history

Revision	Date	Name	Status / Comments
-	30-Oct-2012	sses	Initial release
1	28-Mar-2013	sses	Updated status to Advance Information Updated suggested paste mask Updated current consumption description Updated voice-band processing system block diagram Updated DDC (I <sup>2</sup> C) application circuit for 3V u-blox GPS/GNSS receivers
2	12-Apr-2013	lpah	Updated status to Preliminary (Last revision with old doc number, GSM.G2-HW-12003)
A	03-Jul-2013	sses	Updated status to Advance Information Added integration description for SARA-G350 ATEX modules Updated SARA-G300 / SARA-G310 supported features: Circuit Switched Data, GPRS multi-slot class 10, 32K_OUT pin, Current consumption
A1	08-Aug-2013	lpah	Updated status to Preliminary. FW version for SARA-G300-00S and SARA-G310-00S is 08.58. SIM detection not supported by SARA-G300 and SARA-G310 modules
R06	29-Nov-2013	sses	Added migration between SARA-G3 and SARA-U2 modules Added the ANATEL label SARA-G310 and SARA-G350
R07	23-Jan-2014	lpah / sses	Document applicability extended to SARA-G340
R08	29-Apr-2014	sses	Initial release including SARA-U2 series
R09	20-Jun-2014	sses	Document applicability extended to SARA-G340-01S, SARA-G350-01S and SARA-G350-01B, with minor other corrections and clarifications
R10	23-Jul-2014	sses	Added additional antennas and external audio codecs examples, with minor other corrections and clarifications Updated SSL supported features Added SARA-G350 CCC mark
R11	17-Oct-2014	lpah	Added CE notified body ID for SARA-G340-01S / SARA-G350-01S



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