The IOE registers in each I/O block share the same source for the preset or clear features. You can program preset or clear for each individual IOE, but you cannot use both features simultaneously. You can also program the registers to power-up high or low after configuration is complete. If programmed to power-up low, an asynchronous clear can control the registers. If programmed to power-up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of the active-low input of another device upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

For more information about the input and output pin delay settings, refer to the *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

PCI-Clamp Diode

Cyclone IV devices provide an optional PCI-clamp diode enabled input and output for each I/O pin. Dual-purpose configuration pins support the diode in user mode if the specific pins are not used as configuration pins for the selected configuration scheme. For example, if you are using the active serial (AS) configuration scheme, you cannot use the clamp diode on the `ASDO` and `nCSO` pins in user mode. Dedicated configuration pins do not support the on-chip diode.

The PCI-clamp diode is available for the following I/O standards:

- 3.3-V LVTTL
- 3.3-V LVCMOS
- 3.0-V LVTTL
- 3.0-V LVCMOS
- 2.5-V LVTTL/LVCMOS
- PCI
- PCI-X

If the input I/O standard is one of the listed standards, the PCI-clamp diode is enabled by default in the Quartus II software.

OCT Support

Cyclone IV devices feature OCT to provide I/O impedance matching and termination capabilities. OCT helps prevent reflections and maintain signal integrity while minimizing the need for external resistors in high pin-count ball grid array (BGA) packages. Cyclone IV devices provide I/O driver on-chip impedance matching and R_S OCT for single-ended outputs and bidirectional pins.

When using R_S OCT, programmable current strength is not available.

There are two ways to implement OCT in Cyclone IV devices:

- OCT with calibration
- OCT without calibration

Table 6–2 lists the I/O standards that support impedance matching and series termination.

Table 6–2. Cyclone IV Device I/O Features Support (Part 1 of 2)

I/O Standard	IOH/IOL Current Strength Setting (mA) (1), (9)		R_S OCT with Calibration Setting, Ohm (Ω)		R_S OCT Without Calibration Setting, Ohm (Ω)		Cyclone IV E I/O Banks Support	Cyclone IV GX I/O Banks Support	Slew Rate Option (6)	PCI-clamp Diode Support
	Column I/O	Row I/O	Column I/O	Row I/O (8)	Column I/O	Row I/O (8)				
3.3-V LVTTL	4,8	4,8	—	—	—	—	1,2,3,4,5,6,7,8	3,4,5,6,7,8,9	—	✓
3.3-V LVCMOS	2	2	—	—	—	—			—	✓
3.0-V LVTTL	4,8,12,16	4,8,12,16	50,25	50,25	50,25	50,25			0,1,**2**	✓
3.0-V LVCMOS	4,8,12,16	4,8,12,16	50,25	50,25	50,25	50,25				✓
3.0-V PCI/PCI-X	—	—	—	—	—	—			—	✓
2.5-V LVTTL/LVCMOS	4,8,12,16	4,8,12,16	50,25	50,25	50,25	50,25			0,1,**2**	✓
1.8-V LVTTL/LVCMOS	2,4,6,8,10,12,16	2,4,6,8,10,12,16	50,25	50,25	50,25	50,25				—
1.5-V LVCMOS	2,4,6,8,10,12,16	2,4,6,8,10,12,16	50,25	50,25	50,25	50,25				—
1.2-V LVCMOS	2,4,6,8,10,12	2,4,6,8,10	50,25	50	50,25	50		4,5,6,7,8		—
SSTL-2 Class I	8,12	8,12	50	50	50	50		3,4,5,6,7,8,9		—
SSTL-2 Class II	16	16	25	25	25	25				—
SSTL-18 Class I	8,10,12	8,10,12	50	50	50	50				—
SSTL-18 Class II	12,16	12,16	25	25	25	25				—
HSTL-18 Class I	8,10,12	8,10,12	50	50	50	50				—
HSTL-18 Class II	16	16	25	25	25	25				—
HSTL-15 Class I	8,10,12	8,10,12	50	50	50	50				—
HSTL-15 Class II	16	16	25	25	25	25				—
HSTL-12 Class I	8,10,12	8,10	50	50	50	50		4,5,6,7,8		—
HSTL-12 Class II	14	—	25	—	25	—	3,4,7,8	4,7,8		—
Differential SSTL-2 Class I (2), (7)	8,12	8,12	50	50	50	50	1,2,3,4,5,6,7,8	3,4,5,6,7,8	0,1,**2**	—
Differential SSTL-2 Class II (2), (7)	16	16	25	25	25	25				—
Differential SSTL-18 (2), (7)	8,10,12	—	50	—	50	—				—
Differential HSTL-18 (2), (7)	8,10,12	—	50	—	50	—				—
Differential HSTL-15 (2), (7)	8,10,12	—	50	—	50	—				—
Differential HSTL-12 (2), (7)	8,10,12	—	50	—	50	—	3,4,7,8	4,7,8		—

Table 6–2. Cyclone IV Device I/O Features Support (Part 2 of 2)

I/O Standard	IOH/IOL Current Strength Setting (mA) (1), (9)		R_S OCT with Calibration Setting, Ohm (Ω)		R_S OCT Without Calibration Setting, Ohm (Ω)		Cyclone IV E I/O Banks Support	Cyclone IV GX I/O Banks Support	Slew Rate Option (6)	PCI-clamp Diode Support
	Column I/O	Row I/O	Column I/O	Row I/O (8)	Column I/O	Row I/O (8)				
BLVDS	8,12,16	8,12,16	—	—	—	—	1,2,3,4, 5,6,7,8	3,4,5,6, 7,8	0,1,**2**	—
LVDS (3)	—	—	—	—	—	—		5,6	—	—
PPDS (3), (4)	—	—	—	—	—	—			—	—
RSDS and mini-LVDS (3), (4)	—	—	—	—	—	—			—	—
Differential LVPECL (5)	—	—	—	—	—	—		3,4,5,6, 7,8	—	—

Notes to Table 6–2:

(1) The default current strength setting in the Quartus II software is 50-Ω OCT without calibration for all non-voltage reference and HSTL/SSTL Class I I/O standards. The default setting is 25-Ω OCT without calibration for HSTL/SSTL Class II I/O standards.

(2) The differential SSTL-18 and SSTL-2, differential HSTL-18, HSTL-15, and HSTL-12 I/O standards are supported only on clock input pins and PLL output clock pins.

(3) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only for Cyclone IV E devices and right I/O banks 5 and 6 only for Cyclone IV GX devices. Differential outputs in column I/O banks require an external resistor network.

(4) This I/O standard is supported for outputs only.

(5) This I/O standard is supported for clock inputs only

(6) The default Quartus II slew rate setting is in bold; **2** for all I/O standards that supports slew rate option.

(7) Differential SSTL-18, differential HSTL-18, HSTL-15, and HSTL-12 I/O standards do not support Class II output.

(8) Cyclone IV GX devices only support right I/O pins.

(9) Altera not only offers current strength that meets the industrial standard specification but also other additional current strengths.

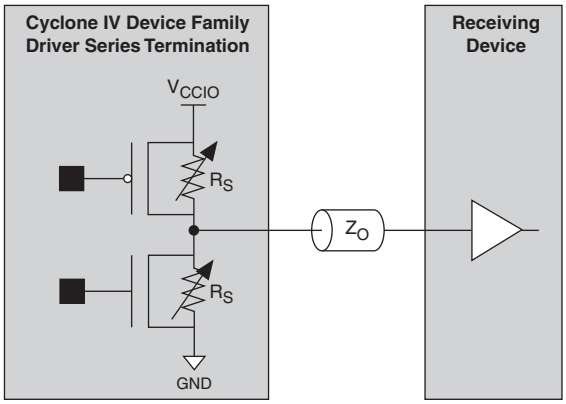
For more details about the differential I/O standards supported in Cyclone IV I/O banks, refer to "High-Speed I/O Interface" on page 6–24.

On-Chip Series Termination with Calibration

Cyclone IV devices support R_S OCT with calibration in the top, bottom, and right I/O banks. The R_S OCT calibration circuit compares the total impedance of the I/O buffer to the external 25-Ω ±1% or 50-Ω ±1% resistors connected to the RUP and RDN pins, and dynamically adjusts the I/O buffer impedance until they match (as shown in Figure 6–2).

The R_S shown in Figure 6–2 is the intrinsic impedance of the transistors that make up the I/O buffer.

Figure 6–2. Cyclone IV Devices R_S OCT with Calibration



OCT with calibration is achieved using the OCT calibration block circuitry. There is one OCT calibration block in each of I/O banks 2, 4, 5, and 7 for Cyclone IV E devices and I/O banks 4, 5, and 7 for Cyclone IV GX devices. Each calibration block supports each side of the I/O banks. Because there are two I/O banks sharing the same calibration block, both banks must have the same V_{CCIO} if both banks enable OCT calibration. If two related banks have different V_{CCIO}, only the bank in which the calibration block resides can enable OCT calibration.

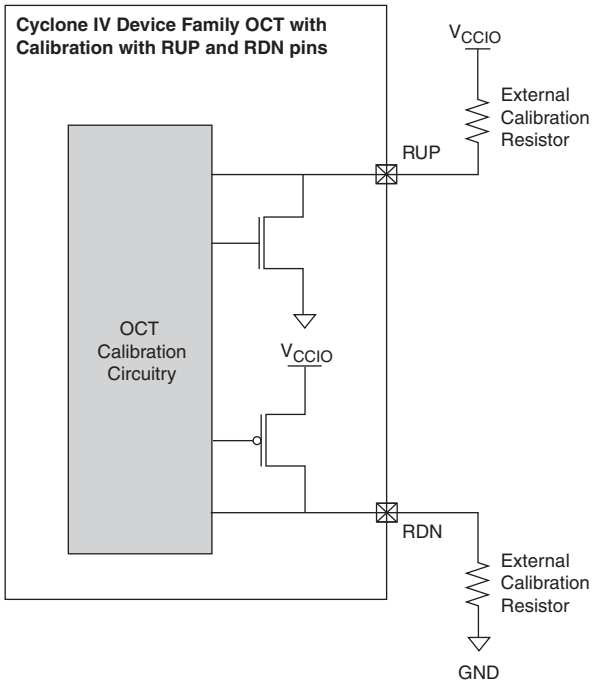
Figure 6–10 on page 6–18 shows the top-level view of the OCT calibration blocks placement.

Each calibration block comes with a pair of RUP and RDN pins. When used for calibration, the RUP pin is connected to V_{CCIO} through an external 25-Ω ±1% or 50-Ω ±1% resistor for an R_S OCT value of 25 Ω or 50 Ω, respectively. The RDN pin is connected to GND through an external 25-Ω ±1% or 50-Ω ±1% resistor for an R_S OCT value of 25 Ω or 50 Ω, respectively. The external resistors are compared with the internal resistance using comparators. The resultant outputs of the comparators are used by the OCT calibration block to dynamically adjust buffer impedance.

☞ During calibration, the resistance of the RUP and RDN pins varies.

Figure 6–3 shows the external calibration resistors setup on the RUP and RDN pins and the associated OCT calibration circuitry.

Figure 6–3. Cyclone IV Devices R_S OCT with Calibration Setup



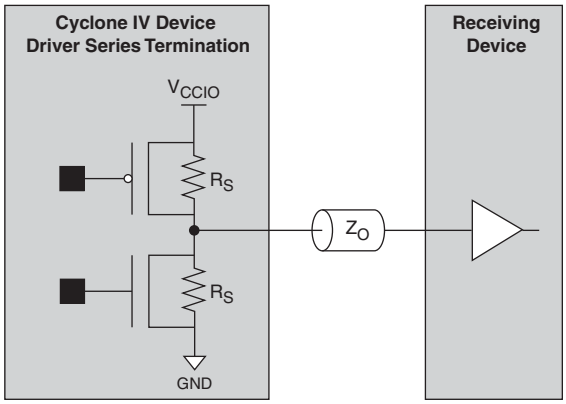
RUP and RDN pins go to a tri-state condition when calibration is completed or not running. These two pins are dual-purpose I/Os and function as regular I/Os if you do not use the calibration circuit.

On-Chip Series Termination Without Calibration

Cyclone IV devices support driver impedance matching to match the impedance of the transmission line, which is typically 25 or 50 Ω. When used with the output drivers, OCT sets the output driver impedance to 25 or 50 Ω. Cyclone IV devices also support I/O driver series termination (R_S = 50 Ω) for SSTL-2 and SSTL-18.

Figure 6–4 shows the single-ended I/O standards for OCT without calibration. The R_S shown is the intrinsic transistor impedance.

Figure 6–4. Cyclone IV Devices R_S OCT Without Calibration



All I/O banks and I/O pins support impedance matching and series termination. Dedicated configuration pins and JTAG pins do not support impedance matching or series termination.

R_S OCT is supported on any I/O bank. V_{CCIO} and V_{REF} must be compatible for all I/O pins to enable R_S OCT in a given I/O bank. I/O standards that support different R_S values can reside in the same I/O bank as long as their V_{CCIO} and V_{REF} do not conflict.

Impedance matching is implemented using the capabilities of the output driver and is subject to a certain degree of variation, depending on the process, voltage, and temperature.

For more information about tolerance specification, refer to the *Cyclone IV Device Datasheet* chapter.

I/O Standards

Cyclone IV devices support multiple single-ended and differential I/O standards. Cyclone IV devices support 3.3-, 3.0-, 2.5-, 1.8-, 1.5-, and 1.2-V I/O standards.

Table 6–3 summarizes I/O standards supported by Cyclone IV devices and which I/O pins support them.

Table 6–3. Cyclone IV Devices Supported I/O Standards and Constraints (Part 1 of 3)

I/O Standard	Type	Standard Support	V_{CCIO} Level (in V)		Column I/O Pins			Row I/O Pins (1)	
			Input	Output	CLK, DQS	PLL_OUT	User I/O Pins	CLK, DQS	User I/O Pins
3.3-V LVTTL, 3.3-V LVCMOS (2)	Single-ended	JESD8-B	3.3/3.0/2.5 (3)	3.3	✓	✓	✓	✓	✓
3.0-V LVTTL, 3.0-V LVCMOS (2)	Single-ended	JESD8-B	3.3/3.0/2.5 (3)	3.0	✓	✓	✓	✓	✓

Table 6–3. Cyclone IV Devices Supported I/O Standards and Constraints (Part 2 of 3)

I/O Standard	Type	Standard Support	V_{CCIO} Level (in V)		Column I/O Pins			Row I/O Pins (1)	
			Input	Output	CLK, DQS	PLL_OUT	User I/O Pins	CLK, DQS	User I/O Pins
2.5-V LVTTL / LVCMOS	Single-ended	JESD8-5	3.3/3.0/2.5 (3)	2.5	✓	✓	✓	✓	✓
1.8-V LVTTL / LVCMOS	Single-ended	JESD8-7	1.8/1.5 (3)	1.8	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single-ended	JESD8-11	1.8/1.5 (3)	1.5	✓	✓	✓	✓	✓
1.2-V LVCMOS (4)	Single-ended	JESD8-12A	1.2	1.2	✓	✓	✓	✓	✓
SSTL-2 Class I, SSTL-2 Class II	voltage-referenced	JESD8-9A	2.5	2.5	✓	✓	✓	✓	✓
SSTL-18 Class I, SSTL-18 Class II	voltage-referenced	JESD815	1.8	1.8	✓	✓	✓	✓	✓
HSTL-18 Class I, HSTL-18 Class II	voltage-referenced	JESD8-6	1.8	1.8	✓	✓	✓	✓	✓
HSTL-15 Class I, HSTL-15 Class II	voltage-referenced	JESD8-6	1.5	1.5	✓	✓	✓	✓	✓
HSTL-12 Class I	voltage-referenced	JESD8-16A	1.2	1.2	✓	✓	✓	✓	✓
HSTL-12 Class II (9)	voltage-referenced	JESD8-16A	1.2	1.2	✓	✓	✓	—	—
PCI and PCI-X	Single-ended	—	3.0	3.0	✓	✓	✓	✓	✓
Differential SSTL-2 Class I or Class II	Differential (5)	JESD8-9A	—	2.5	—	✓	—	—	—
			2.5	—	✓	—	—	✓	—
Differential SSTL-18 Class I or Class II	Differential (5)	JESD815	—	1.8	—	✓	—	—	—
			1.8	—	✓	—	—	✓	—
Differential HSTL-18 Class I or Class II	Differential (5)	JESD8-6	—	1.8	—	✓	—	—	—
			1.8	—	✓	—	—	✓	—
Differential HSTL-15 Class I or Class II	Differential (5)	JESD8-6	—	1.5	—	✓	—	—	—
			1.5	—	✓	—	—	✓	—
Differential HSTL-12 Class I or Class II	Differential (5)	JESD8-16A	—	1.2	—	✓	—	—	—
			1.2	—	✓	—	—	✓	—
PPDS (6)	Differential	—	—	2.5	—	✓	✓	—	✓
LVDS (10)	Differential	ANSI/TIA/EIA-644	2.5	2.5	✓	✓	✓	✓	✓
RSDS and mini-LVDS (6)	Differential	—	—	2.5	—	✓	✓	—	✓
BLVDS (8)	Differential	—	2.5	2.5	—	—	✓	—	✓

Table 6–3. Cyclone IV Devices Supported I/O Standards and Constraints (Part 3 of 3)

I/O Standard	Type	Standard Support	V_{CCIO} Level (in V)		Column I/O Pins			Row I/O Pins (1)	
			Input	Output	CLK, DQS	PLL_OUT	User I/O Pins	CLK, DQS	User I/O Pins
LVPECL (7)	Differential	—	2.5	—	✓	—	—	✓	—

Notes to Table 6–3:

(1) Cyclone IV GX devices only support right I/O pins.

(2) The PCI-clamp diode must be enabled for 3.3-V/3.0-V LVTTL/LVCMOS.

(3) The Cyclone IV architecture supports the MultiVolt I/O interface feature that allows Cyclone IV devices in all packages to interface with I/O systems that have different supply voltages.

(4) Cyclone IV GX devices do not support 1.2-V V_{CCIO} in banks 3 and 9. I/O pins in bank 9 are dual-purpose I/O pins that are used as configuration or GPIO pins. Configuration scheme is not support at 1.2 V, therefore bank 9 can not be powered up at 1.2-V V_{CCIO}.

(5) Differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them. Differential HSTL and SSTL are only supported on CLK pins.

(6) PPDS, mini-LVDS, and RSDS are only supported on output pins.

(7) LVPECL is only supported on clock inputs.

(8) Bus LVDS (BLVDS) output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses LVDS input buffer.

(9) 1.2-V HSTL input is supported at both column and row I/Os regardless of Class I or Class II.

(10) True LVDS, RSDS, and mini-LVDS I/O standards are supported in left and right I/O pins, while emulated LVDS, RSDS, and mini-LVDS I/O standards are supported in the top, bottom, and right I/O pins.

Cyclone IV devices support PCI and PCI-X I/O standards at 3.0-V V_{CCIO}. The 3.0-V PCI and PCI-X I/O are fully compatible for direct interfacing with 3.3-V PCI systems without requiring any additional components. The 3.0-V PCI and PCI-X outputs meet the V_{IH} and V_{IL} requirements of 3.3-V PCI and PCI-X inputs with sufficient noise margin.

For more information about the 3.3/3.0/2.5-V LVTTL & LVCMOS multivolt I/O support, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

Termination Scheme for I/O Standards

This section describes recommended termination schemes for voltage-referenced and differential I/O standards.

The 3.3-V LVTTL, 3.0-V LVTTL and LVCMOS, 2.5-V LVTTL and LVCMOS, 1.8-V LVTTL and LVCMOS, 1.5-V LVCMOS, 1.2-V LVCMOS, 3.0-V PCI, and PCI-X I/O standards do not specify a recommended termination scheme per the JEDEC standard

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figure 6–5 and Figure 6–6.

Figure 6–5. Cyclone IV Devices HSTL I/O Standard Termination

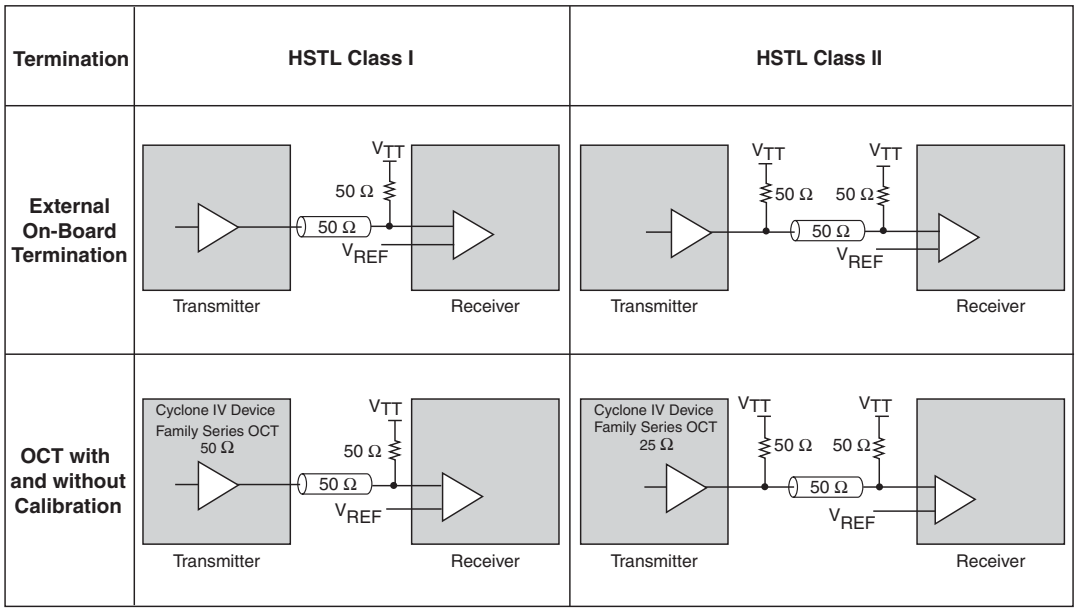
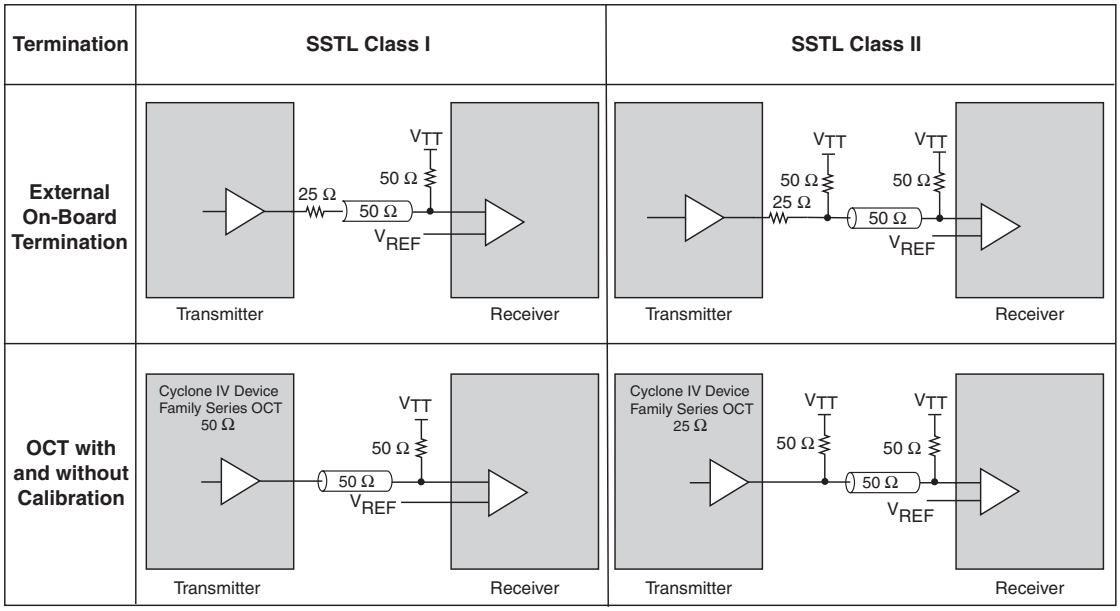


Figure 6–6. Cyclone IV Devices SSTL I/O Standard Termination



Differential I/O Standard Termination

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus (refer to Figure 6–7 and Figure 6–8).

Cyclone IV devices support differential SSTL-2 and SSTL-18, differential HSTL-18, HSTL-15, and HSTL-12, PPDS, LVDS, RSDS, mini-LVDS, and differential LVPECL.

Figure 6–7. Cyclone IV Devices Differential HSTL I/O Standard Class I and Class II Interface and Termination

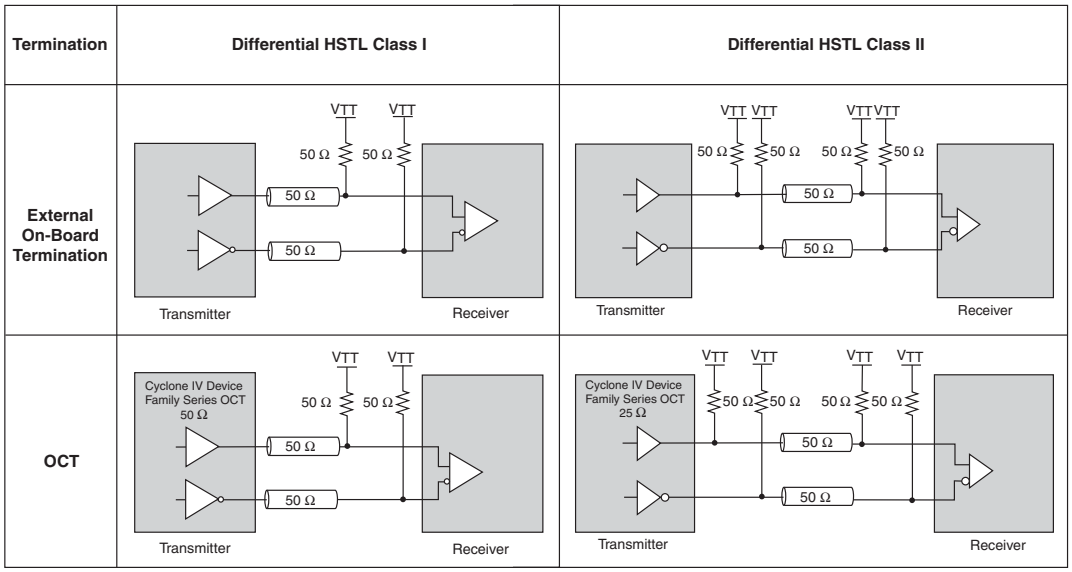
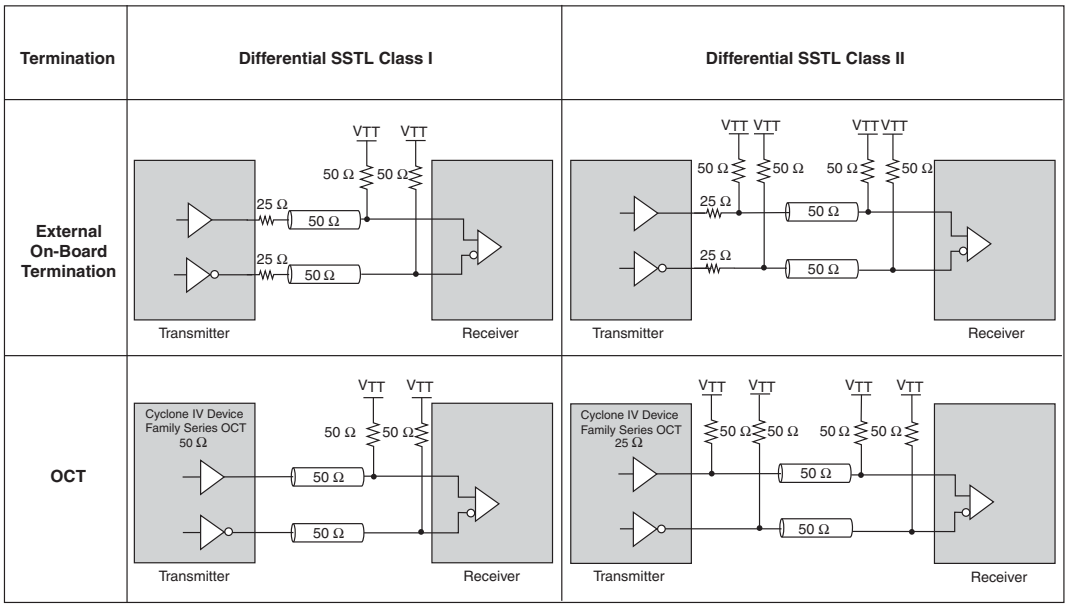


Figure 6–8. Cyclone IV Devices Differential SSTL I/O Standard Class I and Class II Interface and Termination *(1)*



Note to Figure 6–8:

(1) Only Differential SSTL-2 I/O standard supports Class II output.