SHARP

LM32010P

Medium Size Graphic Type LCD Module

Features

- 12 cm [4.7"] QVGA format
- Black & white display
- High brightness (80 cd/m²)
- Mechanically compatible with LM32P10 and LM32K101

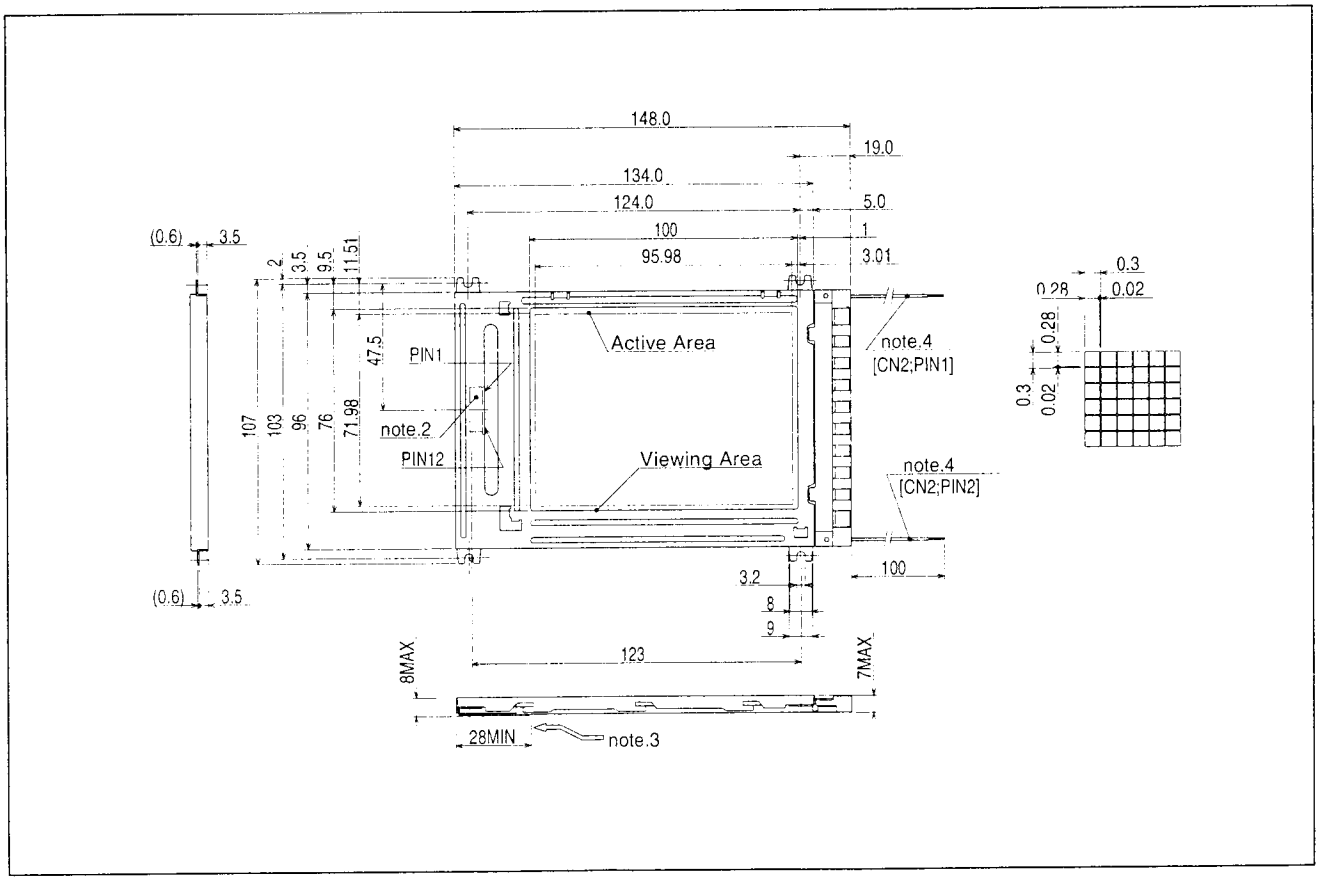
Specifications

Parameter		Unit
Display size	12 [4.7]	cm ["]
Dot format (H x V)	320 x 240	dot
Dot pitch (H x V)	0.30 x 0.30	mm
Active area (H x V)	96.0 x 72.0	mm
Panel type	FSTN	-
Panel mode	Transmissive	-
Color	B/W	color
Contrast ratio	12 : 1	-
Response time	400 [-]	ms

Parameter		Unit
Brightness	80	cd/m²
Duty ratio	1/240	-
Backlight	1CCFT(E)	-
Power consumption panel	178	mW
Backlight	1 250	mW
Outline dimensions (W x H x D)	148.0 x 96.0(107.0) x 8.0	mm
Weight	140	g
Operating temperature	0 to +45	C
Storage temperature	-25 to +60	C

Outline Dimensions

unit : mm



1. Application

This data sheet is to introduce the specification of LM32010P,
Passive Matrix type LCD Unit.
(320×240 dot, FSTN, negative type, with backlight system by cold cathode fluorescent tube (CCFT).)

2. Construction and Outline

Consutruction : 320×240 full dot graphic display unit
Outline : See Fig. 8 .
Connection : See Fig. 8 . and Table. 5 .

There shall be no scrtches, stains, chips, distortions and other external drawbacks that may affect the display function.
Rejection criteria shall be noted in Inspection Standard S-U-012-01.

3. Mechanical Specifications

Table 1

Parameter	Specification		Unit
Outline dimensions	148 (W) × 96 (H) × 8MAX (D)	Note1	mm
Effective viewing area	100 (W) × 76 (H)		mm
Display format	320 (W) × 240 (H) full dot		—
Dot size	0.28 (W) × 0.26 (H)		mm
Dot spacing	0.02		mm
Character color	White	Note2	—
Background color	Black	Note2	—
Weight	Approx. 140		g

Note1 : Excluded the mounting tab. (See Fig. 8)

Note2 : Due to the characteristics of the LC Material, the colors vary with environmental temperature.

Display Data "H" : Dots on : White
"L" : Dots off : Black

4. Absolute Maximum Ratings

4-1. Electrical Absolute Maximum Ratings

Table 2

Parameter	Symbol	Min	MAX	Unit	Remark
Supply voltage (Logic)	$V_{DD}-V_{SS}$	0	6.0	V	Ta=25℃
Supply voltage (LCD Driver)	$V_{DD}-V_{EE}$	0	30.0	V	
Input voltage	V_{IN}	0	VDD	V	
Back Light	VCCFT	0	1500	Vrms	
	ICCFT	0	6.5	mArms	

4-2. Environmental Condition

Table 1

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-25℃	+60℃	0℃	+45℃	
Humidity	Note 1		Note 1		No condensation
Vibration	Note 2		Note 2		3 directions (X/Y/Z)
Shock	Note 3		Note 3		6 directions (±X/±Y/±Z)

Note 1) Ta≦40℃·····90% RH Max
Ta>40℃·····Absolute humidity shall be less than Ta=40℃ / 90% RH

Note 2) These test conditions are in accordance with 'IEC 68-2-6'
Frequency : 10 ~ 55HZ
Vibration width : 1.5mm
Interval : 10HZ ~ 55HZ ~ 10HZ (1 min)
2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490m/S² (50G)
Pulse width : 11ms
3 times for each direction of ±X/±Y/±Z.

5. Electrical Specifications

5.1 Electrical characteristics

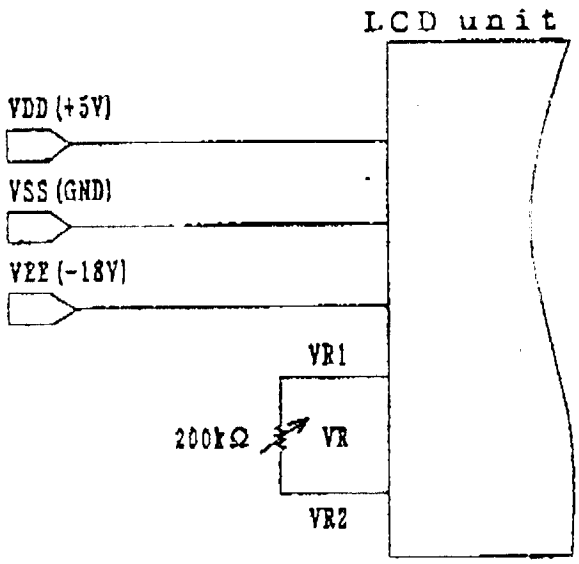
Table 4

Ta=25°C, VDD=5V±5%

Prameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}		4.75	5.0	5.25	V
Supply voltage (LCD drive)	V_{EE}-V_{SS}	V_{DD}=5V (Note 1)	-18.5	-18.0	-17.5	V
Input signal voltage	V_{IN}	'H' level	0.8VDD	--	VDD	V
		'L' level	0	--	0.2VDD	V
Input leakage current	I_{IL}	'H' level	—	—	20	μA
		'L' level	-20.0	—	—	μA
Supply current (Logic)	I_{DD}	V_{DD}=5V, V_{EE}=-18V	—	8	18	mA
Supply current (LCD)	I_{EE}	VR=100kΩ	—	8	12	mA
Power consumption (LCD)	PdLCD	F=80HZ (Note 2)	—	178	356	mW
Start voltage (B/L)	VFTS	Inverter			480	Vrms
Supply voltage (B/L)	VFTL	LM000108	225	250	275	Vrms
Supply current (B/L)	IFT	Input voltage 12V	4	5	6	mArms
Power consumption (B/L)	PdFT			1.25		W

Note 1) The viewing angle(θ) where obtains the maximum contrast can be set by adjusting variable resistor between VR1 and VR2.
Refer to Fig. 4 for the difinition of θ.

Note 2) Display high frequency pattern.



5-2. Interface signals

CN1

Table 5

Pin No.	Symbols	Description	Level
1	S	Scan start-up signal	" H "
2	CP1	Input data latch signal	H→L
3	CP2	Data input clock signal	H→L
4	VDD	Power supply for logic and LCD (+5v)	-
5	VSS	Ground potential (0v)	-
6	VEE	Power supply for LCD (-18)	-
7	D0	Display data signal	H (ON), L (OFF)
8	D1		
9	D2		
10	D3		
11	VR1	LCD Contrast Adjust (A)	-
12	VR2	LCD Contrast Adjust (B)	-

Used Connector : 52103-1217 [Molex]
Mating Cable : 1.0mm pich , 12pins F.F.C.

CN2

Pin No. *1	Symbols	Description
1	VFT1	Power supply for CCFT back light
2	VFT2	Power supply for CCFT back light

*1 : Pin No. and its location are shown in Fig. 8.

6. Unit Driving Method

6-1. Circuit Configuration

Fig. 7 shows the block diagram of the Unit's circuitry.

6-2. Display Face Configuration

The display face electrically consists of signal display segment of 320 × 240 dots.

6-3. Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits.

Display data which are externally divided into data for each row (320 dots) will be sequentially transferred in the form of 4-bit parallel data through shift resisters by Clock Signal CP2 from the left top of the display face.

When data of one row (320 dots) have been inputted, then lached in the from of parallel data for 320 lines of signal electrodes by Latch Signal CP1. Then the corresponding drive signal will be transmitted to the 320 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.
While the 1st rows of data are being displayed, the 2nd rows of data are entered. When 320 dots of data have been transferred then latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

Such data input will be repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing method. Then data input proceeds to the next display face.

Scan start-up Signal S generates scan signal to drive horizontal electrodes.

The unit shall be driven at the speed of 70~80Hz/frame to avoid flickering.

Since DC voltage if applied to LCD panel, causes chemical reaction which will deteriorate LCD panel, drive waveform shall be inverted to prevent the generation of such DC voltage. And to prevent such problem, AC waveform circuit generated by counting CP1 (M generator) is built in this circuit.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit gose up as the operating frequency CP2 increases. Thus the driver LSI applies the system of transferring 4-bit palallel data through the 4 lines of shift resistors to reduce the data transfer speed CP2. Thanks to the LSI, the power consumption of the unit will be minimized.

In this circuit configuration, 4-bit display data shall be therefore inputted to data input pins of D0~D3.

Furthermore the LCD unit adopts bus line system for data input to minimize the power consumption. In this system data input terminal of each driver LSI is activated only when relevant data input is fed.

Data input for colum electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20 CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This process is simultaneously followed at the column driver LSI's of both the upper and the lower display segments. Thus data input through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no reflesh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3.

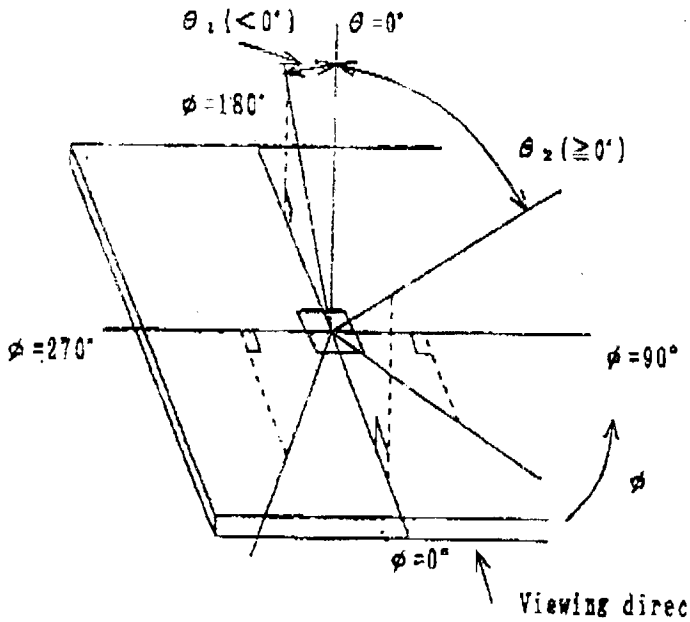
7. Optical Characteristics

(Table 7 shows the optical characteristics when the viewing angle obtaining the maximum contrast (ε) is adjusted to 0 degrees.)

Table 7 VDD=5V, Ta=25°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Remark
Viewing angle range	$\theta_2-\theta_1$	ϕ=0°	$C_o \geq 4.0$	45	—	—	dgr.	Note 1
	θ_1	$\theta_1(\theta_2$	$C_o=4.0$	—	—	-15	dgr.	Note 1
	θ_2			20	—	—	dgr.	Note 1
	$\theta_2-\theta_1$	ϕ=90°	$C_o \geq 4.0$	55	—	—	dgr.	Note 1
	θ_1		$C_o=4.0$	—	—	-25	dgr.	Note 1
	θ_2	$\theta_1(\theta_2$		25	—	—	dgr.	Note 1
Contrast ratio	C_o	θ=0°, ϕ=0°		7.0	12.0	—		Note 2
Response speed	τr	θ=0°, ϕ=0°		—	200	300	ms	Note 3
	τd	θ=0°, ϕ=0°		—	200	300	ms	Note 3

Note 1) The viewing angle range may bedefined as shown below.



* Angles θ_1, θ_2 and ϕ shall fall within the range overwhich the displayed character each be read.

Fig. 4 Definition of Viewing Angle

Note 2) Contrast ratio may be defined as follows:

Contrast ratio is calcurated by using the following formula when the waveform voltage (Fig. 6) is applied in optical characteristics test method (Fig. 5).

$$\text{Contrast ratio} = \frac{\text{Photo-detector output voltage with select waveform being applied}}{\text{Photo-detector output voltage with non-select waveform being applied}}$$

Note 3) The response characteristics of photo-detector output are measured as shown in Fig. 6, assuming that input signals are applide so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig. 5.

Note 4) Table 7 shown the optical characteristics detected when the LCD applied voltage waveforms are in the highest frequency *.

* The most critical condition for the characteristics of LCD.

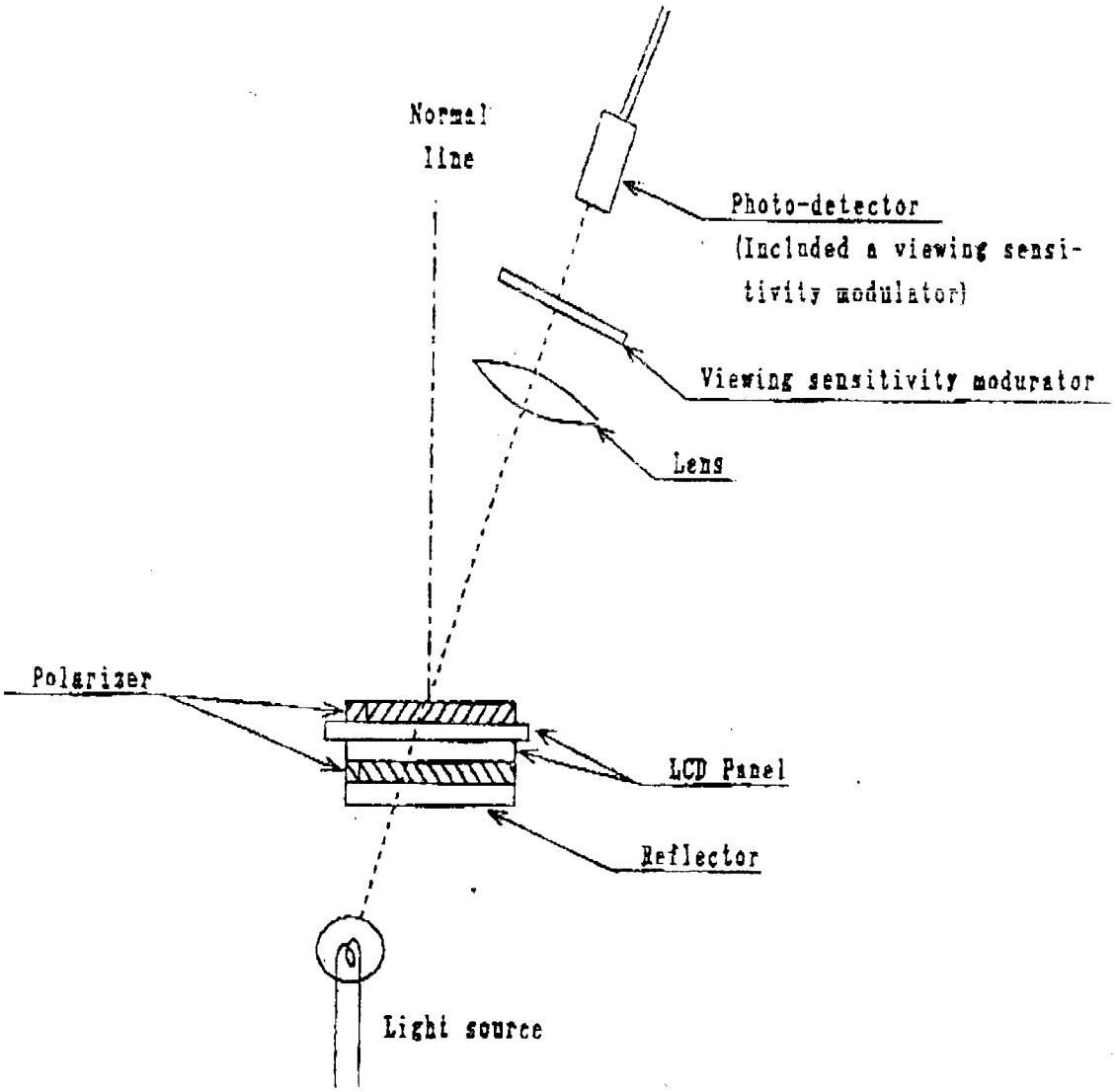
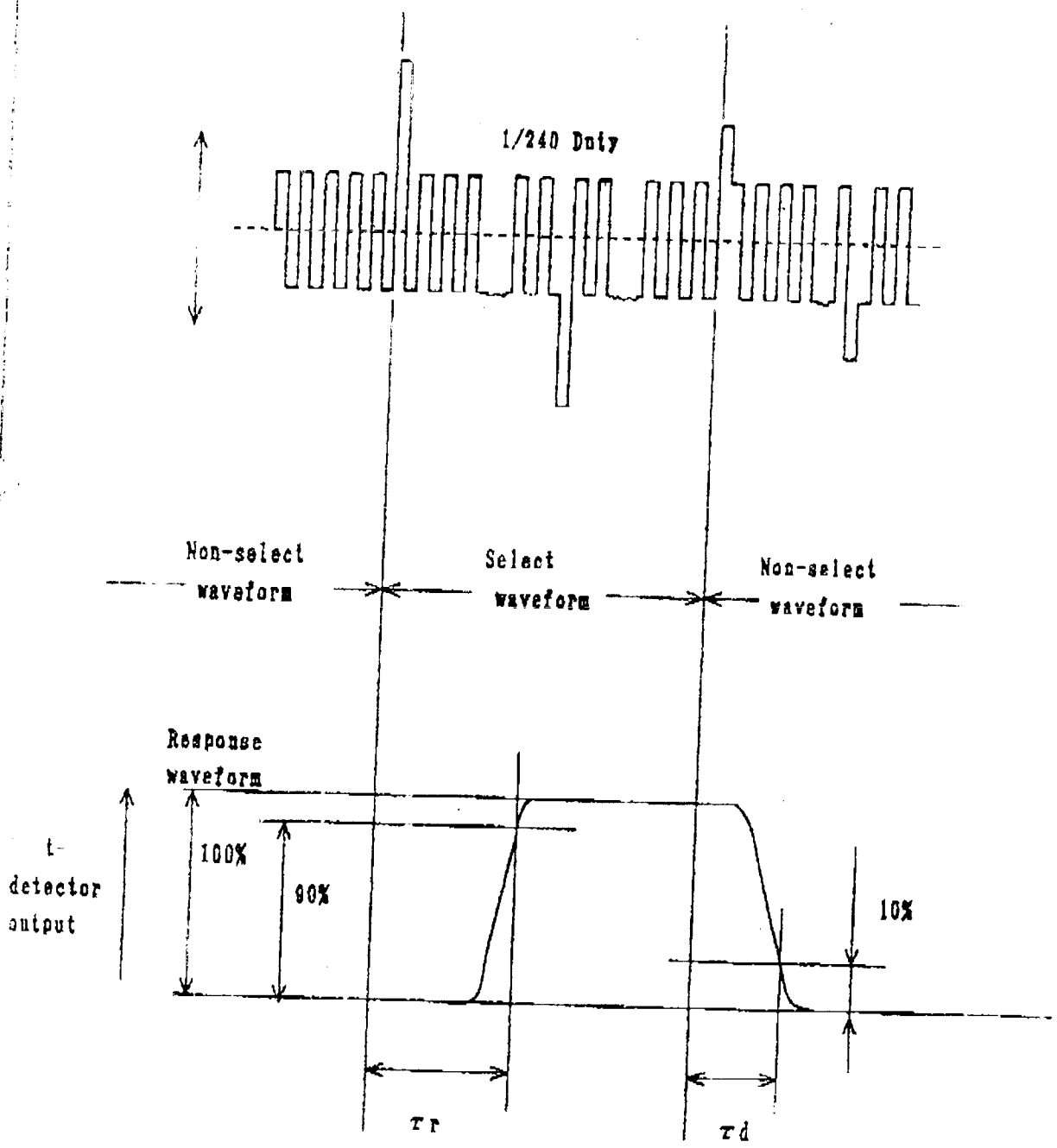


Fig. 5 Optica Characteristics Test Method

[Drive waveform]



τr: Rise time
τd: Decay time

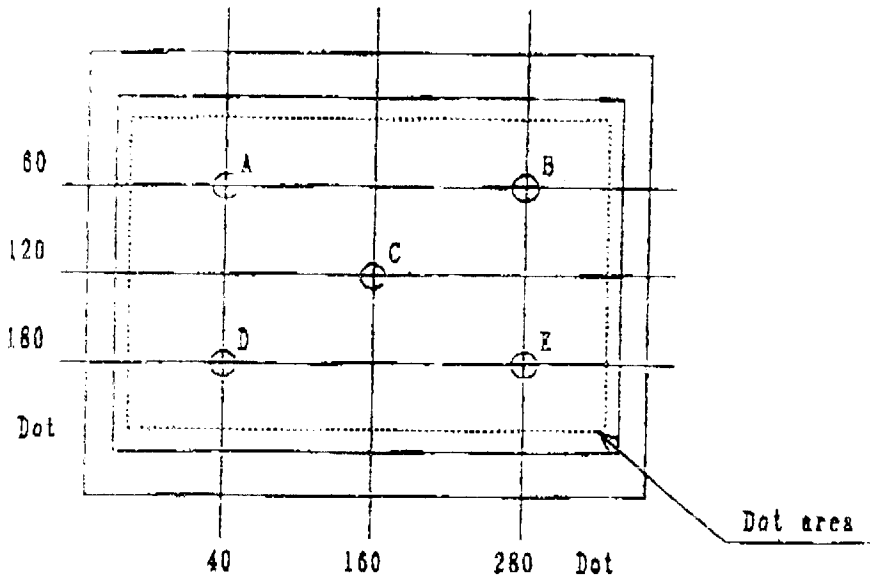
Fig. 8 Definition of Response Time

7-2. Characteristics of Backlightit

(a) Brightness

Parameter	Min.	Typ.	Max.	Unit
Brightness	60	80	—	cd/m²

Rating are defined as the average brightness at 5 measurement points.



(b) Measurement condition

CCFT inverter : LM000106

INPUT voltage : 12.0V IFT : 5mA

LCD unit Condition : LCD is full dot ON (White)
VEE=-16.0V,

Temperature : Ta=25°C, 30 minutes after turning on.

Measurement equipment : BM-7 (TOPCON Corporation)

(C) Operating life time

- The oprating life time is 10,000 hours more under the following conditions.

  CCFT inverter is

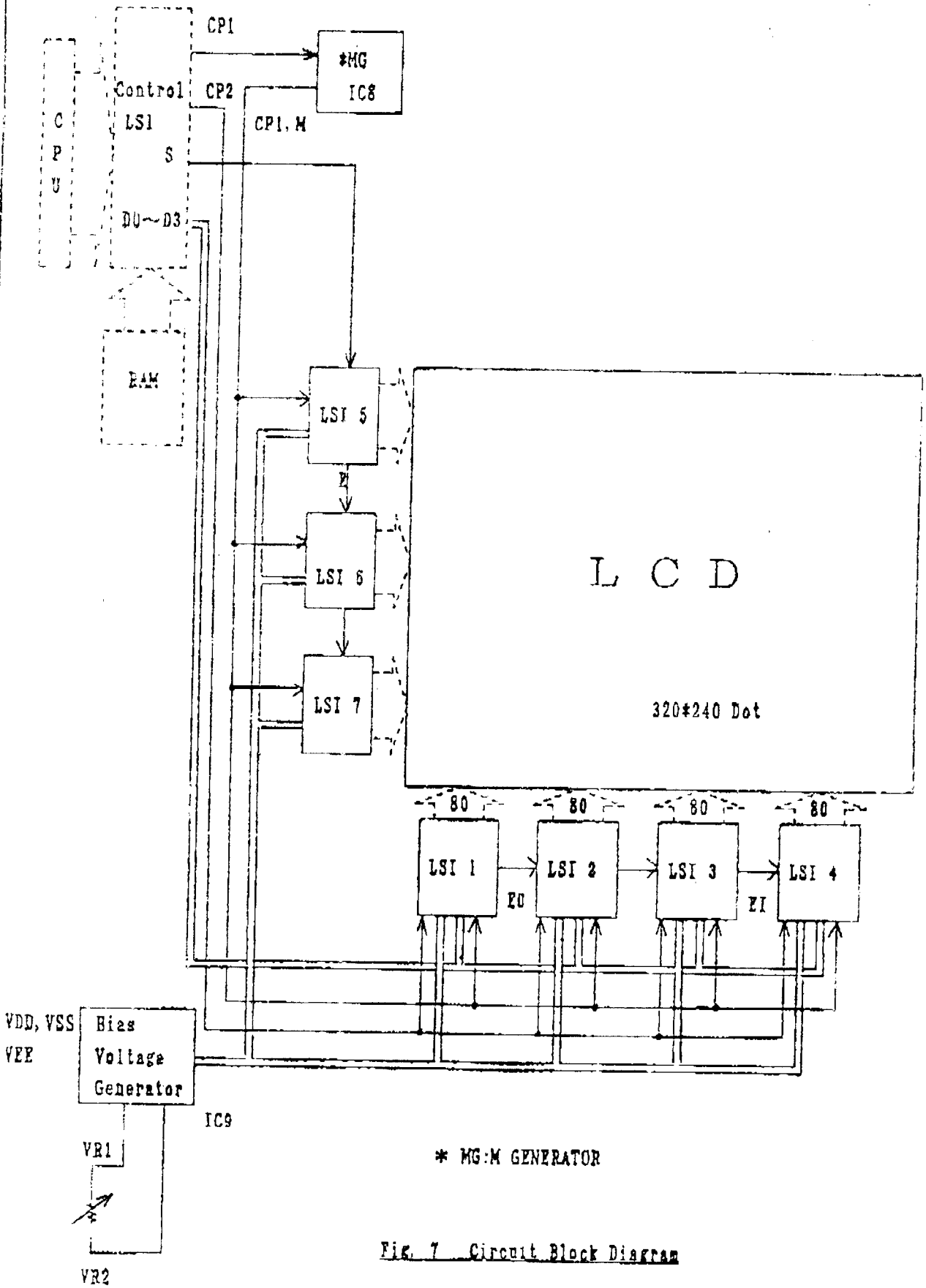
  IFT=5mArms

  Ta=25±5°C

- The operating life time is defined as having ended when any of the following conditions occur.

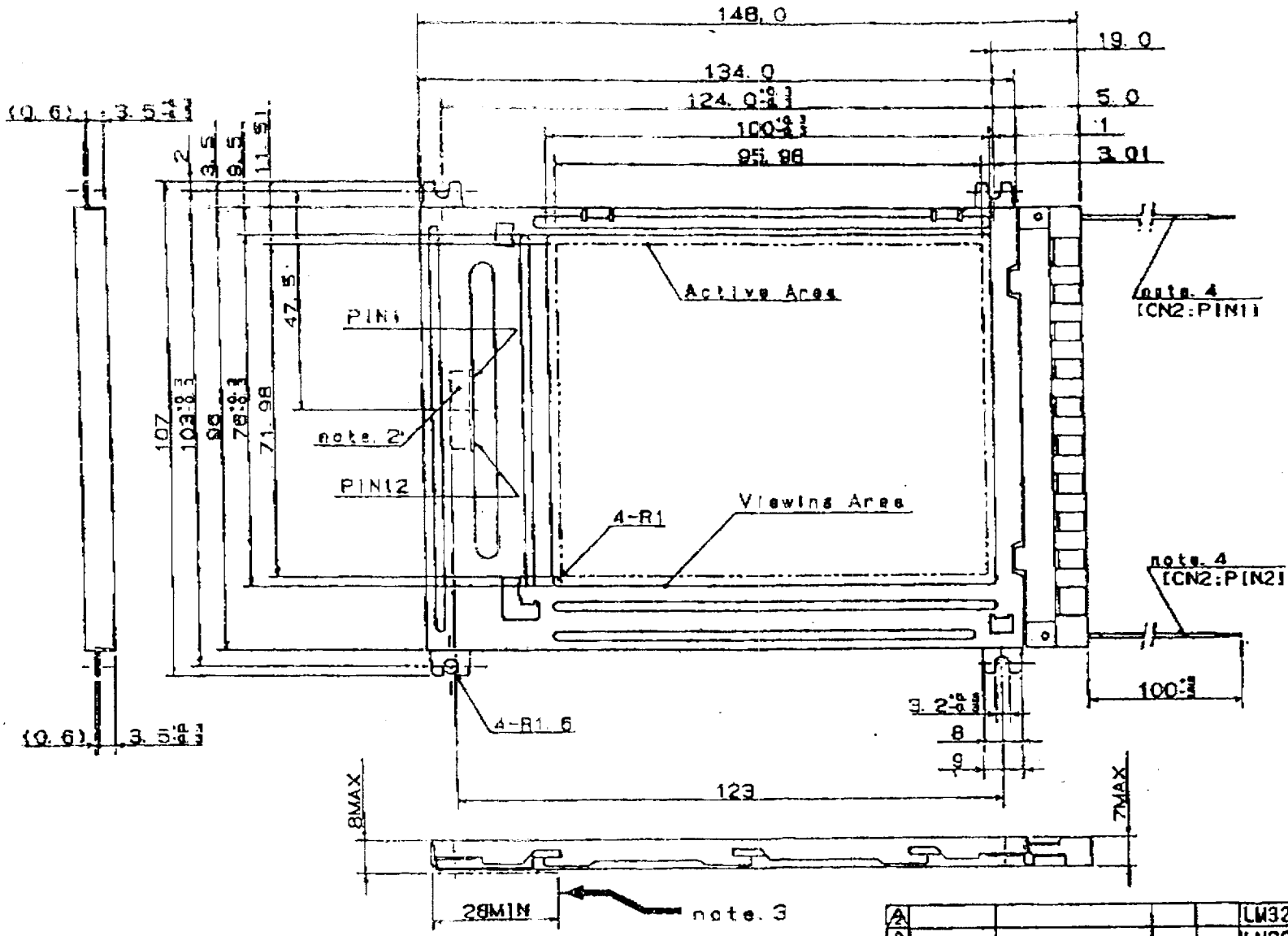
  -When the illuminence or quantity of light has decreased to 50% of the initial value.

  -When the light of CCFT goes to flicker remarkble.

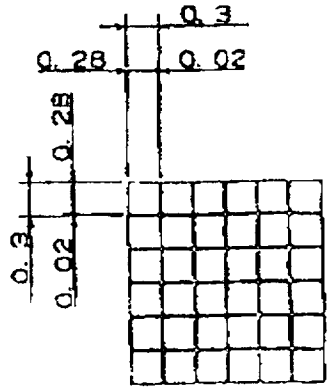


* MG:M GENERATOR

Fig. 7 Circuit Block Diagram



DOT SIZE(20/1)

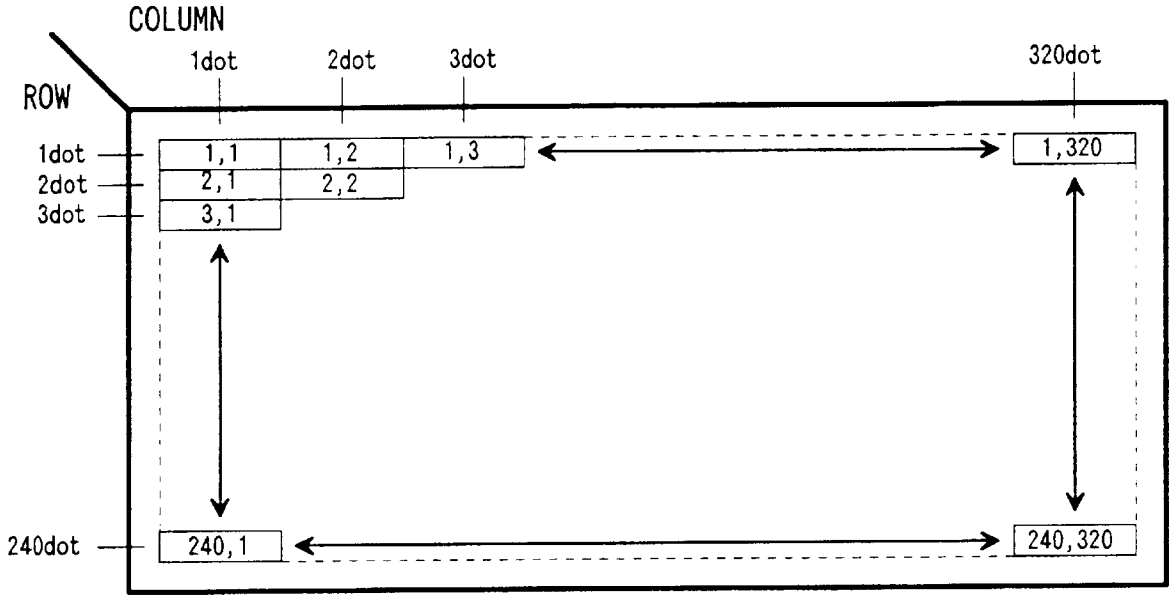


PIN NO.	SYMBOL
1	S
2	CP1
3	CP2
4	VDD
5	VSS
6	VEE
7	D0
8	D1
9	D2
10	D3
11	VR1
12	VR2

4. backlight cable: UL3239, AWG22
3. Cable is a insertion of direction.
2. Connector: 52103-1217 (Molex)
1. Be is plated by white-Zinc.

Fig. 8

MODEL	LM32P10 / LM32010P
SCALE	1/1
NAME	LCD MODULE OUTLINE DIMENSIONS
SHARP CORPORATION	1992. 7. 21.
DRAWING No.	LCD32010C



Note) 1,2 means 1st row 2nd column dot.

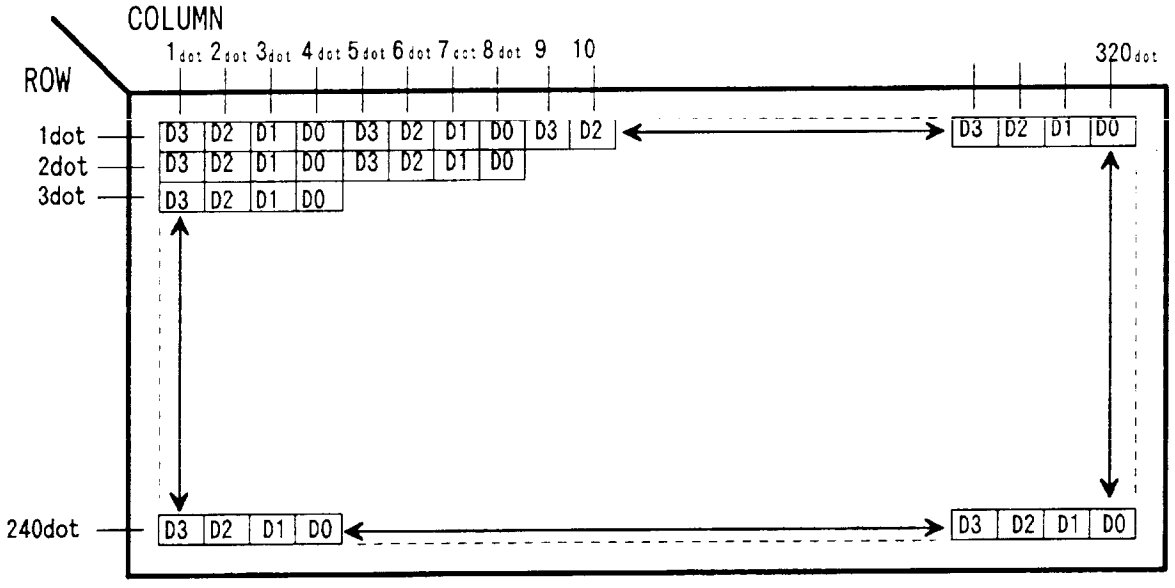


Fig. 1 Dot chart of display area

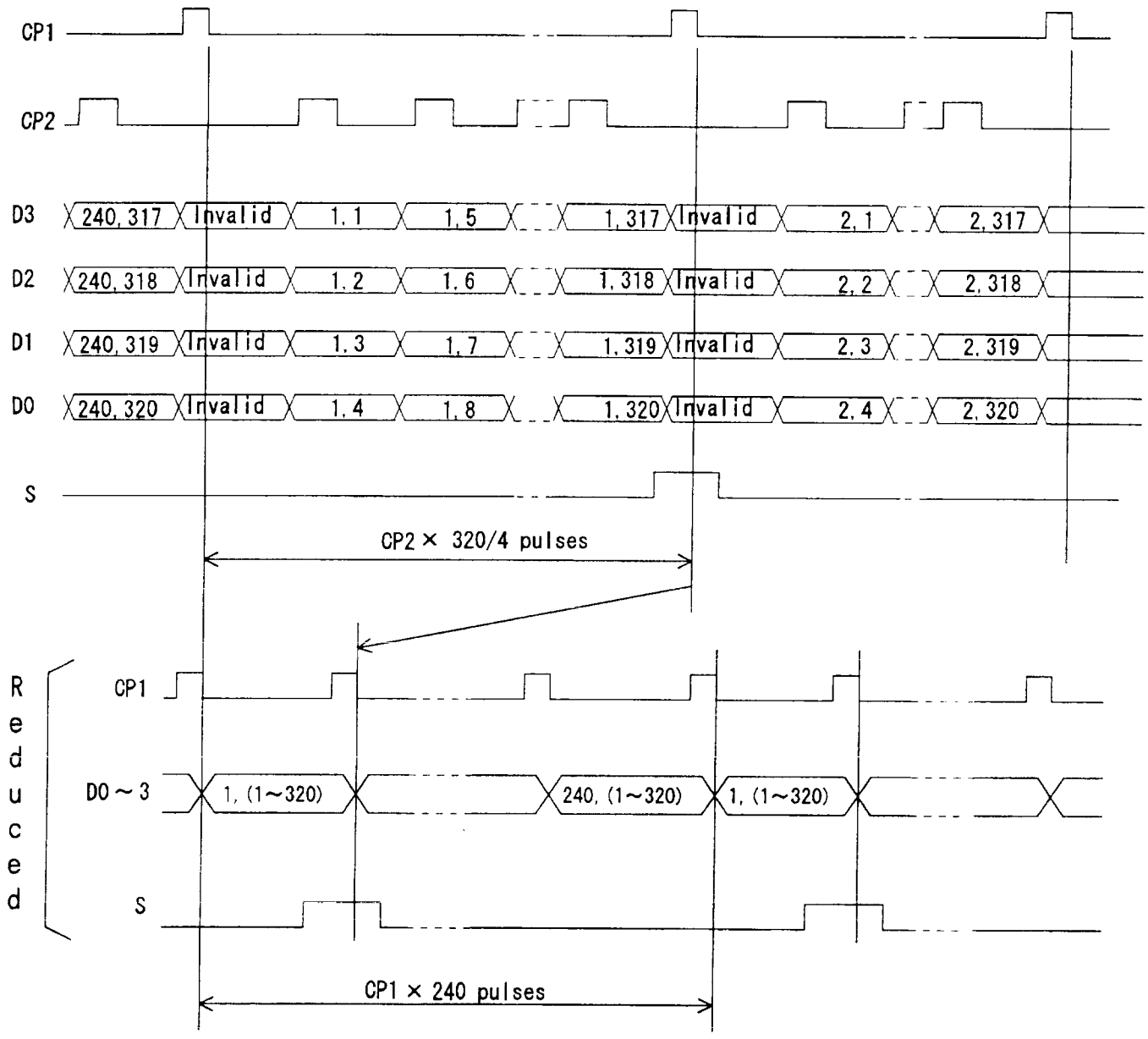


Fig. 2 Data input timing chart

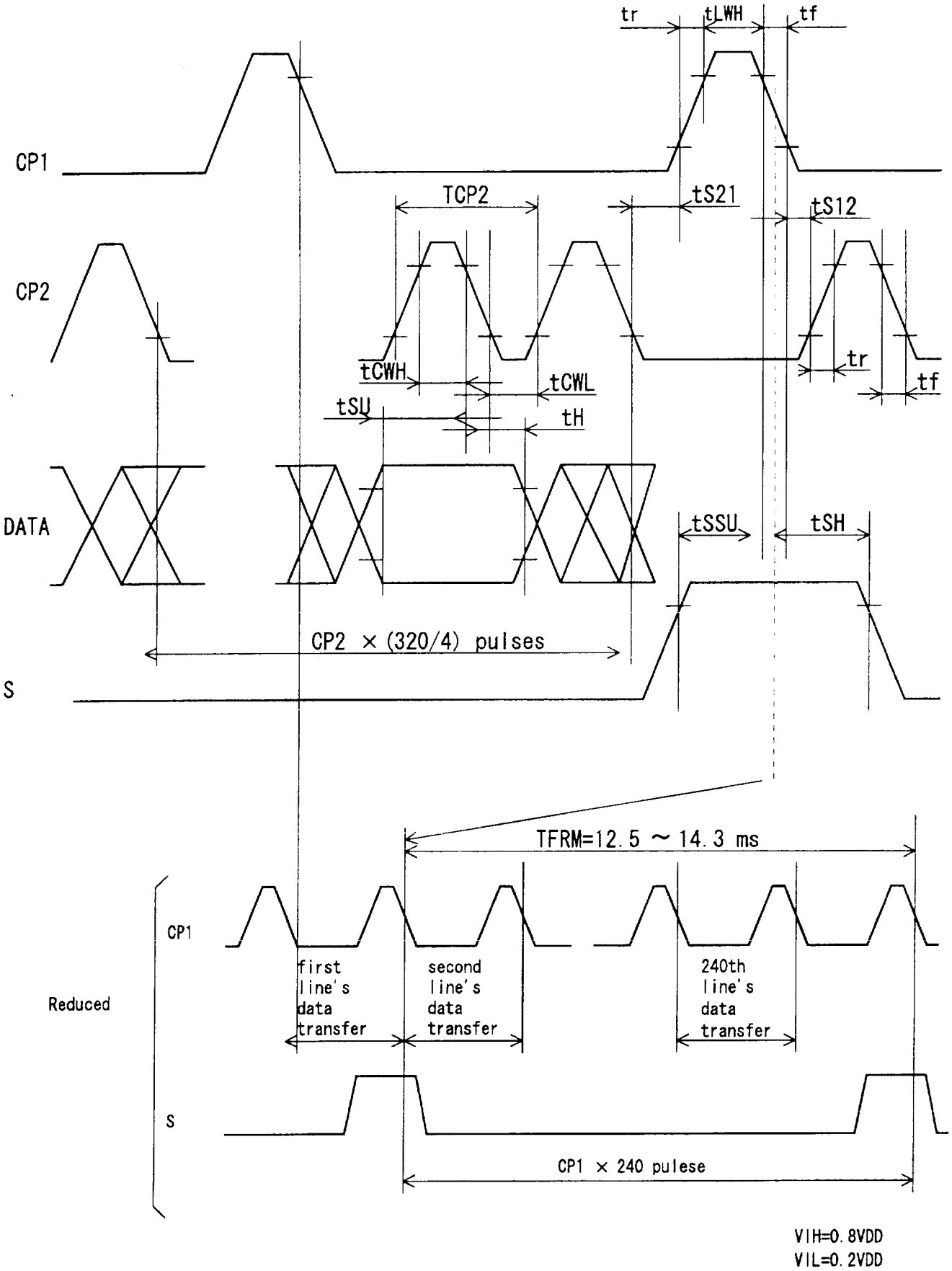


Fig.3 Interface timing chart

Table 7 Interface timing ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	TFRM	12.5	-	14.3	ms
CP2 clock cycle	TCP2	130	-	-	ns
"H" level clock width	tCWH	60	-	-	ns
"L" level clock width	tCWL	60	-	-	ns
"H" level latch clock width	tLWH	60	-	-	ns
Data set up time	tSU	50	-	-	ns
Data hold time	tSH	40	-	-	ns
CP2↑ clock allowance time from CP1↓	tS12	0	-	-	ns
CP1↑ clock allowance time from CP2↓	tS21	0	-	-	ns
Input signal rise/fall time (Note 1)	tr, tf	-	-	trf	ns
S Signal Data set up time	tSSU	40	-	-	ns
S Signal Data hold time	tSH	60	-	-	ns

Note 1) Owing to the characteristics of this LCD module, "shadowing" will become more eminent as frame frequency goes up, flicker will become more eminent as flame frequency goes down. So it is recommended that the module should be driven according to the specified limit.

Note 2)

trf=50 in case tCT=(TCP2-tCWH-tCWL)/2≧50

trf=tCT in case tCT=(TCP2-tCWH-tCWL)/2<0

5-3 Supply voltage sequence condition

The power ON/OFF sequence shown on Fig. 4 shall be followed to avoid latch-up of drive LSIs and application of DC voltage to LCD panel.

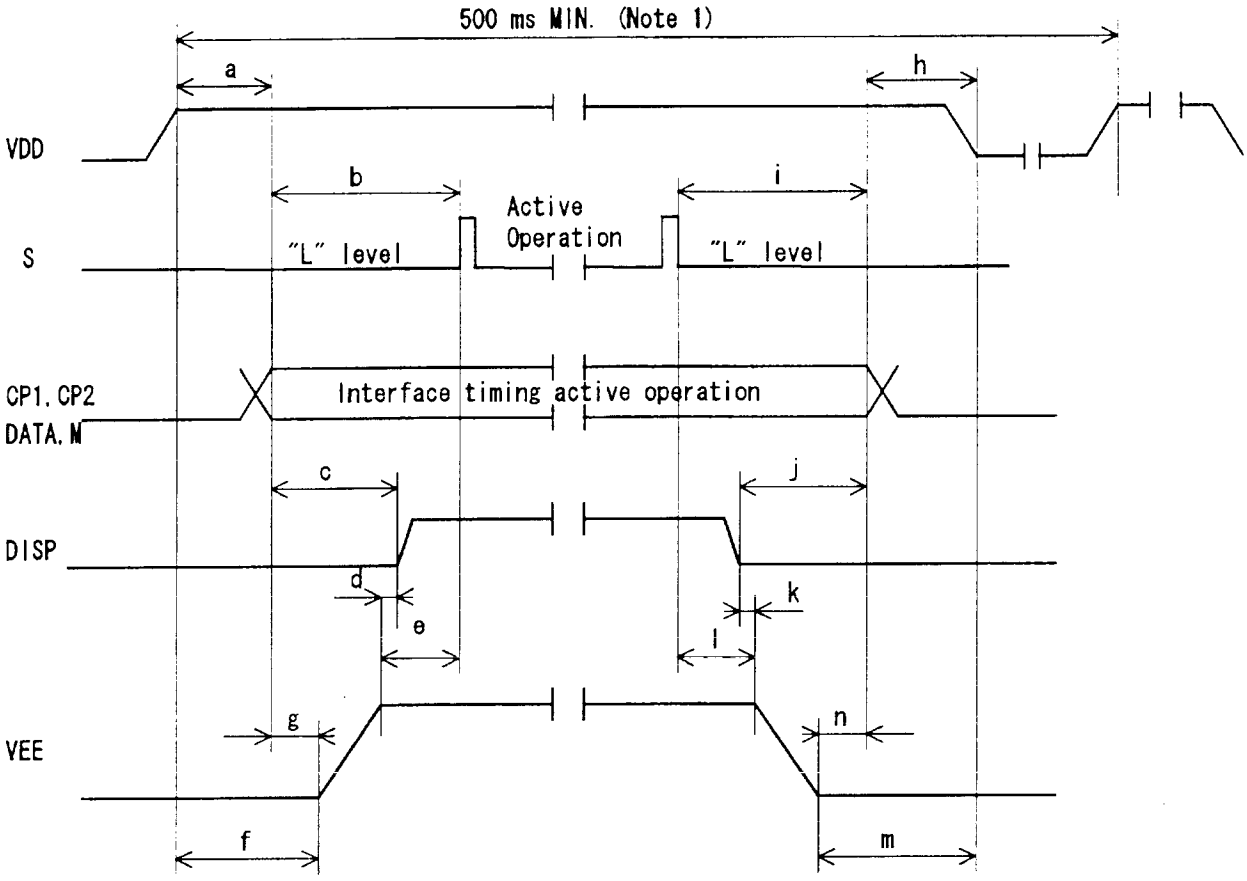


Fig. 4 Power ON/OFF sequence

Table 8 Sequence timing ratings

POWER ON		
SYMBOL	With DISP control	Without DISP control
a	0 ms MIN.	0 ms MIN. 20 ms MAX.
b	0 ms MIN.	20 ms MIN.
c	20 ms MIN.	-
d	0 ms MIN.	-
e	-	0 ms MIN.
f	0 ms MIN.	(Note 2)
g	-	20 ms MIN.

POWER OFF		
SYMBOL	With DISP control	without DISP control
h	0 ms MIN.	0 ms MIN. 20 ms MAX.
i	0 ms MIN.	20 ms MIN.
j	20 ms MIN.	-
k	0 ms MIN.	-
l	-	0 ms MIN.
m	0 ms MIN.	(Note 2)
n	-	0 ms MIN.

Note 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

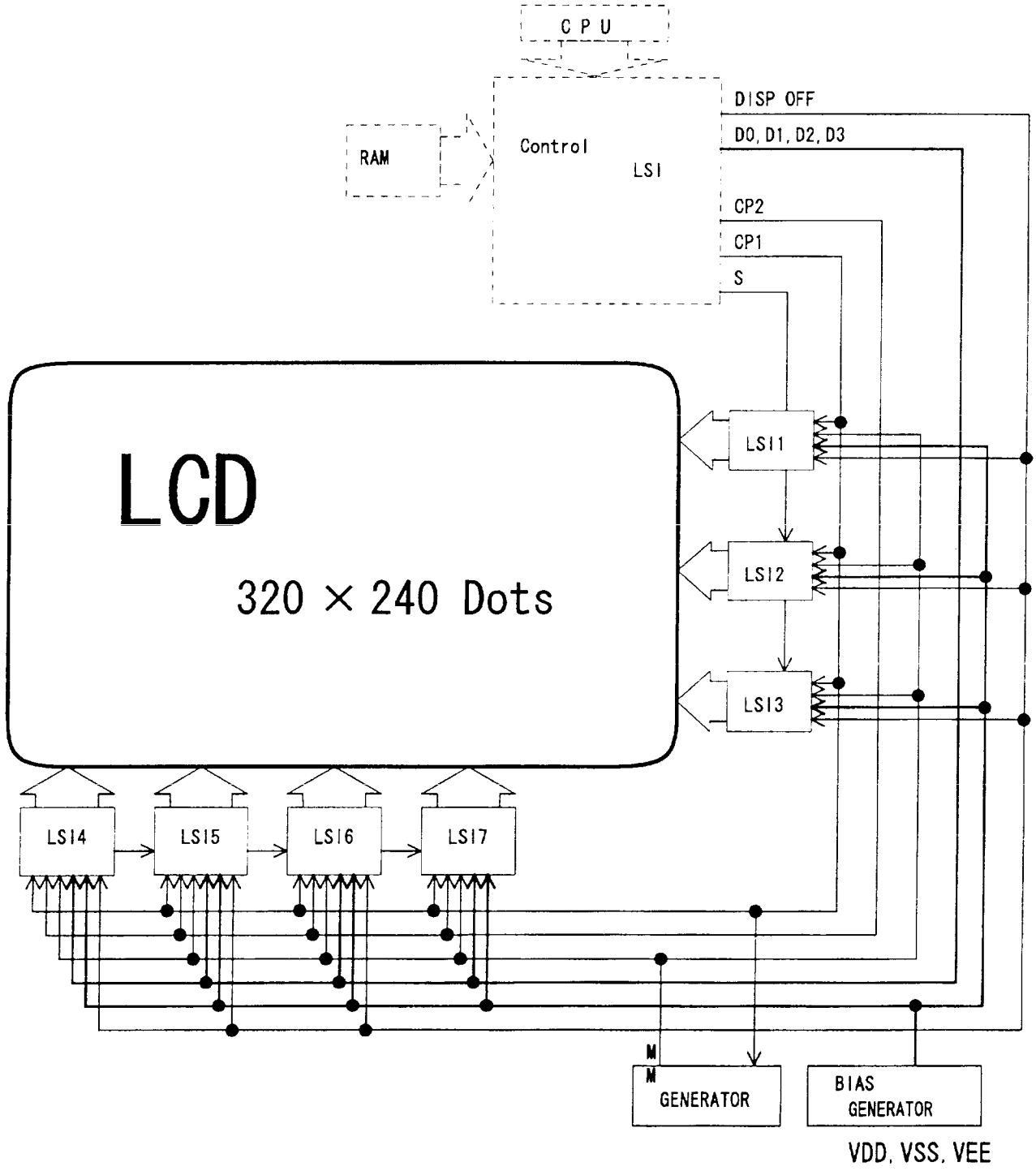
Note 2) VEE to be set at "VSS level"

6. Module driving method

6-1 Circuit configuration

Fig.5 shows the block diagram of the module's circuitry.

Fig.5 Circuit block diagram



6-2 Display face configuration

The display consists of 320×240 dots as shown in Fig.1. The interface is to be driven at 1/240 duty ratio.

6-3 Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (320 dot) will be sequentially transferred in the form of 4 bit parallel data through shift registers from top left of the display together with clock signal (CP2).

When input of one row (320 dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (CP1). Then, the corresponding drive signals will be transmitted to the 320 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (S) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 320 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 240th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

S generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such a role.