

TITLE	<h1>Application Description for DigiHeads</h1>	PAGE	1 OF 3																																																						
MODEL	<h2>AP-I2 Series</h2>	DWG NO./ VER.	<h2>JY0-62-001-SS / A</h2>																																																						
<p>1. This document is applicable to AP-I2 DigiHead Series, including all DigiHead models, in which F2F decoder chip IC2 are adopted.</p> <p>2. Terminal description</p> <table border="1" style="width: 100%; border-collapse: collapse; margin: 10px 0;"> <thead> <tr> <th style="width: 25%;">Terminal symbol</th> <th style="width: 45%;">Description</th> <th style="width: 30%;">Remarks</th> </tr> </thead> <tbody> <tr> <td><math>V_{DD}</math></td> <td>Analog positive power supply</td> <td></td> </tr> <tr> <td><math>V_{SS}</math></td> <td>Analog negative power supply</td> <td></td> </tr> <tr> <td>CPD</td> <td>Card Present Detect</td> <td></td> </tr> <tr> <td>DATA*</td> <td>Track* read data</td> <td></td> </tr> <tr> <td>CLOCK*</td> <td>Track* read clock pulse</td> <td></td> </tr> </tbody> </table> <p>Note: In this document, "*" represents for each track, for exsample CLOCK* means CLOCK-A, CLOCK-B or CLOCK-C for different tracks.</p> <p>3. Absolute maximum ratings (Non operating)</p> <table border="1" style="width: 100%; border-collapse: collapse; margin: 10px 0;"> <thead> <tr> <th style="width: 40%;">Parameter</th> <th style="width: 10%;">Symbol</th> <th style="width: 15%;">Min</th> <th style="width: 15%;">Max</th> <th style="width: 20%;">Note</th> </tr> </thead> <tbody> <tr> <td>DC supply voltage</td> <td><math>V_{DD}</math></td> <td>-0.5V</td> <td>7.0V</td> <td></td> </tr> <tr> <td>Storage temperature</td> <td><math>T_S</math></td> <td>-25°C</td> <td>75°C</td> <td></td> </tr> <tr> <td>Lead temperature</td> <td><math>T_L</math></td> <td></td> <td>260°C</td> <td></td> </tr> <tr> <td>Lead time</td> <td></td> <td></td> <td>6 sec</td> <td></td> </tr> <tr> <td>Humidity</td> <td></td> <td>10%</td> <td>95%</td> <td></td> </tr> <tr> <td>Electronic discharge</td> <td></td> <td><math>\pm 2000V</math></td> <td></td> <td>(1)</td> </tr> </tbody> </table> <p>(1) Human body mode (MIL-STD-883C Method 3015.7)</p>					Terminal symbol	Description	Remarks	$V_{DD}$	Analog positive power supply		$V_{SS}$	Analog negative power supply		CPD	Card Present Detect		DATA*	Track* read data		CLOCK*	Track* read clock pulse		Parameter	Symbol	Min	Max	Note	DC supply voltage	$V_{DD}$	-0.5V	7.0V		Storage temperature	$T_S$	-25°C	75°C		Lead temperature	$T_L$		260°C		Lead time			6 sec		Humidity		10%	95%		Electronic discharge		$\pm 2000V$		(1)
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## 4. Recommended operating conditions

Parameter	Symbol	Min	Max	Note
DC supply voltage	$V_{DD}$	3.5V	7.0V	
Operation supply current	$I_{DD}$		10mA	(1)
Stand by current	$I_{DDST}$		2.9mA	(2)
Circuit ground	$V_{SS}$	0.0V	0.0V	
Ambient temperature	$T_a$	-10°C	55°C	

(1)Supply current is exclusive of output requirement and it is measured at  $V_{DD}=5V$ .

(2)Stand by current is defined with digital pert= off, oscillator= off analog part= on at  $V_{DD}=5V$ .

## 5. DC characteristics---Digital output

## (1) Output CLOCK\* and DATA\*

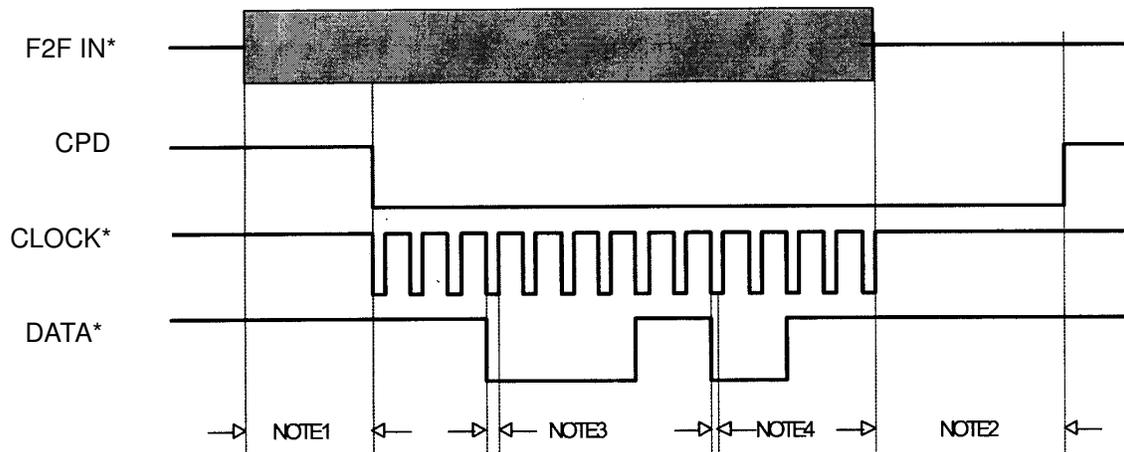
Parameter	Min	Typ	Max	Note
$V_{OH}$	4.5V			$I_{OH}=10\mu A$
$V_{OH}$	3.5V			$I_{OH}=8mA$
$V_{OL}$			0.1V	$I_{OL}=10\mu A$
$V_{OL}$			0.4V	$I_{OL}=8mA$

## (2) Output CPD (open drain)

Parameter	Min	Typ	Max	Note
$V_{OL}$			0.1V	$I_{OL}=10\mu A$
$V_{OL}$			0.4V	$I_{OL}=8mA$



## 6. Signal timing diagram



## △ CPD

CPD goes low after the 16 (17) flux reversals (default). CPD returns to high level approximately 50ms after CLOCK\*'s last transition.

## △ CLOCK\*

CLOCK\* signal indicates DATA\*'s output is valid. The DATA\* output should be loaded for further use when the CLOCK\* signal goes low. (Negative edge)

## △ DATA\*

DATA\* signal is valid when the CLOCK\* is low. If the DATA\* signal is high, the bit is zero (0). If the DATA\* signal is low, the bit is one (1).

## Note:

- (1) Programmable CPD delay for 16 or 8 flux reversals on request.
- (2) Time out of CPD signal occurs approx. 50ms (Clock=2.5Mz) after last flux transition.
- (3) Active duty cycle time is approx. 50% bit time (default). It is selectable as 25%, 50% or 75% bit time on request.
- (4) The DATA\* is valid at 3.2 $\mu$ S (min) before the negative edge of the CLOCK\*.

(END)

