

Module Instance	Base Address	Register Address
usb0	0xFFB00000	0xFFB00440
usb1	0xFFB40000	0xFFB40440

Offset: 0x440

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													prtspd RO 0x0		prttstct l RW 0x0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
prttstctl RW 0x0			prtpwr RW 0x0	prtlnst s RO 0x0		Reser ved	prtrs t RW 0x0	prtsu sp RO 0x0	prtre s RW 0x0	prtov rcurr chn g RO 0x0	prtov rcurr act RO 0x0	prten chn g RO 0x0	prten a RO 0x0	PrtCo nnDet RO 0x0	prtcnns ts RO 0x0

hprt Fields

Bit	Name	Description	Access	Reset														
18:17	prtspd	Indicates the speed of the device attached to this port. <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>High speed</td> </tr> <tr> <td>0x1</td> <td>Full speed</td> </tr> <tr> <td>0x2</td> <td>Low speed</td> </tr> <tr> <td>0x3</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Description	0x0	High speed	0x1	Full speed	0x2	Low speed	0x3	Reserved	RO	0x0				
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16:13	prttstctl	The application writes a nonzero value to this field to put the port into a Test mode, and the corresponding pattern is signaled on the port. <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Test mode disabled</td> </tr> <tr> <td>0x1</td> <td>Test_J mode</td> </tr> <tr> <td>0x2</td> <td>Test_K mode</td> </tr> <tr> <td>0x3</td> <td>Test_SE0_NAK mode</td> </tr> <tr> <td>0x4</td> <td>Test_Packet mode</td> </tr> <tr> <td>0x5</td> <td>Test_force_Enable</td> </tr> </tbody> </table>	Value	Description	0x0	Test mode disabled	0x1	Test_J mode	0x2	Test_K mode	0x3	Test_SE0_NAK mode	0x4	Test_Packet mode	0x5	Test_force_Enable	RW	0x0
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