

ISE Project Navigator

Processes: 📢 🧭 Generate Programming File 🖹 🕑 Programming File Gene Rerun Generate PROM, ACE, Configure Device (iMP/ 📲 Rerun All Stop Ľ 2 📲 🖞 Processes ating Open Withor Properties... UG332_c1_04_120306

Figure 1-5 shows how to set options for the Bitstream Generator from within the ISE

Figure 1-5: Setting Bitstream Generator Options from ISE Project Navigator

- 1. Right-click Generate Programming File.
- 2. Click Properties.

Project Navigator window.

🔤 Process Properties		×	
<u>Category</u>	3		
General Options	General Options		
	Property Name	Value	
	Run Design Rules Checker (DRC)	V	
	Create Bit File	V	
	Create Binary Configuration File		
	Create ASCII Configuration File		
	Create IEEE 1532 Configuration File		
	Enable BitStream Compression	₽ Ň	
	Enable Debugging of Serial Mode BitStream		5
	Enable Cyclic Redundancy Checking (CRC)		
	Other Bitgen Command Line Options		-
	Property display level: Advanced	<u>D</u> efault	
ОК	Cancel <u>Apply</u>	<u>H</u> elp	

Figure 1-6: Bitstream Generator General Options



- 3. Click General Options, as shown in Figure 1-6.
- 4. To compress the FPGA bitstream, check Enable BitStream Compression.
- 5. To enter specific bitstream generator command-line options that are not already supported by the graphical interface, enter the option strings in the space provided.

Category Configuration Options Configuration Options Configuration Options Category Configuration Options Configuration Options Configuration Options Configuration Options Configuration	6 Configuration O	ptions	I
	Property Name	Value	7/
	Configuration Rate	17 💌	
	Configuration Pin Program	Pull Up 📃 🔪	8
	Configuration Pin Done	Pull Up 🖃	
	JTAG Pin TCK	Pull Up 🔄 🔪	9/
	JTAG Pin TDI	Pull Up 📃	
	JTAG Pin TDO	Pull Up 📃 🔪	
	JTAG Pin TMS	Pull Up 💌	
	Unused IOB Pins	Pull Down 💌	
	UserID Code (8 Digit Hexadecimal) 0x01234567		11
	Property display level: Advanced	Default	
ОК	Cancel <u>Apply</u>		/1.

Figure 1-7: Bitstream Generator Configuration Options

- 6. Click **Configuration Options**, as shown in Figure 1-7.
- 7. If using one of the Master configuration modes, set the CCLK **Configuration Rate** frequency. This setting is not used for Slave mode configuration. The specific setting depends on the specific FPGA family, the attached configuration memory, and the configuration mode. Specific values are recommended in later chapters, depending on the speed of the attached memory.
- 8. The FPGA's DONE and PROG_B (Program) pins each have a dedicated pull-up resistor during configuration. These resistors become optional after configuration. The specific example is from a Spartan-3E FPGA application. Spartan-3 and Spartan-3A FPGAs have additional options.
- 9. The FPGA's JTAG pins each have a dedicated pull-up resistor during configuration. These resistors become optional after configuration.
- 10. By default, unused I/O blocks are configured as inputs with a pull-down resistor. Other options are available. See *UnusedPin* bitstream option.
- 11. Each FPGA bitstream can include an 8-digit hexadecimal (32-bit) identifier that can be read via the FPGA's JTAG port.



ategory General Options Configuration Options Startup Options	12 Startup Optio	ons
	Property Name	Value
	FPGA Start-Up Clock	CCLK 👤
	Enable Internal Done Pipe	
	Done (Output Events)	Default (4)
	Enable Outputs (Output Events)	Default (5)
	Release Write Enable (Output Events Release DLL (Output Events)	Default (6) 🔄 📝
		Default (NoWait) 💌
	Drive Done Pin High	
	Property display level: Advanced	
	OK Cancel Apply	<u>H</u> elp

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- 12. Click Startup Options, as shown in Figure 1-8.
- 13. After the FPGA configuration bitstream is loaded into the FPGA, the FPGA enters its Startup phase. The timing of each Startup cycle is controlled by a selectable clock source. See "Startup Clock Source," page 235.
- 14. The Startup phase of FPGA configuration provides six different cycles to synchronize the following startup events. The event can be assigned to a specific cycle or be synchronized to the DONE signal. See "Startup," page 233.
 - The timing of when output drivers are enabled
 - The timing of when the write-protect lock is removed from writable clocked elements
 - The timing of when the DONE pin goes active.
- 15. If the DCM_WAIT=TRUE attribute is set on a Digital Clock Manager (DCM) within the FPGA, the FPGA optionally waits for the Delay-Locked Loop (DLL) within the DCM to lock to the incoming clock signal before finishing configuration. See "Waiting for DCMs to Lock, DCI to Match," page 235.
- 16. The FPGA's DONE pin can actively drive High after configuration. This option should only be set for single-FPGA applications or for the last FPGA in a multi-FPGA configuration daisy chain. See "DONE Pin," page 36.

Category General Options Configuration Options Startup Options Readback Options	Readback	⊠ Options
	Property Name	Value 18
	Security	Disable Readback 💌
	Create ReadBack Data Files	
	Allow SelectMAP Pins to Persist	Γ
	Create Logic Allocation File	Γ
	Create Mask File	Γ
	Prot 19 Jay level: Advan	ced <u>D</u> efault
OK	Cancel <u>A</u> r	pply <u>H</u> elp



- 17. Click **Readback Options**, as shown in Figure 1-9.
- 18. By default, FPGA bitstreams can be read back via JTAG. Other options exist to disable FPGA readback. See "Basic FPGA Hardware-Level Security Options," page 273.
- 19. Click OK when finished.



Pin 2 of the connector provides a reference voltage for the output buffers that drive the TDI, TCK, and TMS pins. Because these pins are powered by V_{CCAUX} on Spartan-3 Generation FPGAs, connect the V_{CCAUX} supply to pin 2 of the connector.

Programming an FPGA Using JTAG

The JTAG interface is also a convenient means for downloading an FPGA design during development and debugging.

First, generate an FPGA bitstream as described in "Setting Bitstream Options, Generating an FPGA Bitstream," page 27

The following steps graphically describe how to create a PROM file using iMPACT from within the ISE Project Navigator. This particular example shows how to configure the XC3S500E FPGA on the <u>Spartan-3E Starter Kit</u> board. Besides the FPGA, the JTAG chain on the board includes a Xilinx Platform Flash PROM and a Xilinx CPLD.

1. From within the ISE Project Navigator, double-click **Configure Device (iMPACT)** from the Processes pane, as shown in Figure 9-7.

Processes:	<u> </u>
	nerate Programming File Programming File Generation Report Generate PROM_ACE_or_ITAG File
	Configure Device (iMPACT)
	es

Figure 9-7: Double-click Configure Device (iMPACT)

2. As shown in Figure 9-8, select Configure devices using Boundary-Scan (JTAG).

	IMPACT - Welcome to IMPACT		
	Please select an action from the list below		
	Configure devices using Boundary-Scan (JTAG)		
·	Automatically connect to a cable and identify Boundary-Scan chair 💽 🗡		
	Prepare a PROM File		
	Prepare a System ACE File		
	C Prepare a Boundary-Scan File		
	C Configure devices		
	using Slave Serial mode		
	< Back Finish Cancel		
	< Back Finish Cancel		

Figure 9-8: Configure Devices Using JTAG

- 3. If the board is powered and the Xilinx programming cable properly connected, the iMPACT software automatically initializes the JTAG chain and detects the various devices on the chain.
- 4. Click Finish.
- 5. As shown in Figure 9-9, the iMPACT software automatically detected the devices on the chain. In this example, a Xilinx XC3S500E Spartan-3E FPGA is first in the chain, followed by a Xilinx XCF04S Platform Flash PROM, followed by a Xilinx XC2C64A CPLD in the final position. The devices are yet unprogrammed.





- 6. As shown in Figure 9-10, the iMPACT software automatically prompts for the FPGA bitstream. Select the desired bitstream to download specifically to the FPGA.
- 7. Click Open.



	Same and the second sec	? ×
	Look in: 🔄 C:/Data/my_designs/S3E_Simple/ 💽 🖛	t 💣 🔝 🏢
	_ngo	
	🗀 _xmsgs	
6		7
	MyFPGA.bit	
	File name: MyFPGA.bit	<u>O</u> pen
	File type: All Design Files (*.bit *.rbt *.nky *.isc *.bsd) 💌	Cancel
	Cancel <u>A</u> ll	<u>B</u> ypass
		UG332 c9 09 112006

Figure 9-10: iMPACT Prompts for FPGA Bitstream

8. As shown in Figure 9-11, the iMPACT software automatically detects that the FPGA bitstream was generated for a non-JTAG configuration method. The iMPACT software automatically adjusts the Startup clock setting for successful JTAG configuration (*StartupClk:JtagClk*). The original bitstream file is unaffected.

🖳 Warni	ing X
<u>.</u>	WARNING: IMPACT: 2257 - Startup Clock has been changed to 'JtagClk' in the bitstream stored in memory, but the original bitstream file remains unchanged.
	UG332 c9 09 112006

Figure 9-11: iMPACT Automatically Adjusts FPGA Startup Clock for JTAG Configuration

9. For faster downloading and a shorter FPGA debugging cycle, there is no need to program the Platform Flash PROM or CPLD unless actually desired. To skip programming the Platform Flash PROM, click Bypass, as shown in Figure 9-12.

Assign New Configuration File
Look jn: 🔄 C:/Data/my_designs/S3E_Simple/ 💽 🗲 🗈 📸 🏢
<u></u>
🚞 xst 📾 MuPlatformElash mos
File <u>n</u> ame: Upen
File type: All Design Files (*.mcs *.exo *.isc *.bsd) 🔽 Cancel
UG332_c9_10_112006

Figure 9-12: Click Bypass to Skip Platform Flash Programming

10. Similarly, click Bypass to skip programming of the CPLD, as shown in Figure 9-13.

Assign New Configuration File	<
Look in: 🔄 C:/Data/my_designs/S3E_Simple/ 💽 🗲 🗈 📸 🇱	
ngo	
📥initigu	
MyPlatformFlash.mcs	
File <u>n</u> ame:	
File type: All Design Files (*.mcs *.exo *.isc *.bsd) 💌 Cancel	
Cancel <u>A</u> ll <u>Bypass</u>	
	<u> </u>

Figure 9-13: Click Bypass to Skip CPLD Programming

11. As shown in Figure 9-14, the iMPACT software updates the display, showing the files assigned to each device in the JTAG chain. In this example, the XCF04S Platform Flash and XC2C64A CPLD are "bypassed" and are not programmed. Click the FPGA to highlight it on the display.





Figure 9-14: Double-Click Program to Configure FPGA via JTAG

- 12. Once the FPGA is highlighted, the associated **Available Operations** are enabled on the display. Double-click **Program**.
- 13. The Programming Properties dialog box appears, as shown in Figure 9-15.

Programming Properties	×
Category	
13 Programming Properties Advanced PROM Programming Properties Bevision Properties	Programming Properties General Programming Properties
14	C Verify
	General CPLD And PROM Properties
	🗖 Erase Before Programming 🗖 Read Protect
	CoolRunner-II Usercode (8 Hex Digits)
	OK Cancel Apply Help
	LIG332 cg 13 112006

Figure 9-15: FPGA Programming Options

- 14. The iMPACT software provides a **Verify** feature, even for FPGA programming. Typically, the Verify function is not used when downloading the FPGA for debugging purposes.
- 15. Click OK to start the programming process.
- 16. The iMPACT software indicates when programming is complete, as shown in Figure 9-14. The iMPACT software also forces the FPGA to reconfigure on the board. The FPGA is downloaded with the specified FPGA bitstream.