ISE Project Navigator

Figure 1-5 shows how to set options for the Bitstream Generator from within the ISE Project Navigator window.

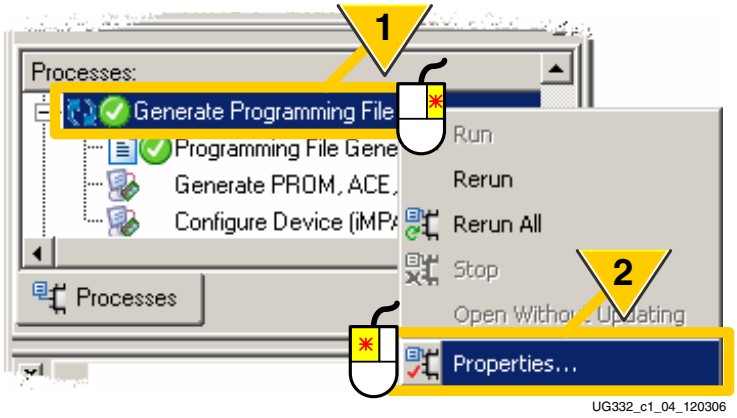

Figure 1-5: **Setting Bitstream Generator Options from ISE Project Navigator**

1. Right-click **Generate Programming File**.
2. Click **Properties**.

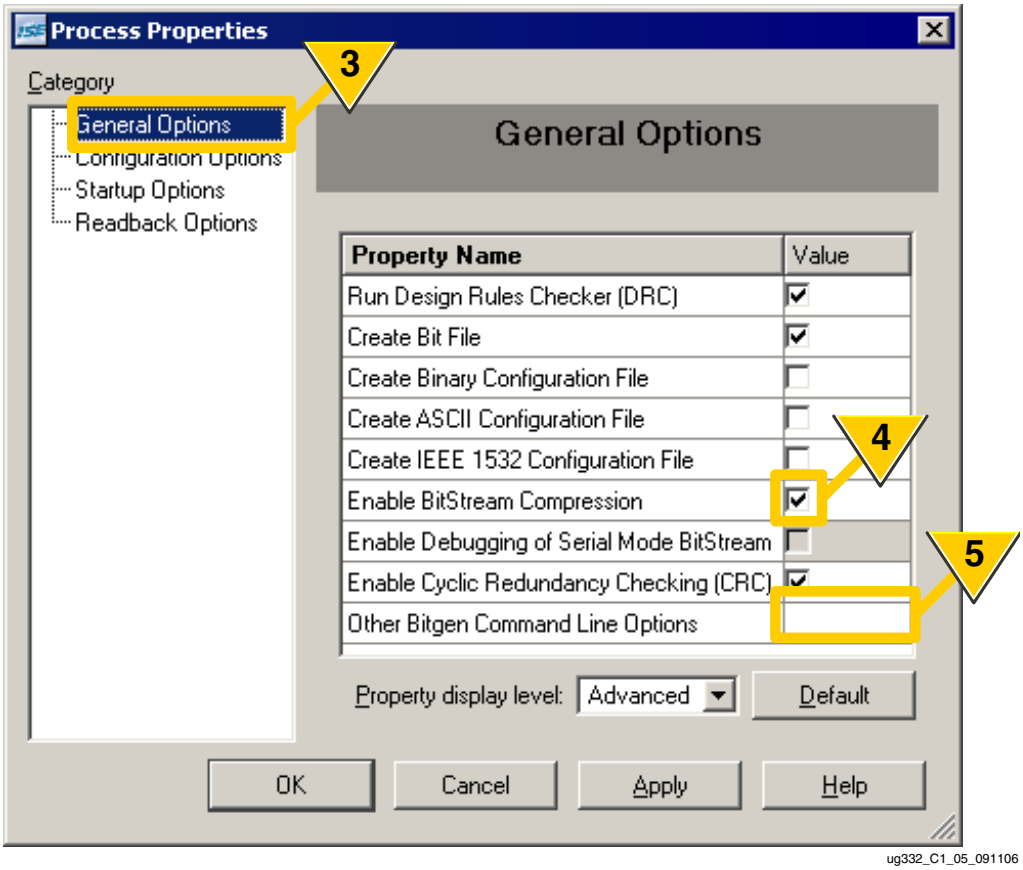

Figure 1-6: **Bitstream Generator General Options**

3. Click **General Options**, as shown in Figure 1-6.
4. To compress the FPGA bitstream, check **Enable BitStream Compression**.
5. To enter specific bitstream generator command-line options that are not already supported by the graphical interface, enter the option strings in the space provided.

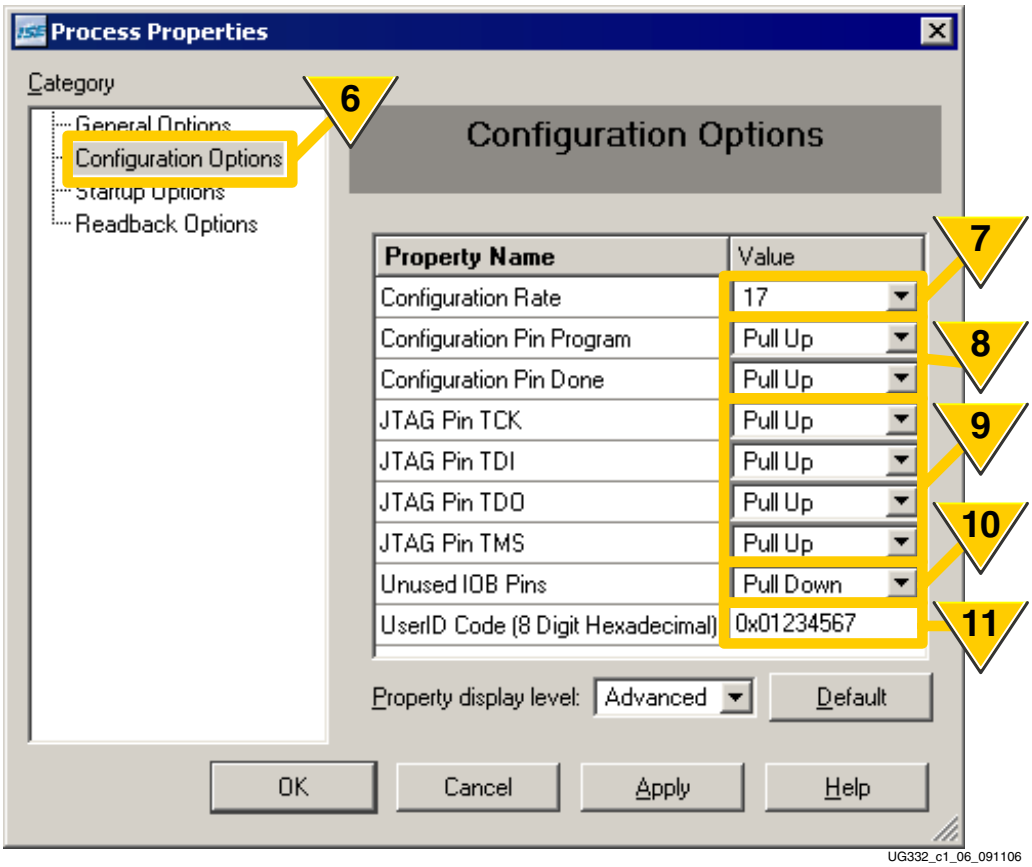

Figure 1-7: **Bitstream Generator Configuration Options**

6. Click **Configuration Options**, as shown in Figure 1-7.
7. If using one of the Master configuration modes, set the CCLK **Configuration Rate** frequency. This setting is not used for Slave mode configuration. The specific setting depends on the specific FPGA family, the attached configuration memory, and the configuration mode. Specific values are recommended in later chapters, depending on the speed of the attached memory.
8. The FPGA's DONE and PROG_B (Program) pins each have a dedicated pull-up resistor during configuration. These resistors become optional after configuration. The specific example is from a Spartan-3E FPGA application. Spartan-3 and Spartan-3A FPGAs have additional options.
9. The FPGA's JTAG pins each have a dedicated pull-up resistor during configuration. These resistors become optional after configuration.
10. By default, unused I/O blocks are configured as inputs with a pull-down resistor. Other options are available. See ***UnusedPin*** bitstream option.
11. Each FPGA bitstream can include an 8-digit hexadecimal (32-bit) identifier that can be read via the FPGA's JTAG port.

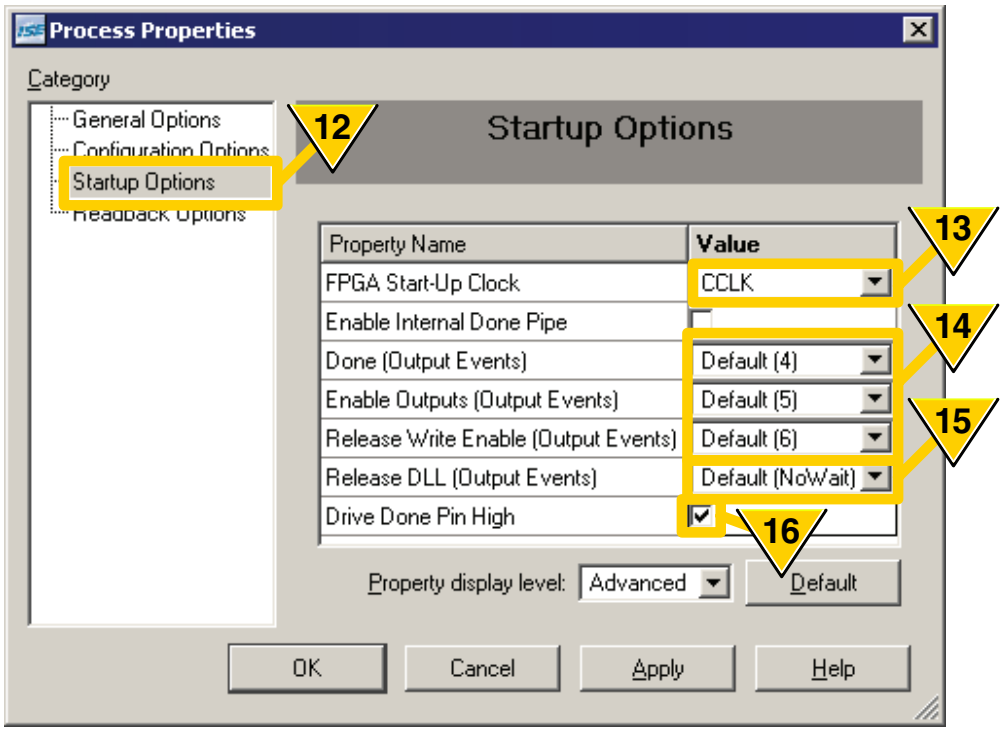

Figure 1-8: **Bitstream Generator Startup Options**

12. Click **Startup Options**, as shown in Figure 1-8.
13. After the FPGA configuration bitstream is loaded into the FPGA, the FPGA enters its Startup phase. The timing of each Startup cycle is controlled by a selectable clock source. See "Startup Clock Source," page 235.
14. The Startup phase of FPGA configuration provides six different cycles to synchronize the following startup events. The event can be assigned to a specific cycle or be synchronized to the DONE signal. See "Startup," page 233.
    - The timing of when output drivers are enabled
    - The timing of when the write-protect lock is removed from writable clocked elements
    - The timing of when the DONE pin goes active.
15. If the DCM_WAIT=TRUE attribute is set on a Digital Clock Manager (DCM) within the FPGA, the FPGA optionally waits for the Delay-Locked Loop (DLL) within the DCM to lock to the incoming clock signal before finishing configuration. See "Waiting for DCMs to Lock, DCI to Match," page 235.
16. The FPGA's DONE pin can actively drive High after configuration. This option should only be set for single-FPGA applications or for the last FPGA in a multi-FPGA configuration daisy chain. See "DONE Pin," page 36.

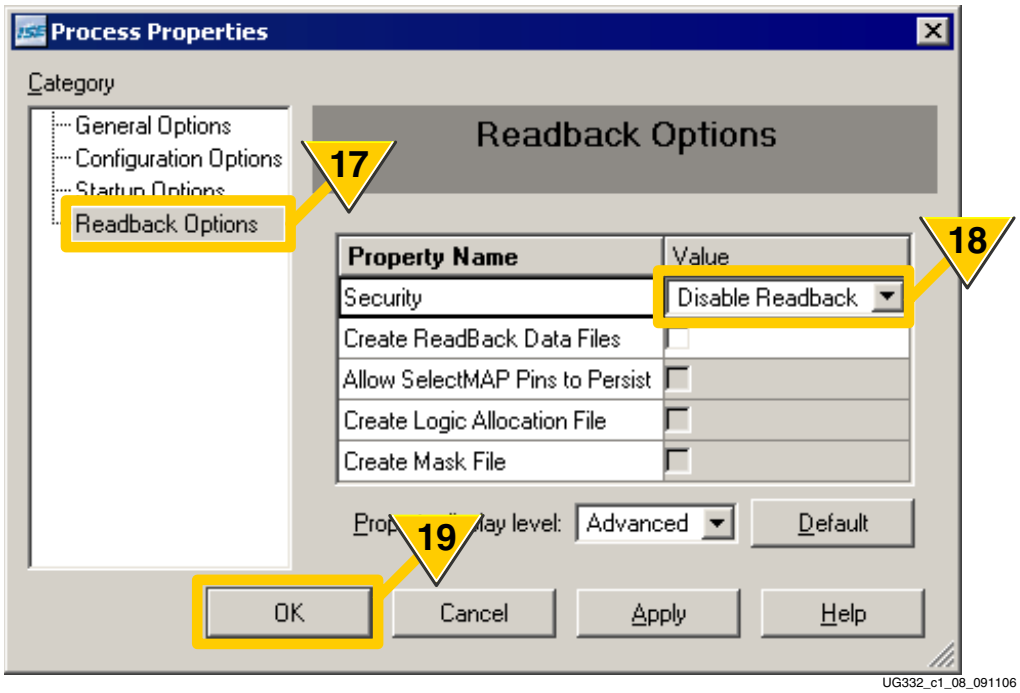

Figure 1-9: **Bitstream Generator Readback Options**

17. Click **Readback Options**, as shown in Figure 1-9.
18. By default, FPGA bitstreams can be read back via JTAG. Other options exist to disable FPGA readback. See "Basic FPGA Hardware-Level Security Options," page 273.
19. Click **OK** when finished.

Pin 2 of the connector provides a reference voltage for the output buffers that drive the TDI, TCK, and TMS pins. Because these pins are powered by V_{CCAUX} on Spartan-3 Generation FPGAs, connect the V_{CCAUX} supply to pin 2 of the connector.

Programming an FPGA Using JTAG

The JTAG interface is also a convenient means for downloading an FPGA design during development and debugging.

First, generate an FPGA bitstream as described in "Setting Bitstream Options, Generating an FPGA Bitstream," page 27

The following steps graphically describe how to create a PROM file using iMPACT from within the ISE Project Navigator. This particular example shows how to configure the XC3S500E FPGA on the Spartan-3E Starter Kit board. Besides the FPGA, the JTAG chain on the board includes a Xilinx Platform Flash PROM and a Xilinx CPLD.

1. From within the ISE Project Navigator, double-click **Configure Device (iMPACT)** from the Processes pane, as shown in Figure 9-7.

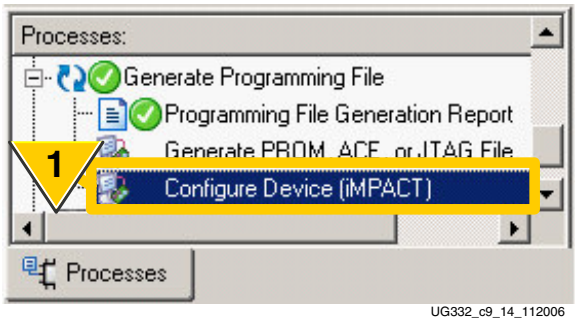

Figure 9-7: **Double-click Configure Device (iMPACT)**

2. As shown in Figure 9-8, select **Configure devices using Boundary-Scan (JTAG)**.

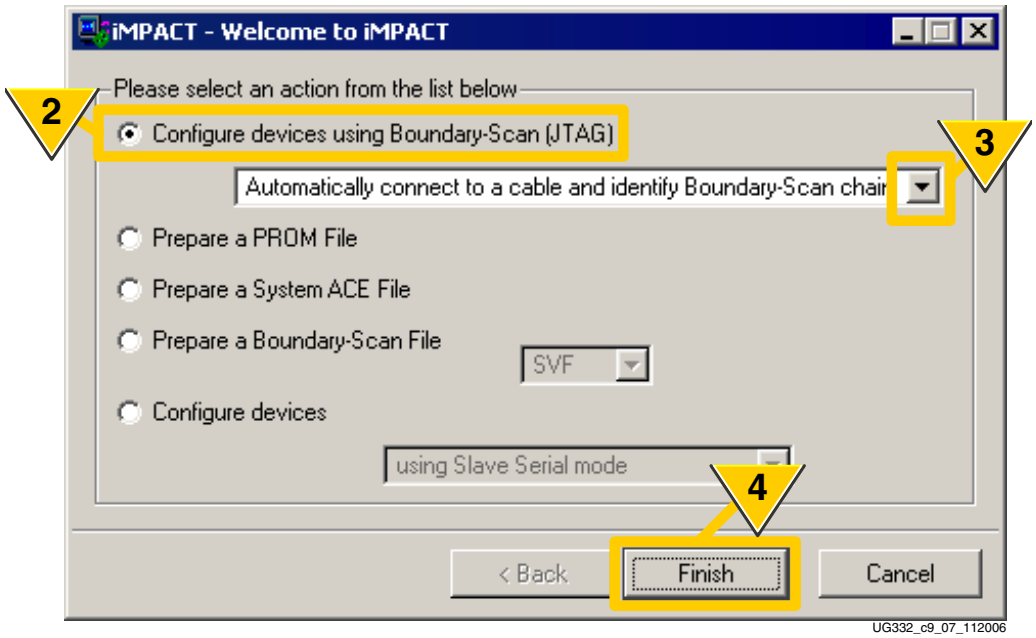

Figure 9-8: **Configure Devices Using JTAG**

3. If the board is powered and the Xilinx programming cable properly connected, the iMPACT software automatically initializes the JTAG chain and detects the various devices on the chain.
4. Click **Finish**.
5. As shown in Figure 9-9, the iMPACT software automatically detected the devices on the chain. In this example, a Xilinx XC3S500E Spartan-3E FPGA is first in the chain, followed by a Xilinx XCF04S Platform Flash PROM, followed by a Xilinx XC2C64A CPLD in the final position. The devices are yet unprogrammed.

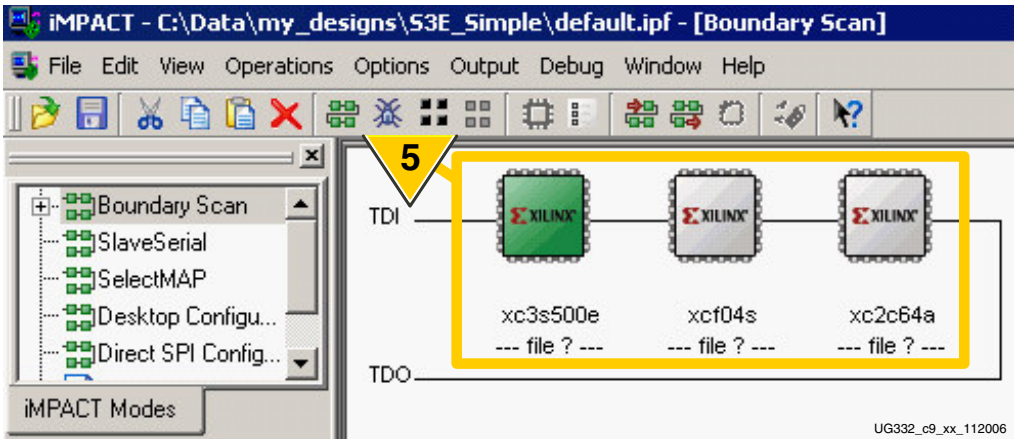

Figure 9-9: **iMPACT Automatically Detects Devices on the JTAG Chain**

6. As shown in Figure 9-10, the iMPACT software automatically prompts for the FPGA bitstream. Select the desired bitstream to download specifically to the FPGA.
7. Click **Open**.

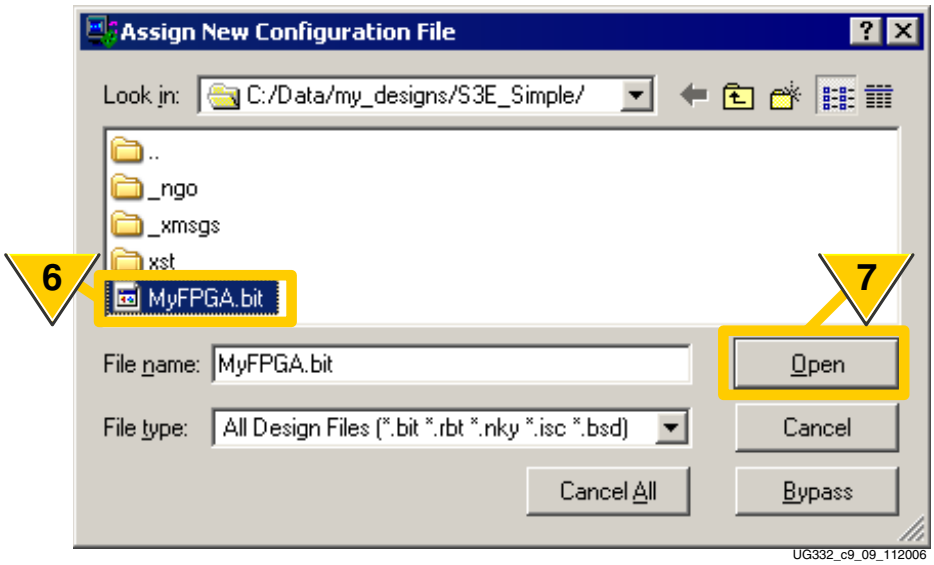

Figure 9-10: **iMPACT Prompts for FPGA Bitstream**

8. As shown in Figure 9-11, the iMPACT software automatically detects that the FPGA bitstream was generated for a non-JTAG configuration method. The iMPACT software automatically adjusts the Startup clock setting for successful JTAG configuration (***StartupClk*:*JtagClk***). The original bitstream file is unaffected.

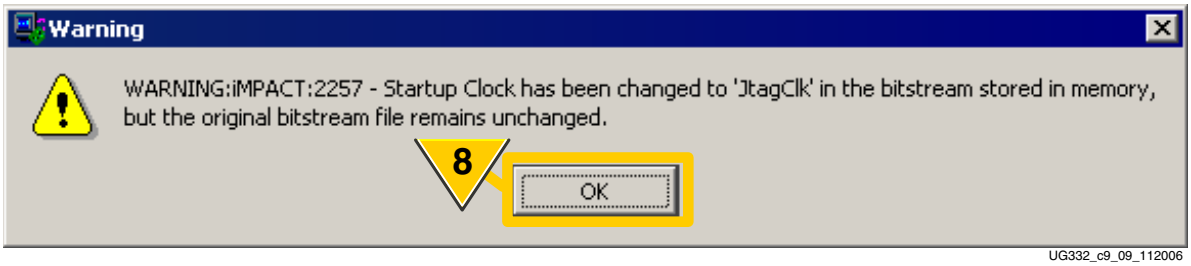

Figure 9-11: **iMPACT Automatically Adjusts FPGA Startup Clock for JTAG Configuration**

9. For faster downloading and a shorter FPGA debugging cycle, there is no need to program the Platform Flash PROM or CPLD unless actually desired. To skip programming the Platform Flash PROM, click Bypass, as shown in Figure 9-12.

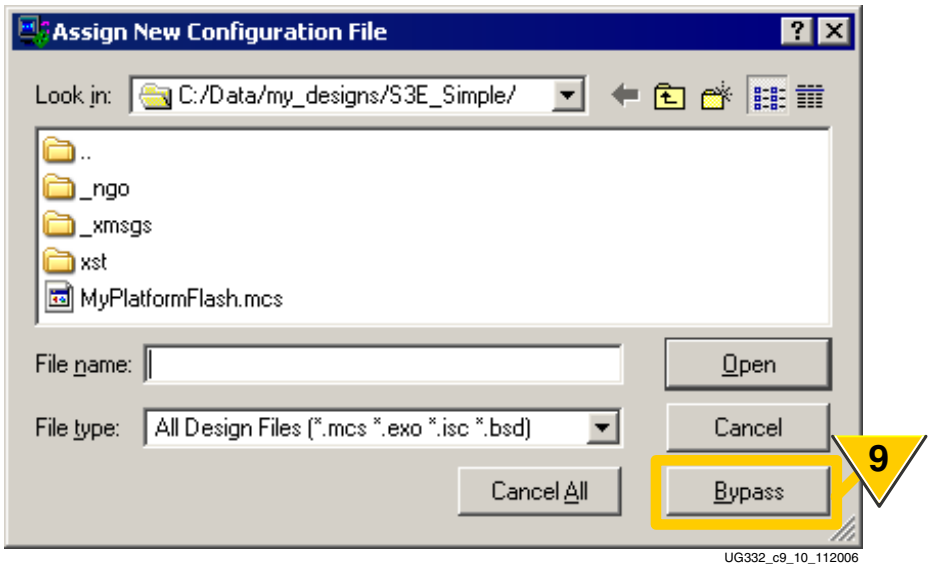

Figure 9-12: **Click Bypass to Skip Platform Flash Programming**

10. Similarly, click Bypass to skip programming of the CPLD, as shown in Figure 9-13.

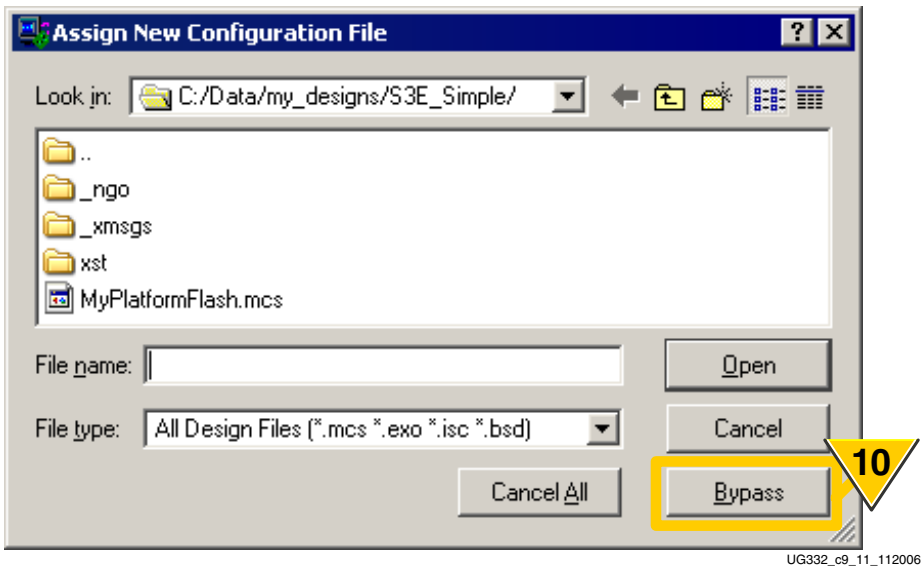

Figure 9-13: **Click Bypass to Skip CPLD Programming**

11. As shown in Figure 9-14, the iMPACT software updates the display, showing the files assigned to each device in the JTAG chain. In this example, the XCF04S Platform Flash and XC2C64A CPLD are "bypassed" and are not programmed. Click the FPGA to highlight it on the display.

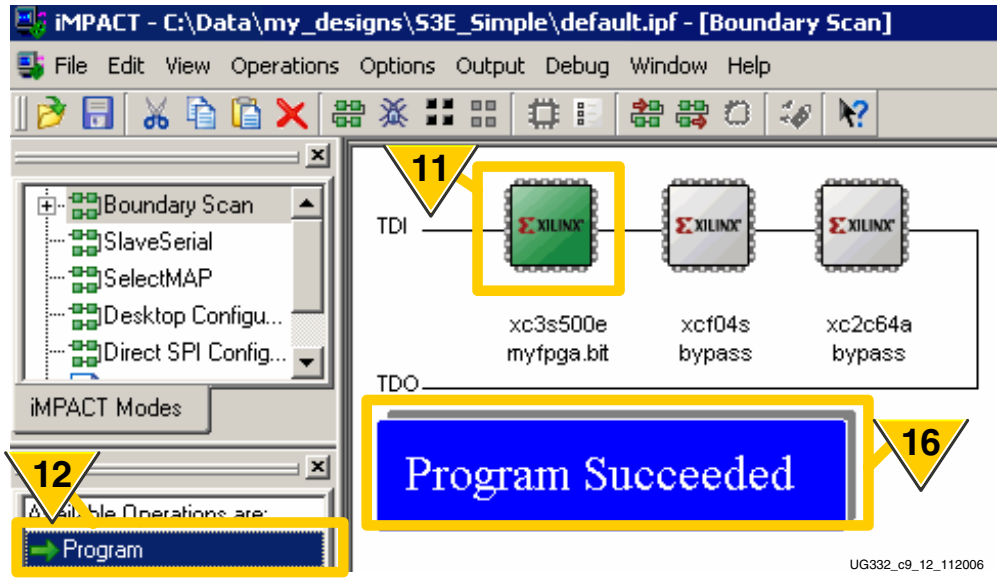

Figure 9-14: **Double-Click Program to Configure FPGA via JTAG**

12. Once the FPGA is highlighted, the associated **Available Operations** are enabled on the display. Double-click **Program**.
13. The **Programming Properties** dialog box appears, as shown in Figure 9-15.

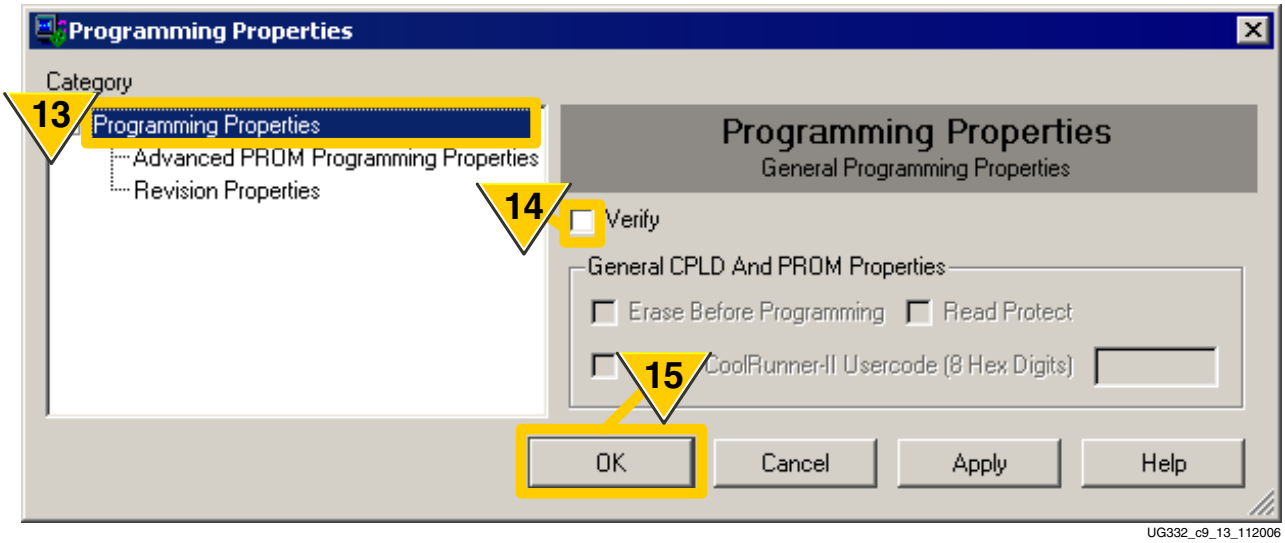

Figure 9-15: **FPGA Programming Options**

14. The iMPACT software provides a **Verify** feature, even for FPGA programming. Typically, the Verify function is not used when downloading the FPGA for debugging purposes.
15. Click **OK** to start the programming process.
16. The iMPACT software indicates when programming is complete, as shown in Figure 9-14. The iMPACT software also forces the FPGA to reconfigure on the board. The FPGA is downloaded with the specified FPGA bitstream.