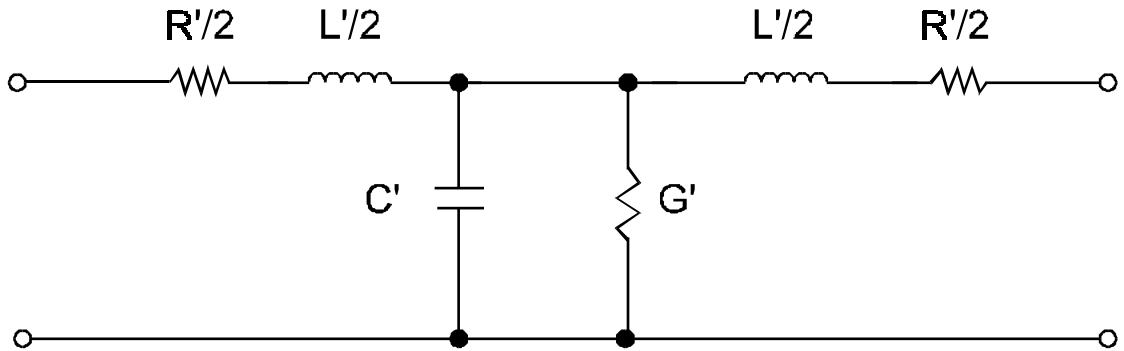
Basics and Practical Examples of Transmission

Circuit Diagram of a Transmission Line

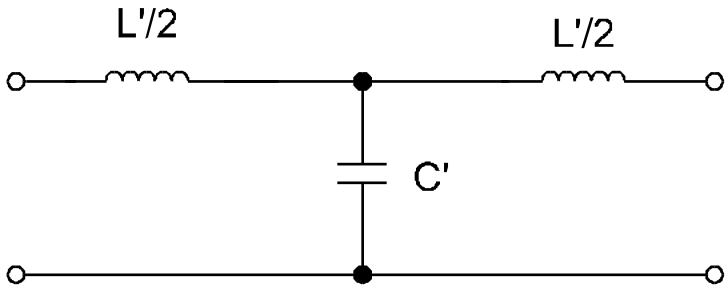


L’	Characteristic Inductance per Unit Length	nH/cm
C’	Characteristic Capacitance per Unit Length	pF/cm
R’	Characteristic Resistance per Unit Length	Ω/cm
G’	Characteristic Conductance per Unit Length	S/cm

$$\text{Line Impedance} \quad \vec{Zo} = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}}$$

Loss-free Transmission Lines

At high frequencies the transmission line losses on printed circuit boards in digital systems can be neglected.



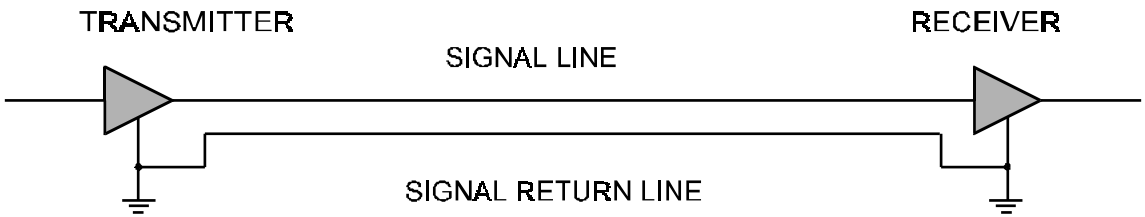
With R' << jϖL' and G' << jϖC':

Line impedance $Z_O = \sqrt{\frac{L'}{C'}}$ **(real number !)**

Propagation time $\tau = \sqrt{L' \times C'}$

Cut-off-frequency $f_O = \frac{1}{2\pi\sqrt{L' \times C'}}$ **with L',C' $\rightarrow$ 0 $\Rightarrow$ fO = ∞**

Transmission Line



A transmission line consists of

- a signal line which carries the signal current

- a signal return line (mostly GND) which carries a return current of the same magnitude.

Any DC interconnect between the GND terminals of the two circuits (e.g. safety earth) will not provide a signal return path according to the transmission line theory.

The area between the signal line and the return lines determines the capability of the circuit to radiate RF and also its immunity against EMI.

Transmission Line Theory

Rule of Thumb:

The transmission line theory has to be applied, when the rise time of the signal is shorter than twice the propagation time.

Example 1 : Twisted pair cable; τ = 5 ns/m ; t_r = 2 ns

$$L = \frac{t_r}{2\tau} \quad \frac{2\,ns}{2 \times 5\,ns/m} = 0.2\ m$$

Example 2 : Bus Line; t = 20 ns/m ; tr = 2 ns

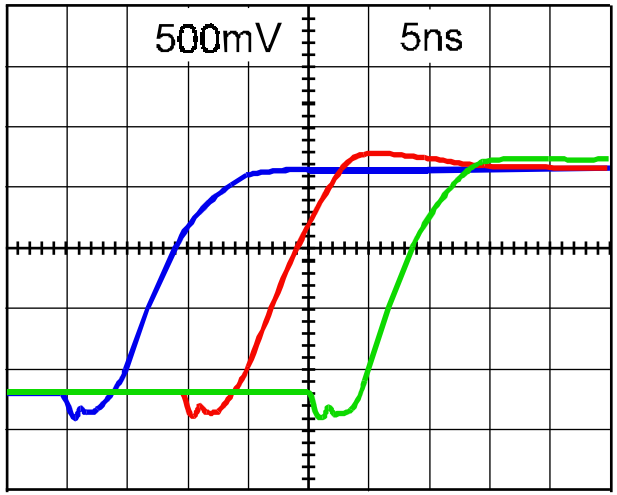
$$L = \frac{t_r}{2\tau} \quad \frac{2\,ns}{2 \times 20\,ns/m} = 0.05\ m$$

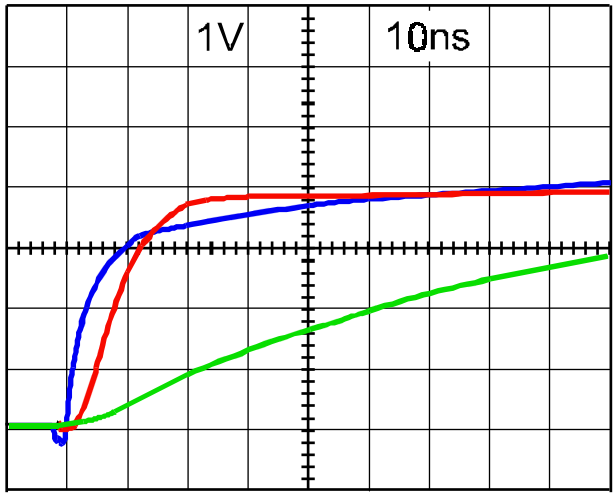
With shorter signal lines all line reflections occur during the rise/fall time of the signal. In this case it is allowed to use the simplified capacitive load line model.

Typical Line Impedances

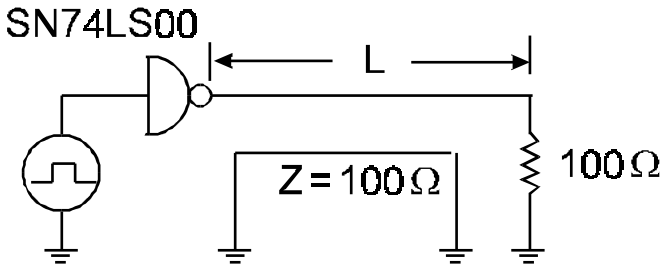
	L' (nH/cm)	C' (pF/cm)	Z (Ω)	τ (ns/m)
SINGLE WIRE (FAR AWAY FROM GND)	20	0.06	600	~4
SPACE	μ_o	ε_o	370	3,3
TWISTED PAIR CABLE	5-10	0.5-1	80-120	5
FLAT CABLE (ALTERNATING SIGNAL AND GND WIRE)	5-10	0.5-1	80-120	5
WIRE ON PC BOARD	5-10	0.5-1.5	70-100	~5
COAX CABLE	2,5	1.0	50	5
BUS LINE	5-10	10-30	20-40	10-20

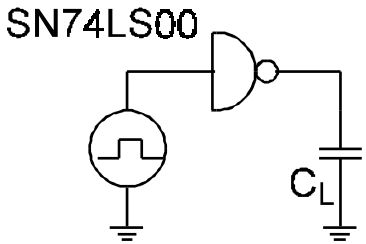
Waveforms with Transmission Lines and Capacitive Load





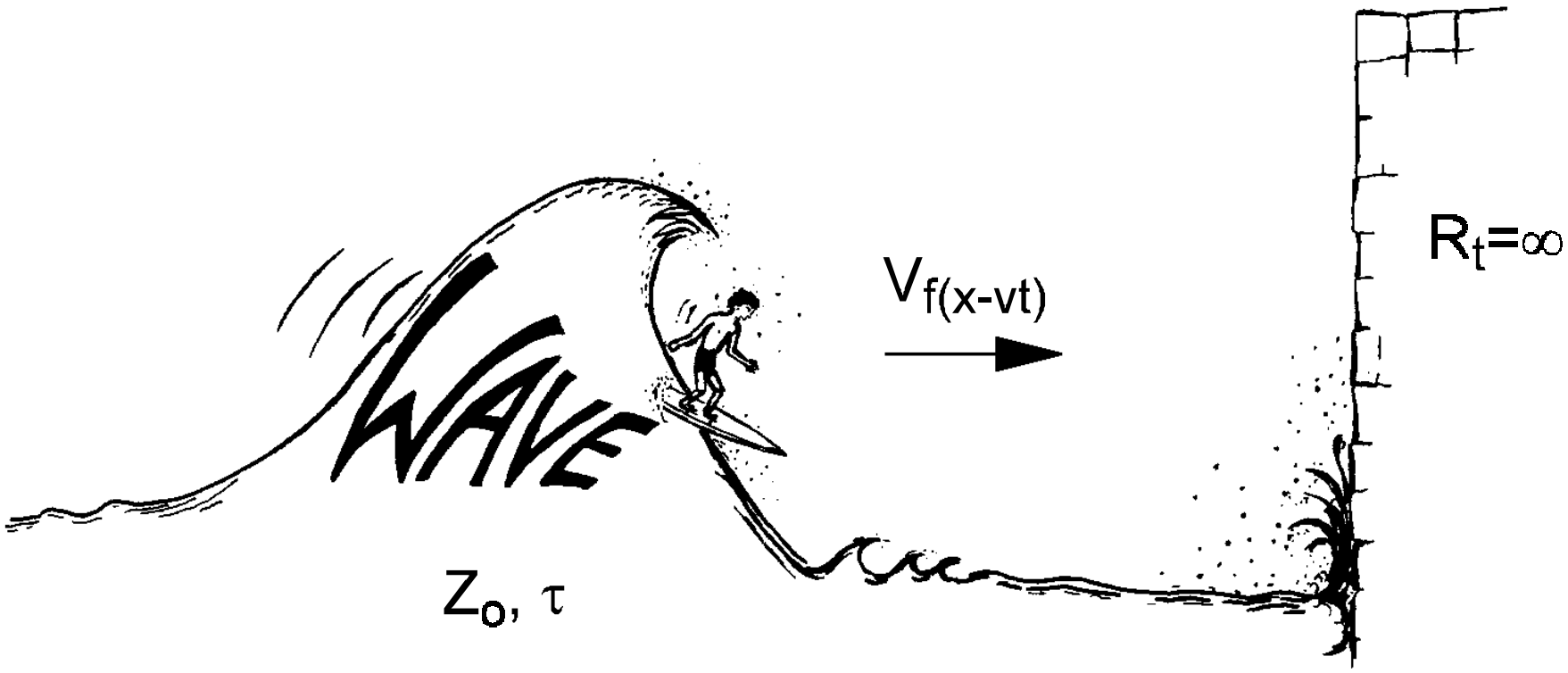
L=0m (~10pF)
L=1m (~56pF)
L=11m (~616pF)



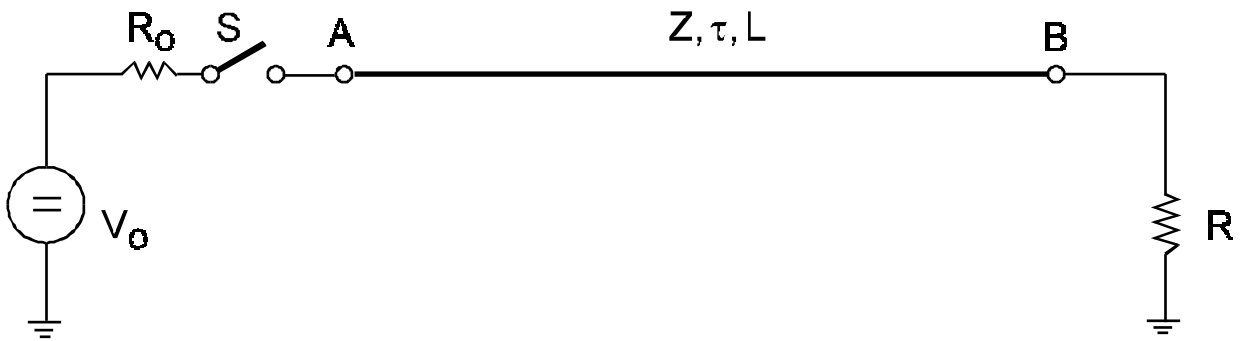


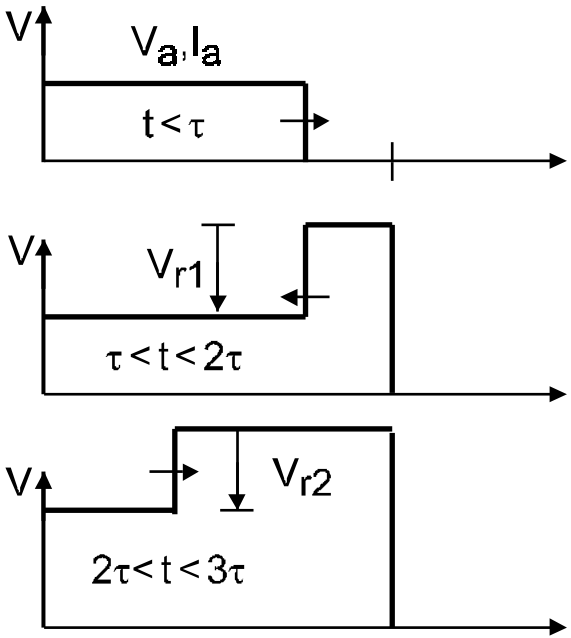
C_L = 10 pF
C_L = 56 pF
C_L = 616 pF

Analysis of Line Reflections



Waveforms caused by Line Reflections





Incident wave at the generator output

$$V_a = V_o \frac{Z}{Z + R_O}$$

Wave reflected at the line end

$$V_{r1} = V_a \times \rho_B \qquad \rho_B = \frac{R - Z}{R + Z}$$

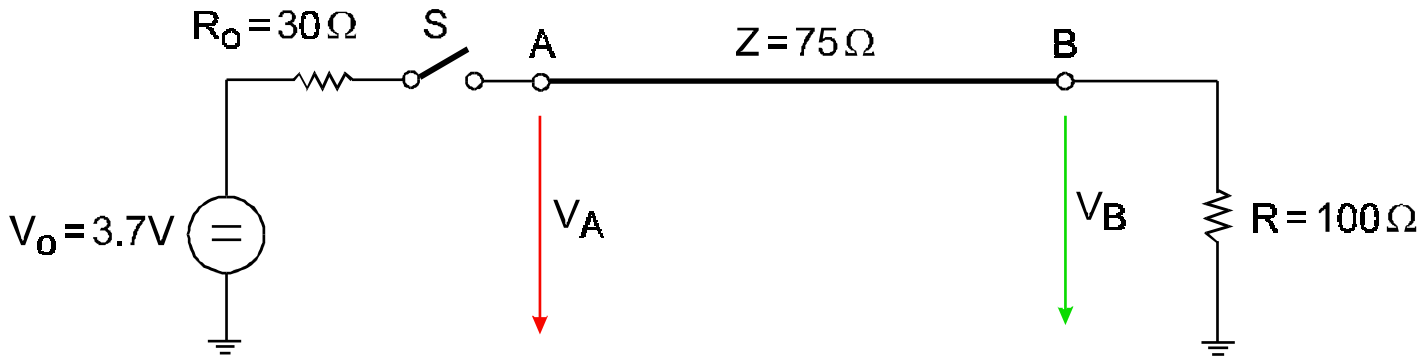
Wave reflected at the generator output

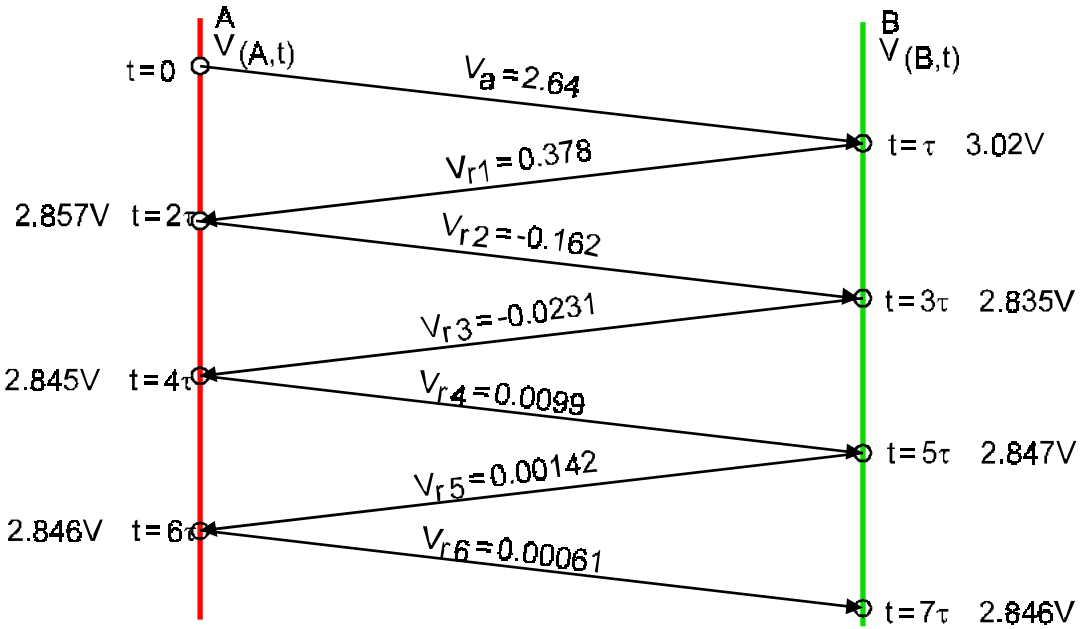
$$V_{r2} = V_{r1} \times \rho_A \qquad \rho_A = \frac{R_o - Z}{R_o + Z}$$

Quiescent state

$$V_\infty = V_o \frac{R}{R_o + R}$$

Lattice Diagram





$$\rho_A = \frac{30-75}{30+75} = -0.429$$

$$\rho_B = \frac{100-75}{100+75} = 0.143$$

$V_o = 3.70\,V$

$V_a = V_o \times 75\,\Omega/(75\,\Omega + 30\,\Omega) = 2.64\,V$

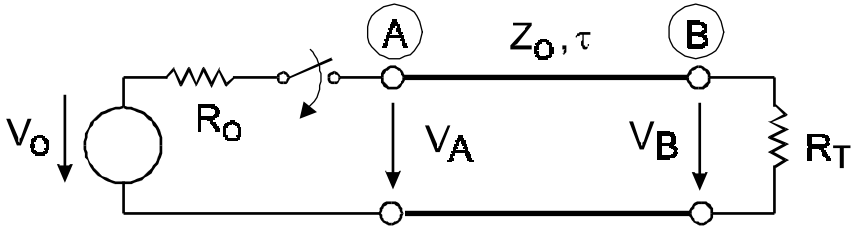
$V_{r1} = 2.64\,V \times 0.14 = 0.37\,V$

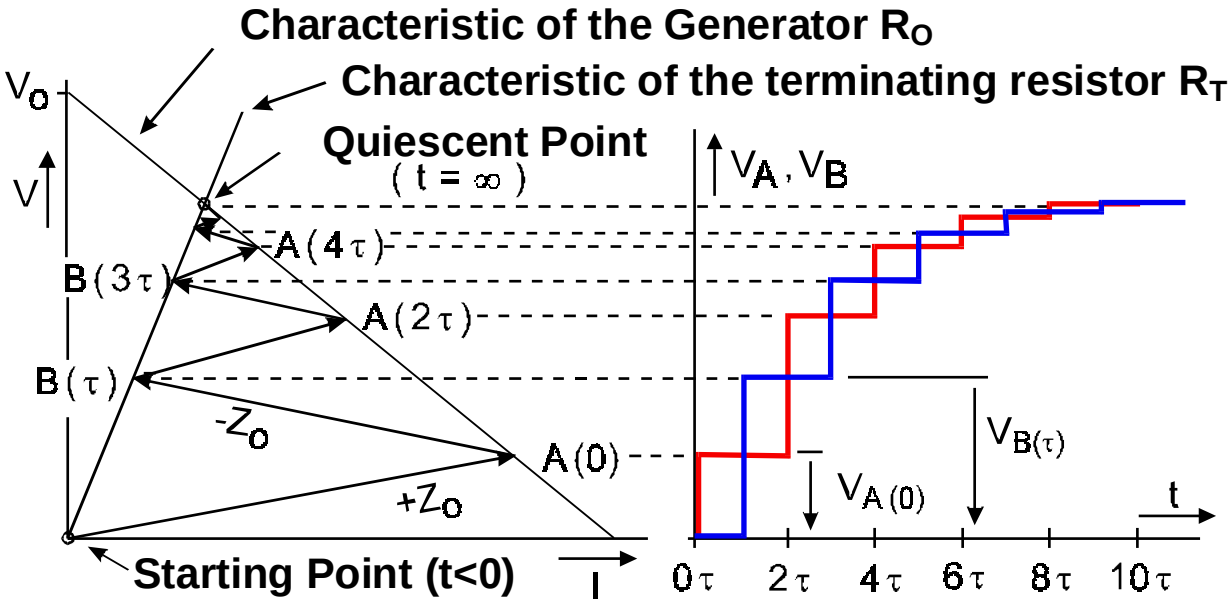
$V_{r2} = 0.37\,V \times (-0.42) = -0.16\,V$

$V_{r3} = -0.16\,V \times 0.14 = -0.02\,V$

$V_{r4} = -0.02\,V \times (-0.42) = 0.009\,V$

Bergeron Diagram





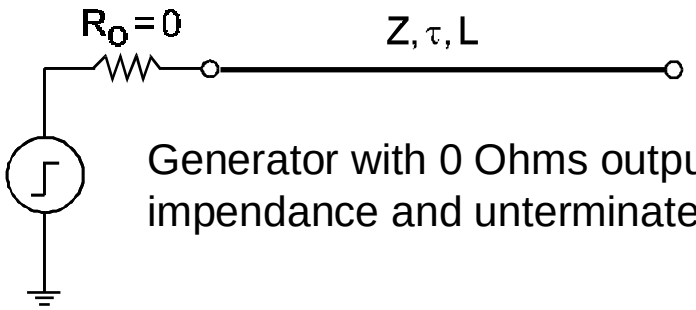
Voltage changes only after twice the propagation time. Incident wave is independent from line termination.

$$V_{A(0<t<2\tau)} = V_o \times \frac{Z_o}{R_o + Z_o}$$

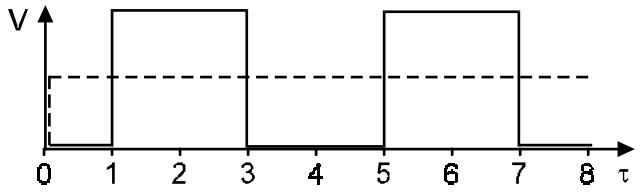
Steady state condition:

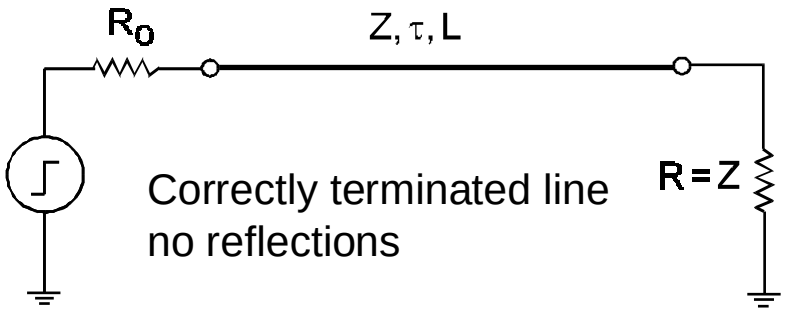
$$V_{(t=\infty)} = V_o \times \frac{R_T}{R_o + R_T}$$

Line Reflections - Special Cases

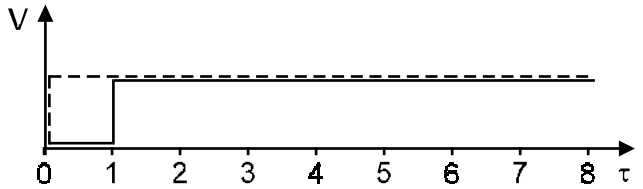


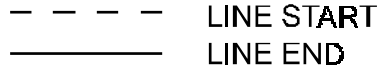
Generator with 0 Ohms output impendance and unterminated line

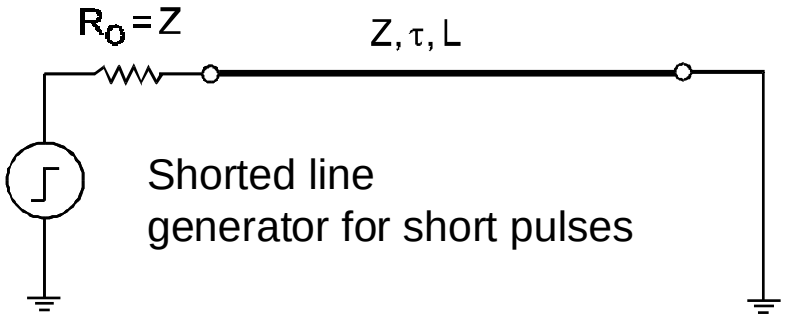




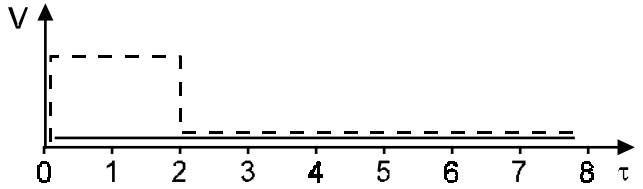
Correctly terminated line no reflections



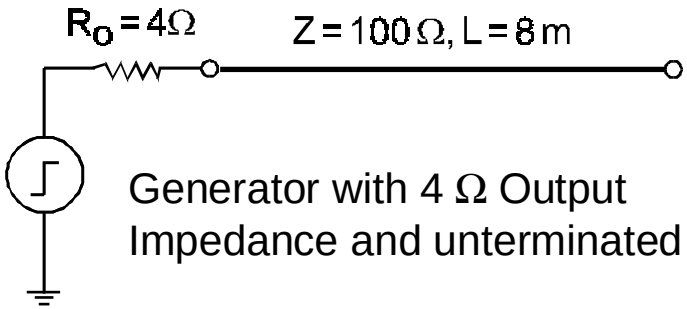




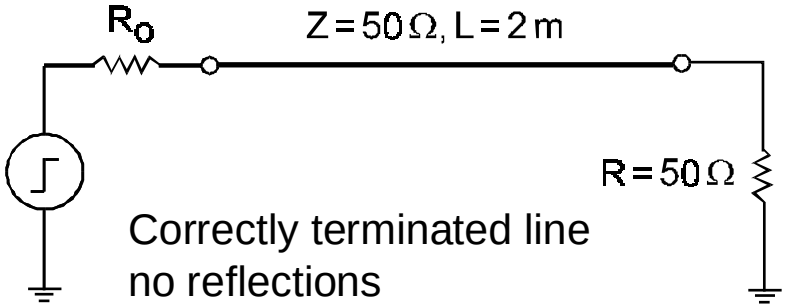
Shorted line generator for short pulses



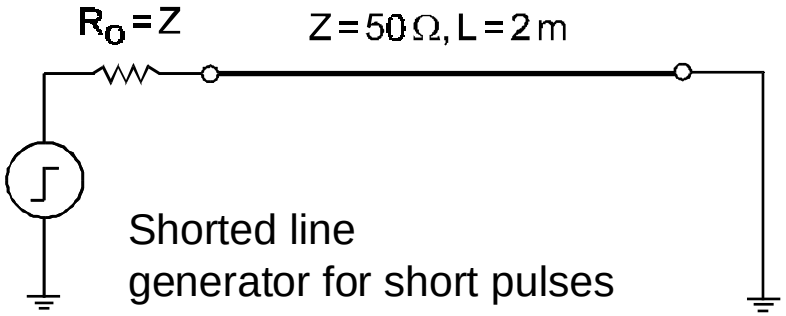
Line Reflections - Special Cases



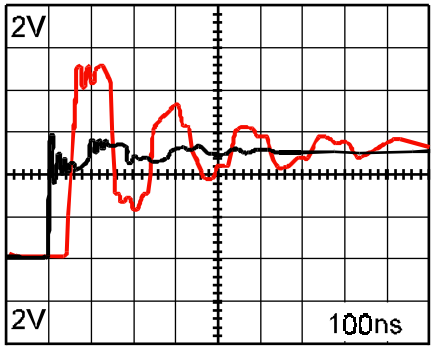
Generator with 4 Ω Output
Impedance and unterminated line

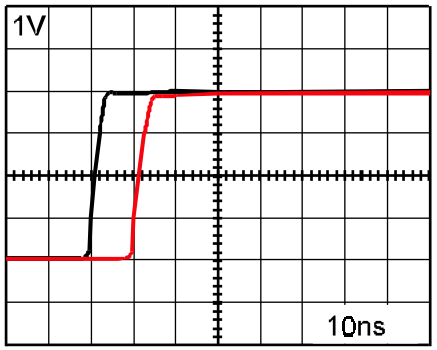


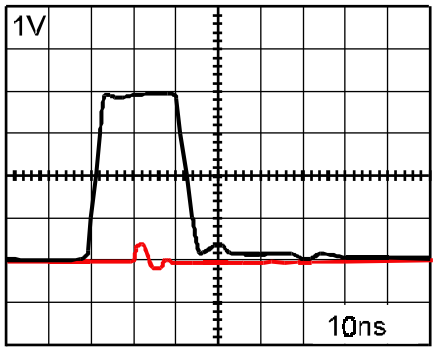
Correctly terminated line
no reflections



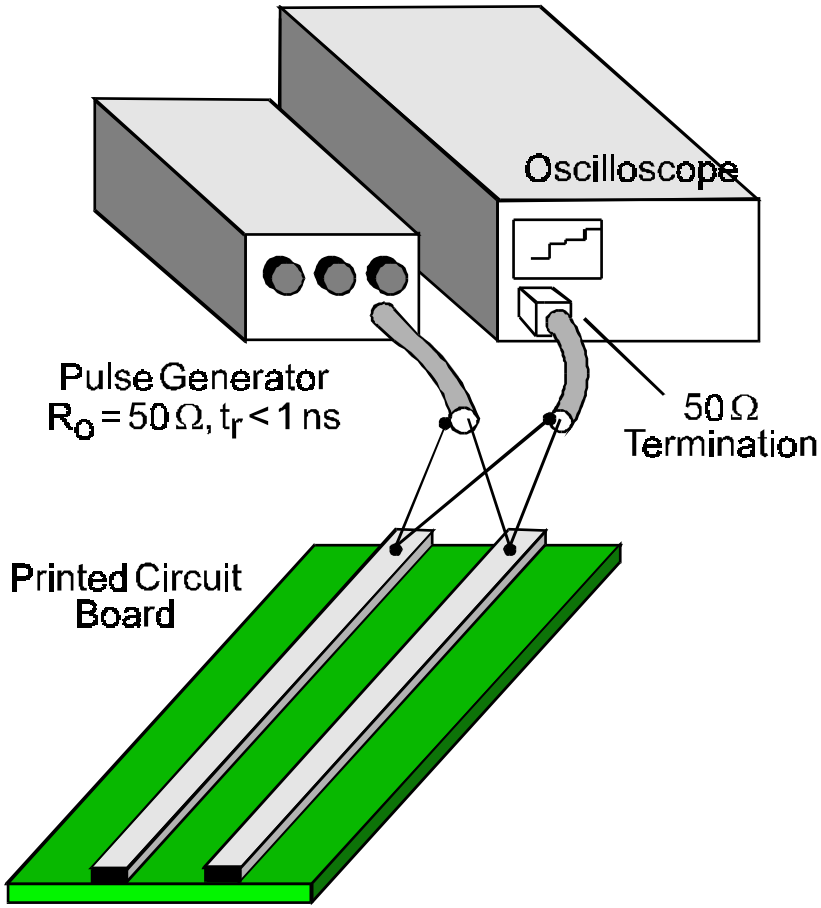
Shorted line
generator for short pulses

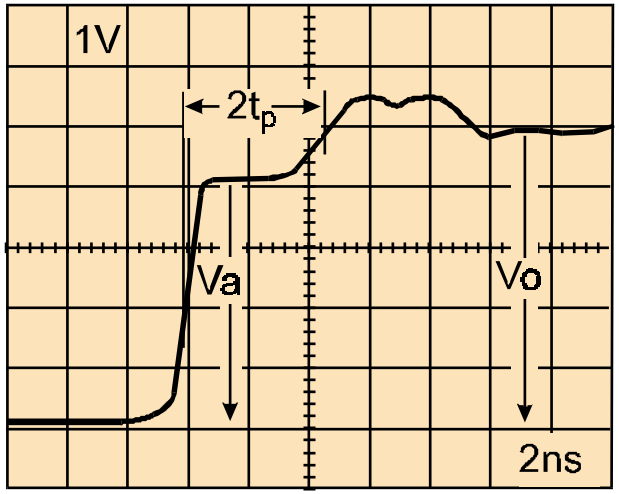






Measurement of the Line Impedance





$$Z_o = \frac{R_o\ ^{*)}}{V_o/V_a - 1}$$

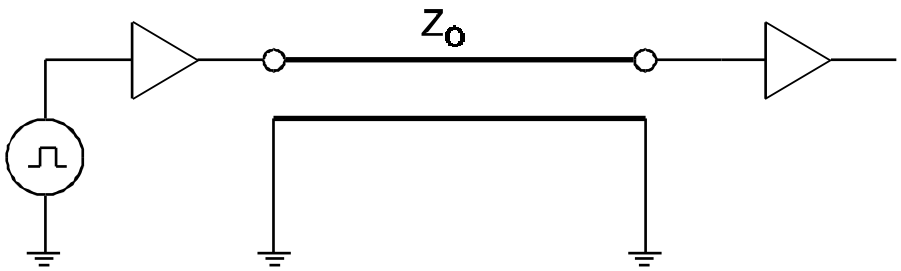
$$\tau \times Z_o = L'$$

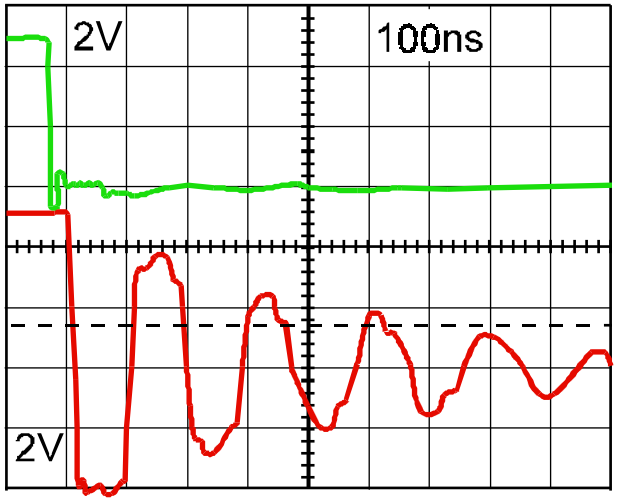
$$\tau / Z_o = C'$$

*) Note: R_o = 50 Ω // 50 Ω = 25 Ω

Line Reflections

Open Circuit



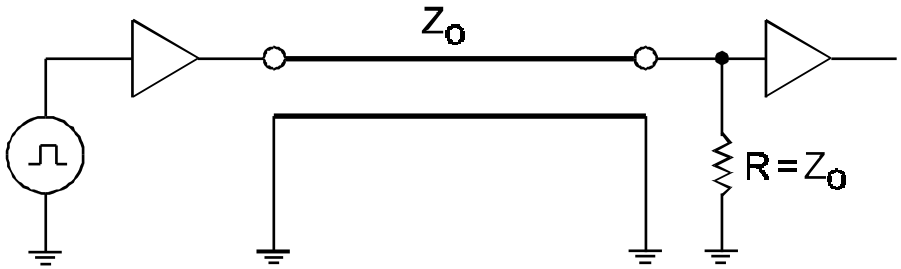


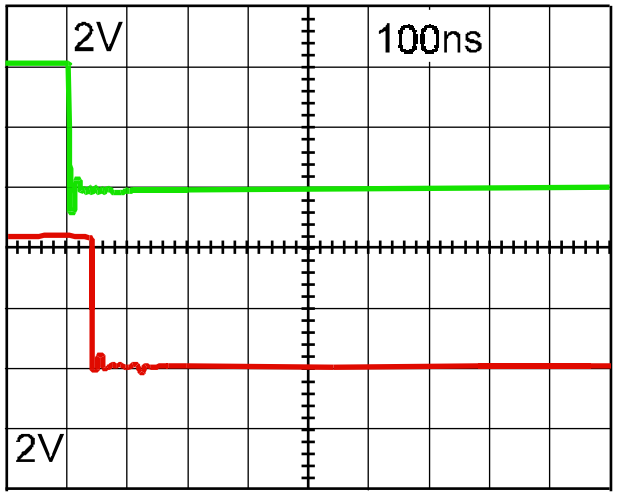
An open circuit at the line end causes under- and overshoots which may exceed the maximum rated input voltage of the receiving circuit.

The following over- and undershoots may cross the threshold voltage of the receiver serveral times and may generate system errors.

Line Reflections

Terminated Line



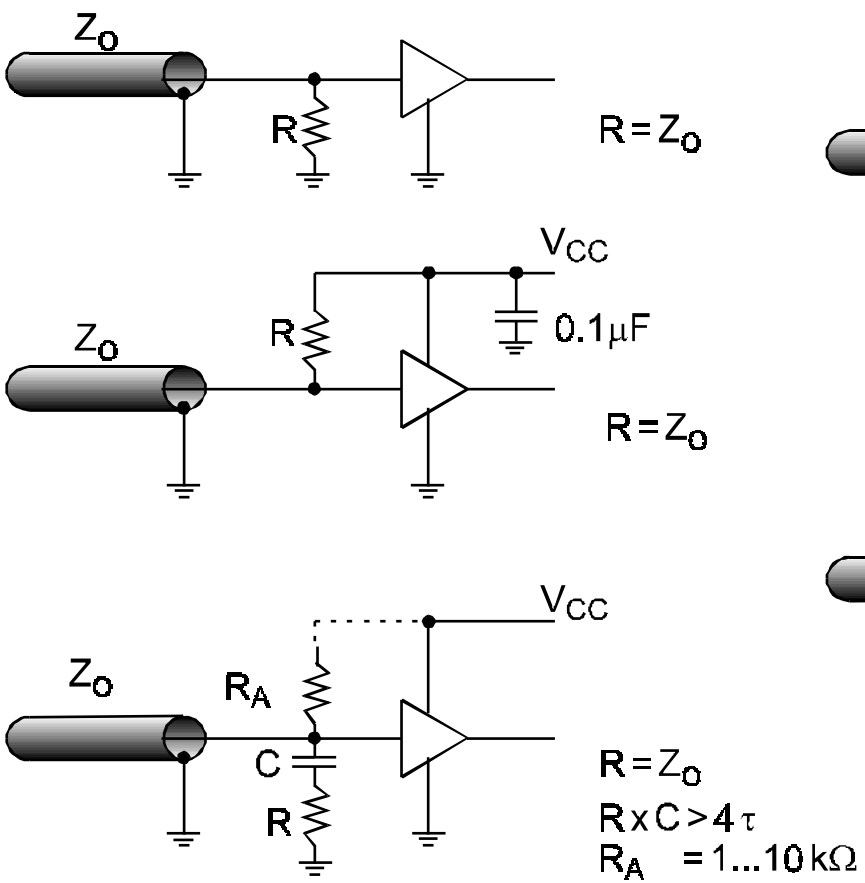


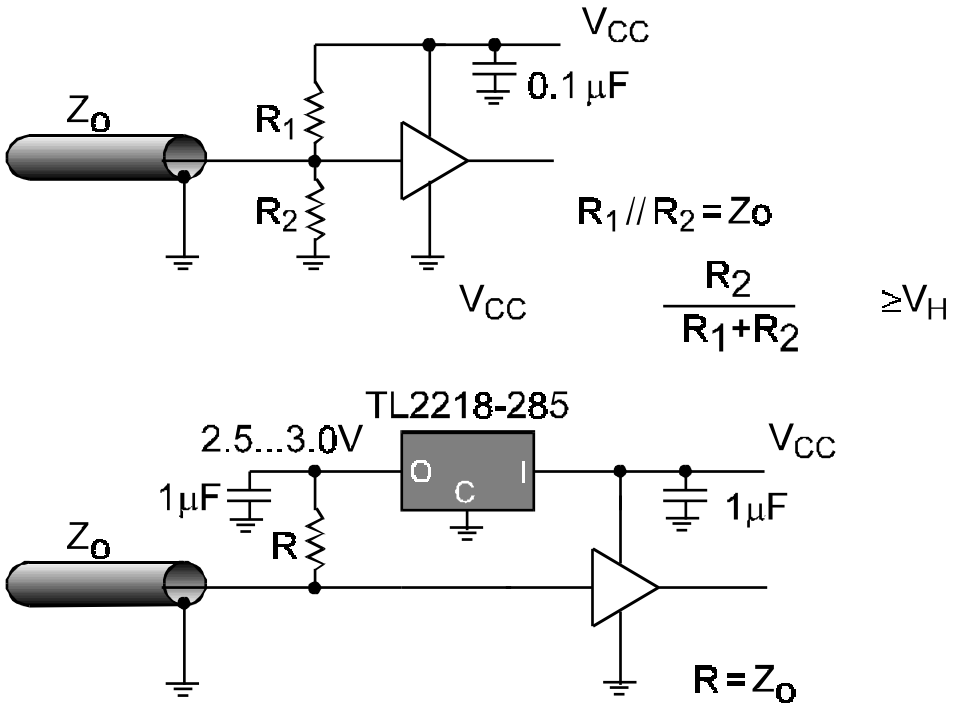
Line reflections are eliminated by a correct line termination.

A mismatch up to 50% is acceptable.

Note: - Increased Power Dissipation
- High drive Capability required.

Line Termination Circuits

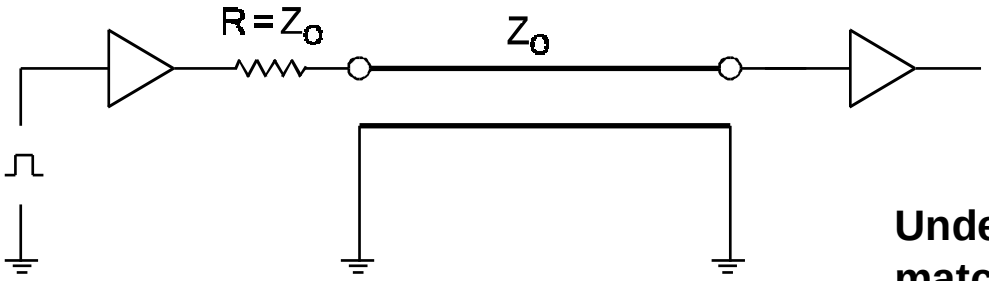


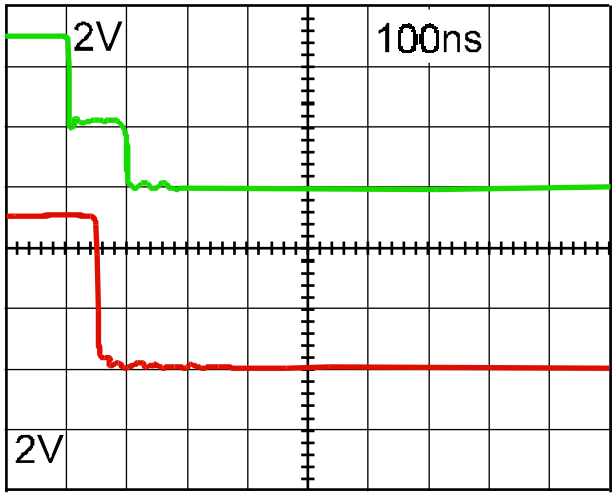


Mismatch of 50%...100% acceptable (with low impedance bus lines up to 400%).

Line Reflections

Matching of Generator Impedance



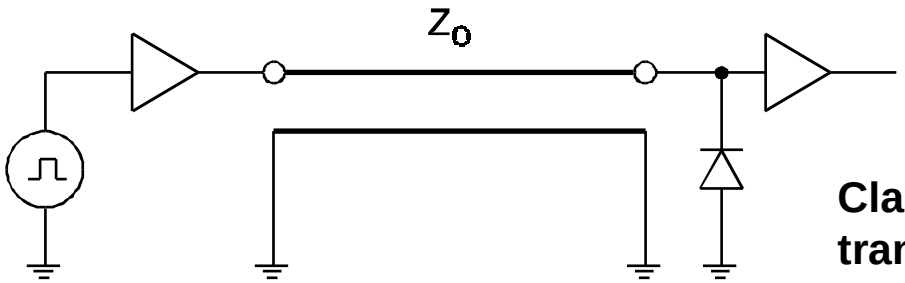


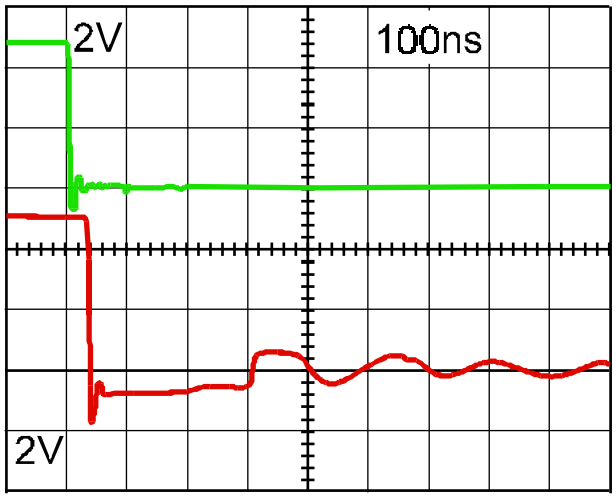
Under- and overshoots are avoided by matching the output impedance of the line driver to the line impedance by means of a series resistor. Power dissipation is not increased (recommended in CMOS systems).

Note: Undefined logic levels along the transmission line for up to twice the propagation time.

Circuits with built-in serial termination (25Ω to 30Ω):
8 Bit: SN74ABT2244
16 Bit: SN74ABT162244
18 Bit: SN74ABT162501

Line Reflections
Clamping Diodes





Clamping diodes at the end of the transmission line absorbe the energy of under- and overshoots and ensure a clean signal waveform.
Input circuits of logic ICs contain these clamping diodes.

Note: The clamping diodes of VLSI circuits are often not capable to handle the high currents generated by line reflections (parasitic transistors!). Provide additional Schottly clamping diodes!

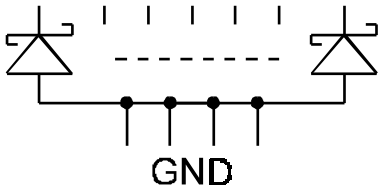
Schottky Diode Arrays:
SN74S1050, SN74S1051, SN74S1052, SN74S1053, SN74S1056, SN74F1056, SN74F1016, SN74F1018

Bus Termination Arrays

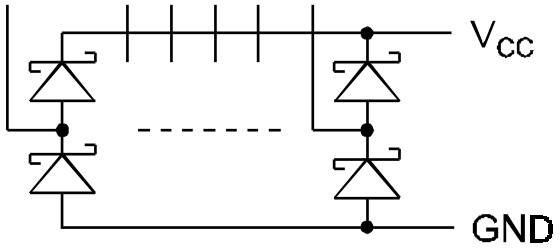
Released Functions :

SN74S1050 12-Bit Schottky Diode Array
SN74S1051 12-Bit Schottky Diode Network
SN74S1052 16-Bit Schottky Diode Array
SN74S1053 16-Bit Schottky Diode Network
SN74S1056 8-Bit Schottky Diode Array
SN74F1056 9-Bit Schottky Diode Array
SN74F1016 16-Bit Schottky Diode
R-C Bus Termination Array
SN74F1018 18-Bit Schottky Diode
R-C Bus Termination Array

ARRAY



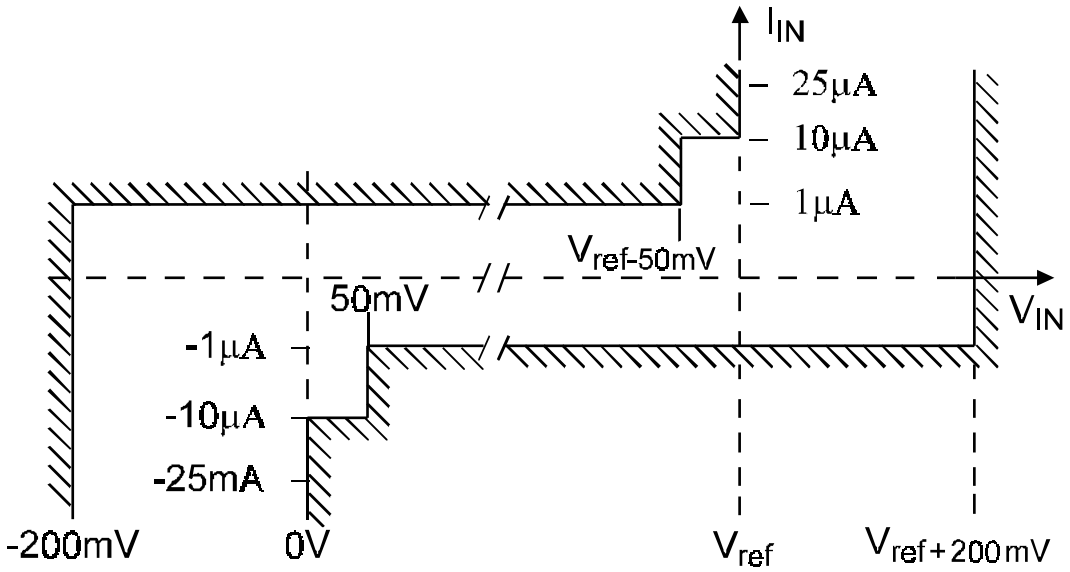
NETWORK

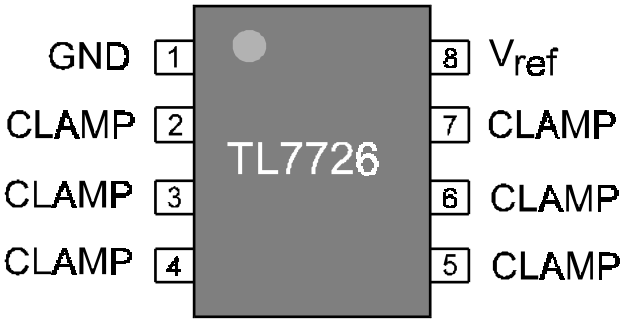


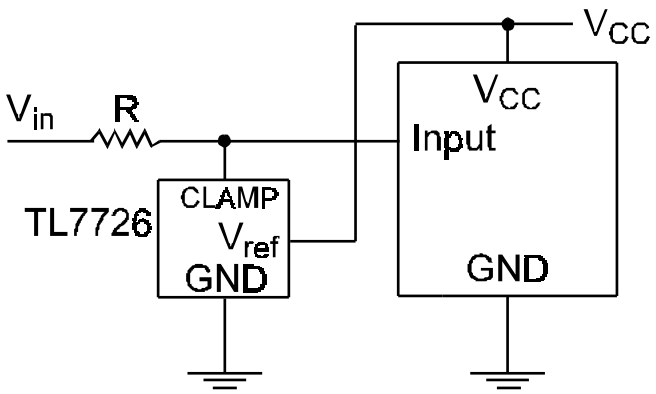
Applications :

★Arrays in TTL systems
★Networks in CMOS systems (positive overshoots)
★Small buses, e.g. Memory Arrays
★System bus in personal computers

Clamping Circuit TL7726







★**The clamping circuit TL7726 protects sensitive analog and digital inputs against excessive overvoltages and by that ensures the function of the circuit.**