Table 10. SC16IS740/750/760 internal registers

Register address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
General register set[1]										
0x00	RHR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R
0x00	THR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	W
0x01	IER	$\overline{\text{CTS}}$ interrupt enable[2]	$\overline{\text{RTS}}$ interrupt enable[2]	$\overline{\text{Xoff}}$[2]	Sleep mode[2]	modem status interrupt	receive line status interrupt	THR empty interrupt	RX data available interrupt	R/W
0x02	FCR	RX trigger level (MSB)	RX trigger level (LSB)	TX trigger level (MSB)[2]	TX trigger level (LSB)[2]	reserved[3]	TX FIFO reset[4]	RX FIFO reset[4]	FIFO enable	W
0x02	IIR[5]	FIFO enable	FIFO enable	interrupt priority bit 4[2]	interrupt priority bit 3[2]	interrupt priority bit 2	interrupt priority bit 1	interrupt priority bit 0	interrupt status	R
0x03	LCR	Divisor Latch Enable	set break	set parity	even parity	parity enable	stop bit	word length bit 1	word length bit 0	R/W
0x04	MCR	clock divisor[2]	IrDA mode enable[2]	Xon Any[2]	loopback enable	reserved[3]	TCR and TLR enable[2]	$\overline{\text{RTS}}$	$\overline{\text{DTR}}$/(IO5)[6]	R/W
0x05	LSR	FIFO data error	THR and TSR empty	THR empty	break interrupt	framing error	parity error	overrun error	data in receiver	R
0x06	MSR	CD/(IO6)[6]	RI/(IO7)[6]	DSR/ (IO4)[6]	CTS	ΔCD/ (IO6)[6]	ΔRI/(IO7)[6]	ΔDSR/ (IO4)[6]	ΔCTS	R
0x07	SPR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x06	TCR[7]	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x07	TLR[7]	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x08	TXLVL	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R
0x09	RXLVL	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R
0x0A	IODir[6]	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x0B	IOState[6]	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x0C	IOIntEna[6]	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x0D	reserved[3]	reserved[3]	reserved[3]	reserved[3]	reserved[3]	reserved[3]	reserved[3]	reserved[3]	reserved[3]	
0x0E	IOControl[6]	reserved[3]	reserved[3]	reserved[3]	reserved[3]	UART software reset[8]	reserved[3]	I/O[7:4] or $\overline{\text{RI}}$, $\overline{\text{CD}}$, $\overline{\text{DTR}}$, $\overline{\text{DSR}}$	latch	R/W
0x0F	EFCR	IrDA mode (slow/ fast)[9]	reserved[3]	auto RS-485 RTS output inversion	auto RS-485 RTS direction control	reserved[3]	transmitter disable	receiver disable	9-bit mode enable	R/W

Table 10. SC16IS740/750/760 internal registers *...continued*

Register address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
Special register set[10]										
0x00	DLL	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x01	DLH	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
Enhanced register set[11]										
0x02	EFR	Auto $\overline{CTS}$	Auto $\overline{RTS}$	special character detect	enable enhanced functions	software flow control bit 3	software flow control bit 2	software flow control bit 1	software flow control bit 0	R/W
0x04	XON1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x05	XON2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x06	XOFF1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x07	XOFF2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W

[1] These registers are accessible only when LCR[7] = 0.

[2] These bits in can only be modified if register bit EFR[4] is enabled.

[3] These bits are reserved and should be set to 0.

[4] After Receive FIFO or Transmit FIFO reset (through FCR[1:0]), the user must wait at least $2 \times T_{clk}$ of XTAL1 before reading or writing data to RHR and THR, respectively.

[5] Burst reads on the serial interface (that is, reading multiple elements on the I²C-bus without a STOP or repeated START condition, or reading multiple elements on the SPI bus without de-asserting the $\overline{CS}$ pin), should not be performed on the IIR register.

[6] Only available on the SC16IS750/SC16IS760.

[7] These registers are accessible only when MCR[2] = 1 and EFR[4] = 1.

[8] Device returns NACK on I²C-bus when this bit is written.

[9] IrDA mode slow/fast for SC16IS760, slow only for SC16IS750.

[10] The special register set is accessible only when LCR[7] = 1 and not 0xBF.

[11] Enhanced Feature Registers are only accessible when LCR = 0xBF.