AVR094: Replacing ATmega8 by ATmega88

8-bit AVR® Microcontrollers

Application Note

Features

- **Interrupt Vectors**
- **Bit and Register names and locations**
- **Oscillators and Start up Delay**
- **Brown Out Detection**
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Introduction

This application note is a guide to help current ATmega8 users convert existing designs to ATmega88. ATmega88 is not designed to be a replacement for ATmega8, but is pin compatible and has a very similar feature set.

Improvements or added features in the ATmega88 that are not in conflict with those in ATmega8 are not in general covered by the scope of this document. However, to provide an understanding why it could be of interest to replace the ATmega8 by the ATmega88 a list of new/improved features in the ATmega88 are available below.

- Extended operating ranges as e.g.
  4MHz@1.8V, 10MHz@2.7V, 20MHz@4.5V
- Lower Power Consumption
- Decreased EEPROM write time
- Prescaler on system clock
- On-Chip Debugging with debugWire
- Pin Change Interrupt
- Enhanced Watchdog Timer with Interrupt mode
- 10 bit resolution on all ADC channels
- Timer/Counter0,2 extended with PWM and Compare units
- Master SPI mode in the USART
- General Purpose I/O Registers
- Output the system clock on I/O pin

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Interrupt Vector Table

All interrupt vectors on ATmega8 have an equivalent on ATmega88. Due to the fact that ATmega88 has more interrupts, the vectors have moved to other locations. Some interrupts have changed names, but the functionality is the same.

Table 1. Comparison of the interrupt vectors

ATmega8			ATmega88		
Vector No.	**Program Address**	**Interrupt**	**Vector No.**	**Program Address**	**Interrupt**
1	0x000	RESET	1	0x000	RESET
2	0x001	INT0	2	0x001	INT0
3	0x002	INT1	3	0x002	INT1
			4	0x003	PCINT0
			5	0x004	PCINT1
			6	0x005	PCINT2
			7	0x006	WDT
4	0x003	TIMER2 COMP	8	0x007	TIMER2 COMPA
			9	0x008	TIMER2 COMPB
5	0x004	TIMER2 OVF	10	0x009	TIMER2 OVF
6	0x005	TIMER1 CAPT	11	0x00A	TIMER1 CAPT
7	0x006	TIMER1 COMPA	12	0x00B	TIMER1 COMPA
8	0x007	TIMER1 COMPB	13	0x00C	TIMER1 COMPB
9	0x008	TIMER1 OVF	14	0x00D	TIMER1 OVF
10	0x009	TIMER0 OVF	15	0x00E	TIMER0 COMPA
			16	0x00F	TIMER0 COMPB
			17	0x010	TIMER0 OVF
11	0x00A	SPI, STC	18	0x011	SPI, STC
12	0x00B	USART, RXC	19	0x012	USART, RX
13	0x00C	USART, UDRE	20	0x013	USART, UDRE
14	0x00D	USART, TXC	21	0x014	USART, TX
15	0x00E	ADC	22	0x015	ADC
16	0x00F	EE_RDY	23	0x016	EE READY
17	0x010	ANA_COMP	24	0x017	ANALOG COMP
18	0x011	TWI	25	0x018	TWI
19	0x012	SPM_RDY	26	0x019	SPM READY

I/O Registers and Bits

This section lists all the I/O Registers and I/O Register Bits that do not have the same position and/or functionality between ATmega8 and ATmega88.

ATmega88 has more I/O registers then ATmega8. The I/O register file in the ATmega88 has been expanded with an Extended I/O memory (0x60 - 0xFF in data space). Almost all registers from ATmega8 have been reorganized to new memory locations on ATmega88. Note that ST/STS/STD and LD/LDS/LDD instructions must be used to access the Extended I/O space.

In Table 2 all I/O registers in ATmega8 are listed with their equivalent in ATmega88. The list is sorted to emphasize the new location in ATmega88. Note that in addition to changing locations, registers may also have changed names and functionality. I/O registers that have changed names but preserve the same functionality are listed in Table 3. I/O registers that do not have the same functionality as in ATmega8 are described in detail in Table 4.

Table 2. All I/O registers on ATmega8 with their Atmega88 equivalent. Bolded I/O registers are not functionally equivalent, see Table 4 for detailed information.

ATmega8		**ATmega88**		
I/O Register name	**I/O Register address**	**I/O Register name**	**I/O Register address**	
UDR	0x0C (0x2C)	UDR0	(0xC6)	Extended I/O Memory (0x60-0xFF)
UBRRH	0x20 (0x40)	**UBRR0H**	**(0xC5)** [1]	
UBRRL	0x09 (0x29)	UBRR0L	(0xC4)	
UCSRC	0x20 (0x40)	**UCSR0C**	**(0xC2)** [1]	
UCSRB	0x0A (0x2A)	UCSR0B	(0xC1)	
UCSRA	0x0B (0x2B)	UCSR0A	(0xC0)	
TWCR	0x36 (0x56)	TWCR	(0xBC)	
TWDR	0x03 (0x23)	TWDR	(0xBB)	
TWAR	0x02 (0x22)	TWAR	(0xBA)	
TWSR	0x01 (0x21)	TWSR	(0xB9)	
TWBR	0x00 (0x20)	TWBR	(0xB8)	
ASSR	0x22 (0x42)	**ASSR**	**(0xB6)**	
OCR2	0x23 (0x43)	OCR2A	(0xB3)	
TCNT2	0x24 (0x44)	TCNT2	(0xB2)	
TCCR2	0x25 (0x45)	**TCCR2B**	**(0xB1)**	
TCCR2	0x25 (0x45)	**TCCR2A**	**(0xB0)**	
OCR1BH	0x29 (0x49)	OCR1BH	(0x8B)	
OCR1BL	0x28 (0x48)	OCR1BL	(0x8A)	
OCR1AH	0x2B (0x4B)	OCR1AH	(0x89)	
OCR1AL	0x2A (0x4A)	OCR1AL	(0x88)	
ICR1H	0x27 (0x47)	ICR1H	(0x87)	
ICR1L	0x26 (0x46)	ICR1L	(0x86)	
TCNT1H	0x2D (0x4D)	TCNT1H	(0x85)	
TCNT1L	0x2C (0x4C)	TCNT1L	(0x84)	
TCCR1A	0x2F (0x4F)	**TCCR1C**	**(0x82)**	

Table 2. All I/O registers on ATmega8 with their Atmega88 equivalent. Bolded I/O registers are not functionally equivalent, see Table 4 for detailed information. (cont.)

ATmega8		ATmega88		
I/O Register name	**I/O Register address**	**I/O Register name**	**I/O Register address**	
TCCR1B	0x2E (0x4E)	TCCR1B	(0x81)	Extended I/O Memory (0x60-0xFF)
TCCR1A	0x2F (0x4F)	**TCCR1A**	**(0x80)**	
ADMUX	0x07 (0x27)	ADMUX	(0x7C)	
SFIOR	0x30 (0x50)	**ADCSRB**	**(0x7B)**	
ADCSRA	0x06 (0x26)	ADCSRA	(0x7A)	
ADCH	0x05 (0x25)	ADCH	(0x79)	
ADCL	0x04 (0x24)	ADCL	(0x78)	
TIMSK	0x39 (0x59)	**TIMSK2**	**(0x70)**	
TIMSK	0x39 (0x59)	**TIMSK1**	**(0x6F)**	
TIMSK	0x39 (0x59)	**TIMSK0**	**(0x6E)**	
MCUCR	0x35 (0x55)	**EICRA**	**(0x69)**	
OSCCAL	0x31 (0x51)	OSCCAL	(0x66)	
WDTCR	0x21 (0x41)	**WDTCSR**	**(0x60)**	
SREG	0x3F (0x5F)	SREG	0x3F (0x5F)	I/O Memory 0x20-0x3F (0x40-0x5F)
SPH	0x3E (0x5E)	SPH	0x3E (0x5E)	
SPL	0x3D (0x5D)	SPL	0x3D (0x5D)	
SPMCR	0x37 (0x57)	SPMCSR	0x37 (0x57)	
GICR	0x3B (0x5B)	**EIMSK**	**0x1D (0x3D)**	
GICR	0x3B (0x5B)	**MCUCR**	**0x35 (0x55)**	
SFIOR	0x30 (0x50)	**MCUCR**	**0x35 (0x55)**	
MCUCSR	0x34 (0x54)	MCUSR	0x34 (0x54)	
MCUCR	0x35 (0x55)	**SMCR**	**0x33 (0x53)**	
ACSR	0x08 (0x28)	ACSR	0x30 (0x50)	
SPDR	0x0F (0x2F)	SPDR	0x2E (0x4E)	
SPSR	0x0E (0x2E)	SPSR	0x2D (0x4D)	
SPCR	0x0D (0x2D)	SPCR	0x2C (0x4C)	
TCNT0	0x32 (0x52)	TCNT0	0x26 (0x46)	
TCCR0	0x33 (0x53)	TCCR0B	0x25 (0x45)	
SFIOR	0x30 (0x50)	**GTCCR**	**0x23 (0x43)**	
EEARH	0x1F (0x3F)	EEARH	0x22 (0x42)	
EEARL	0x1E (0x3E)	EEARL	0x21 (0x41)	
EEDR	0x1D (0x3D)	EEDR	0x20 (0x40)	
EECR	0x1C (0x3C)	EECR	0x1F (0x3F)	I/O Memory 0x00-0x1F (0x20-0x3F)
GICR	0x3B (0x5B)	**EIMSK**	**0x1D (0x3D)**	
GIFR	0x3A (0x5A)	**EIFR**	**0x1C (0x3C)**	
TIFR	0x38 (0x58)	**TIFR2**	**0x17 (0x37)**	
TIFR	0x38 (0x58)	**TIFR1**	**0x16 (0x36)**	
TIFR	0x38 (0x58)	**TIFR0**	**0x15 (0x35)**	

Table 2. All I/O registers on ATmega8 with their Atmega88 equivalent. Bolded I/O registers are not functionally equivalent, see Table 4 for detailed information. (cont.)

ATmega8		**ATmega88**		
I/O Register name	**I/O Register address**	**I/O Register name**	**I/O Register address**	
PORTD	0x12 (0x32)	PORTD	0x0B (0x2B)	I/O Memory 0x00-0x1F (0x20-0x3F)
DDRD	0x11 (0x31)	DDRD	0x0A (0x2A)	
PIND	0x10 (0x30)	PIND	0x09 (0x29)	
PORTC	0x15 (0x35)	PORTC	0x08 (0x28)	
DDRC	0x14 (0x34)	DDRC	0x07 (0x27)	
PINC	0x13 (0x33)	PINC	0x06 (0x26)	
PORTB	0x18 (0x38)	PORTB	0x05 (0x25)	
DDRB	0x17 (0x37)	DDRB	0x04 (0x24)	
PINB	0x16 (0x36)	PINB	0x03 (0x23)	

(1) The I/O register is accessed different in each device. See "Accessing the USART Control Registers".

Table 3. I/O registers that have changed names, and preserve the same functionality

ATmega8	**ATmega88**
MCUCSR	MCUSR
OCR2	OCR2A
SPMCR	SPMCSR
TCCR0	TCCR0B
UBRRL	UBRR0L
UCSRA	UCSR0A
UCSRB	UCSR0B
UDR	UDR0

The I/O Registers listed in Table 4 have not maintained the same functionality as some of the bits are changed or moved compared to ATmega88. The functionality of the bits listed is preserved although they moved to other registers. See Table 5 for information on I/O register bits that have changed names.

Table 4. I/O registers that are not functionally equal to their equivalent. The table shows where to find the I/O register bits that are not located in the same position between the devices.

ATmega8									ATmega88								
Name	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Name**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	ASSR	–	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB
GICR	INT1	INT0	–	–	–	–	IVSEL	IVCE	MCUCR	–	–	–	PUD	–	–	IVSEL	IVCE
									EIMSK	–	–	–	–	–	–	INT1	INT0
GIFR	INTF1	INTF0	–	–	–	–	–	–	EIFR	–	–	–	–	–	–	INTF1	INTF0
MCUCR	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	EICRA	–	–	–	–	ISC11	ISC10	ISC01	ISC00
									SMCR	–	–	–	–	SM2	SM1	SM0	SE
SFIOR	–	–	–	–	ACME	PUD	PSR2	PSR10	GTCCR	TSM	–	–	–	–	–	PSRASY	PSRSYNC
									ADCSRB	–	ACME	–	–	–	ADTS2	ADTS1	ADTS0
									MCUCR	–	–	–	PUD	–	–	IVSEL	IVCE
TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10
									TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–
TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	TCCR2B	FOC2A	FOC2B	–	–	WGM22	CS22	CS21	CS20
									TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	–	–	WGM21	WGM20
TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	–	TOV0	TIFR0	–	–	–	–	–	OCF0B	OCF0A	TOV0
									TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1
									TIFR2	–	–	–	–	–	OCF2B	OCF2A	TOV2
TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	TIMSK0	–	–	–	–	–	OCIE0B	OCIE0A	TOIE0
									TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1
									TIMSK2	–	–	–	–	–	OCIE2B	OCIE2A	TOIE2

Table 5 contains a list of I/O register bits that have changed names, but fully preserved the same functionality. Note that the bits may have changed location to different IO register (See Table 4). Both old and new bit and register names are listed in Table 5.

Table 5. I/O Register Bits that have changed names, but preserve the same functionality.

Bit name in ATmega8	**Located in I/O Register in ATmega8**	**Bit name in ATmega88**	**Located in I/O Register in ATmega88**
ADFR	ADCSRA	ADATE	ADCSRA
OCR2UB	ASSR	OCR2AUB	ASSR
TCR2UB	ASSR	TCR2AUB	ASSR
EEMWE	EECR	EEMPE	EECR
EEWE	EECR	EEPE	EECR
PSR10	SFIOR	PSRSYNC	GTCCR
PSR2	SFIOR	PSRASY	GTCCR
COM20	TCCR2	COM2A0	TCCR2B
COM21	TCCR2	COM2A1	TCCR2B
FOC2	TCCR2	FOC2A	TCCR2B
DOR	UCSRA	DOR0	UCSR0A
FE	UCSRA	FE0	UCSR0A
MPCM	UCSRA	MPCM0	UCSR0A
PE	UCSRA	UPE0	UCSR0A
RXC	UCSRA	RXC0	UCSR0A
TXC	UCSRA	TXC0	UCSR0A
U2X	UCSRA	U2X0	UCSR0A
UDRE	UCSRA	UDRE0	UCSR0A
RXB8	UCSRB	RXB80	UCSR0B
RXCIE	UCSRB	RXCIE0	UCSR0B
RXEN	UCSRB	RXEN0	UCSR0B
TXB8	UCSRB	TXB80	UCSR0B
TXCIE	UCSRB	TXCIE0	UCSR0B
TXEN	UCSRB	TXEN0	UCSR0B
UCSZ2	UCSRB	UCSZ02	UCSR0B
UDRIE	UCSRB	UDRIE0	UCSR0B
UCPOL	UCSRC	UCPOL0	UCSR0C
UCSZ0	UCSRC	UCSZ00	UCSR0C
UCSZ1	UCSRC	UCSZ01	UCSR0C
UMSEL	UCSRC	UMSEL00	UCSR0C
UPM0	UCSRC	UPM00	UCSR0C
UPM1	UCSRC	UPM01	UCSR0C
USBS	UCSRC	USBS0	UCSR0C

Oscillators and Start-up Delays

ATmega88 has nearly all the same clock options, settings and timing as the ATmega8. An exception is that ATmega88 does not support the use of an External RC Oscillator. All start-up delays on ATmega88 have a constant of 14 clock cycles added to the standard value. The functionality of the Clock Select bits (CKSEL3..0, SUT1,0, CKOPT) themselves are not equal between the devices. Refer to the datasheet to find new matching settings for the clock select configuration.

The ATmega88 has a new system clock prescaler that can/has to be altered runtime from the application code to achieve the desired system clock frequency.

Brown Out Detection

The Brown Out Detection (BOD) options are similar between the devices. However, the bit setting to select the BOD configuration varies. Table 6 and Table 7 show the settings for the two devices. Note that the voltage BOD levels are higher on ATmega88 then on ATmega8.

Table 6. BOD fuse configuration on ATmega8

BODEN	BODLEVEL	Typical V_{BOT}
0	1	2.6
0	0	4.0
1	1	BOD disabled
1	0	BOD disabled

Table 7. BOD fuse configuration on ATmega88

BODLEVEL 2..0	Typical VBOT
111	BOD disabled
110	1.8
101	2.7
100	4.3

Accessing the USART Control Registers

In ATmega8, UCSRC and UBRRH share the same I/O register address, and special handling involving presetting the URSEL bit is necessary to access the desired register.

In ATmega88 UCSRC and UBRRH are split into separate I/O registers addresses, and must be accessed as two individual registers. The MSB bit in the UCSRC register that contained the register select bit (URSEL) in ATmega8, is used for other purposes in ATmega88.

Table 8. Register bits in the USART that have changed functionality

Device	I/O register	Bit #							
		7	6	5	4	3	2	1	0
ATmega8	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL
ATmega88	UCSRnC	UMSELn1	UMSELn0	UPMn1	UPMn0	USBSn	UCSZn1	UCSZn0	UCPOLn

Internal Voltage Reference

The internal voltage reference can be used as input to the Analog Comparator and Analog to Digital Converter. Table 9 lists the typical values for these references.

Table 9. Typical internal voltage references values

	ATmega8	**ATmega88**
Analog Comparator	1.23 V	1.1 V
Analog to Digital Converter	2.56 V	1.1 V

The Watchdog Timer

The Watchdog Timer Prescaler settings are different from ATmega8 to ATmega88. Please refer to the WDTCSR register description in the datasheets for details.

The Programming Interface

Changes have been made to the programming interfaces. The changes apply to both serial programming (ISP) and parallel programming. E.g. added support for new fuses.

See the datasheets for details.

Fuse settings

ATmega88 has more fuses than ATmega8. Many fuses are located in different locations in each of the devices. However the functionality remains the same for each fuse bit. Except the fuses for clock settings (CKOPT, CKSEL3..0, SUT1,0) and the Brown Out Detection Level (BODLEVEL). For more information on these settings refer to the Clock settings section and “Brown Out Detection” section in this document or the datasheet.

Table 10. Comparison of Fuse bits. Moved fuse bits are marked in bold face. Fuses with new functionality or removed, are marked in italic.

Bit #		**ATmega8**	**ATmega88**
Extended Fuse Byte	7	N/A	–
	6	N/A	–
	5	N/A	–
	4	N/A	–
	3	N/A	–
	2	N/A	BOOTSZ1
	1	N/A	BOOTSZ0
	0	N/A	BOOTRST
High Fuse Byte	7	RSTDISBL	RSTDISBL
	6	**WDTON**	DWEN
	5	SPIEN	SPIEN
	4	*CKOPT*	WDTON
	3	EESAVE	EESAVE
	2	**BOOTSZ1**	BODLEVEL2
	1	**BOOTSZ0**	BODLEVEL1
	0	**BOOTRST**	BODLEVEL0
Low Fuse Byte	7	***BODLEVEL***	CKDIV8
	6	***BODEN***	CKOUT
	5	*SUT1*	SUT1
	4	*SUT0*	SUT0
	3	*CKSEL3*	CKSEL3
	2	*CKSEL2*	CKSEL2
	1	*CKSEL1*	CKSEL1

	0	*CKSEL0*	CKSEL0

Device Signatures

ATmega8 has Signature Bytes: 0x1E 0x93 0x07.

ATmega88 has Signature Bytes 0x1E 0x93 0x0A.

Internal RC Oscillator Calibration Byte

ATmega8 has four different calibration values, where special actions need to be taken to load the values for 2, 4 and 8 MHz into the Oscillator Calibration Register (OSCCAL) at runtime.

ATmega88 has only one calibration value, and this value is loaded automatically during startup. The clock prescaler is hence used to change the MCU speed. Refer the clock options chapter in the datasheet for detailed information.

EERPOM Write time

The EEPROM programming time has decreased from ATmega8 to ATmega88.

On ATmega8 t_{WD_EEPROM}, from CPU, is typical 8.5ms.

On ATmega88 t_{WD_EEPROM}, from CPU, is typical 3.4ms

Analog to Digital Converter

The ADC characteristics on ATmega88 are different then on ATmega8. See datasheet for detailed information.

Operational Voltage Ranges

Table 11. Operating voltage and Speed grades.

	Operating Voltage	Speed Grade
ATmega8	4.5 - 5.5V	0 - 16 MHz
ATmega8L	2.7 - 5.5V	0 - 8 MHz
ATmega88	2.7 - 5.5V	0 - 10 MHz @ 2.7 - 5.5V 0 - 20 MHz @ 4.5 - 5.5V
ATmega88V	1.8 - 5.5V	0 - 4 MHz @ 1.8 - 5.5V 0 - 10 MHz @ 2.7 - 5.5V

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