LX1720: High Efficiency Class-D Stereo Audio Amplifier Controller IC

LINFINITY

M I C R O E L E C T R O N I C S

INTRODUCTION

The LX1720 controller IC contains the necessary functions to implement a stereo Class-D audio amplifier. A Class-D amplifier is a "switching" amplifier that converts a low-level, analog, audio input signal into a high-power, pulse-width modulated (PWM) output. The switching frequency is much higher than the audio band which allows high frequency out-of-band components to be removed with a simple LC filter. The LX1720 generates a PWM output by controlling external MOSFET's connected in a full-bridge configuration. Because the MOSFET's are either full "on" or full "off", their power dissipation is minimal allowing maximum power to be delivered to the speaker. The LX1720 can deliver 10 Watts (rms) per channel into an 8 ohm load using a single 15-volt supply.

THEORY OF OPERATION

The block diagram for a single channel is shown in Figure 1. Each channel consists of a control loop that adjusts the PWM output to "track" the audio input signal.
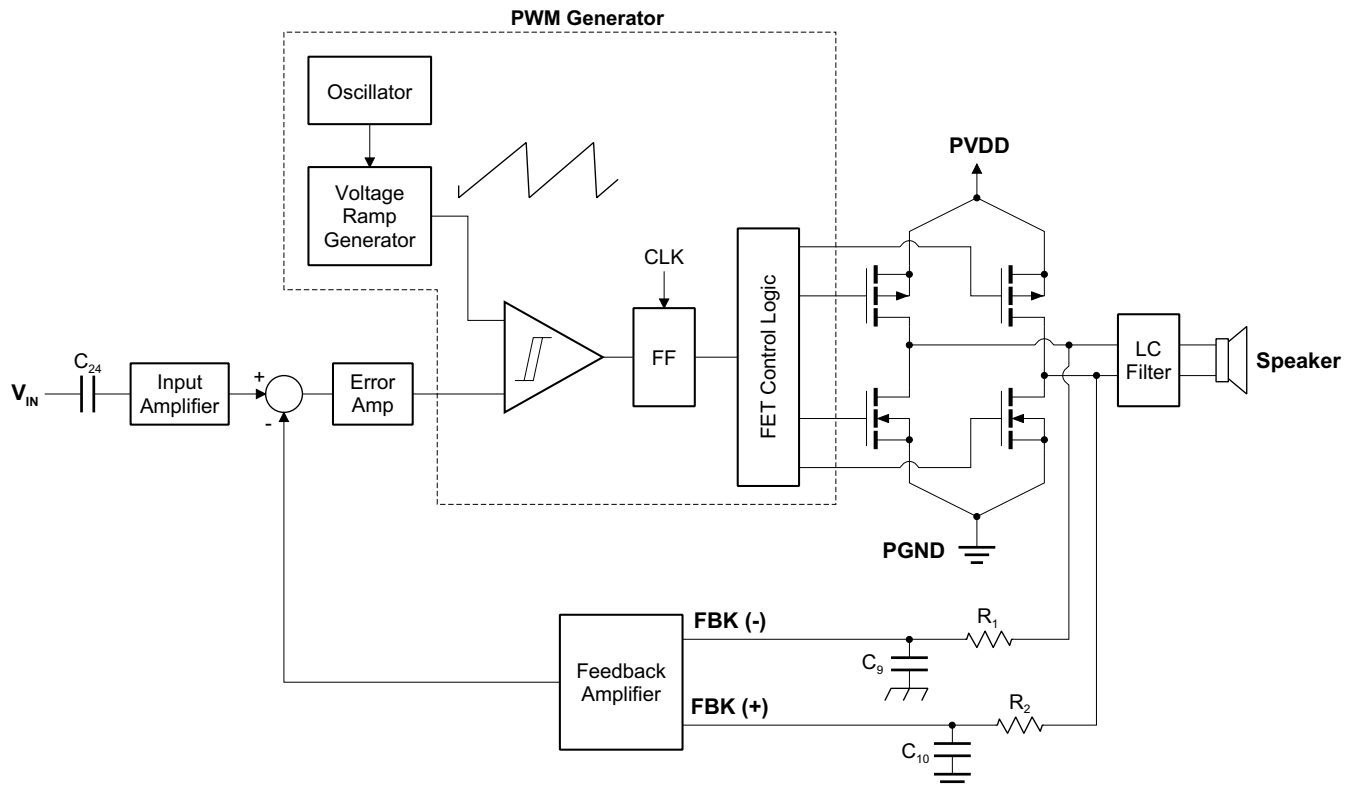

Figure 1: Single Channel Block Diagram

Output Stage

Four external MOSFETs are connected in a full-bridge configuration connected between a single supply (PVDD) and ground (PGND). The output of the MOSFET bridge drives a differential LC filter which removes the switching frequency components of the PWM output prior to driving the speaker. In practice, the bridge alternately connects the LC filter inputs between PVDD and PGND as shown in Figure 1. (Note that no multiple or split-supplies are required – all large currents flow between PVDD and PGND.)

Feedback Amplifier

The bridge output also drives two single-pole RC lowpass filters consisting of components R_1, C_9 and R_2, C_{10}. The RC filter outputs provide the feedback for the control loop via the FBK+ and FBK- inputs. Inside the LX1720, these two differential inputs are converted to a single-ended signal by the feedback amplifier. The feedback amplifier also attenuates the feedback signals and level shifts its output to 2.5 volts.

Input Amplifier

The single-ended audio input is AC coupled into the LX1720 via external capacitor C24. An op-amp inside the LX1720 level shifts the input signal to 2.5 volts and also provides gain.

Error Amplifier

The input amplifier's output is fed to the error amplifier. The output of the feedback amplifier is also fed to the error amplifier. The error amplifier integrates the "error signal" i.e. it integrates the difference between the audio input and the feedback signal. The output of the error amplifier represents the desired audio output signal.

PWM Generator

The output of the error amplifier, EAOUT, is fed to a comparator that compares EAOUT to a voltage ramp waveform. The voltage ramp repeats at the switching frequency which is much greater than the audio band of interest. At the beginning of the ramp, the comparator output is reset high. When the ramp voltage exceeds EAOUT, the comparator output switches low. Thus, the pulse-width or duty-cycle of the comparator output is proportional to the voltage at EAOUT.

The comparator output is latched into a flip-flop which drives the external MOSFETs to complete the control loop. The action of the control loop causes the PWM output to accurately track the audio input signal.

IMPLEMENTATION DETAILS AND DESIGN EQUATIONS

Amplifiers

There are three amplifiers for each channel that are critical for the operation of the circuit. To avoid redundancy, only the right channel will be described.   Referring to Figure 2, these amplifiers are the Input Amplifier, the Feedback Amplifier, and the Error Amplifier.

Figure 2: Amplifiers

The Input Amplifier is an inverting amplifier with a gain of $G_{IN}=3.5$ set by on-chip resistors. The input must be AC coupled via an external capacitor C_{24}.   The input resistance is approximately $R_{IN} = 42k\Omega$. This results in a high-pass characteristic with a low frequency roll-off starting at

$$f_{LOWER} = \frac{1}{2\pi R_{IN} C_{24}}$$

Therefore, the minimum value for C_{24} required to pass signals as low as 20Hz is given by

$$C_{24} = \frac{1}{2\pi f_{LOWER} R_{IN}} = \frac{1}{2\pi (42k\Omega)(20Hz)} = 190nF$$

There are two external RC filters that smooth the PWM output prior to feeding the signal back into the LX1720. The transfer function for these low-pass filters is given by

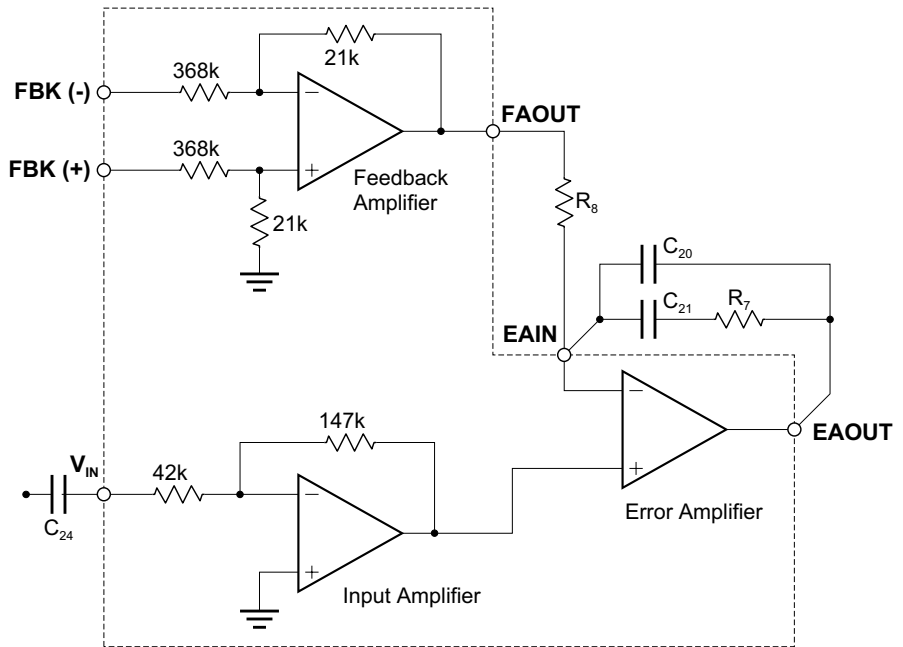$$G_{RC} = \frac{1}{(sR_1 C_9 + 1)}$$

The upper roll-off frequency of the RC filter should be set equal to the upper edge of the desired audio band.

$$f_{UPPER} = \frac{1}{2\pi R_1 C_9}$$

A good starting value for R_1 is to make sure it is less than 1/10 of the 368kΩ input impedance of the feedback amplifier. (This minimizes loading effects.) Therefore, R_1 should be set to 32kΩ or less. C_9 can then be calculated as

$$C_9 = \frac{1}{2\pi \ R_1 \ f_{UPPER}}$$

For R_1=32kΩ and f_{UPPER}=20kHz, C_9=249pF.

The Feedback Amplifier has a gain of either G_{FB}=1/11=0.091. Because the range of the feedback signals is from PGND to PVDD attenuation is required...i.e. the feedback amplifier gain is less than 1.

V
The inverting input and the output of the error amplifier are brought off-chip so that the user can set the resistor and capacitor values. The error amplifier acts primarily as an integrator. As shown in Figure 2, the external components consist of an input resistor R_8, integrator capacitors C_{20} and C_{21}, and a zero forming resistor R_7. The transfer function of the error amplifier is given by

$$G_{EA} = \frac{EAOUT}{FAOUT} = -\left(\frac{1}{sR_8(C_{20}+C_{21})}\right)\frac{(1+sR_7C_{21})}{\left(1+sR_7\left(\frac{C_{20}C_{21}}{C_{20}+C_{21}}\right)\right)}$$

A discussion on determining the external component values for the error amplifier is found in the section "Calculating the Loop Gain".

Oscillator

The on-chip oscillator sets the switching frequency for the LX1720. The frequency of the oscillator is controlled by an external resistor and capacitor. The oscillator frequency is given by

$$f_{OSC} = \frac{1}{(R_T + 1250)C_T}$$

where it should be remembered that the value of C_T must include the contributions from package pin and PCB trace capacitance. This parasitic capacitance is usually on the order of 3pF to 5pF. A good choice for CT is 100pF.

PWM Generator

The PWM generator shown in Figure 3 consists of a voltage ramp generator, a comparator, and logic. The voltage ramp is generated by charging an off-chip capacitor (C_{PWM}) with a current that is set by an off-chip resistor (R_{PWM}). The charging current is proportional to the supply voltage VDD and is given by

$$I_{PWM} = \frac{\left(\frac{3}{8}V_{DD}\right)}{R_{PWM}}$$

I_{PWM} should be set between 75uA and 300uA. Thus for V_{DD}(max.) = 15V and R_{PWM} = 30kΩ, the value of I_{PWM} is 187.5μA.

The period of the PWM voltage ramp is set by the oscillator and is given by $T_{OSC} = 1/f_{OSC}$. For optimal dynamic range the PWM voltage ramp should travel it's full 3 volt range within the time period T_{OSC}. Therefore the value of C_{PWM} can be found by

$$C_{PWM} = \frac{(I_{PWM})(T_{OSC})}{3volts} = \frac{(V_{DD}\max)(T_{OSC})}{8R_{PWM}}$$

Note that when the error amplifier output, EAOUT, matches the minimum value of the PWM voltage ramp the output duty-cycle should be zero. Conversely, when EAOUT matches the maximum value of the PWM voltage ramp the output duty-cycle should be 100%. Thus as the error amplifier output ranges over the full range of the PWM ramp during T_{OSC}, the average value of the bridge output ranges from $-V_{DD}$ to $+V_{DD}$. The gain of the PWM generator can therefore be calculated by

Figure 3: PWM Generation

$$G_{PWM} = \frac{V_{OUT}}{EA_{OUT}} = \frac{2V_{DD}}{\left(\frac{I_{PWM}T_{OSC}}{C_{PWM}}\right)} = \frac{2V_{DD}C_{PWM}}{\left(\frac{(3/8)V_{DD}}{R_{PWM}}T_{OSC}\right)} = \frac{f_{OSC}R_{PWM}C_{PWM}}{0.1875}$$

Note that the gain of the PWM generator is independent of VDD. This makes it easier to insure the stability of the feedback loop over a wide range of supply voltages.

CALCULATING THE LOOP GAIN

The loop gain for the LX1720 is the product of all the gains derived in the prior sections.

$$G_{RC}G_{FB}G_{EA}G_{PWM} = \frac{1}{(sC_9R_1 + 1)}G_{FB}\left(\frac{1}{sR_8(C_{20} + C_{21})}\right)\frac{(1 + sR_7C_{21})}{\left(1 + sR_7\left(\frac{C_{20}C_{21}}{C_{20} + C_{21}}\right)\right)}\frac{f_{OSC}R_{PWM}C_{PWM}}{0.1875}$$

In order increase the bandwidth and improve phase margin of the control loop, the value of the feed-forward zero in the error amplifier is set equal to the low-pass pole of the feedback RC filter. Thus we set

$$R_1C_9 = R_7C_{21}$$

The loop gain can therefore be simplified to

$$LoopGain = G_{RC}G_{FB}G_{EA}G_{PWM} = G_{FB}\left(\frac{1}{sR_8(C_{20} + C_{21})}\right)\frac{1}{\left(1 + sR_7\left(\frac{C_{20}C_{21}}{C_{20} + C_{21}}\right)\right)}\frac{f_{OSC}R_{PWM}C_{PWM}}{0.1875}$$
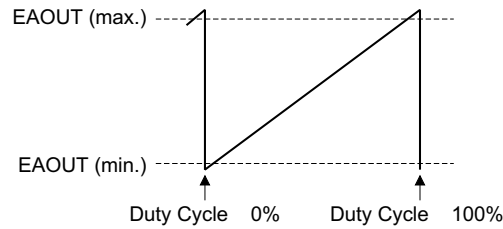
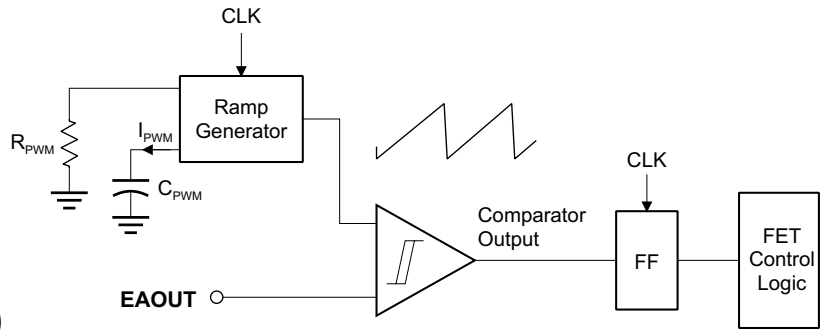Note that there is one pole at zero frequency formed by R_8 and the sum of the integrator capacitors C_{20} and C_{21}. There is also a high frequency pole formed by R_7 and the series combination of C_{20} and C_{21}. If C_{21} is much larger than C_{20}, then the unity gain frequency, f_U, for the control loop can be found by

$$f_U = \frac{G_{FB} f_{OSC} R_{PWM} C_{PWM}}{0.1875(2\pi) R_8 (C_{20} + C_{21})}$$

Assuming the $C_{21} = 9C_{20}$ yields

$$f_U = \frac{G_{FB} f_{OSC} R_{PWM} C_{PWM}}{0.1875(2\pi) R_8 (10)(C_{20})}$$

Given R_8 and a desired unity gain frequency, C_{20} is given by

$$C_{20} = \frac{G_{FB} f_{OSC} R_{PWM} C_{PWM}}{0.1875(2\pi) R_8 (10)(f_U)}$$

The input resistor R_8 can be conveniently chosen as 10kΩ. A design guideline is to place the unity gain frequency well above the audio band but below the high frequency pole. Since the audio band normally ends around 20kHz and the high frequency pole is normally set around ½ of the switching frequency at approximately 150kHz, the unity gain frequency can be targeted at 60kHz.

DESIGN EXAMPLE

The design process starts by deciding the oscillator frequency. Typical operating frequencies for full audio bandwidth will be in the range of 300kHz to 500kHz. For this design, the oscillator frequency is chosen to be 330kHz. The audio band for this example extends from 20Hz to 20kHz. The speakers to be driven have an impedance of 8Ω. The maximum supply voltage is V_{DD}(max.)=15 volts.

Step 1 – Calculate the Oscillator Component Values

The LX1720 allows both the R_T and C_T components to be external for maximum flexibility.
Choosing C_T=100pF, R_T is given by

$$R_T = \frac{1}{f_{OSC} C_T} = \frac{1}{(330kHz)(100pf)} = 30.3k\Omega \qquad \text{A standard 1\% value for } R_T \text{ is } 30.1k\Omega.$$

Step 2 – Calculate the PWM Ramp Component Values

Choosing R_{PWM}=56kΩ, the PWM ramp current is given by

$$I_{PWM} = \frac{\left(\frac{3}{8} V_{DD}\right)}{R_{PWM}} = \frac{(3/8)(15 volts)}{56k\Omega} = 100\mu a \qquad \text{A standard 1\% value for } R_{PWM} \text{ is } 56.2k\Omega.$$

which is acceptable. The value for C_{PWM} is given by

$$C_{PWM} = \frac{(V_{DD} \max)(R_T C_T)}{8 R_{PWM}} = \frac{(15 volts)(30.3k\Omega)(100 pF)}{8(56k\Omega)} = 101 pF \qquad \text{A standard value for } C_{PWM} \text{ is } 100pF.$$

Step 3 – Calculate the Feedback Lowpass Filter Component Values

Choosing the value of 32kΩ for R_1 and R_2 and given the upper audio band-edge of 20kHz, the values for $C_9=C_{10}$ are given by

$$C_9 = C_{10} = \frac{1}{2\pi\,R_1 f_{UPPER}} = \frac{1}{2\pi\,(32k\Omega)(20kHz)} = 249\,pF$$

Step 4 – Calculate the Error Amplifier Component Values

The value for R_8 is chosen to be 10kΩ. Choosing 60kHz as the unity gain frequency for the loop gain and assuming that $C_{21} = 9C_{20}$, the value of C_{20} can be determined by

$$C_{20} = \frac{G_{FB}\,f_{OSC}\,R_{PWM}\,C_{PWM}}{0.1875\,(2\pi)R_8(10)(f_U)} = \frac{(0.091)(330kHz)(56\,k\Omega)(101\,pf)}{0.1875\,(2\pi)(10k\Omega)(10)(60kHz)} = 24\,pF$$

$C_{21} = 9C_{20}$ is therefore 216pF. R_7 can now be calculated by equating the feedback pole to the feed-forward zero.

$$R_1 C_9 = R_7 C_{21}$$

Such that

$$R_7 = \frac{R_1 C_9}{C_{21}} = \frac{(32k\Omega)(249\,pF)}{216\,pF} = 36.9k\Omega$$

Step 5 – Calculate the Input DC Decoupling Capacitor Values

The input decoupling capacitors see an input impedance of approximately 42kΩ. In order to pass audio input signals down to 20Hz, the minimum value for C_{24} is given by

$$C_{24} = \frac{1}{2\pi\,f_{LOWER} R_{IN}} = \frac{1}{2\pi\,(42k\Omega)(20Hz)} = 190nF$$

Note that the LX1720 has an under-voltage lockout circuit which prevents the output drivers from switching until the IC has sufficient voltage to operate. In addition, at power-up, the oscillator runs 10 times slower. A 10-bit delay counter counts 976 of these longer clock cycles prior to enabling the output. This allows time for the input capacitors to charge to their DC values and minimizes the "pop" that might be heard in the loudspeaker. For a nominal switching frequency of 330kHz the enable delay is given by

$$T_{DELAY} = (976)(10)(T_{OSC}) = (976)(10)(3.03\mu\sec) = 30m\sec$$

Once the counter times out, the oscillator frequency is returned to its nominal value. Note from Figure 2 that at power-up, C_{24} must charge to 2.5 volts through resistances of 42kΩ and 147kΩ. The voltage change across C_{24} can be calculated by

$$\Delta V = 2.5 - 5.216 e^{\frac{-t}{42k*C}} = 2.5 - 5.216 e^{\frac{-30m\sec}{(42k)(190nF)}} \qquad for\,\Delta V < 1.78V, use:\ \Delta V = 5\left(1 - e^{\frac{-t}{189k*C}}\right)$$

Thus it can be seen that C_{24} may not charge completely. In order to reduce any remaining "pop" further, the built-in MUTE function of the LX1720 can be used. Pin 23 and Pin 24 are active high, logic inputs that mute their respective channels by "shorting" the internal 147kΩ feedback resistor in the input amplifier. By connecting an external, series RC network between the CN pin and GND as shown in Figure 4, the external input capacitors C_{24} and C_{25} will charge four times faster and any power-on "pop" will be further reduced. The CN pin will rises from GND to 5 volts upon power up. This will pull the MUTE pins high until C_{MUTE} is discharged by R_{MUTE}.

Step 6 – Power MOSFET's and Current Sense Resistors

The maximum undistorted RMS power is roughly proportional to the square of the supply voltage and inversely proportional to the speaker or load impedance. It can be calculated by using the following formula:

$$P_{OUT}(\max) = \frac{R_{LOAD}(V_{DD} - V_{RIPPLE})^2}{2(R_{LOAD} + R_{DISS})^2} = \frac{(8\Omega)(15V - 1V)^2}{2(8\Omega + 1\Omega)^2} = 9.68Watts$$

R_{LOAD} is the load resistance, V_{DD} is the supply voltage, and V_{RIPPLE} is the peak ripple across C_9 (it is calculated to be approximately 1V in this case). R_{DISS} is the total resistance in the current path to the load, including the "ON" resistance of the MOSFETs, the output filter inductor resistances and the current limit resistors.

The RMS value of the load corresponding to the above maximum power is

$$I_{RMS}(\max) = \sqrt{\frac{P_{OUT}(\max)}{R_{LOAD}}} = \sqrt{\frac{(9.68W)}{(8\Omega)}} = 1.1A_{RMS}$$

Thus the conduction power dissipated in the Power MOSFETs will be approximately

$$P_{FETS} = 2R_{DS(ON)}I^2_{RMS(MAX)}$$

Figure 4

The factor of "2" signifies that two MOSFETs are conducting at any given time. Assuming 0.1Ω FETs, only 250mW of conduction power will be dissipated in the MOSFETs with a continuous output power of almost 10 Watts.

The current sense resistors R_5 and R_6 are used for current limiting purposes. The voltage across these resistors is sensed with on-chip comparators having a threshold of approximately 200mV. The value of these resistors can be calculated as follows

$$R_5 = R_6 = \frac{(200mV)}{(\sqrt{2}I_{RMS} + I_{RIPPLE})} = \frac{(200mV)}{(1.555A + 0.2A)} = 115m\Omega$$

where I_{RIPPLE} is the peak filter inductor ripple current. This will typically be 0.2A. In most cases it is advisable to use a somewhat lower value than the one calculated above. In this case 100mΩ will be used.

Step 7 – Calculating the Components for the Output LC Filter

The output L/C filter stages help to reconstruct the amplified audio signal and filter out the switching frequency. The design of these filters depends on the attenuation that is desired at the output. If the amplifier circuit is in close proximity to the speakers then even a single stage filter is sufficient. In this example however, a four-element dual stage filter is used. Each bridge junction will have a two-stage filter section.

There are several different strategies that can be used in the design of this filter. A Legendre-Papoulis approximation for a four-element filter has been used in this case. The corner frequency has been selected to be 80kHz. Thus providing approximately $18mV_{RMS}$ of 330kHz ripple at the speaker outputs. Reducing the corner frequency of the filter can reduce the ripple, however it is not recommended that the corner frequency be lower than 60kHz for full audio band amplification.
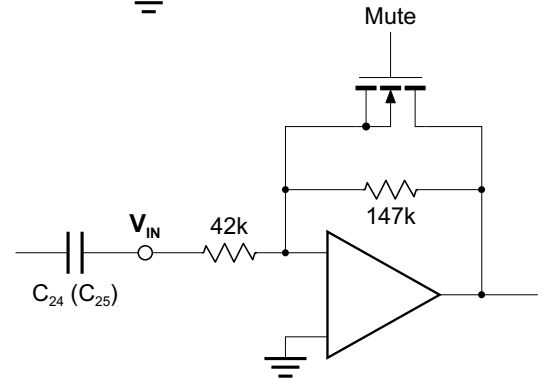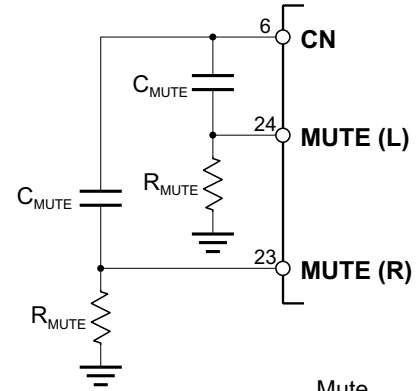
The resultant values from standard filter look-up tables yielded the values shown below. Load resistance was assumed to be 8Ω.

$\ell_1 = 25\mu H$

$c_1 = 413nF$

$\ell_2 = 22.7\mu H$

$c_2 = 159nF$

The following values were chosen for the actual design:

$\ell_1 = 25\mu H$

$c_1 = 470nF$

$\ell_2 = 25\mu H$

$c_2 = 150nF$

The table below gives the normalized circuit elements for a four-element Butterworth and Legendre-Papoulis filter circuits. A zero source impedance is assumed.

Fiter Type	Normalized Filter Elements			
	ℓ_1	c_1	ℓ_2	c_2
Butterworth	1.5307	1.5772	1.0824	0.3827
Legendre-Papoulis	1.612	1.6616	1.4292	0.6399

Actual values can be calculated from the above table by the following transformations:

$$L_1 \ (actual) = \frac{\ell_1 RL}{2\pi f_C}$$

$$C_1 \ (actual) = \frac{c_1}{2\pi f_C \ RL}$$

$$L_2 \ (actual) = \frac{\ell_2 RL}{2\pi f_C}$$

$$C_2 \ (actual) = \frac{c_2}{2\pi f_C \ RL}$$

Where RL is the load (speaker) impedance connected to the output of the filter, and f_C is the desired 3db corner frequency of the filter network.

SELECTION OF FIXED COMPONENT VALUES (Please refer to Figure 5 below)

The prior example demonstrated how to chose values for the external components in the signal path. This section discusses the selection of fixed components and provides further information on component type and power rating.

As each application has its own criteria, the trade-offs require the user to decide what are acceptable deviations from the items listed below.

- C_P is the supply capacitor or charge transfer capacitor for the FET gate drive. This capacitor should be greater than 1µF (basic Di/Dt rules apply)
- Audio input path capacitors C_{24} and C_{25} should be film capacitors. A quality Poly Phenylene Sulfide (PPS) surface mount device will work well here (tolerance = 1% resistors, 5% capacitors).
- Elements C_{20}, C_{21}, R_7 and R_8 (C_{22}, C_{23}, R_9 and R_{10}) create the right (left) channel compensation network. It is recommended that these devices be surface-mount metal-film resistors and NPO ceramic capacitors when air flow is restricted.
- C_{PWM} and C_T are timing capacitors and should be a stable material at the frequency of operation. For a frequency of 300kHz, a ceramic dielectric is a good choice (tolerance 5%).
- C_N is a filter capacitor that holds the internal voltage reference stable. This capacitor must be greater than 1µF. Using a capacitor larger than 1µF is recommended if space allows. A tantalum 22µF/25V capacitor is a good choice.
- Q_1 through Q_8 can be discrete devices, however there are complimentary P/N channel devices in SO-8 packages. A gate charge of 10nC or less should be chosen. Variations are based upon the LX1720 source sink capabilities to charge/discharge the gate capacitance.
- R_5 and R_6 are the switching circuit current sense resistors, generating a sense voltage proportional to the load current. They should be non-inductive or low inductance.
- C_{16} through C_{19} are power supply bypass capacitors. Their ESR and location effect the capacitance value chosen. The further away from the MOSFETs, the larger the capacitance and the lower the ESR should be. Use Aluminum Electrolytic radial capacitors of no less than 100µF/25V. Capacitors of 220µF placed adjacent to the FETs perform quite well. If the location of bypass is more than 12mm then a low ESR type capacitor will provide better margin against tripping the under-voltage detect mechanism within the IC.
- R_1/C_9 filter elements are used in a 300kHz circuit and the dielectric for C should be suited for high frequency operations.
- Inductors for the filter are commercially available (or may be designed by the user; most ferrite manuals have good magnetics design reference material). The biggest concern is keeping the inductor in its linear region. The first inductor sees the switching signal and is unipolar. The second inductor sees a DC shifted signal. Care should be taken to ensure the inductor will not saturate with a DC bias.
- The capacitor C_1 is a low Xc path to ground for 300kHz, so its dielectric is best selected for that frequency of operation. Ceramic surface mount devices are well suited here. The capacitor C_2 will see predominately low frequency and its dielectric should be chosen (as with C_1) to shunt the residual high-frequency energy to ground.
- L_1 through L_8 inductors can be either hand-wound toroids or purchased button inductors. Using an ungapped core will require a much larger core to ensure operation in the linear region. By choosing a gapped core the high reluctance in the magnetic path keeps the core from saturating (within input power supply ranges).

Layout Notes
- There are 3 grounds in this circuit (Figure 5): audio signal, IC and power for the FETs.
- The power to the IC (IS+, PVDD and VDD) should be their own separate traces that do not carry high current pulses from the switching circuit.
- Care should be taken to keep the high-frequency, high-power currents from flowing through the same piece of copper that the audio signal references to.
- Stray capacitance at RPWM, RT, EAOUT, EAIN, and FAOUT can deteriorate the circuit performance. Keep components associated with these pins close to the body of the IC.
- A sheet of copper (a.k.a. ground plane) is not a generic solution. We have actually had better performance from a well thought out (large) board than a 4 layer board that did not take into account the location of the components.
- Configure the layout so R_5/R_6 and C_{16}-C_{19} are "on top of" the FETs. For example, if 200µF is needed for that channel, 100µF at each SO-8 package for that channel was used.
- Place an additional bypass capacitor at the IS+ pin to compensate for C_{16}-C_{19} being near the FETs.
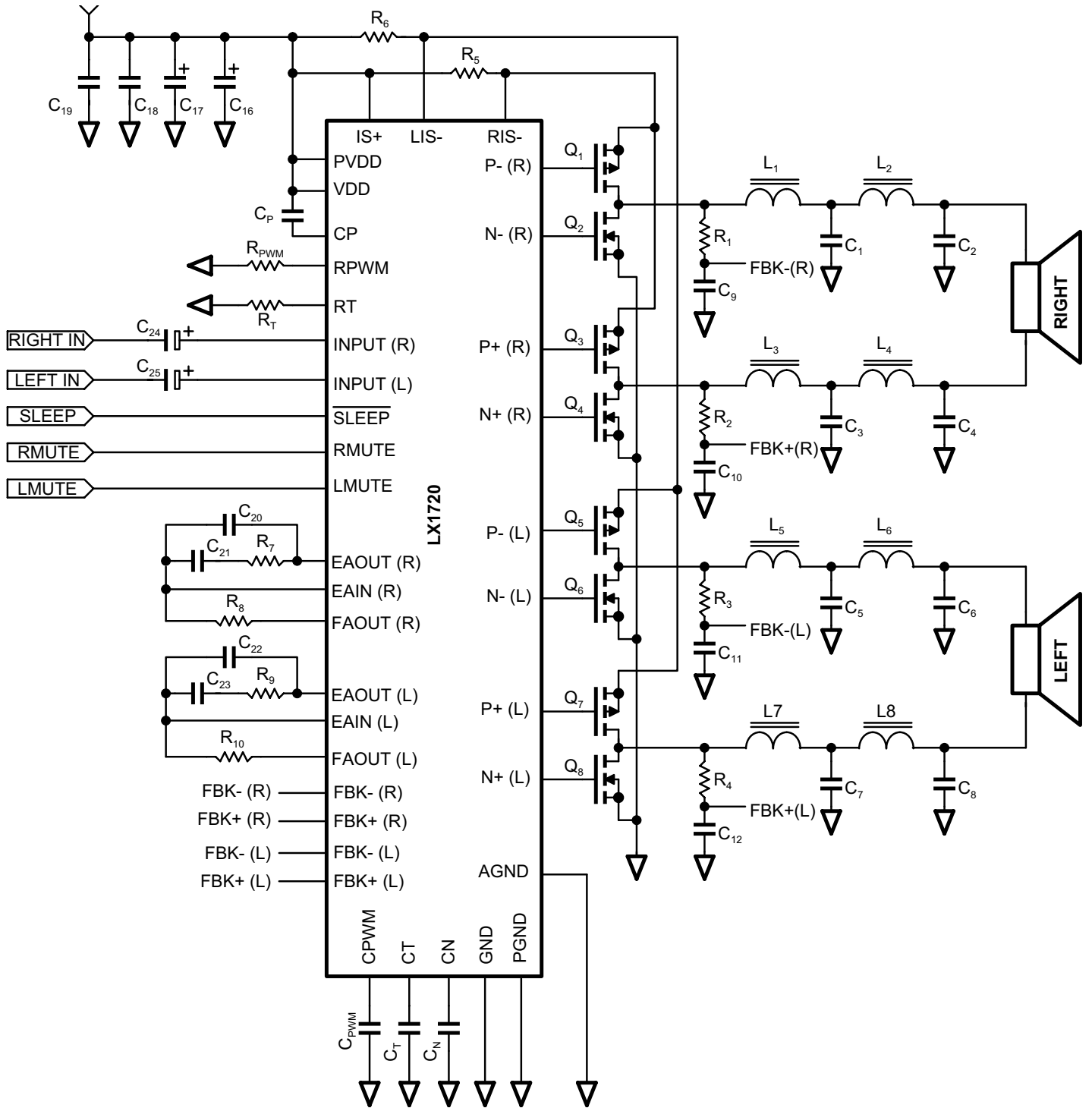
Figure 5