TPG051

RGB Driver/Timing Controller IC

For

LTPS TFT LCD

Product Design department

Toppoly Optoelectronics Corp.

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TPG051

RGB Driver/Timing Controller IC for LTPS TFT LCD

<Description>

This is digital signal processing IC for low temperature poly-silicon TFT-LCD. Handles 8 bits of input data(256-level gray scale data) for each of the RGB or YUV colors and output analog RGB signals from internal Opamp.

This is green product and spec refers to Toppoly's Green Product Chemical Substance Specification Standard Hand Book.

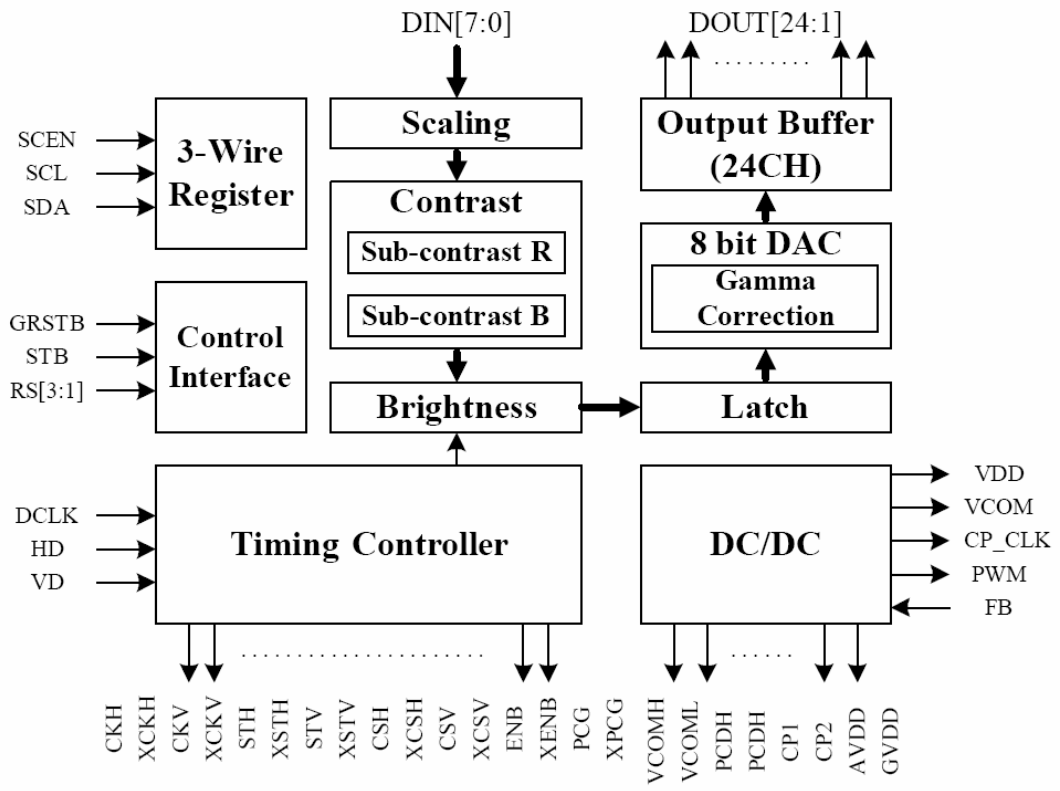
<Features>

* Handles digital signals of serial 8bit(RGB or YUV).
* Installed timing controller to drive LCD panel.
* Output analog RGB signals from internal Opamp.
* Inputs: digital 8 bit serial [RGB or YUV-4:2:2] DCLK, synchronous pulse (HD, VD) serial-control signals.
* Outputs: analog RGB, common data.
* Supply voltage: VCC (digital): 3.0V.
* Supports NTSC and PAL timings.
* 24 channels source driver output with 8-bit DAC.
* 3-wire register control for display and function selection.
* Build-in contrast, brightness and gamma modulation.
* Build-in DC/DC circuit, charge pump circuit, Vcom and pre-charge adjustment circuit.
* Panel dot: 492x240, 558x240, 640x240, 720x240 and 960x240.
* Support strip color filter 960x240(through mode, RGB dummy, YUV input).
* COG package.

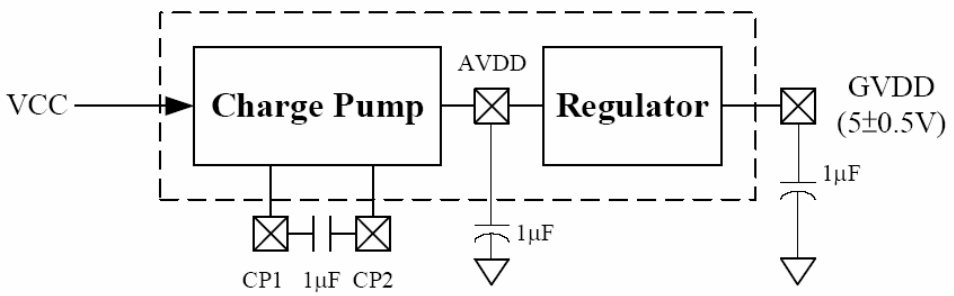
<Absolute Maximum Ratings>

Item	Symbol	Min.	Max.	Unit
Logic supply voltage	V_{CC}	-0.5	+5V	V
Storage temperature	T_{ST}	-50	+100	℃
Operating temperature	T_{OP}	-30	+85	℃

<Block Diagram>

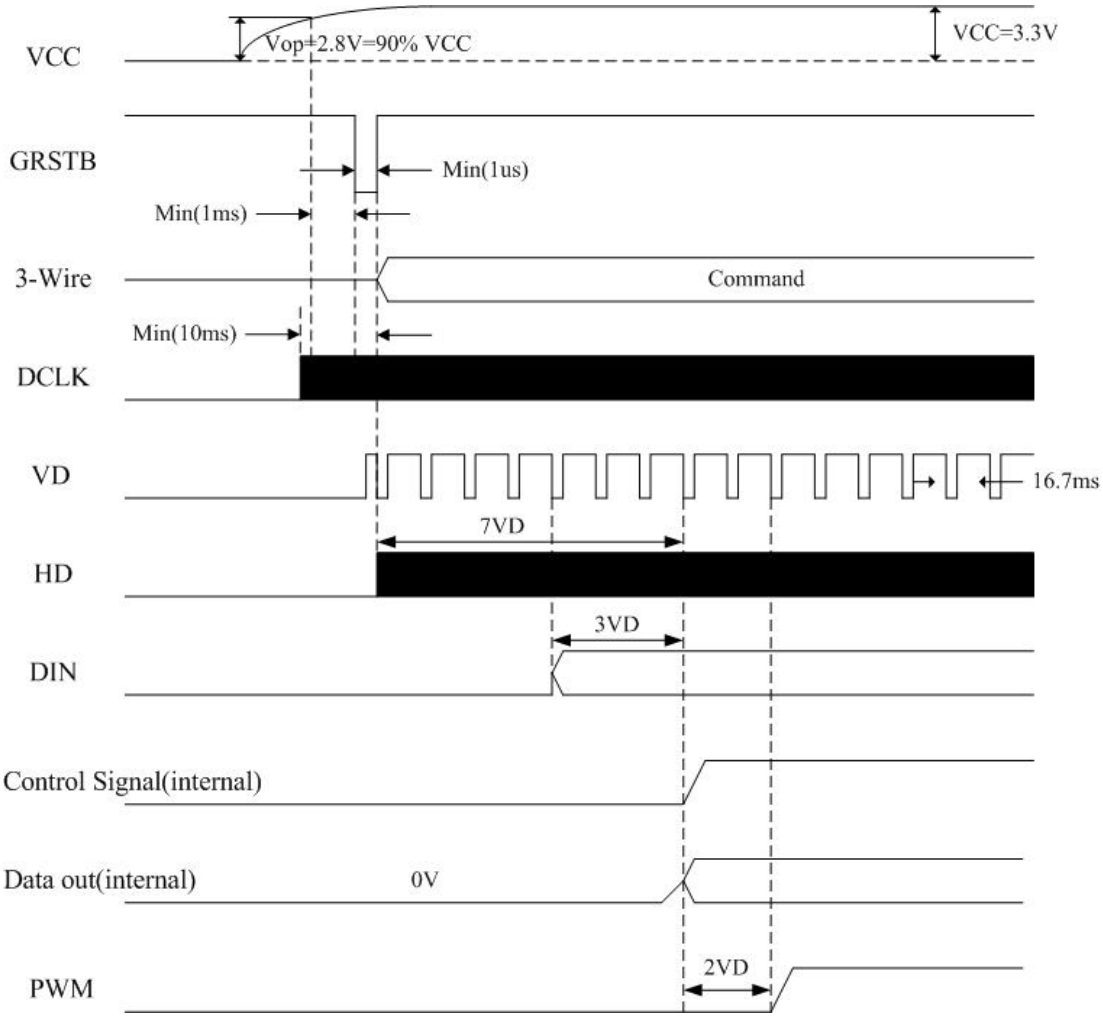


<Charge Pump Circuit>

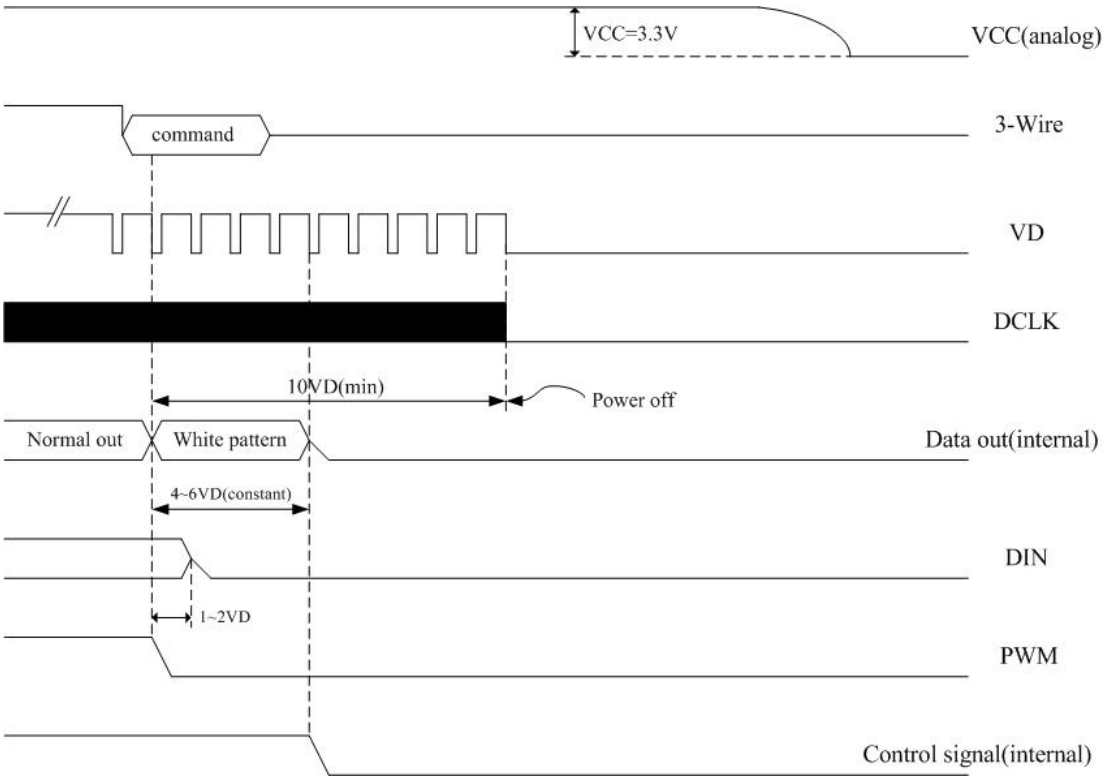


<Power on/off and mode change sequence>

Power on (low power mode, global reset) to normal mode sequence

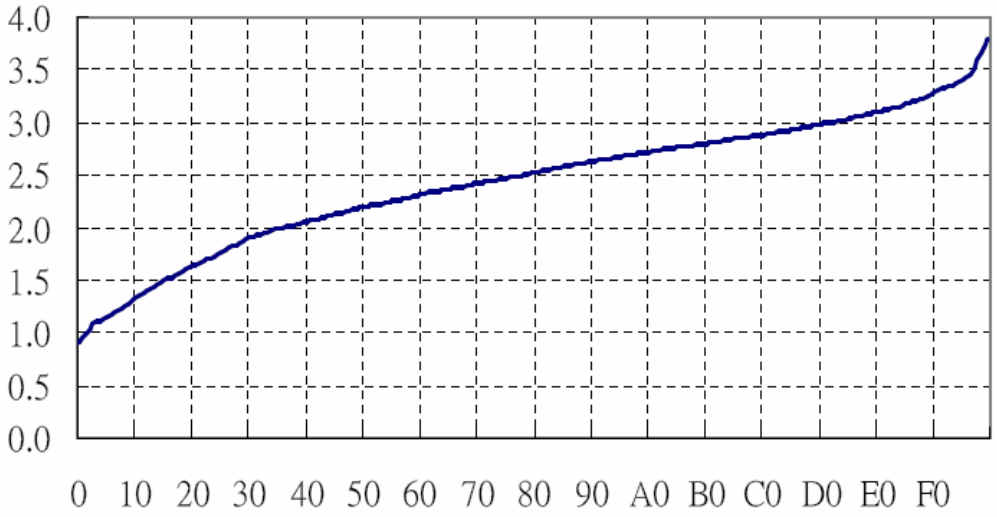


Normal mode to power off (low power mode) sequence

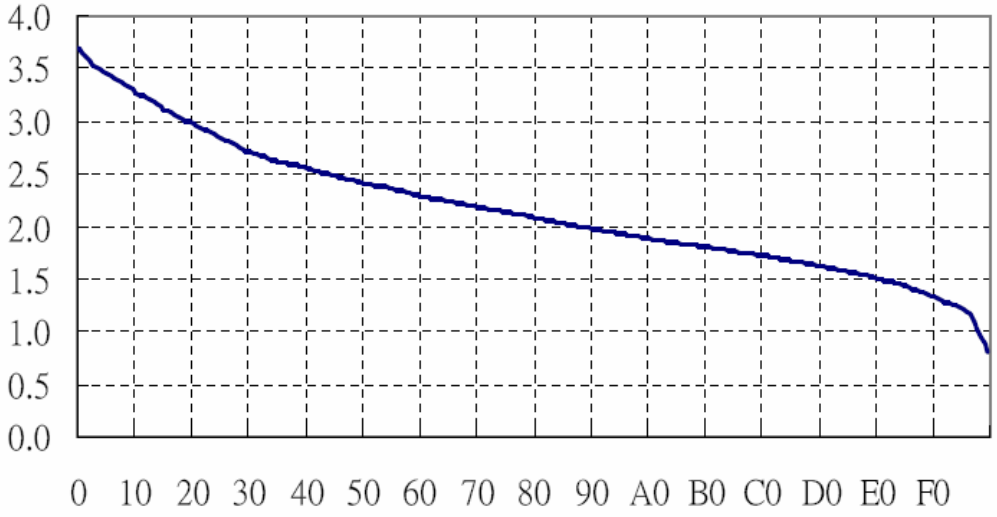


<Relationship between input data and output voltage>

The figure below shows the relationship between the input data and output voltage, please refer to the following pages to get the relative resistor value and voltage calculation method.



Negative Polarity (Vcom = H)



Positive Polarity (Vcom = L)

Output Voltage vs Input Data

(GV_{DD}=5.0V)

Num	Vn	Vp	Num	Vn	Vp	Num	Vn	Vp	Num	Vn	Vp
0	0.900	3.700	40	2.056	2.544	80	2.523	2.077	C0	2.880	1.720
1	0.945	3.655	41	2.064	2.536	81	2.532	2.068	C1	2.886	1.714
2	0.990	3.610	42	2.072	2.528	82	2.538	2.062	C2	2.893	1.707
3	1.035	3.565	43	2.080	2.520	83	2.544	2.056	C3	2.898	1.702
4	1.079	3.521	44	2.089	2.511	84	2.550	2.050	C4	2.904	1.696
5	1.098	3.502	45	2.098	2.502	85	2.556	2.044	C5	2.909	1.691
6	1.117	3.483	46	2.107	2.493	86	2.563	2.037	C6	2.914	1.686
7	1.136	3.464	47	2.117	2.483	87	2.571	2.029	C7	2.922	1.678
8	1.155	3.445	48	2.126	2.474	88	2.578	2.022	C8	2.929	1.671
9	1.174	3.426	49	2.134	2.466	89	2.586	2.014	C9	2.936	1.664
A	1.193	3.407	4A	2.142	2.458	8A	2.591	2.009	CA	2.943	1.657
B	1.212	3.388	4B	2.149	2.451	8B	2.596	2.004	CB	2.948	1.652
C	1.230	3.370	4C	2.157	2.443	8C	2.601	1.999	CC	2.954	1.646
D	1.255	3.345	4D	2.167	2.433	8D	2.606	1.994	CD	2.959	1.641
E	1.280	3.320	4E	2.178	2.422	8E	2.612	1.988	CE	2.964	1.636
F	1.305	3.295	4F	2.188	2.412	8F	2.619	1.981	CF	2.971	1.629
10	1.330	3.270	50	2.198	2.402	90	2.625	1.975	D0	2.978	1.622
11	1.349	3.251	51	2.203	2.397	91	2.632	1.968	D1	2.985	1.615
12	1.368	3.232	52	2.208	2.392	92	2.637	1.963	D2	2.992	1.608
13	1.387	3.213	53	2.212	2.388	93	2.641	1.959	D3	2.998	1.602
14	1.405	3.195	54	2.217	2.383	94	2.646	1.954	D4	3.004	1.596
15	1.427	3.173	55	2.222	2.378	95	2.651	1.949	D5	3.011	1.589
16	1.449	3.151	56	2.230	2.370	96	2.658	1.942	D6	3.017	1.583
17	1.471	3.129	57	2.239	2.361	97	2.664	1.936	D7	3.025	1.575
18	1.492	3.108	58	2.247	2.353	98	2.671	1.929	D8	3.033	1.567
19	1.508	3.092	59	2.256	2.344	99	2.677	1.923	D9	3.041	1.559
1A	1.525	3.075	5A	2.263	2.337	9A	2.682	1.918	DA	3.049	1.551
1B	1.541	3.059	5B	2.271	2.329	9B	2.687	1.913	DB	3.057	1.543
1C	1.557	3.043	5C	2.278	2.322	9C	2.692	1.908	DC	3.064	1.536
1D	1.576	3.024	5D	2.286	2.314	9D	2.697	1.903	DD	3.072	1.528
1E	1.596	3.004	5E	2.295	2.305	9E	2.704	1.896	DE	3.079	1.521
1F	1.615	2.985	5F	2.304	2.296	9F	2.711	1.889	DF	3.088	1.512
20	1.634	2.966	60	2.314	2.286	A0	2.717	1.883	E0	3.098	1.502
21	1.649	2.951	61	2.323	2.277	A1	2.724	1.876	E1	3.107	1.493
22	1.664	2.936	62	2.329	2.271	A2	2.729	1.871	E2	3.117	1.483
23	1.678	2.922	63	2.335	2.265	A3	2.734	1.866	E3	3.124	1.476
24	1.693	2.907	64	2.341	2.259	A4	2.739	1.861	E4	3.130	1.470
25	1.711	2.889	65	2.347	2.253	A5	2.744	1.856	E5	3.137	1.463
26	1.729	2.871	66	2.353	2.247	A6	2.749	1.851	E6	3.144	1.456
27	1.746	2.854	67	2.360	2.240	A7	2.754	1.846	E7	3.157	1.443
28	1.764	2.836	68	2.367	2.233	A8	2.759	1.841	E8	3.171	1.429
29	1.782	2.818	69	2.373	2.227	A9	2.764	1.836	E9	3.184	1.416
2A	1.799	2.801	6A	2.379	2.221	AA	2.770	1.830	EA	3.197	1.403
2B	1.816	2.784	6B	2.384	2.216	AB	2.773	1.827	EB	3.207	1.393
2C	1.834	2.766	6C	2.390	2.210	AC	2.777	1.823	EC	3.218	1.382
2D	1.851	2.749	6D	2.395	2.205	AD	2.781	1.819	ED	3.228	1.372
2E	1.867	2.733	6E	2.403	2.197	AE	2.785	1.815	EE	3.239	1.361
2F	1.884	2.716	6F	2.411	2.189	AF	2.791	1.809	EF	3.258	1.342
30	1.901	2.699	70	2.419	2.181	B0	2.797	1.803	F0	3.277	1.323
31	1.911	2.689	71	2.427	2.173	B1	2.804	1.796	F1	3.296	1.304
32	1.921	2.679	72	2.432	2.168	B2	2.810	1.790	F2	3.315	1.285
33	1.931	2.669	73	2.438	2.162	B3	2.815	1.785	F3	3.325	1.275
34	1.941	2.659	74	2.444	2.156	B4	2.820	1.780	F4	3.336	1.264
35	1.954	2.646	75	2.449	2.151	B5	2.826	1.774	F5	3.346	1.254
36	1.967	2.633	76	2.456	2.144	B6	2.831	1.769	F6	3.357	1.243
37	1.980	2.620	77	2.463	2.137	B7	2.836	1.764	F7	3.377	1.223
38	1.993	2.607	78	2.470	2.130	B8	2.841	1.759	F8	3.397	1.203
39	1.998	2.602	79	2.477	2.123	B9	2.847	1.753	F9	3.417	1.183
3A	2.003	2.597	7A	2.481	2.119	BA	2.852	1.748	FA	3.437	1.163
3B	2.007	2.593	7B	2.485	2.115	BB	2.856	1.744	FB	3.510	1.090
3C	2.012	2.588	7C	2.490	2.110	BC	2.860	1.740	FC	3.582	1.018
3D	2.023	2.577	7D	2.494	2.106	BD	2.863	1.737	FD	3.655	0.945
3E	2.034	2.566	7E	2.504	2.096	BE	2.867	1.733	FE	3.727	0.873
3F	2.045	2.555	7F	2.513	2.087	BF	2.874	1.726	FF	3.800	0.800

<DC Electrical Characteristics>

For the digital circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	2.7	3.0	3.6	V	Digital power
Low Level Input Voltage	V_{il}	GND	-	0.3xV_{CC}	V	Digital input pins
High Level Input Voltage	V_{ih}	0.7xV_{CC}	-	V_{CC}	V	Digital input pins
Input Leakage Current	I_i	-	-	±1	μA	Digital input pins
Pull-high/low Impedance	R_{in}	150k	200k	250k	Ω	
Digital Stand-by Current	I_{st}	-	-	60	μA	DCLK is stopped, Outputs are High-Z Without pull high or low current
Digital Operating Current	I_{CC}	-	TBD	10	mA	DCLK=27MHz, V_{CC}=3.0V, PWM on load, RS[2:0]=HHL(960x240)

For the analog circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Internal Supply Voltage	AV_{DD}	5.0	5.5	6.0	V	Power supply for the analog circuit
	GV_{DD}	4.5	5.0	5.5	V	Power supply for the gamma resistor
Voltage Deviation of Output	V_{CD}	-	±15	±20	V	V_O =0.5V~GV_{DD}-0.5V
Vcom offset	V_{CO}			±5	μA	
Dynamic Range of Output	V_{DR}	0.1	-	AV_{DD}-0.1	Ω	DOUT[24:1]
Low-Level Output Current of Vcom	I_{OLC}	-	20	-	μA	V_{COM} output =0.1V vs. 1.0V(External)
High-Level Output Current of Vcom	I_{OHC}	-	20	-	mA	V_{COM} output =4.1V vs. 3.2V(External)
Low-Level Output Current	I_{OL}	-	-1200	-		DOUT[24:1]; V_O=0.8V vs. 1.7V(External)
High-Level Output Current	I_{OH}	-	1200	-		DOUT[24:1]; V_O=3.8V vs. 2.9V(External)
Analog Standby Current	I_{st}	-	-	1		Shutdown mode. V_{CC}=3.0V
Analog Operating Current	I_{DD}	-	-	4		V_{CC}=3.0V, Line inversion, DOUT[24:1] no load, Vcom no load
PWM output voltage	V_{PWM}	0	-	V_{CC}		
Feed back voltage	V_{FB}	0.55	0.6	0.65		DC/DC operating
Base drive current	I_{PWMD}	-	-	1		V_{PWM} output =3.0V vs. 2.3V(External)
Base sink current	I_{PWMS}	-	-	1		V_{PWM} output =0V vs. 0.7V(External)

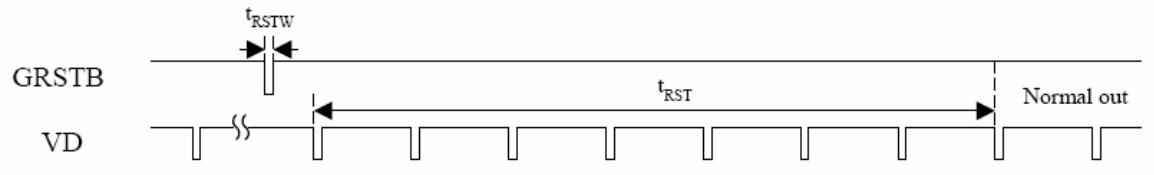
<AC Electrical Characteristics>

Output Voltage

Function pin	Symbol	Min.	Typ.	Max.	Unit	Conditions
CKH1, CKH2 CKV1, CKV2 STH, XSTH STV, XSTV ENB, XENB CSVO, CSHO PCG, XPCG	V_{OH}	Vcc-0.2	-	-	V	I_{OH}=4mA
	V_{OL}	-	-	0.2		I_{OL}=4mA
CP_CLK1, CP_CLK2, CP_CLK3, CP_CLK4	V_{OH}	AV_{DD}-0.2	-	-	V	I_{OH}=4mA
	V_{OL}	-	-	0.2		I_{OL}=4mA

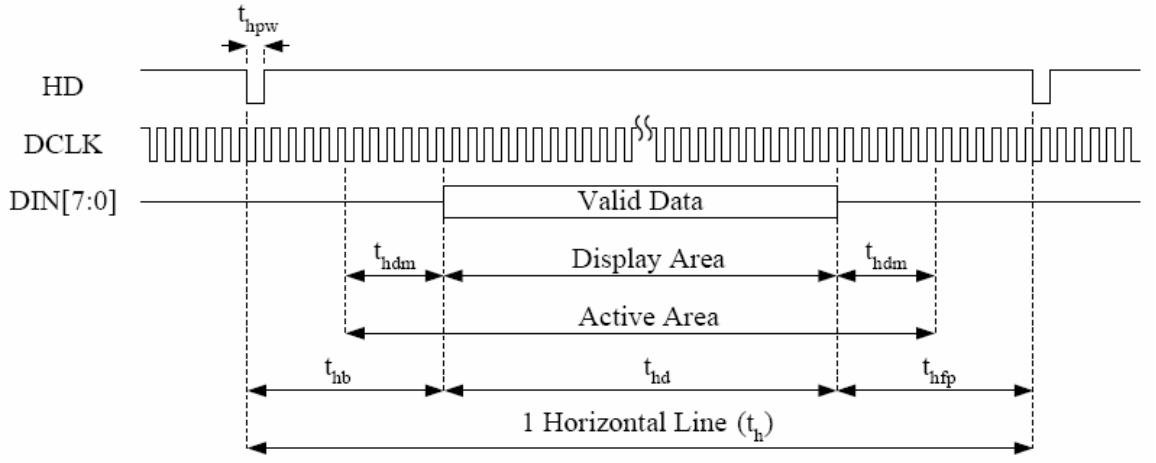
<Global Reset>

Function pin	Symbol	Min.	Typ.	Max.	Unit	Condition
GRSTB	t_{RSTW}	10	--	--	ns	V_{CC}=3.0
	t_{RST}	7	--	--	Field	



<Input timing 1>Serial RGBDummy or Serial-YUV 4:2:2 mode

--Horizontal--



Parameter		Symbol	Mode					Unit
			NTSC		PAL		QVGA	
DCLK Frequency		F_{DCLK}	27	24.54	27	24.38	25	MHz
Horizontal valid data		t_{hd}	1440	1280	1440	1280	1280	DCLK
1 Horizontal Line		t_h	1716	1560	1728	1560	1560	DCLK
HSYNC Pulse Width	Min.	t_{hpw}	1					DCLK
	Typ.		1					
	Max.		-					
Hsync blanking		t_{hp}	240					DCLK
Hsync front porch		t_{hfp}	36	40	48	40	40	DCLK
Horizontal dummy time	640x240	t_{hdm}	4					DCLK
	960x240		0					

***This mode is only for 640x240 and 960x240.**

*YCbCr to RGB conversion:

Format A

$$\begin{cases} R = Y + 1.402C_r \\ G = Y - 0.714C_r - 0.344C_b ; [Y = 0 \sim 255, C_r \ \& \ C_b = -128 \sim 127] \\ B = Y + 1.772C_b \end{cases}$$

Format B

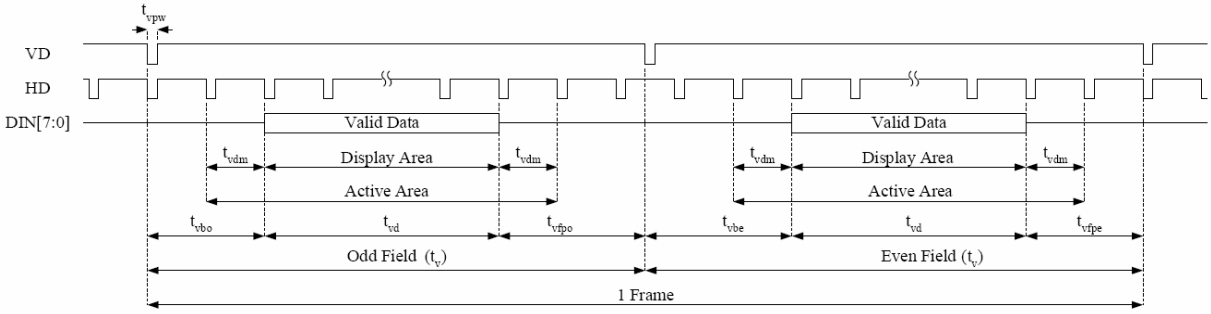
$$\begin{cases} R = 1.16(Y - 16) + 1.60(C_r - 128) \\ G = 1.16(Y - 16) - 0.81(C_r - 128) - 0.39(C_b - 128); [Y = 16 \sim 235, C_r \ \& \ C_b = 16 \sim 240] \\ B = 1.16(Y - 16) + 2.02(C_b - 128) \end{cases}$$

--Vertical--

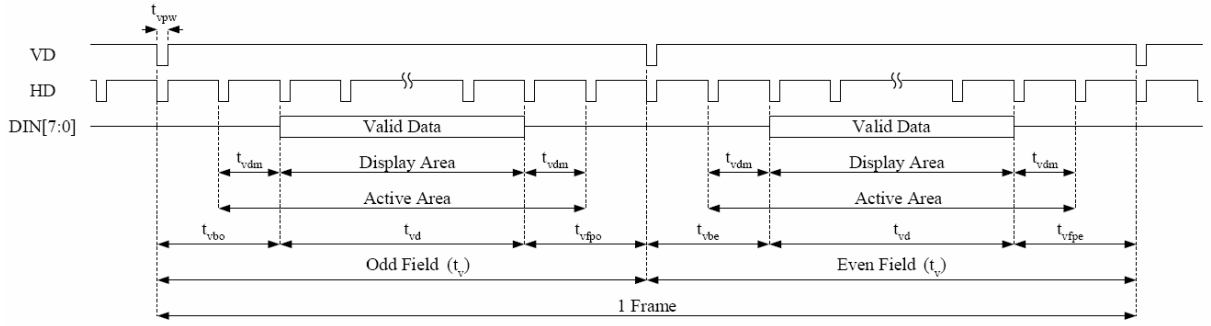
Interlace

ODD Field: same phase VD and HD

EVEN Field: same phase VD and Half-HD



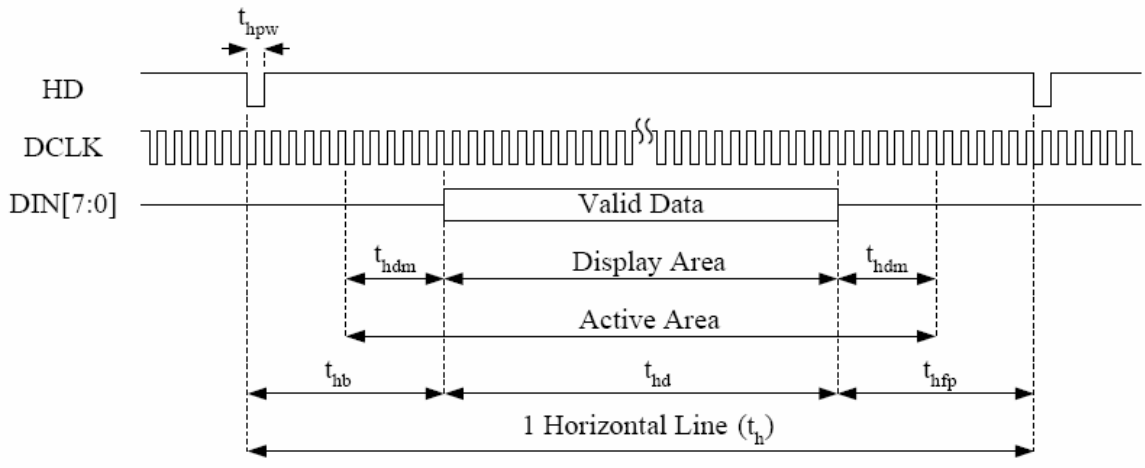
Non-interlace



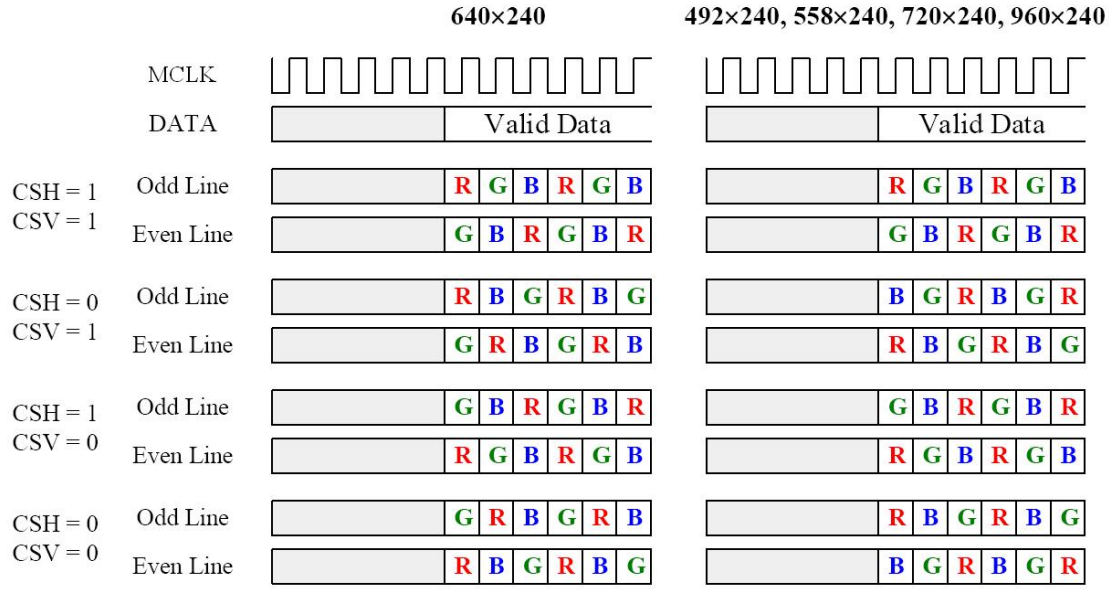
Parameter		Symbol	Interlace		Non-interlace		Unit
			NTSC/QVGA	PAL	NTSC/QVGA	PAL	
Vertical valid data		t_{vd}	240	288	240	288	H
1 Vertical field		t_v	262.5	312.5	262	312	H
Vsync pulse width	Min.	t_{vpw}	1		1		DCLK
	Typ.		1		1		DCLK
	Max.		-		-		H
Vsync blanking	Odd field	t_{vbo}	21	24	21	24	H
	Even field	t_{vbe}	21.5	24.5			H
Vsync front porch	Odd field	t_{vfpo}	1.5	0.5	1	0	H
	Even field	t_{vfpe}	1	0			H
Vertical dummy time		t_{vdm}	0	0	0	0	H

<Input timing 2>Through mode

--Horizontal-



Parameter		Symbol	Panel Resolution					Unit
DCLK Frequency		F_{DCLK}	10.36	11.63	12.90	14.18	18.42	MHz
Horizontal valid data		t_{hd}	492	558	640	720	960	DCLK
1 Horizontal Line		t_h	659	739	820	901	1171	DCLK
HSYNC Pulse Width	Min.	t_{hpw}	1					DCLK
	Typ.		1					
	Max.		-					
Hsync blanking		t_{hp}	102	113	117	122	152	DCLK
Hsync front porch		t_{hfp}	65	68	63	59	59	DCLK
Horizontal dummy time		t_{hdm}	6	9	4	0	0	DCLK

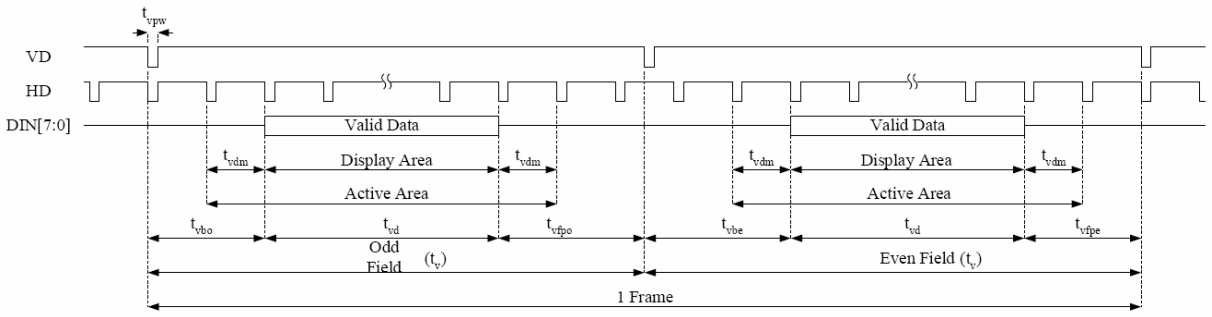


--Vertical—

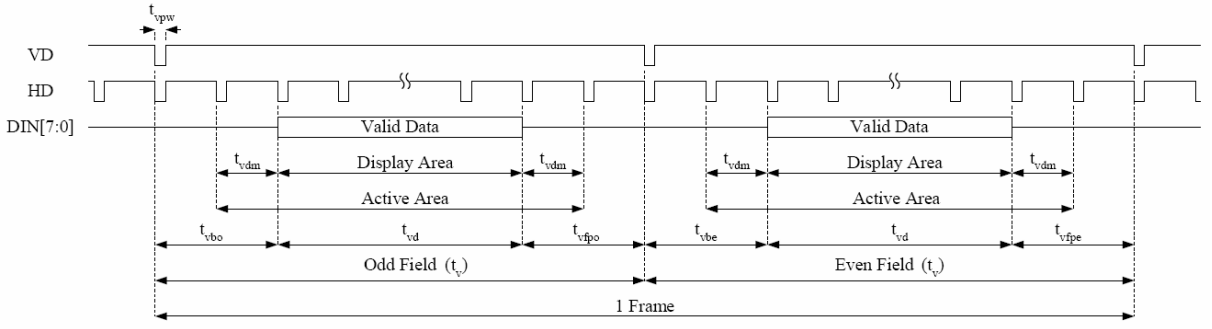
Interlace

ODD Field: same phase VD and HD

EVEN Field: same phase VD and Half-HD

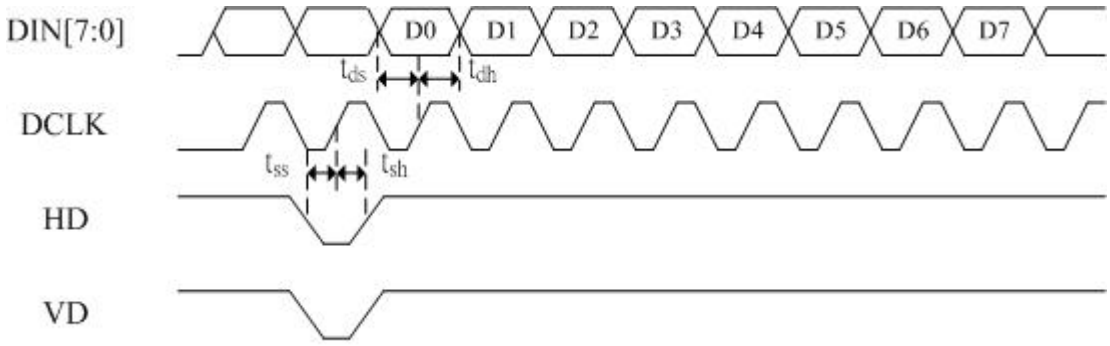


Non-interlace



Parameter		Symbol	Interlace	Non-interlace	Unit
Vertical valid data		t_{vd}	240	240	H
1 Vertical field		t_v	262.5	262	H
Vsync pulse width	Min.	t_{vpw}	1	1	DCLK
	Typ.		1	1	DCLK
	Max.		-	-	H
Vsync blanking	Odd field	t_{vbo}	14	14	H
	Even field	t_{vbe}	14.5	14	H
Vsync front porch	Odd field	t_{vfpo}	8.5	8	H
	Even field	t_{vfpe}	8	8	H
Vertical dummy time		t_{vdm}	0	0	H

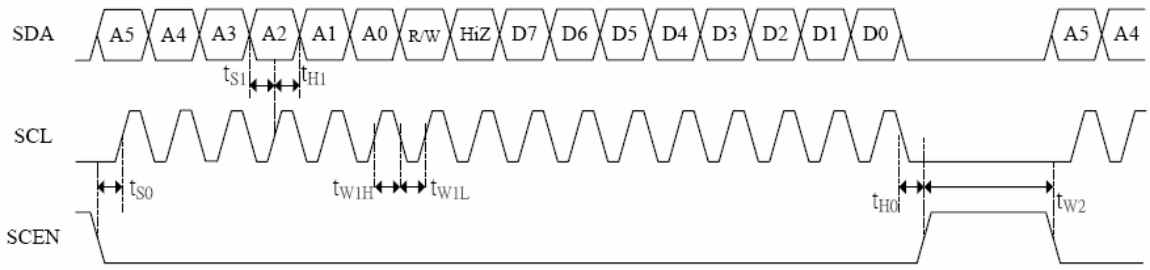
<Input timing 3>Timing Diagram



Item	symbol	min	typ	Max	Unit
DCLK duty ratio	Duty	40	-	60	%
Data setup time	t_{ds}	12	-	-	ns
Data hold time	t_{dh}	12	-	-	ns
Control signal setup time	t_{ss}	12	-	-	ns
Control signal hold time	t_{sh}	12	-	-	ns

<3-Wires Serial control>

3 wires Serial data transfer format



Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDA Setup Time	t_{s0}	SCEN to SCL	150			ns
	t_{s1}	SDA to SCL	150			ns
SDA Hold Time	t_{h0}	SCEN to SCL	150			ns
	t_{h1}	SDA to SCL	150			ns
Pulse Width	t_{w1L}	SCL pulse width	160			ns
	t_{w1H}	SCL pulse width	160			ns
	t_{w2}	SCEN pulse width	1.0			us
Clock duty			40		60	%

1. Only when SCL is input in 16-bit clock while LOAD is in the "Low" period, DATA is accepted at rise of LOAD.
2. If SCL is in 15-bit or 17-bit clock while SCEN is in the "Low" period, SDA is not accepted.

*) It is necessary DCLK input for SDA setting

3. Items are set at fall of the vertical sync.

<Register description>

Address	Default	Read/Write	Meaning
0x01	0x51	R	[7:4]: Chip ID [3:0]: Chip version
0x02	0x09	R/W	[1:0]: Input data format [2]: format standard [3]: Valid data for RGBDm or YUV mode [4]: Input clock latch data edge [5]: HD polarity [6]: VD polarity
0x03	0x30	R/W	[0]: Select of interlace mode [1]: Select of field mix [3:2]: YCbCr sequence [4]: YUV input transfer matrix [5]: UV offset for matrix A
0x04	0x0F	R/W	[0]: Power management [1]: CP_CLK output on/off [2]: PWM output on/off [3]: Pre-charge on/off [5:4]: Output driver capability
0x05	0x13	R/W	[0]: Horizontal reverse mode [1]: Vertical reverse mode [2]: Color filter selection for 960x240 [5:3]: Sample and hold phase
0x06	0x18	R/W	[5:0]: Horizontal start position for through mode
0x07	0x08	R/W	[3:0]: Vertical start position for through mode
0x08	0x00	R/W	[5:0]: ENB negative position
0x09	0x20	R/W	[5:0]: Gain of contrast
0x0A	0x20	R/W	[5:0]: R gain of sub-contrast
0x0B	0x20	R/W	[5:0]: B gain of sub-contrast
0x0C	0x10	R/W	[5:0]: Offset of brightness
0x10	0x3A	R/W	[5:0]: Vcom high level
0x11	0x3A	R/W	[5:0]: Vcom low level
0x12	0x1D	R/W	[5:0]: PCD high level
0x13	0x17	R/W	[5:0]: PCD low level
0x14	0x98	R/W	[3:0]: GAMAA0 of gamma Correction [7:4]: GAMA28 of gamma Correction
0x15	0x9A	R/W	[3:0]: GAMA60 of gamma Correction [7:4]: GAMA93 of gamma Correction

0x16	0xA9	R/W	[3:0]: GAMA125 of gamma Correction [7:4]: GAMA157 of gamma Correction
0x17	0x99	R/W	[3:0]: GAMA190 of gamma Correction [7:4]: GAMA222 of gamma Correction
0x18	0x08	R/W	[3:0]: GAMA255 of gamma Correction

<Input format standard>

R02[1:0]	0	1(Default)	2
Input Format	RGBDummy	YUV	Through mode

R02[2]	0(Default)	1
Format standard	NTSC/QVGA	PAL

R02[3]	0	1(Default)
Valid data for RGBDm or YUV	1280	1440

<Input data and clock>

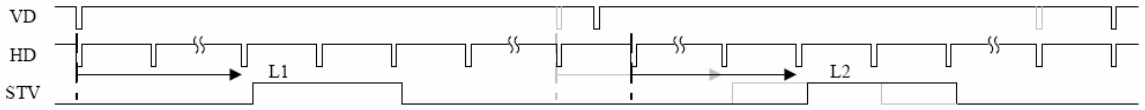
R02[4]	0(Default)	1
Latch data edge	Positive Edge	Negative

R02[5]	0(Default)	1
HD Polarity	Low pulse	High pulse

R02[6]	0(Default)	1
VD Polarity	Low pulse	High pulse

R03[0]	0(Default)	1
Interlace Mode	Interlace	Non-interlace

R03[1]	0(Default)	1
Even Field Blanking	L2=L1	L2=L1-1



R03[3:2]	0(Default)	1	2	3
YCbCr sequence	CbYCrY	YCrYCb	CrYCbY	YCbYCr

R03[4]	0	1(Default)
YUV transfer matrix	Format A	Format B

R03[5]	0	1(Default)
UV offset for Format A	Binary (0~255)	2's complement (-18~127)

<Power management>

R04[0]	0	1(Default)
Low power mode	Standby	Normal

Function pin	DOUT[24:1] PCD, VCOM, PWM	CP_CLK1, CP_CLK2, CP_CLK3, CP_CLK4,	XSTV, XSTH CKV, CKH ENB, XPCG	STV, STH XCKV, XCKH XENB, PCG
Standby	Low	Low	High	Low

R04[1]	0	1(Default)
CP_CLK	Disable	Enable

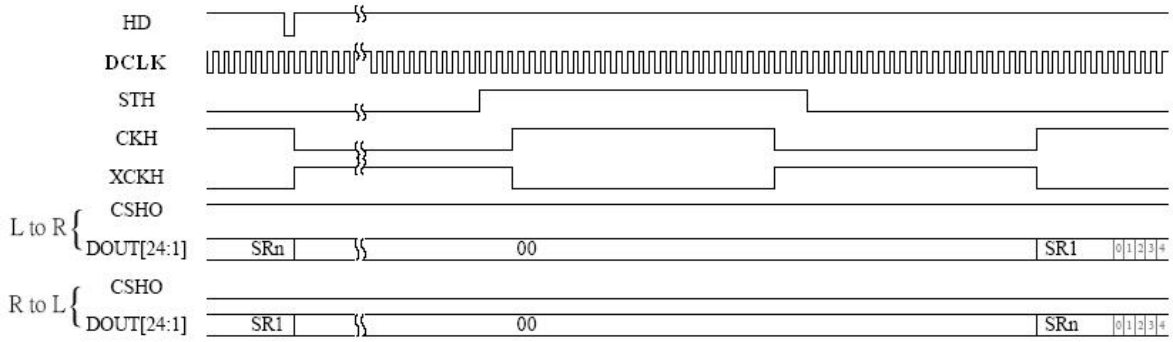
R04[2]	0	1(Default)
PWM	Disable	Enable

R04[3]	0	1(Default)
Pre-charge	Disable	Enable

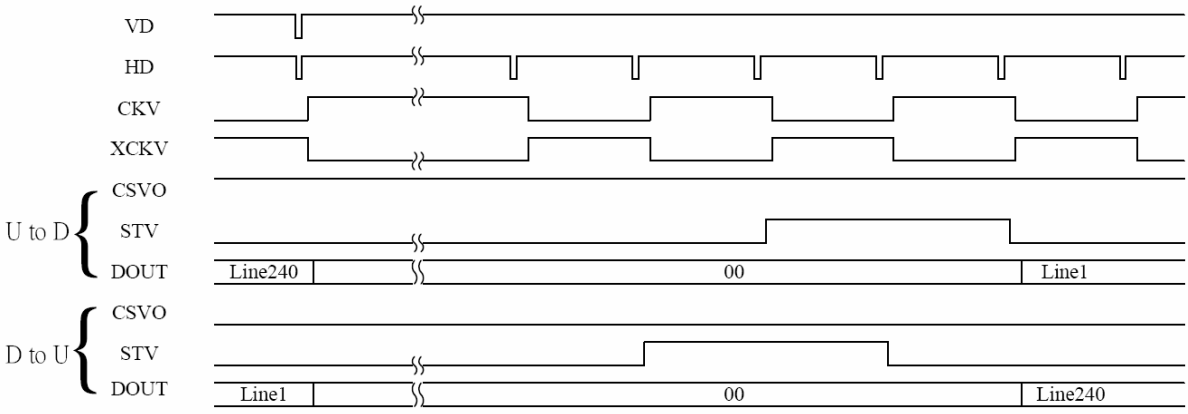
R04[5:4]	0(Default)	1	2	3
Driver capability	50%	65%	80%	100%

<Direction Control>

R05[0]	0	1(Default)
Horizontal reverse	Reverse	Normal



R05[1]	0	1(Default)
Vertical reverse	Reverse	Normal

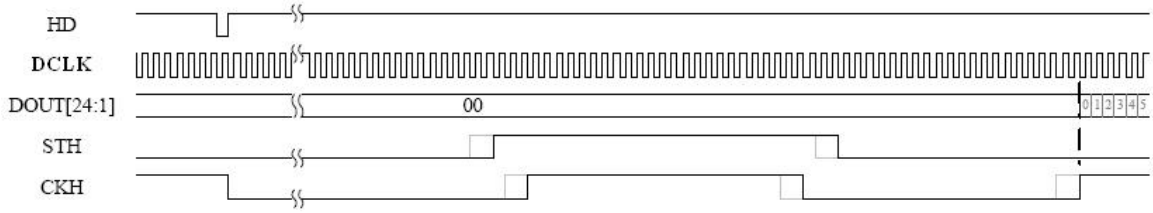


<Color filter selection for 960x240>

R05[2]	0(Default)	1
Color filter	Delta	Strip

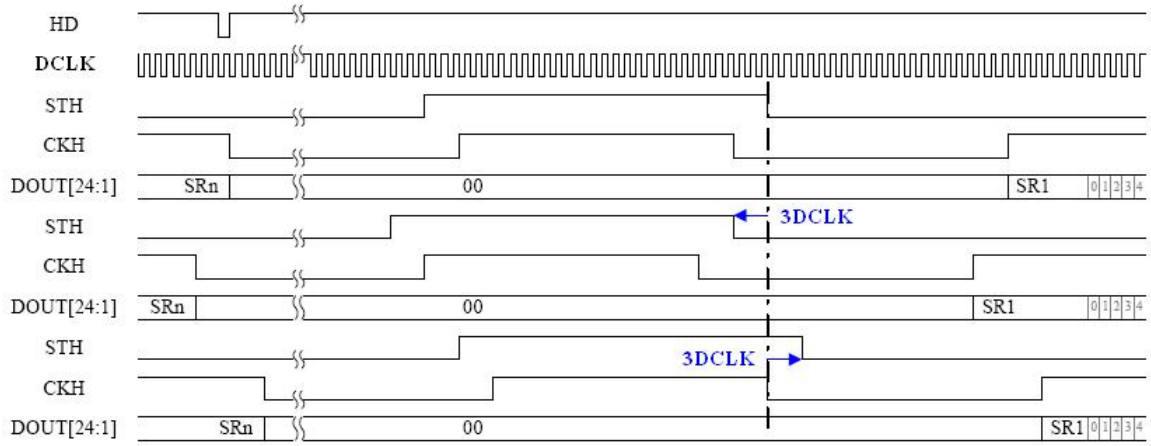
<Output sample and hold phase>

R05[5:3]	0	1	2(Default)	3	4	5	6	7
Output phase	Normal	SH2	SH4	SH6	SH8	SH10	SH12	SH14

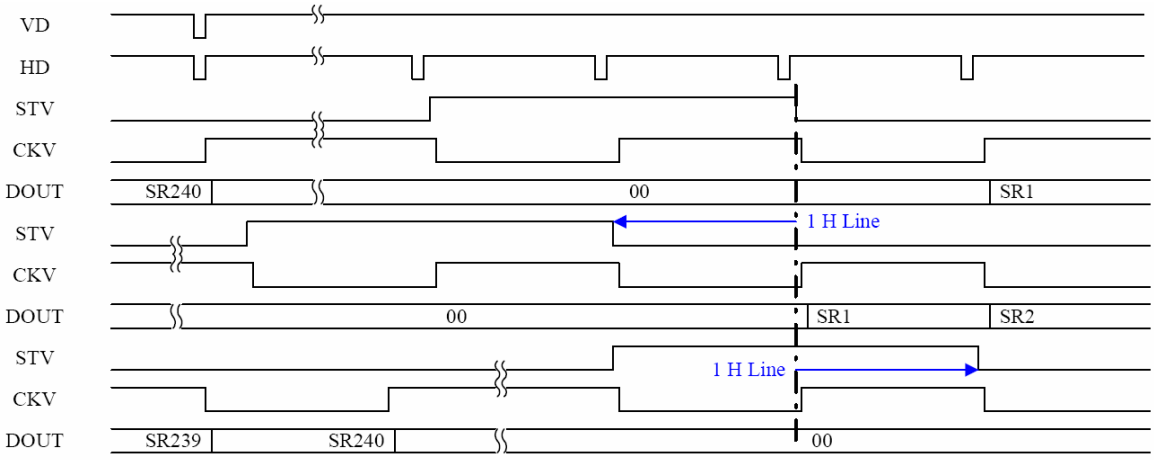


<Shift display area>

R06[5:0]	0x0	0x18(Default)	0x2D
STH phase	Advance 24 DCLK	Center	Delay 21 DCLK
Display position	Shift right 24 dot	Center	Shift left 21 dot

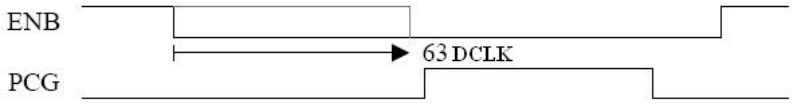


R07[3:0]	0x0	0x8(Default)	0xF
STV phase	Advance 8H	Center	Delay 7H
Display position	Shift down 8 Line	Center	Shift up 7 Line



<Gate non-overlap>

R08[5:0]	0x0(Default)	0x3F
ENB negative position	Origin	Shift right 63 DCLK



<Contrast and Brightness>

$D_{contrast} = D_{in} * Gain$, $D_{brightness} = D_{contrast} + Offset$

R09[5:0]	0x00	0x20(Default)	0x3F
Gain of Contrast	0.00000	1.00000	1.96875

R0A[5:0]	0x00	0x20(Default)	0x3F
R gain of Sub-contrast	0.00000	1.00000	1.96875

R0B[5:0]	0x00	0x20(Default)	0x3F
B gain of Sub-contrast	0.00000	1.00000	1.96875

R0C[5:0]	0x00	0x10(Default)	0x3F
Offset of Brightness	-16	0	47

<Contrast and Brightness>

V_{comH} = 2.84 + 0.02 * R10, V_{comL} = 1.36 – 0.02 * R11

R10[5:0]	0x00	0x3A(Default)	0x3F
Vcom high level	2.84	4.00	4.10

R11[5:0]	0x00	0x3A(Default)	0x3F
Vcom low level	1.36	0.20	0.10

V_{pcdH} = 0.22 + 0.08 * R12, V_{pcdL} = 0.22 – 0.08 * R13

R12[5:0]	0x00	0x1D(Default)	0x2F
PCD high level	0.22	2.54	3.98

R13[5:0]	0x00	0x17(Default)	0x2F
PCD low level	0.22	2.06	3.98

<Gamma Correction>

$V_{gcH} = V_{gnH} + 0.04*(R_n-8)$, $V_{gcL} = V_{gnL} + 0.04*(8-R_n)$,

R14[3:0]		0x0	0x8(Default)	0xF
GAMA0	VcomH	0.580	0.900	1.180
	VcomL	4.020	3.700	3.420

R14[7:4]		0x0	0x9(Default)	0xF
GAMA28	VcomH	1.237	1.597	1.837
	VcomL	3.630	3.003	2.763

R15[3:0]		0x0	0x10(Default)	0xF
GAMA60	VcomH	1.692	2.092	2.292
	VcomL	2.908	2.508	2.308

R15[7:4]		0x0	0x9(Default)	0xF
GAMA93	VcomH	1.966	2.326	2.566
	VcomL	2.634	2.274	2.034

R16[3:0]		0x0	0x9(Default)	0xF
GAMA125	VcomH	2.174	2.534	2.774
	VcomL	2.426	2.066	1.826

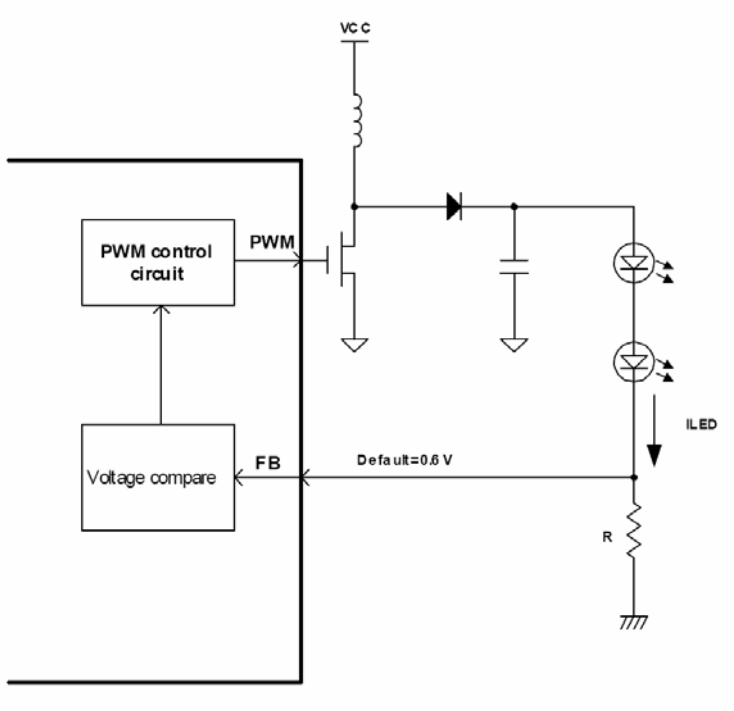
R16[7:4]		0x0	0x10(Default)	0xF
GAMA157	VcomH	2.377	2.777	2.977
	VcomL	2.223	1.823	1.623

R17[3:0]		0x0	0x9(Default)	0xF
GAMA190	VcomH	2.547	2.907	3.147
	VcomL	2.053	1.693	1.453

R17[7:4]		0x0	0x9(Default)	0xF
GAMA222	VcomH	2.759	3.119	3.359
	VcomL	1.841	1.481	1.241

R18[3:0]		0x0	0x8(Default)	0xF
GAMA255	VcomH	3.480	3.800	4.080
	VcomL	1.120	0.800	0.520

<LED voltage generate circuit>



*To obtain high efficiency B/L drive capability, it is recommended that the dedicated LED driver IC is used.

Revision History

Rev.	Issued Date	Revised Contents
1.0	2004/11/17	NEW
1.1	2005/4/1	Modify Power on/off and mode change sequence
1.2	2005/6/6	Add absolute maximum ratings and application circuit
1.3	2005/8/2	Modify power sequence
		Add LED voltage generate circuit description