



Analog-to-Digital Converter (ADC)

This section describes the on-chip 10 bit analog-to-digital converter of the A/T89C51AC2. Eight ADC channels are available for sampling of the external sources AN0 to AN7. An analog multiplexer allows the single ADC converter to select one from the 8 ADC channels as ADC input voltage (ADCIN). ADCIN is converted by the 10-bit cascaded potentiometric ADC.

Two modes of conversion are available:

- Standard conversion (8 bits).
- Precision conversion (10 bits).

For the precision conversion, set bit PSIDLE in ADCON register and start conversion. The device is in a pseudo-idle mode, the CPU does not run but the peripherals are always running. This mode allows digital noise to be as low as possible, to ensure high precision conversion.

For this mode it is necessary to work with end of conversion interrupt, which is the only way to wake the device up.

If another interrupt occurs during the precision conversion, it will be served only after this conversion is completed.

Features

- 8 channels with multiplexed inputs
- 10-bit cascaded potentiometric ADC
- Conversion time 16 micro-seconds (typ.)
- Zero Error (offset) ± 2 LSB max
- Positive External Reference Voltage Range (VAREF) 2.4 to 3.0 Volt (typ.)
- ADCIN Range 0 to 3Volt
- Integral non-linearity typical 1 LSB, max. 2 LSB
- Differential non-linearity typical 0.5 LSB, max. 1 LSB
- Conversion Complete Flag or Conversion Complete Interrupt
- Selectable ADC Clock

ADC Port 1 I/O Functions

Port 1 pins are general I/O that are shared with the ADC channels. The channel select bit in ADCF register define which ADC channel/port1 pin will be used as ADCIN. The remaining ADC channels/port1 pins can be used as general-purpose I/O or as the alternate function that is available.

A conversion launched on a channel which are not selected on ADCF register will not have any effect.

VAREF

VAREF should be connected to a low impedance point and must remain in the range specified in Table 77. If the ADC is not used, it is recommended to connect VAREF to VAGND.

Figure 45. ADC Description

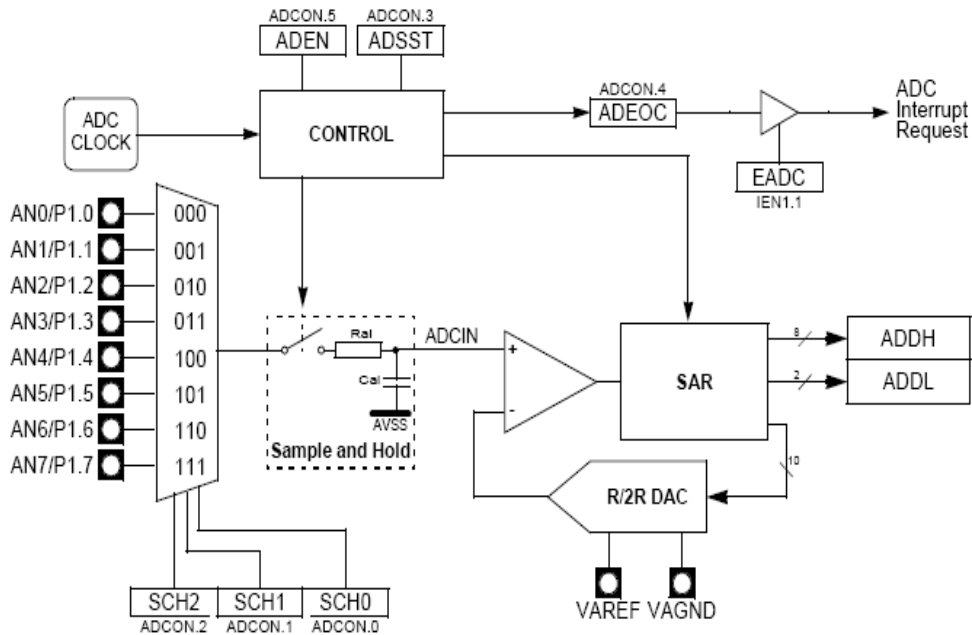
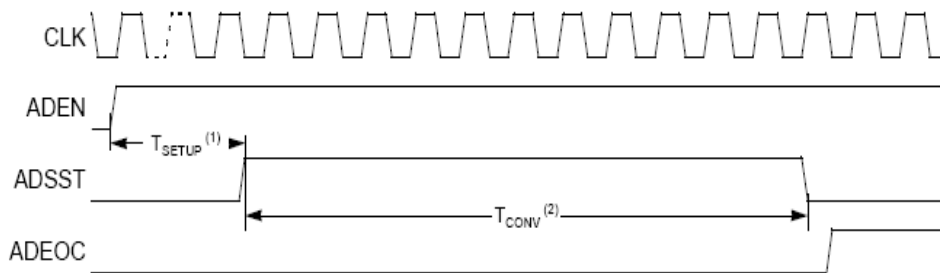


Figure 46 shows the timing diagram of a complete conversion. For simplicity, the figure depicts the waveforms in idealized form and do not provide precise timing information. For ADC characteristics and timing parameters refer to the Section "AC Characteristics" of the A/T89C51AC2 datasheet.

Figure 46. Timing Diagram



- Notes: 1. Tsetup min, see the AC Parameter for A/D conversion.
 2. Tconv = 11 clock ADC = 1sample and hold + 10 bit conversion
 The user must ensure that Tsetup time between setting ADEN and the start of the first conversion.



ADC Converter Operation

A start of single A/D conversion is triggered by setting bit ADSST (ADCON.3).

After completion of the A/D conversion, the ADSST bit is cleared by hardware.

The end-of-conversion flag ADEOC (ADCON.4) is set when the value of conversion is available in ADDH and ADDL, it must be cleared by software. If the bit EADC (IEN1.1) is set, an interrupt occur when flag ADEOC is set (see Figure 48). Clear this flag for re-arming the interrupt.

The bits SCH0 to SCH2 in ADCON register are used for the analog input channel selection.⁽¹⁾

Note: 1. Always leave Tsetup time before starting a conversion unless ADEN is permanently high. In this case one should wait Tsetup only before the first conversion.

Table 62. Selected Analog input

SCH2	SCH1	SCH0	Selected Analog input
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

Voltage Conversion

When the ADCIN is equals to VAREF the ADC converts the signal to 3FFh (full scale). If the input voltage equals VAGND, the ADC converts it to 000h. Input voltage between VAREF and VAGND are a straight-line linear conversion. All other voltages will result in 3FFh if greater than VAREF and 000h if less than VAGND.

Note: ADCIN should not exceed VAREF absolute maximum range (see "Absolute Maximum Ratings" on page 141)

Clock Selection

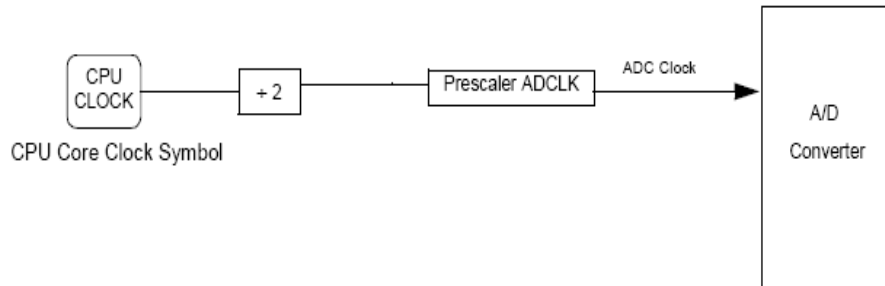
The ADC clock is the same as CPU.

The maximum clock frequency is defined in the DC parameter for A/D converter. A prescaler is featured (ADCCLK) to generate the ADC clock from the oscillator frequency.

if PRS > 0 then $f_{ADC} = F_{periph} / 2 \times PRS$

if PRS = 0 then $f_{ADC} = F_{periph} / 64$

Figure 47. A/D Converter clock



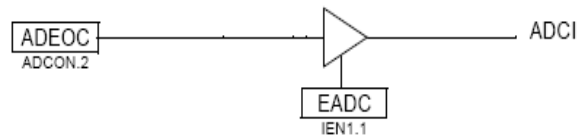
ADC Standby Mode

When the ADC is not used, it is possible to set it in standby mode by clearing bit ADEN in ADCON register. In this mode its power dissipation is reduced.

IT ADC Management

An interrupt end-of-conversion will occurs when the bit ADEOC is activated and the bit EADC is set. For re-arming the interrupt the bit ADEOC must be cleared by software.

Figure 48. ADC Interrupt Structure



Routines examples

1. Configure P1.2 and P1.3 in ADC channels


```

// configure channel P1.2 and P1.3 for ADC
ADCF = 0ch

// Enable the ADC
ADCON = 20h
      
```
2. Start a standard conversion


```

// The variable "channel" contains the channel to convert
// The variable "value_converted" is an unsigned int
// Clear the field SCH[2:0]
ADCON and = F8h
// Select channel
ADCON | = channel
// Start conversion in standard mode
ADCON | = 08h
// Wait flag End of conversion
while((ADCON and 01h) != 01h)
// Clear the End of conversion flag
ADCON and = EFh
// read the value
value_converted = (ADDH << 2)+(ADDL)
      
```
3. Start a precision conversion (need interrupt ADC)


```

// The variable "channel" contains the channel to convert
// Enable ADC
EADC = 1
      
```



```
// clear the field SCH[2:0]
ADCON and = F8h
// Select the channel
ADCON | = channel
// Start conversion in precision mode
ADCON | = 48h
```

Note: to enable the ADC interrupt:
EA = 1

Registers

Table 63. ADCF Register

ADCF (S:F6h)
ADC Configuration

7	6	5	4	3	2	1	0
CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
Bit Number	Bit Mnemonic	Description					
7-0	CH 0:7	Channel Configuration Set to use P1.x as ADC input. Clear to use P1.x as standart I/O port.					

Reset Value = 0000 0000b

Table 64. ADCON Register

ADCON (S:F3h)
ADC Control Register

7	6	5	4	3	2	1	0
-	PSIDLE	ADEN	ADEOC	ADSST	SCH2	SCH1	SCH0
Bit Number	Bit Mnemonic	Description					
7	-						
6	PSIDLE	Pseudo Idle Mode (Best Precision) Set to put in idle mode during conversion Clear to convert without idle mode.					
5	ADEN	Enable/Standby Mode Set to enable ADC Clear for Standby mode (power dissipation 1 uW).					
4	ADEOC	End Of Conversion Set by hardware when ADC result is ready to be read. This flag can generate an interrupt. Must be cleared by software.					
3	ADSST	Start and Status Set to start an A/D conversion. Cleared by hardware after completion of the conversion					
2-0	SCH2:0	Selection of Channel to Convert see Table 62					

Reset Value = X000 0000b



Table 65. ADCLK Register

ADCLK (S:F2h)
ADC Clock Prescaler

7	6	5	4	3	2	1	0
-	-	-	PRS 4	PRS 3	PRS 2	PRS 1	PRS 0
Bit Number	Bit Mnemonic	Description					
7-5	-	Reserved The value read from these bits are indeterminate. Do not set these bits.					
4-0	PRS4:0	Clock Prescaler $f_{ADC} = f_{cpu\ clock} / (4 \text{ (or 2 in X2 mode)} * PRS)$					

Reset Value = XXX0 0000b

Table 66. ADDH Register

ADDH (S:F5h Read Only)
ADC Data High Byte Register

7	6	5	4	3	2	1	0
ADAT 9	ADAT 8	ADAT 7	ADAT 6	ADAT 5	ADAT 4	ADAT 3	ADAT 2
Bit Number	Bit Mnemonic	Description					
7-0	ADAT9:2	ADC result bits 9-2					

Reset Value = 00h

Table 67. ADDL Register

ADDL (S:F4h Read Only)
ADC Data Low Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	ADAT 1	ADAT 0
Bit Number	Bit Mnemonic	Description					
7-2	-	Reserved The value read from these bits are indeterminate. Do not set these bits.					
1-0	ADAT1:0	ADC result bits 1-0					

Reset Value = 00h