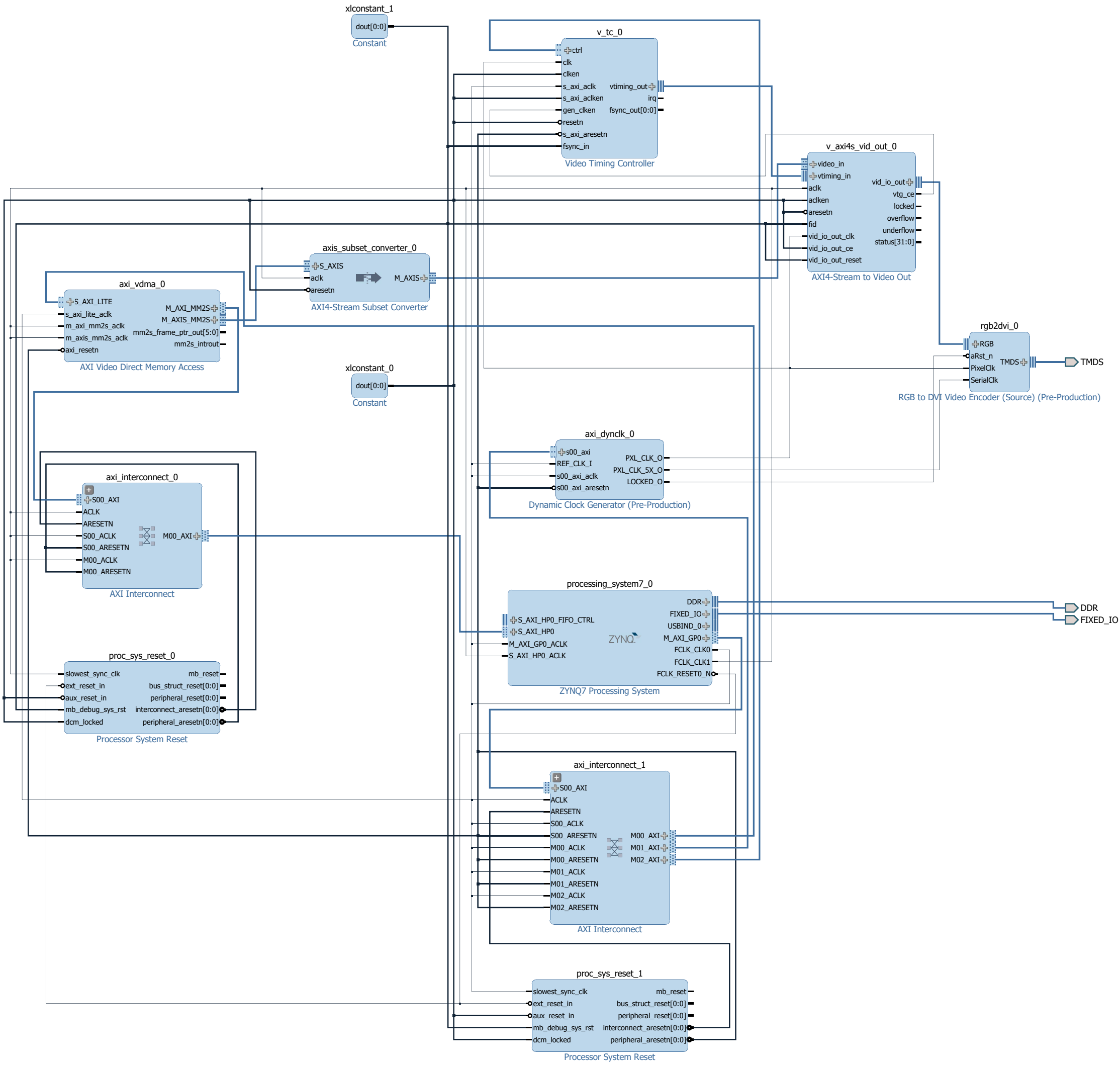
xlconstant_1
dout[0:0]
Constant
v_tc_0
ctrl
clk
clken
s_axi_aclk
s_axi_aclken
gen_clken
resetn
s_axi_aresetn
fsync_in
vtiming_out
irq
fsync_out[0:0]
Video Timing Controller
v_axi4s_vid_out_0
video_in
vtiming_in
aclk
aclken
aresetn
fid
vid_io_out_clk
vid_io_out_ce
vid_io_out_reset
vid_io_out
vtg_ce
locked
overflow
underflow
status[31:0]
AXI4-Stream to Video Out
axis_subset_converter_0
S_AXIS
aclk
aresetn
M_AXIS
AXI4-Stream Subset Converter
axi_vdma_0
S_AXI_LITE
s_axi_lite_aclk
m_axi_mm2s_aclk
m_axis_mm2s_aclk
axi_resetn
M_AXI_MM2S
M_AXIS_MM2S
mm2s_frame_ptr_out[5:0]
mm2s_introut
AXI Video Direct Memory Access
rgb2dvi_0
RGB
aRst_n
PixelClk
SerialClk
TMDS
RGB to DVI Video Encoder (Source) (Pre-Production)
TMDS
xlconstant_0
dout[0:0]
Constant
axi_dynclk_0
s00_axi
REF_CLK_I
s00_axi_aclk
s00_axi_aresetn
PXL_CLK_O
PXL_CLK_5X_O
LOCKED_O
Dynamic Clock Generator (Pre-Production)
axi_interconnect_0
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
processing_system7_0
S_AXI_HP0_FIFO_CTRL
S_AXI_HP0
M_AXI_GP0_ACLK
S_AXI_HP0_ACLK
ZYNQ
DDR
FIXED_IO
USBIND_0
M_AXI_GP0
FCLK_CLK0
FCLK_CLK1
FCLK_RESET0_N
ZYNQ7 Processing System
DDR
FIXED_IO
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axi_interconnect_1
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M02_ACLK
M02_ARESETN
M00_AXI
M01_AXI
M02_AXI
AXI Interconnect
proc_sys_reset_1
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset