SHARP CORPORATION

No. KS-83C078

ORIGINAL

TECHNICAL LITERATURE

FOR

LCD Driver LSI

MODEL NO. LH5006A

DATE September 24, 1983

** The technical literature is subject to be changed without notice **

SHARP CORPORATION
ELECTRONIC COMPONENTS GROUP

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1. General Description

The LH5006A is a LCD driver LSI fabricated with a CMOS silicon-gate process. It contains 2 sets of 20-stage bidirectional shift registers (SR1 ∿ SR20, SR21 ∿ SR40), 2 sets of 20-bit latches (LT1 ∿ LT20, LT21 ∿ LT40) and 2 sets of 20-circuit LCD drivers (Ch1 = LD1 ∿ LD20 , Ch2 = LD21 ∿ LD40). The LH-5006 converts serial input data for display pattern into parallel output data and generates an LCD-On or LCD-Off signal waveform according to the content of the output data, "1" or "0". Interconnection of the external pins (DL1, DR1, DL2 and DR2) may allow 2 sets of bidirectional shift registers to be connected in series. Ch1 20-circuits out of the LCD driver circuits are used exclusively to drive segment signals, while Ch2 20-circuits, to drive both segment signals and common signals.

2. Features

- o CMOS process
- o 2 sets of 20-stage bidirectional shift registers, 2 sets of 20-bit latches, and 2 sets of 20-circuit LCD drivers (Ch1 = LD1 ∿ LD20 exclusive for segment signals: Ch2 = LD21 ∿ LD40 switchable to drive either of segment signals or common signals)
- o 60-pin flat package

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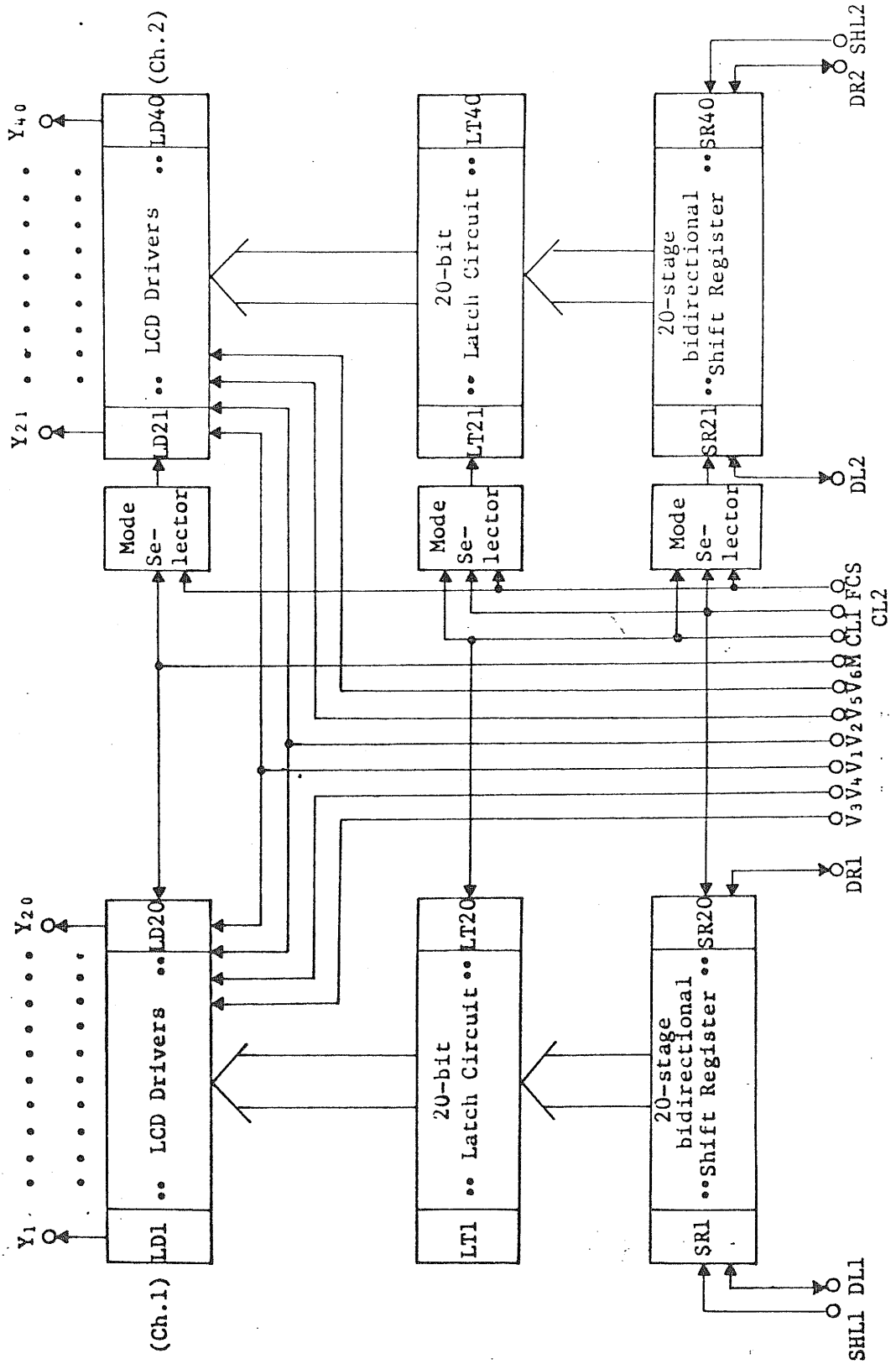
3. System Configuration



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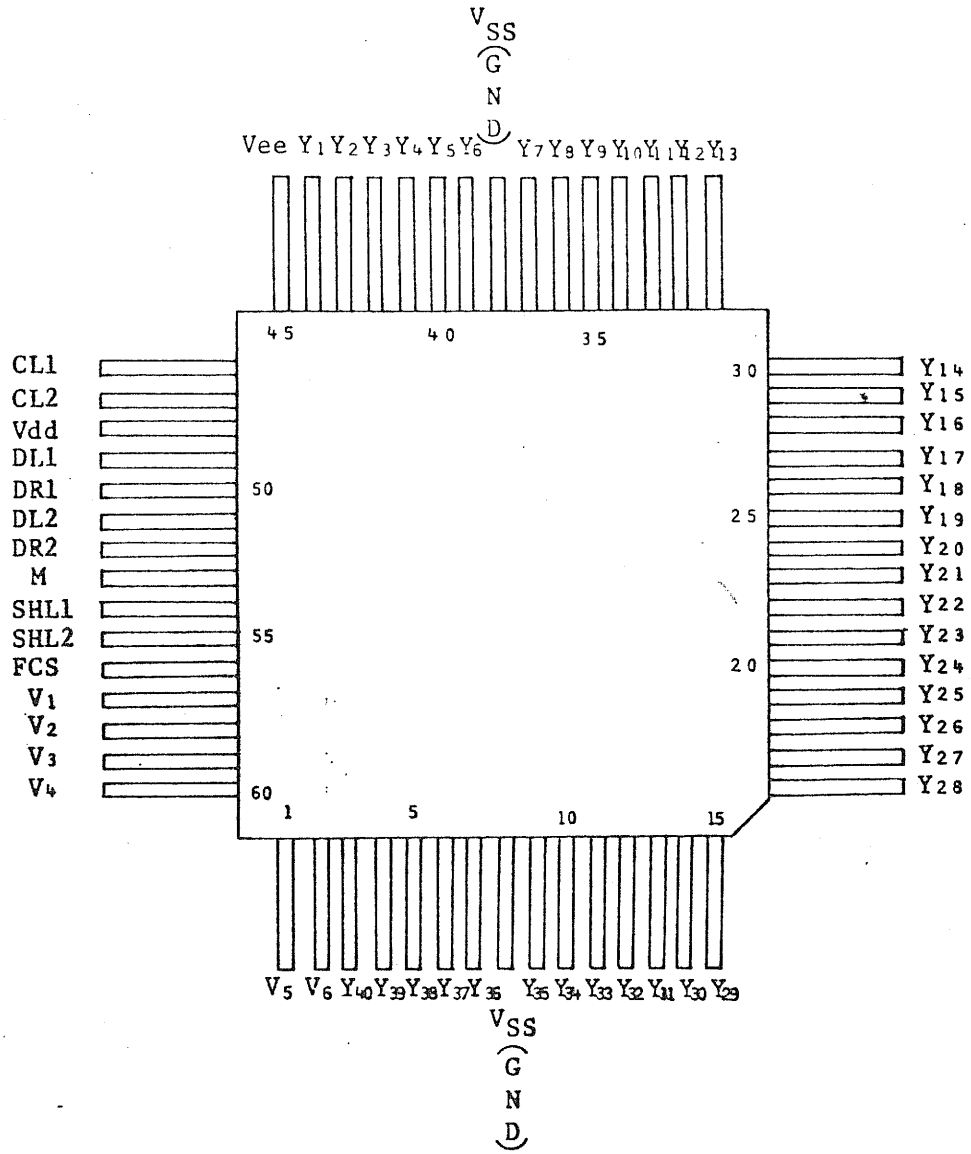
4. Pin Assignment and Pin Names

4.1. Pin Assignment



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4.2 Pin Names

Pin No.	Power Supply	Input	Output	Pin No.	Power Supply	Input	Output
1		V_5		31			Y_{13}
2		V_6		32			Y_{12}
3			Y_{40}	33			Y_{11}
4			Y_{39}	34			Y_{10}
5			Y_{38}	35			Y_9
6			Y_{37}	36			Y_8
7			Y_{36}	37			Y_7
8	V_{SS}(GND)*			38	V_{SS}(GND)*		
9			Y_{35}	39			Y_6
10			Y_{34}	40			Y_5
11			Y_{33}	41			Y_4
12			Y_{32}	42			Y_3
13			Y_{31}	43			Y_2
14			Y_{30}	44			Y_1
15			Y_{29}	45	V_{ee}(-17V)		
16			Y_{28}	46		CL1	
17			Y_{27}	47		CL2	
18			Y_{26}	48	V_{dd}(-5)		
19			Y_{25}	49		DL1	
20			Y_{24}	50		DR1	
21			Y_{23}	51		DL2	
22			Y_{22}	52		DR2	
23			Y_{21}	53		M	
24			Y_{20}	54		SHL1	
25			Y_{19}	55		SHL2	
26			Y_{18}	56		FCS	
27			Y_{17}	57		V_1	
28			Y_{16}	58		V_2	
29			Y_{15}	59		V_3	
30			Y_{14}	60		V_4	

* V_{SS}(GND) may be connected to either of No.8 or No.38 pin because both pins are interconnected in the LSI.

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5. Pin Functions

<table>
<tr><th>Parameter</th><th>I/O</th><th>Function</th></tr>
<tr><td>Vdd</td><td></td><td>Power supply to logic (-5V)</td></tr>
<tr><td>Vee</td><td></td><td>Power supply to LCD driver (-17V)</td></tr>
<tr><td>Vss</td><td></td><td>GND pin (common to logic and LCD driver)</td></tr>
<tr><td>$Y_1 \sim Y_{20}$</td><td>Output</td><td>Ch1 LCD driver output</td></tr>
<tr><td>$Y_{21} \sim Y_{40}$</td><td>Output</td><td>Ch2 LCD driver output</td></tr>
<tr><td>V_1, V_2</td><td>Input</td><td>Voltage level (selected) inputs for LCD driver</td></tr>
<tr><td>V_3, V_4</td><td>Input</td><td>Voltage level (non-selected) inputs for LCD driver of CH1</td></tr>
<tr><td>V_5, V_6</td><td>Input</td><td>Voltage level (non-selected) inputs for LCD driver of CH2</td></tr>
<tr><td>SHL1</td><td>Input</td><td>Selection of Ch1 data shift direction
<table>
<tr><th>SHL1</th><th>DL1</th><th>DR1</th><th>Shift Direction</th></tr>
<tr><td>"L"</td><td>IN</td><td>OUT</td><td>SR1 → SR20</td></tr>
<tr><td>"H"</td><td>OUT</td><td>IN</td><td>SR20 → SR1</td></tr>
</table></td></tr>
<tr><td>SHL2</td><td>Input</td><td>Selection of Ch2 data shift direction
<table>
<tr><th>SHL2</th><th>DL2</th><th>DR2</th><th>Shift Direction</th></tr>
<tr><td>"L"</td><td>IN</td><td>OUT</td><td>SR21 → SR40</td></tr>
<tr><td>"H"</td><td>OUT</td><td>IN</td><td>SR40 → SR21</td></tr>
</table></td></tr>
<tr><td>DL1, DR1</td><td>I/O</td><td>Ch1 input and output</td></tr>
<tr><td>DL2, DR2</td><td>I/O</td><td>Ch2 input and output</td></tr>
</table>

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<table>
<tr><th>Parameter</th><th>I/O</th><th>Function</th></tr>
<tr><td>FCS</td><td>Input</td><td>Ch2 mode selection
<table>
<tr><th>FCS</th><th>Mode</th></tr>
<tr><td>"H"</td><td>Common signal drive mode</td></tr>
<tr><td>"L"</td><td>Segment signal drive mode</td></tr>
</table></td></tr>
<tr><td>M</td><td>Input</td><td>LCD driver clock
<table>
<tr><th colspan="3">Common signal drive mode</th></tr>
<tr><th>M</th><th>Display-On</th><th>Display-Off</th></tr>
<tr><td>"H"</td><td>V_2</td><td>V_6</td></tr>
<tr><td>"L"</td><td>V_1</td><td>V_5</td></tr>
</table>
<table>
<tr><th colspan="4">Segment signal drive mode</th></tr>
<tr><th rowspan="2">M</th><th rowspan="2">Display-On</th><th colspan="2">Display-Off</th></tr>
<tr><th>(Ch2)</th><th>(Ch1)</th></tr>
<tr><td>"H"</td><td>V_1</td><td>V_5</td><td>V_3</td></tr>
<tr><td>"L"</td><td>V_2</td><td>V_6</td><td>V_4</td></tr>
</table></td></tr>
<tr><td>CL1</td><td>Input</td><td>Data latch clock</td></tr>
<tr><td>CL2</td><td>Input</td><td>Data shift clock</td></tr>
</table>

6. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Applied Voltage*(Logic)	Vdd	+0.3 ∿ -7.0	V
Applied Voltage*(LCD Driver)	Vee	+0.3 ∿ -20.0	V
Input Voltage*	Vt	+0.3 ∿ Vdd − 0.3	V
Operating Temperature Range	Topr	-20 ∿ +70	°C
Storage Temperature Range	Tstg	-55 ∿ +150	°C

* Maximum voltage on any pin with respect to V_{SS}

7. Electrical Characteristics

7.1 DC Characteristics

V_{SS}=0V, Vdd=-5V±5%, Vee=-17V±1V, Ta=-20°C ∿ +70°C

Parameter	Symbol	Ratings			Unit	Conditions
		MIN.	TYP.	MAX.		
Input "LOW" Voltage	V_{IL}			-3.5	V	
Input "HIGH" Voltage	V_{IH}	-1.5			V	
Output "LOW" Voltage	V_{OL}			Vdd+0.4	V	I_{OL} = 0.4mA
Output "HIGH" Voltage	V_{OH}	-0.4			V	I_{OH} = 0.4mA
Voltage Drop between Vi and Yi	Vd_1			1.1	V	When 1 mA current flows into one of the pins Y_1 through Y_{40}
Voltage Drop between Vi and Yi	Vd_2			1.5	V	When 0.2 mA current flows into each of pins Y_1 through Y_{40}
Input Leakage Current	$\|I_{LI}\|$			5.0	μA	
Output Leakage Current	$\|I_{LO}\|$			10.0	μA	
Logic Current Dissipation	I_{LOG}			3.0	mA	Logic clock 1.6MHz
LCD Driver Current Dissipation	I_{DRV}			10.0	μA	LCD Driver Clock 1kHz

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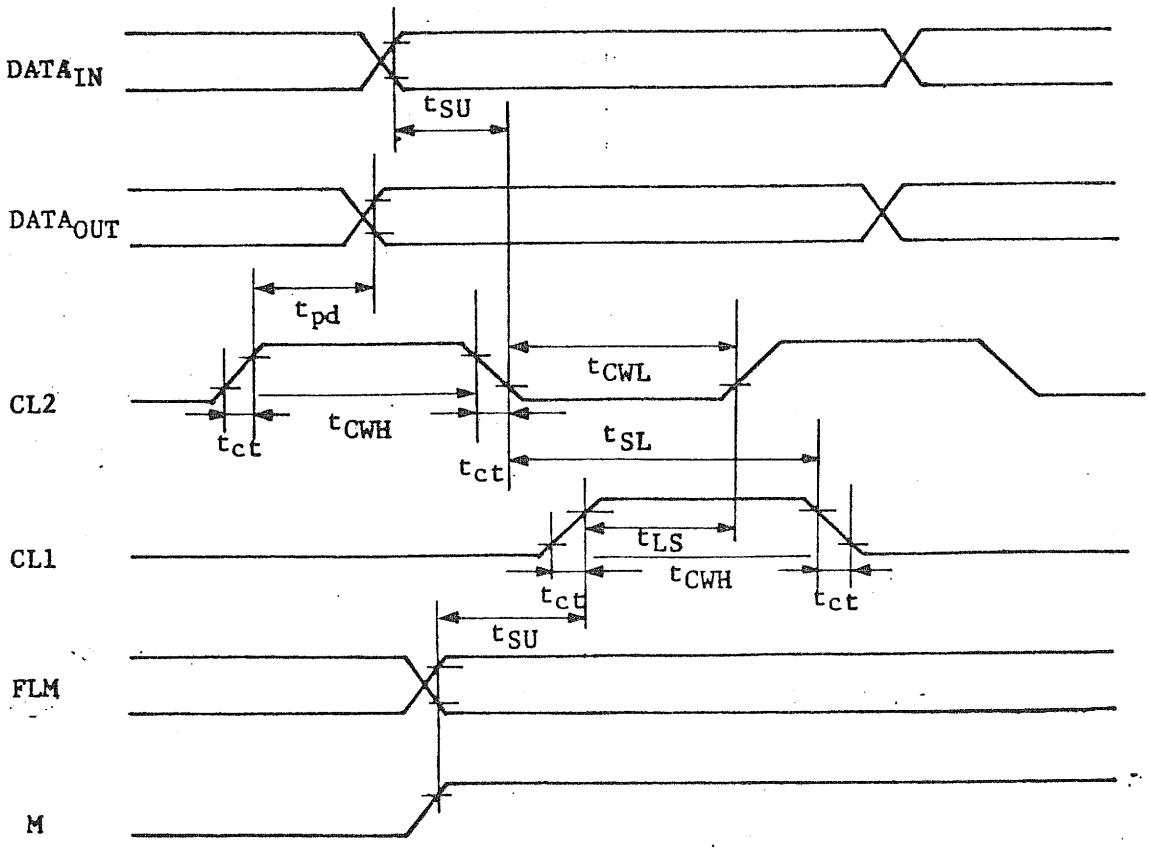
7.2 AC Characteristics

Vss=0V, Vdd=-5V±5%, Vee=-17V±1V
Ta=-20°C ∿ +70°C

Parameter	Symbol	Conditions	Ratings		Unit	Application Pins
			Min.	Max.		
High Level Clock Width	t_{CWH}		250		nS	CL1, CL2
Low Level Clock Width	t_{CWL}		250		nS	CL2
Data Setup Time	t_{SU}		70		nS	DL1, DR1, DL2, DR2
Clock Setup Time (CL2 → CL1)	t_{SL}		200		nS	CL1, CL2
Clock Setup Time (CL1 → CL2)	t_{LS}		200		nS	CL1, CL2
Output Delay Time	t_{pd}	CL = 15(pF)		180	nS	DL1, DR1, DL2, DR2
Clock Rise and Fall Times	t_{ct}			50	nS	CL1, CL2



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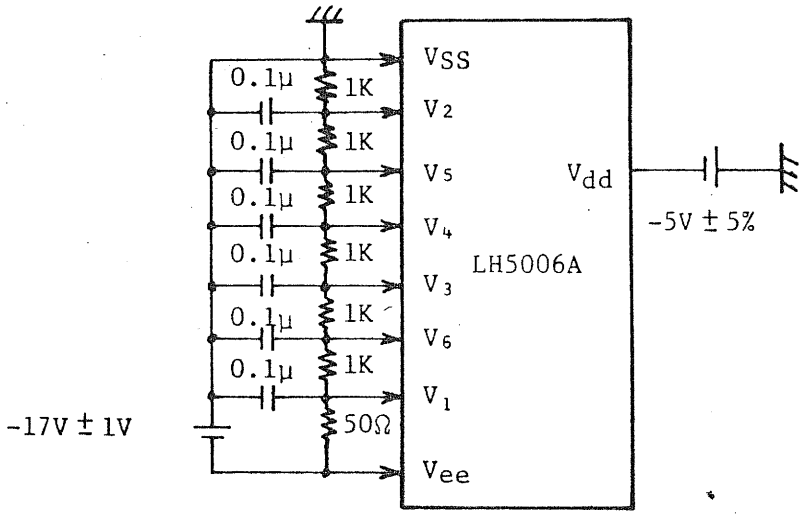
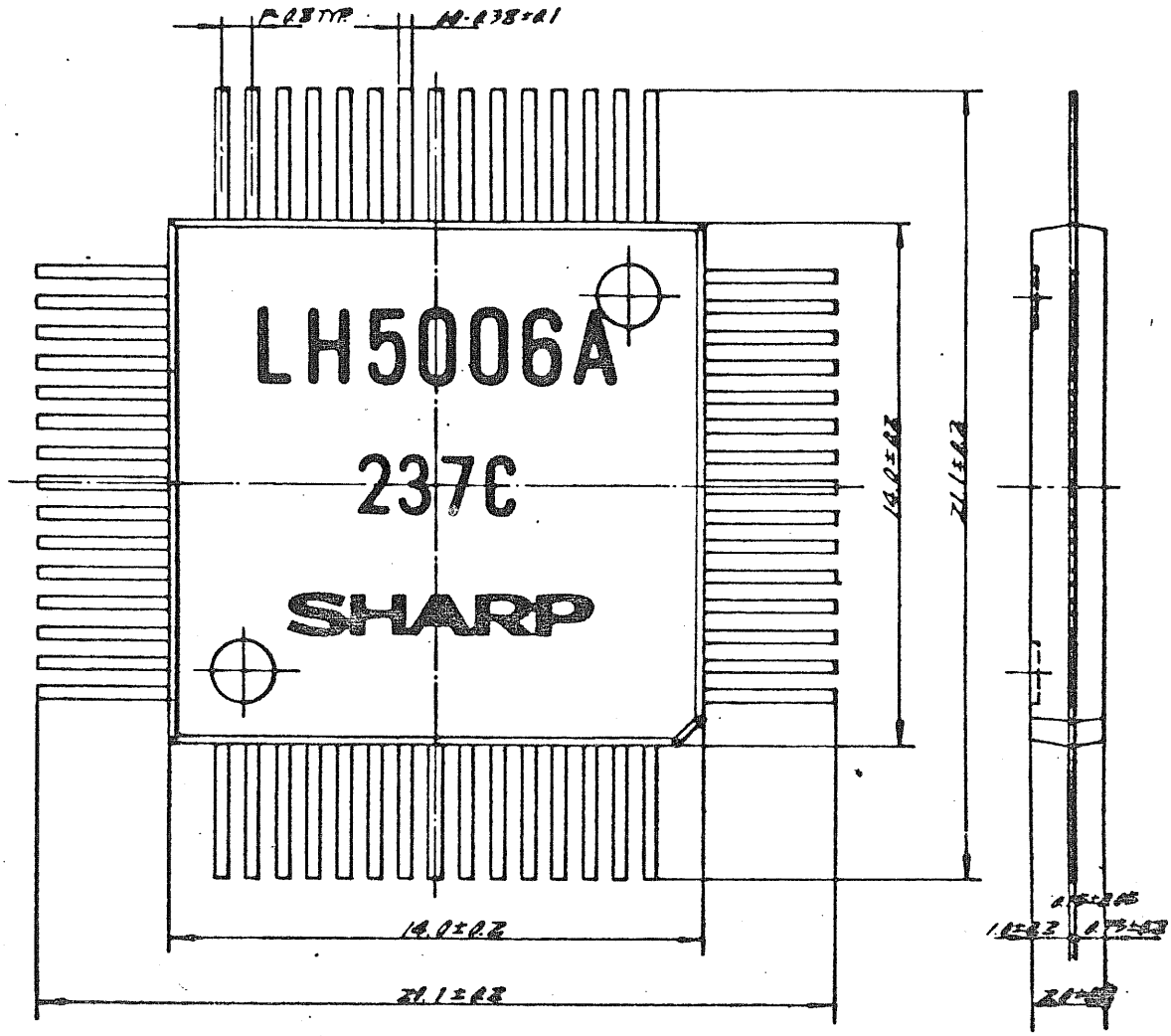
AC characteristics test circuit

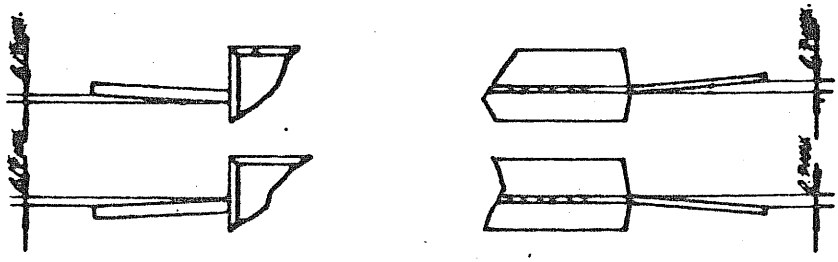


7-3. Pin capacitance

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Rating			Unit	Applicable pin
		MIN.	TYP.	MAX.		
Input capacitance (LCD driver voltage)	Ci_1			18	pF	V_1, V_2, V_3 V_4, V_5, V_6
Input capacitance (control signal)	Ci_2			5	pF	CL1, CL2, M, SHL1 SHL2, FCS
Input/output capacitance	Cio			8	pF	DL1, DR1, DL2, DR2
Output capacitance	Co			6	pF	Yi, i = 1∿40





Horizontal tolerance

Vertical tolerance

適用機種 APPLICABLE MODEL: LH5006A		尺度 SCALE: 5/1	単位 UNIT: 1 = 1/1 mm				
				改訂DATE	改訂記事 REVISE	承認 CHARGE	
板厚 THICKNESS	仕数 PIECES	材質 MATERIAL	仕上 FINISH	名称 NAME: FPT60AP			
			Sn plating				
日付 DATE: 59. 7. 18				コード CODE			
立体 DESIGN	製図 DRAW	写図 TRACE	検図 CHECK	承認 APPROVE	シャープ株式会社 電子部品事業本部		
					Integrated Circuits Div.		
					SHARP CORPORATION	図番 DRAWING No.: A-A655-129	