MCS8140 Network USB Processor

Data Sheet

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Network USB Processor

1. General Description

The MosChip MCS8140 is a highly integrated general purpose network processor that can be used in a variety of products that require network connectivity. The CPU subsystem of the MCS8140 consists of a 170 MHz ARM926EJ-S, 32-bit RISC microprocessor delivering approximately 1.1 MIPS per MHz.

The MCS8140 network processor contains four high speed USB 2.0 Ports. These ports have been designed to connect a wide range of USB-based devices to an Ethernet network (Internet or Intranet).

The 32-bit, 33MHz PCI host interface supports PCI devices which are compatible / compliant to the PCI 2.2 or 2.3 standard. The PCI controller can support up to two PCI devices. This allows the MCS8140 to connect to a variety of PCI devices such as 802.11x peripherals, Audio Controllers, PCI-SATA and PCI-IDE controllers.

The Ethernet controller in the MCS8140 contains a media access controller (MAC) and physical layer (PHY). The Ethernet interface can be connected directly to external magnetics, LED's and connectors.

In addition, the MCS8140 provides an alternate Ethernet configuration that does not use the internal PHY. In this configuration all the MII pins are available on the GPIO interface.

A robust Security Engine handles all IPSec functions including the DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms.

The interface pins for the on-chip I^2S audio controller are multiplexed with the GPIO pins and can be used for controlling an external I^2S Codec. The MCS8140 also has a software emulated serial interface which can be used to connect to a standard SPI EPROM. It also provides a local bus for system expansion.

2. Features

CPU

- 32-bit, 170 MHz ARM926EJS CPU with MMU
- 16Kbyte, 4-way associative Instruction and Data caches
- V5 instruction set

USB Host

- Four USB 2.0 ports with on-chip transceivers
- Single Enhanced Host Controller Interface (EHCI) controller
- Two Open Host Controller Interface (OHCI) controllers
- Compatible with bulk, interrupt and isochronous type USB devices
- OTG features supported on USB port 0
- On-chip OTG PHY

Ethernet

- IEEE 802.3 compliant 10/100Mbps Ethernet MAC and PHY with full/half duplex operation
- Supports Auto MDIX feature
- MII interface option for connecting an external PHY

Memory Controller

- Up to 64 MB, 100 MHz SDRAM Interface with x16 and x32 bit modes
- Up to 16 MB, 8-bit parallel Flash Interface
- 8/16-bit Local bus interface

Security Engine

- AES and DES/3DES hardware encryption and decryption
- SHA1, SHA256 and MD5 authentication in hardware

Other

- TOE (TCP / IP Offload Engine)
- Ethernet List Processing Engine
- 32bit, 33MHz PCI Host supports two PCI devices
- Standard UART supports up to 115200 bps
- I^2S controller to interface with an external I^2S audio Codec
- Up to 20 interrupt-capable GPIOs
- Software emulated SPI EEPROM interface
- JTAG interface for advanced debugging

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3. Block Diagram

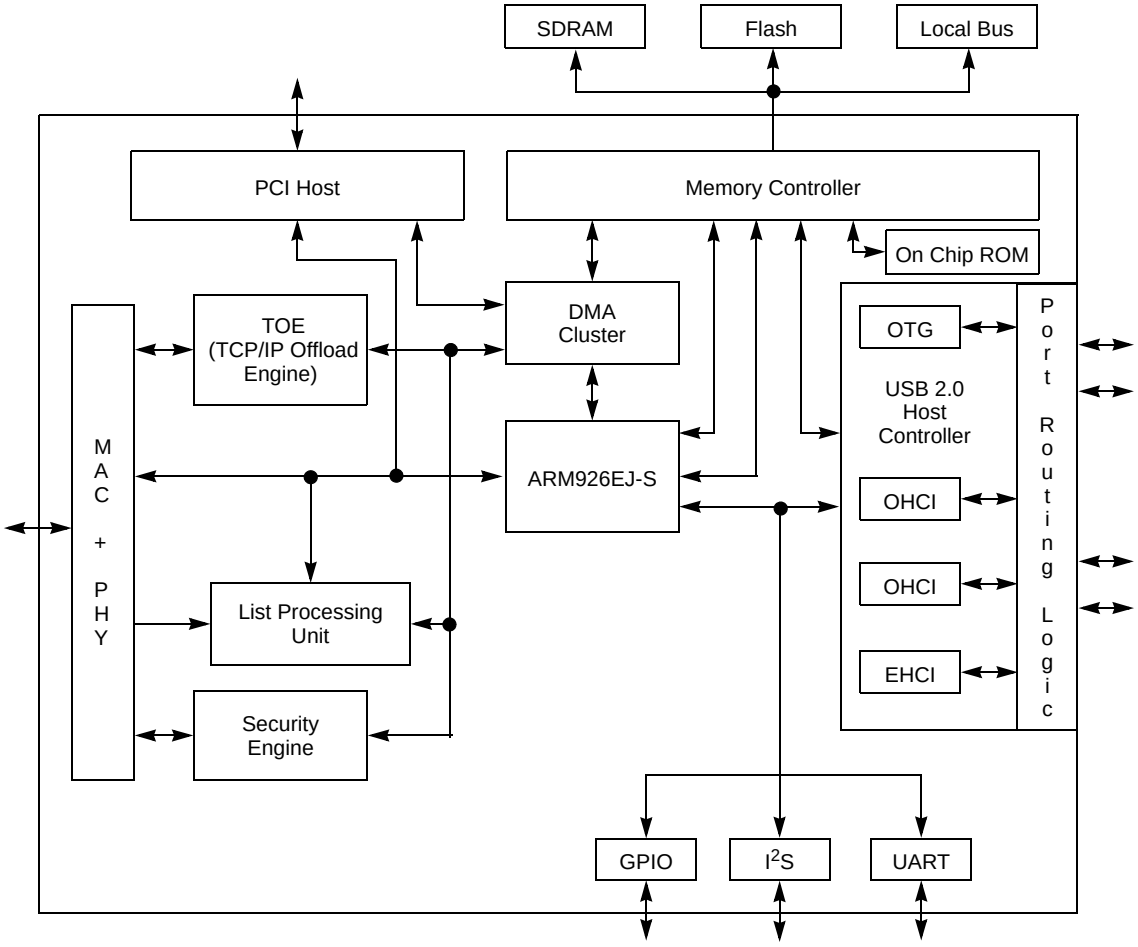

Figure 1. MCS8140 Block Diagram

4. Applications

The MCS8140 can be used in the following sample applications:

- Networked USB server/extended USB ports
- Networked USB print server
- Secure NAS (Network Attached Storage)
- WAP — Wireless Access Point / Gateway

4.1 Reference Schematics

MCS8140-SCH

4.2 Evaluation Board

MCS8140-EVB

Refer to the MCS8140 Evaluation Board manual for more information.

5. Ordering Information

Commercial Grade (0 °C to +70 °C)		
MCS8140CV	256 Pin QFP	RoHS

6. Pin Diagram

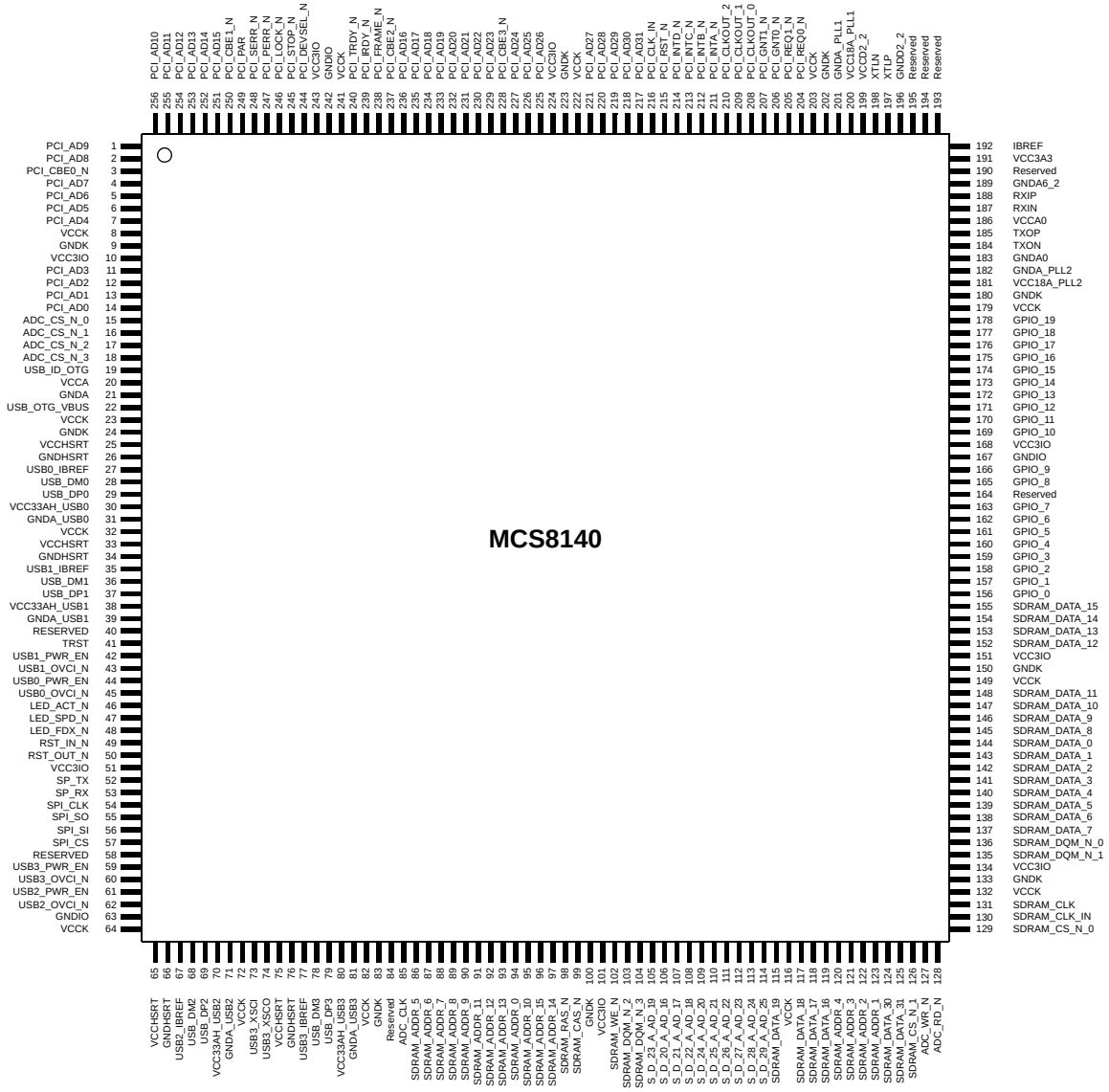

Figure 2. MCS8140 Pin Diagram

7. Pin Descriptions

Table 1 provides the pin descriptions for the MCS8140. The pins are listed in numerical order.

Table 1. MCS8140 Pin Descriptions

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
1	PCI_AD9	PCI	I/O	8 mA	PU	PCI address/data bit 9.
2	PCI_AD8	PCI	I/O	8 mA	PU	PCI address/data bit 8.
3	PCI_CBE0_N	PCI	I/O	8mA	PU	PCI command/byte enable bit 0. The command and byte enable signals for PCI data byte 0 are multiplexed onto PCI_CBE0_N. During the address phase of a transaction, PCI_CBE0_N defines the bus command. During the data phase PCI_CBE0_N defines the byte enable for data byte 0.
4	PCI_AD7	PCI	I/O	8 mA	PU	PCI address/data bit 7.
5	PCI_AD6	PCI	I/O	8 mA	PU	PCI address/data bit 6.
6	PCI_AD5	PCI	I/O	8 mA	PU	PCI address/data bit 5.
7	PCI_AD4	PCI	I/O	8 mA	PU	PCI address/data bit 4.
8	VCCK	Power	P	--	--	1.8V core supply.
9	GNDK	Power	P	--	--	Digital ground.
10	VCC3IO	Power	P	--	--	3.3V digital I/O supply.
11	PCI_AD3	PCI	I/O	8 mA	PU	PCI address/data bit 3.
12	PCI_AD2	PCI	I/O	8 mA	PU	PCI address/data bit 2.
13	PCI_AD1	PCI	I/O	8 mA	PU	PCI address/data bit 1.
14	PCI_AD0	PCI	I/O	8 mA	PU	PCI address/data bit 0.
15	ADC_CS_N_0	Memory	O	8 mA	PU	Local bus/Flash chip select 0, active low.
16	ADC_CS_N_1	Memory	O	8 mA	PU	Local bus/Flash chip select 1, active low.
17	ADC_CS_N_2	Memory	O	8 mA	PU	Local bus/Flash chip select 2, active low.
18	ADC_CS_N_3	Memory	O	8 mA	PU	Local bus/Flash chip select 3, active low.
19	USB_ID_OTG	USB	I	--	PU	ID detector for OTG (Port 0). This pin should be left unconnected if port 0 is used as a standard USB port.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
20	VCCA	Power	P	--	--	3.3V analog supply for voltage detector logic.
21	GNDA	Power	P	--	--	Analog ground for voltage detector logic.
22	USB_OTG_VBUS	USB	I	--	--	5V VBUS from USB port 0. Used if OTG functionality is enabled. This pin should be left unconnected if port 0 is used as a standard USB port.
23	VCCK	Power	P	--	--	1.8V core supply.
24	GNDK	Power	P	--	--	Digital ground.
25	VCCHSRT	Power	P	--	--	3.3V analog supply voltage for USB.
26	GNDHSRT	Power	P	--	--	Analog ground.
27	USB0_IBREF	USB	I	--	--	Connect external reference resistor (12k Ω ±1%) to analog GND.
28	USB_DM0	USB	I/O	--	--	USB 2.0 data in, negative pin terminal (port 0).
29	USB_DP0	USB	I/O	--	--	USB 2.0 data in, positive pin terminal (port 0).
30	VCC33AH_USB0	Power	P	--	--	3.3V supply for USB PHY digital portion.
31	GNDA_USB0	Power	P	--	--	USB port 0 analog ground.
32	VCCK	Power	P	--	--	1.8V core supply.
33	VCCHSRT	Power	P	--	--	3.3V analog supply voltage for USB.
34	GNDHSRT	Power	P	--	--	Analog ground.
35	USB1_IBREF	USB	I	--	--	Connect external reference resistor (12k Ω ±1%) to analog GND.
36	USB_DM1	USB	I/O	--	--	USB 2.0 data in, negative pin terminal (Port 1).
37	USB_DP1	USB	I/O	--	--	USB 2.0 data in, positive pin terminal (Port 1).
38	VCC33AH_USB1	Power	P	--	--	3.3V supply for USB PHY digital portion.
39	GNDA_USB1	Power	P	--	--	USB port 1 digital ground.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
40	RESERVED	--	--	--	--	Reserved.
41	TRST	Reset	I	--	--	JTAG interface test reset. Connect an external RC circuit to this pin.
42	USB1_PWR_EN	USB	O	4 mA	PU	USB port power is enabled by default with power-up. Furthermore, this pin can be used to turn on/off the specific USB port power with the help of external power management circuits. In case of over current detection through an external power management circuit, this pin can be transitioned by the host controller.
43	USB1_OVCI_N	USB	I	--	PU	Over-current signal input from external power management circuit for USB host port 1. This signal indicates that this external circuit has sensed an over-current condition. It can be set active high or active low depending on the boot strap settings.
44	USB0_PWR_EN	USB	O	4 mA	PU	USB port power is enabled by default with power-up. Furthermore, this pin can be used to turn on/off the specific USB port power with the help of external power management circuits. In case of over current detection through an external power management circuit, this pin can be transitioned by the host controller.
45	USB0_OVCI_N	USB	I	--	PU	Over-current signal input from external power management circuit for USB host port 0. This signal indicates that this external circuit has sensed an over-current condition. It can be set active high or active low depending on the boot strap settings.
46	LED_ACT_N	Ethernet	O	8 mA	PD	Ethernet transmit/receive activity LED. It is an active low signal which indicates Transmit or Receive activity.
47	LED_SPD_N	Ethernet	O	8 mA	PD	Ethernet speed LED. When asserted, this active low signal indicates 100 Mbps operation.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
48	LED_FDX_N	Ethernet	O	8 mA	PD	Ethernet full duplex LED. When asserted, this active low signal indicates full duplex operation.
49	RST_IN_N	Reset	I	--	--	Active low system reset input. Connect a 100ms RC circuit to this pin.
50	RST_OUT_N	Reset	O	4 mA	--	Active low reset out for other peripherals.
51	VCC3IO	Power	P	--	--	3.3V digital I/O supply.
52	SP_TX	Console	O	4 mA	PU	Debug console/UART transmit data line.
53	SP_RX	Console	I	--	PU	Debug console/UART receive data line.
54	SPI_CLK	EEPIO	I/O	4 mA	PROG	Programmable SPI serial EEPROM clock.
55	SPI_SO	EEPIO	I/O	4 mA	PROG	EEPROM I/O programmable SO.
56	SPI_SI	EEPIO	I/O	4 mA	PROG	EEPROM I/O programmable SI.
57	SPI_CS	EEPIO	I/O	4 mA	PROG	Programmable SPI serial EEPROM chip select.
58	RESERVED	--		--	--	Reserved.
59	USB3_PWR_EN	USB	O	4 mA	PU	USB port power is enabled by default with power-up. Furthermore, this pin can be used to turn on/off the specific USB port power with the help of external power management circuits. In case of over-current detection through an external power management circuit, this pin can be transitioned by the host controller.
60	USB3_OVCI_N	USB	I	--	PU	Over-current signal input from external power management circuit for USB host port 3. This signal indicates that this external circuit has sensed an over-current condition. It can be set active high or active low depending on the boot strap settings.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
61	USB2_PWR_EN	USB	O	4 mA	PU	USB Port Power is enabled by default with power-up. Further this pin can be used turn on / off the specific USB Port power with the help of external power management circuits. In case of over-current detection through an external power management circuit, this pin can be transitioned by the host controller.
62	USB2_OVCI_N	USB	I	--	PU	Over-current signal input from external power management circuit for USB host port 2. This signal indicates that this external circuit has sensed an over-current condition. It can be set active high or active low depending on the boot strap settings.
63	GNDIO	Power	P	--	--	Digital Ground.
64	VCCK	Power	P	--	--	1.8V core supply.
65	VCCHSRT	Power	P	--	--	3.3V analog supply voltage for USB.
66	GNDHSRT	Power	P	--	--	Analog ground.
67	USB2_IBREF	USB	I	--	--	Connect external reference resistor (12k Ω ±1%) to analog GND.
68	USB_DM2	USB	I/O	--	--	USB 2.0 data in, negative pin terminal (Port 2).
69	USB_DP2	USB	I/O	--	--	USB 2.0 data in, positive pin terminal (Port 2).
70	VCC33AH_USB2	Power	P	--	--	3.3V supply for USB PHY digital portion.
71	GNDA_USB2	Power	P	--	--	Analog Ground.
72	VCCK	Power	P	--	--	1.8V core supply.
73	USB3_XSCI	Clock	I	--	--	12 MHz crystal oscillator input.
74	USB3_XSCO	Clock	O	--	--	12 MHz crystal oscillator output.
75	VCCHSRT	Power	P	--	--	3.3V analog supply voltage for USB.
76	GNDHSRT	Power	P	--	--	Analog ground.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
77	USB3_IBREF	USB	I	--	--	Connect external reference resistor (12k Ω ±1%) to analog GND.
78	USB_DM3	USB	I/O	--	--	USB 2.0 data in, negative pin terminal (Port 3).
79	USB_DP3	USB	I/O	--	--	USB 2.0 data in, positive pin terminal (Port 3).
80	VCC33AH_USB3	Power	P	--	--	3.3V supply for USB PHY digital portion.
81	GNDA_USB3	Power	P	--	--	Analog Ground.
82	VCCK	Power	P	--	--	1.8V core supply.
83	GNDK	Power	P	--	--	Digital ground.
84	RESERVED	--	--	--	PD	Reserved pin.
85	ADC_CLK	Memory	O	8 mA	PD	Programmable local bus clock out.
86	SDRAM_ADDR_5	Memory	O	8 mA	PD	Address bit 5 for SDRAM interface and local bus.
87	SDRAM_ADDR_6	Memory	O	8 mA	PD	Address bit 6 for SDRAM interface and local bus.
88	SDRAM_ADDR_7	Memory	O	8 mA	PD	Address bit 7 for SDRAM interface and local bus.
89	SDRAM_ADDR_8	Memory	O	8 mA	PD	Address bit 8 for SDRAM interface and local bus.
90	SDRAM_ADDR_9	Memory	O	8 mA	PD	Address bit 9 for SDRAM interface and local bus.
91	SDRAM_ADDR_11	Memory	O	8 mA	PD	Address bit 11 for SDRAM interface and local bus.
92	SDRAM_ADDR_12	Memory	O	8 mA	PD	Address bit 12 for SDRAM interface and local bus.
93	SDRAM_ADDR_13	Memory	O	8 mA	PD	Address bit 13 for SDRAM interface and local bus.
94	SDRAM_ADDR_0	Memory	O	8 mA	PD	Address bit 0 for SDRAM interface and local bus.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
95	SDRAM_ADDR_10	Memory	O	8 mA	PD	Address bit 10 for SDRAM interface and local bus.
96	SDRAM_ADDR_15	Memory	O	8 mA	PD	Address bit 15 for SDRAM interface and local bus.
97	SDRAM_ADDR_14	Memory	O	8 mA	PD	Address bit 14 for SDRAM interface and local bus.
98	SDRAM_RAS_N	Memory	O	8 mA	PU	Row Address Select (RAS) for SDRAM interface.
99	SDRAM_CAS_N	Memory	O	8 mA	PU	Column Address Select (CAS) for SDRAM interface.
100	GNDK	Power	P	--	--	Digital ground.
101	VCC3IO	Power	P	--	--	3.3V digital I/O supply.
102	SDRAM_WE_N	Memory	O	8 mA	PU	Write enable for SDRAM interface.
103	SDRAM_DQM_N_2	Memory	O	8 mA	PU	Memory byte enable signal 2 – DQM for SDRAM.
104	SDRAM_DQM_N_3	Memory	O	8 mA	PU	Memory byte enable signal 3 – DQM for SDRAM.
105	S_D_23_A_AD_19	Memory	I/O	8 mA	--	SDRAM data bit 23 multiplexed with address bit 19 for local bus.
106	S_D_20_A_AD_16	Memory	I/O	8 mA	--	SDRAM Data bit 20 multiplexed with address bit 16 for local bus.
107	S_D_21_A_AD_17	Memory	I/O	8 mA	--	SDRAM Data bit 21 multiplexed with address bit 17 for local bus.
108	S_D_22_A_AD_18	Memory	I/O	8 mA	--	SDRAM Data bit 22 multiplexed with address bit 18 for local bus.
109	S_D_24_A_AD_20	Memory	I/O	8 mA	--	SDRAM Data bit 24 multiplexed with address bit 20 for local bus.
110	S_D_25_A_AD_21	Memory	I/O	8 mA	--	SDRAM Data bit 25 multiplexed with address bit 21 for local bus.
111	S_D_26_A_AD_22	Memory	I/O	8 mA	--	SDRAM Data bit 26 multiplexed with address bit 22 for local bus.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
112	S_D_27_A_AD_23	Memory	I/O	8 mA	--	SDRAM Data bit 27 multiplexed with address bit 27 for local bus.
113	S_D_28_A_AD_24	Memory	I/O	8 mA	--	SDRAM Data bit 28 multiplexed with address bit 24 for local bus.
114	S_D_29_A_AD_25	Memory	I/O	8 mA	--	SDRAM Data bit 29 multiplexed with address bit 25 for local bus.
115	SDRAM_DATA_19	Memory	I/O	8 mA	--	Data bit 19 for SDRAM interface.
116	VCCK	Power	P	--	--	1.8V core supply.
117	SDRAM_DATA_18	Memory	I/O	8 mA	--	Data bit 18 for SDRAM interface.
118	SDRAM_DATA_17	Memory	I/O	8 mA	--	Data bit 17 for SDRAM interface.
119	SDRAM_DATA_16	Memory	I/O	8 mA	--	Data bit 16 for SDRAM interface.
120	SDRAM_ADDR_4	Memory	O	8 mA	PD	Address bit 4 for SDRAM interface and local bus.
121	SDRAM_ADDR_3	Memory	O	8 mA	PD	Address bit 3 for SDRAM interface and local bus.
122	SDRAM_ADDR_2	Memory	O	8 mA	PD	Address bit 2 for SDRAM interface and local bus.
123	SDRAM_ADDR_1	Memory	O	8 mA	PD	Address bit 1 for SDRAM interface and local bus.
124	SDRAM_DATA_30	Memory	I/O	8 mA	--	Data bit 30 for SDRAM interface.
125	SDRAM_DATA_31	Memory	I/O	8 mA	--	Data bit 31 for SDRAM interface.
126	SDRAM_CS_N_1	Memory	O	8 mA	PU	Chip select signal 1 for SDRAM memory.
127	ADC_WR_N	Memory	O	8 mA	PU	Local bus write, active low.
128	ADC_RD_N	Memory	O	8 mA	PU	Local bus read, active low.
129	SDRAM_CS_N_0	Memory	O	8 mA	PU	Chip select signal 0 for SDRAM memory.
130	SDRAM_CLK_IN	Memory	I	--	--	The SDRAM_CLK_IN is the SDRAM feed-back clock input. This pin is connected to SDRAM_CLK out pin and is used to latch the data from the SDRAM.
131	SDRAM_CLK	Memory	O	8 mA	--	100 MHz clock output for SDRAM's.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
132	VCCK	Power	P	--	--	1.8V core supply.
133	GNDK	Power	P	--	--	Digital ground.
134	VCC3IO	Power	P	--	--	3.3V digital I/O supply.
135	SDRAM_DQM_N_1	Memory	O	8 mA	PU	Memory Byte enable signal 1 – DQM for SDRAM.
136	SDRAM_DQM_N_0	Memory	O	8 mA	PU	Memory Byte enable signal 0 – DQM for SDRAM.
137	SDRAM_DATA_7	Memory	I/O	8 mA	--	Data bit 7 for SDRAM interface and local bus.
138	SDRAM_DATA_6	Memory	I/O	8 mA	--	Data bit 6 for SDRAM interface and local bus.
139	SDRAM_DATA_5	Memory	I/O	8 mA	--	Data bit 5 for SDRAM interface and local bus.
140	SDRAM_DATA_4	Memory	I/O	8 mA	--	Data bit 4 for SDRAM interface and local bus.
141	SDRAM_DATA_3	Memory	I/O	8 mA	--	Data bit 3 for SDRAM interface and local bus.
142	SDRAM_DATA_2	Memory	I/O	8 mA	--	Data bit 2 for SDRAM interface and local bus.
143	SDRAM_DATA_1	Memory	I/O	8 mA	--	Data bit 1 for SDRAM interface and local bus.
144	SDRAM_DATA_0	Memory	I/O	8 mA	--	Data bit 0 for SDRAM interface and local bus.
145	SDRAM_DATA_8	Memory	I/O	8 mA	--	Data bit 8 for SDRAM interface and local bus.
146	SDRAM_DATA_9	Memory	I/O	8 mA	--	Data bit 9 for SDRAM interface and local bus.
147	SDRAM_DATA_10	Memory	I/O	8 mA	--	Data bit 10 for SDRAM interface and local bus.
148	SDRAM_DATA_11	Memory	I/O	8 mA	--	Data bit 11 for SDRAM interface and local bus.
149	VCCK	Power	P	--	--	1.8V core supply.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
150	GNDK	Power	P	--	--	Digital ground.
151	VCC3IO	Power	P	--	--	3.3V digital I/O supply.
152	SDRAM_DATA_12	Memory	I/O	8 mA	--	Data bit 12 for SDRAM interface and local bus.
153	SDRAM_DATA_13	Memory	I/O	8 mA	--	Data bit 13 for SDRAM interface and local bus.
154	SDRAM_DATA_14	Memory	I/O	8 mA	--	Data bit 14 for SDRAM interface and local bus.
155	SDRAM_DATA_15	Memory	I/O	8 mA	--	Data bit 15 for SDRAM interface and local bus.
156	GPIO_0	GPIO	I/O	8 mA	PROG	General purpose I/O line 0.
157	GPIO_1	GPIO	I/O	8 mA	PROG	General purpose I/O line 1.
158	GPIO_2	GPIO	I/O	8 mA	PROG	General purpose I/O line 2.
159	GPIO_3	GPIO	I/O	8 mA	PROG	General purpose I/O line 3.
160	GPIO_4	GPIO	I/O	8 mA	PROG	General purpose I/O line 4.
161	GPIO_5	GPIO	I/O	8 mA	PROG	General purpose I/O line 5.
162	GPIO_6	GPIO	I/O	8 mA	PROG	General purpose I/O line 6.
163	GPIO_7	GPIO	I/O	8 mA	PROG	General purpose I/O line 7.
164	RESERVED	--	--	--	--	Reserved pin.
165	GPIO_8	GPIO	I/O	8 mA	PROG	General purpose I/O line 8.
166	GPIO_9	GPIO	I/O	8 mA	PROG	General purpose I/O line 9.
167	GNDIO	Power	P	--	--	Digital Ground.
168	VCC3IO	Power	P	--	--	3.3V digital I/O supply.
169	GPIO_10	GPIO	I/O	8 mA	PROG	General purpose I/O line 10.
170	GPIO_11	GPIO	I/O	8 mA	PROG	General purpose I/O line 11.
171	GPIO_12	GPIO	I/O	8 mA	PROG	General purpose I/O line 12.
172	GPIO_13	GPIO	I/O	8 mA	PROG	General purpose I/O line 13.
173	GPIO_14	GPIO	I/O	8 mA	PROG	General purpose I/O line 14.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
174	GPIO_15	GPIO	I/O	8 mA	PROG	General purpose I/O line 15.
175	GPIO_16	GPIO	I/O	8 mA	PROG	General purpose I/O line 16.
176	GPIO_17	GPIO	I/O	8 mA	PROG	General purpose I/O line 17.
177	GPIO_18	GPIO	I/O	8 mA	PROG	General purpose I/O line 18.
178	GPIO_19	GPIO	I/O	8 mA	PROG	General purpose I/O line 19.
179	VCCK	Power	P	--	--	1.8V core supply.
180	GNDK	Power	P	--	--	Digital ground.
181	VCC18A_PLL2	Power	P	--	--	1.8V analog supply for internal PLL.
182	GNDA_PLL2	Power	P	--	--	Analog ground (PLL).
183	GNDA0	Power	P	--	--	Analog ground (Ethernet PHY).
184	TXON	Ethernet	O	--	--	10/100 transmit data channel A Negative (-).
185	TXOP	Ethernet	O	--	--	10/100 transmit data channel A Positive (+).
186	VCCA0	Power	P	--	--	1.8V analog supply for Ethernet PHY.
187	RXIN	Ethernet	I	--	--	10/100 receive data channel B Negative (-).
188	RXIP	Ethernet	I	--	--	10/100 receive data channel B Positive (+).
189	GNDA6_2	Power		--	--	Analog Ground (Ethernet PHY).
190	RESERVED	--	--	--	--	Reserved pin.
191	VCC3A3	Power	P	--	--	3.3V power supply for Ethernet analog portion.
192	IBREF	Ethernet	I	--	--	Off-chip resistor. Connects 12.3±1% K ohm resistor to ground.
193	RESERVED	--	--	--	--	Reserved pin.
194	RESERVED	--	--	--	--	Reserved pin.
195	RESERVED	--	--	--	--	Reserved pin.
196	GNDD2_2	Power	P	--	--	Analog ground (Ethernet PHY).

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
197	XTLP	Clock	I	--	--	25 MHz crystal input / output. A 25 MHz parallel-resonant crystal may be connected between these pins to stabilize the internal oscillator. One terminal of the crystal is connected to XTLP, and the other is connected to XTLN.
198	XTLN	Clock	O	--	--	See description for XTLP above.
199	VCCD2_2	Power	P	--	--	1.8V analog supply for Ethernet PHY.
200	VCC18A_PLL1	Power	P	--	--	1.8V analog supply for PLL.
201	GNDA_PLL1	Power	P	--	--	Analog ground.
202	GNDK	Power	P	--	--	Digital ground.
203	VCCK	Power	P	--	--	1.8V core supply.
204	PCI_REQ0_N	PCI	I	--	PU	PCI request for 1st device.
205	PCI_REQ1_N	PCI	I	--	PU	PCI request for 2nd device.
206	PCI_GNT0_N	PCI	O	8 mA	--	PCI grant for 1st device.
207	PCI_GNT1_N	PCI	O	8 mA	--	PCI grant for 2nd device.
208	PCI_CLKOUT_0	PCI	O	8 mA	--	PCI clock to PCI Slot 1.
209	PCI_CLKOUT_1	PCI	O	8 mA	--	PCI clock to PCI Slot 2.
210	PCI_CLKOUT_2	PCI	O	8 mA	--	Connect this pin to PCI_CLK_IN (pin 216).
211	PCI_INTA_N	PCI	I		PU	PCI interrupt A.
212	PCI_INTB_N	PCI	I		PU	PCI interrupt B.
213	PCI_INTC_N	PCI	I		PU	PCI interrupt C.
214	PCI_INTD_N	PCI	I		PU	PCI interrupt D.
215	PCI_RST_N	PCI	O	8 mA	PU	PCI Reset out.
216	PCI_CLK_IN	PCI	I	--	--	The PCI_CLK_IN pin is used as the PCI host feedback clock input. This pin is connected to the PCI_CLK_OUT2 pin.
217	PCI_AD31	PCI	I/O	8 mA	PU	PCI address/data bit 31.
218	PCI_AD30	PCI	I/O	8 mA	PU	PCI address/data bit 30.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
219	PCI_AD29	PCI	I/O	8 mA	PU	PCI address/data bit 29.
220	PCI_AD28	PCI	I/O	8 mA	PU	PCI address/data bit 28.
221	PCI_AD27	PCI	I/O	8 mA	PU	PCI address/data bit 27.
222	VCCK	Power	P	--	--	1.8V core supply.
223	GNDK	Power	P	--	--	Digital ground.
224	VCC3IO	Power	P	--	--	3.3V digital I/O supply.
225	PCI_AD26	PCI	I/O	8 mA	PU	PCI address/data bit 26.
226	PCI_AD25	PCI	I/O	8 mA	PU	PCI address/data bit 25.
227	PCI_AD24	PCI	I/O	8 mA	PU	PCI address/data bit 24.
228	PCI_CBE3_N	PCI	I/O	8 mA	PU	PCI command/byte enable bit 3. The command and byte enable signals for PCI data byte 3 are multiplexed onto PCI_CBE3_N. During the address phase of a transaction, PCI_CBE3_N defines the bus command. During the data phase PCI_CBE3_N defines the byte enable for data byte 3.
229	PCI_AD23	PCI	I/O	8 mA	PU	PCI address/data bit 23.
230	PCI_AD22	PCI	I/O	8 mA	PU	PCI address/data bit 22.
231	PCI_AD21	PCI	I/O	8 mA	PU	PCI address/data bit 21.
232	PCI_AD20	PCI	I/O	8 mA	PU	PCI address/data bit 20.
233	PCI_AD19	PCI	I/O	8 mA	PU	PCI address/data bit 19.
234	PCI_AD18	PCI	I/O	8 mA	PU	PCI address/data bit 18.
235	PCI_AD17	PCI	I/O	8 mA	PU	PCI address/data bit 17.
236	PCI_AD16	PCI	I/O	8 mA	PU	PCI address/data bit 16.
237	PCI_CBE2_N	PCI	I/O	8 mA	PU	PCI command/byte enable bit 2. The command and byte enable signals for PCI data byte 2 are multiplexed onto PCI_CBE2_N. During the address phase of a transaction, PCI_CBE2_N defines the bus command. During the data phase PCI_CBE2_N defines the byte enable for data byte 2.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
238	PCI_FRAME_N	PCI	I/O	8 mA	PU	PCI Start of Frame. The current initiator drives PCI_FRAME to indicate the beginning and duration of a PCI transaction. While the initiator asserts PCI_FRAME, data transfer continues. When the initiator negates PCI_FRAME, the transaction is in the final data phase. PCI_FRAME is an input to the MCS8140 when it is the target, and PCI_FRAME is an output of the MCS8140 when it is the initiator. PCI_FRAME remains tri-stated by the MCS8140 until driven by an initiator.
239	PCI_IRDY_N	PCI	I/O	8 mA	PU	PCI Initiator ready. PCI_IRDY indicates the ability of the device as an initiator to complete the current data phase of the transaction. It is used in conjunction with PCI_TRDY. When a data phase is completed on any clock, both PCI_IRDY and PCI_TRDY are sampled asserted. During a write transaction, PCI_IRDY indicates the valid data present on PCI_AD [31:0]. During a read transaction, it indicates the readiness of the MCS8140 to latch data. PCI_IRDY is an input to the MCS8140 when it is the target and an output of the MCS8140 when it is an initiator. PCI_IRDY remains tri-stated by the MCS8140 until driven by an initiator.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
240	PCI_TRDY_N	PCI	I/O	8 mA	PU	PCI target ready. PCI_TRDY_N indicates the ability of the MCS8140 as a target to complete the current data phase of the transaction. PCI_TRDY_N is used in conjunction with PCI_IRDY_N. A data phase is completed when both PCI_IRDY_N and PCI_TRD_N are sampled asserted. During a read transaction PCI_TRDY_N indicates the valid data on the PCI_AD [31:0]. During a write transaction PCI_TRDY_N indicates the readiness of the MCS8140 as a target to latch the data. PCI_TRDY_N is an input to the MCS8140 when it is the initiator and an output of the MCS8140 when it is a target. PCI_TRDY_N is tri-stated signal and remains tri-stated by the MCS8140 until driven by a target.
241	VCCK	Power	P	--	--	1.8V core supply.
242	GNDIO	Power	P	--	--	Digital Ground.
243	VCC3IO	Power	P	--	--	3.3V digital I/O supply.
244	PCI_DEVSEL_N	PCI	I/O	8 mA	PU	Active low host PCI device select: As an output, the MCS8140 asserts PCI_DEVSEL_N when a PCI master peripheral attempts an access to an internal address or an address in the main memory. As an input, PCI_DEVSEL_N indicates the response to a transaction on the PCI bus. PCI_DEVSEL_N is a tri-stated signal and remains tri-stated by MCS8140 until driven by a target device.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
245	PCI_STOP_N	PCI	I/O	8 mA	PU	Active low host PCI stop. PCI_STOP_N indicates that the MCS8140 as a target is requesting the initiator to stop the current transaction. PCI_STOP_N causes the MCS8140 as an initiator to stop the current transaction. PCI_STOP is an output when the MCS8140 as a target and an input when the SP16 is an initiator. PCI_STOP_N is used together with PCI_TRDY_N and PCI_DEVSEL_N during the data phase to terminate the current transaction with or without data transfer.
246	PCI_LOCK_N	PCI	I/O	8 mA	PU	Active low PCI bus lock. This pin is asserted by either the host or the MCS8140 to indicate an atomic transaction that may require more than one bus transaction to complete. PCI_LOCK_N is asserted at the beginning of the operation, then deasserted at the end of the operation.
247	PCI_PERR_N	PCI	I/O	8 mA	PU	PCI parity error signal. An external PCI device drives PCI_PERR_N when it receives data that has a parity error. The MCS8140 drives PCI_PERR when it detects a parity error.
248	PCI_SERR_N	PCI	I/O	8 mA	PU	PCI system error signal. PCI_SERR_N can be pulsed active by any PCI device that detects a system error condition. Upon sampling PCI_SERR active, the MCS8140 has the ability to generate an interrupt.

Table 1. MCS8140 Pin Descriptions (Continued)

Pin Number	Pin Name	Group	Type	Drive Strength	Internal Status	Description
249	PCI_PAR	PCI	I/O	8 mA	PU	PCI Parity signal. PCI_PAR uses even parity calculated on 36 bits (PCI_AD [31:0] plus PCI_CBE_N [3:0]. Even parity means that the device counts the number of ones within the 36 bits plus PCI_PAR and the sum is always even. The MCS8140 always calculates PCI_PAR on 36 bits regardless of the valid byte enables. The MCS8140 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The MCS8140 drives and tri-states PAR identically to the PCI_AD [31:0] lines except that the MCS8140 delays PAR by exactly one PCI clock. PCI_PAR is an output during the address phase (delayed one clock) for all MCS8140-initiated transactions. PCI_PAR is an output during the data phase (delayed one clock) when the MCS8140 is the initiator of a PCI write transaction, and when it is the target of a read transaction.
250	PCI_CBE1_N	PCI	I/O	8 mA	PU	PCI command/byte enable bit 1. The command and byte enable signals for PCI data byte 1 are multiplexed onto PCI_CBE1_N. During the address phase of a transaction, PCI_CBE1_N defines the bus command. During the data phase PCI_CBE1_N defines the byte enable for data byte 1.
251	PCI_AD15	PCI	I/O	8 mA	PU	PCI address/data bit 15.
252	PCI_AD14	PCI	I/O	8 mA	PU	PCI address/data bit 14.
253	PCI_AD13	PCI	I/O	8 mA	PU	PCI address/data bit 13.
254	PCI_AD12	PCI	I/O	8 mA	PU	PCI address/data bit 12.
255	PCI_AD11	PCI	I/O	8 mA	PU	PCI address/data bit 11.
256	PCI_AD10	PCI	I/O	8 mA	PU	PCI address/data bit 10.

8. Architectural Overview

The following subsections provide an architectural overview of the MCS8140 network processor.

8.1 CPU

The MCS8140 network processor is based on the ARM926EJ-S processor core. The MCS8140 includes all the standards functions of the ARM926EJ-S, including the ARMv5TEJ instruction set, memory management unit (MMU), caches, Jazelle™ processing engine (Java), and JTAG interface. The ARM926EJ-S has 16 KByte instruction and data caches.

8.2 MCS8140 Clocking Scheme

The MCS8140 requires two external clock sources:

- 25 MHz for MAC and other blocks
- 12MHz dedicated for USB PHY

Two built-in PLL's generate clocks for CPU, SDRAM controller, PCI controller, as well as the system clock for the remaining logic blocks.

8.3 Boot ROM

The on-chip ROM is a 32 KByte read only memory that consists of initial configuration information for the MCS8140. The ROM is used to initialize the ARM core, memory controller and internal modules. In addition, the boot loader has a in-built serial EEPROM utility for loading dynamic configuration data from an SPI-type serial EEPROM. This ROM is factory masked and is not user programmable.

8.4 UART Interface

The UART interface implements an industry standard 16550-compatible protocol, including transmit (TX), receive (RX), Request to Send (RTS), Clear to Send (CTS), Data Set Ready (DSR), Data Terminal Ready (DTR), Data Carrier Detect (DCD), and Ring Indicator (RI) pins for serial mode of operation. Except for TX and RX, all UART pins listed above are multiplexed on the GPIO interface. The serial mode of operation is selected through boot strap options.

An RS-232 Line driver is required in order to achieve standard RS-232 levels. The registers in the UART are compatible with the 16550 and can support baud rates from 1200 bps to 115.2 Kbps.

8.5 GPIO Interface

The MCS8140 contains up to twenty general purpose I/O (GPIO) pins used for system control and connection to various devices. Each GPIO pin can be programmed as an input or output and can also be used as interrupt request lines.

The GPIO Interface register layout can be configured so that the direction and level of each I/O can be configured using either a single register for all I/O's, or discrete registers for each I/O. The GPIO lines are multiplexed with the MII, JTAG, and I^2S interfaces and can be selected through pin straps at the system level.

GPIO Pin	Pin Function				
	After disabling JTAG and enabling GPIO	Default on power-up if no other mode is selected	I^2S Mode	Serial Mode	MII Mode
GPIO_0	GPIO_0	GPIO_0	GPIO0	GPIO0	MAC_MII_RX_DATA[0]
GPIO_1	GPIO_1	GPIO_1	GPIO1	GPIO1	MAC_MII_RX_DATA[1]
GPIO_2	GPIO_2	GPIO_2	GPIO2	GPIO2	MAC_MII_RX_DATA[2]
GPIO_3	GPIO_3	GPIO_3	GPIO3	GPIO3	MAC_MII_RX_DATA[3]
GPIO_4	GPIO_4	GPIO_4	BCLK	DTR	MAC_MII_TX_CLK
GPIO_5	GPIO_5	GPIO_5	DATAO	RI	MAC_MII_TX_EN
GPIO_6	GPIO_6	GPIO_6	WS	DCD	MAC_MII_RX_ERR
GPIO_7	GPIO_7	GPIO_7	DATAI	DSR	MAC_MII_RX_CLK
GPIO_8	GPIO_8	GPIO_8	SYSCLK(O)	RTS	MAC_MII_RX_DV
GPIO_9	GPIO_9	GPIO_9	SYSCLK(I)	CTS	MAC_MII_COLL
GPIO_10	GPIO_10	GPIO_10	GPIO10	GPIO10	MAC_MII_CRS
GPIO_11	GPIO_11	GPIO_11	GPIO11	GPIO11	MAC_MII_MDC
GPIO_12	GPIO_12	GPIO_12	GPIO12	GPIO12	MAC_MII_MDIO
GPIO_13	GPIO_13	GPIO_13	GPIO13	GPIO13	MAC_MII_TX_DATA[0]
GPIO_14	GPIO_14	GPIO_14	GPIO14	GPIO14	MAC_MII_TX_DATA[1]
GPIO_15	GPIO_15	GPIO_15	GPIO15	GPIO15	MAC_MII_TX_DATA[2]
GPIO_16	GPIO_16	TMS(I)	GPIO16	GPIO16	MAC_MII_TX_DATA[3]
GPIO_17	GPIO_17	TCK(I)	GPIO17	GPIO17	RESERVED
GPIO_18	GPIO_18	TDI(I)	GPIO18	GPIO18	GPIO18
GPIO_19	GPIO_19	TDO(O)	GPIO19	GPIO19	GPIO19

8.6 Software Emulated Serial EEPROM Interface

The software emulated SPI interface can be used to connect a serial EEPROM utilizing the SPI mode of operation. The on-chip boot ROM uses this interface to load configuration data from 25010/020/040 types of serial EEPROM's.

This software emulated SPI interface can also be used to connect SPI based Real Time Clock (RTC) chips for embedded applications.

8.7 PCI Host Interface

In the MCS8140, the PCI host bridge connects the CPU to external PCI devices through the internal PCI controller, The host bridge contains an internal PCI arbiter and is used to initialize and communicate with PCI devices. The CPU controls and configures the PCI host bridge as well as external PCI devices connected to the PCI bus. The MCS8140 can access PCI devices using the master interface channel. The PCI host bridge contains an internal arbiter and can support up to two external PCI devices.

8.8 External Memory Controller Interface

The Memory Controller unit shares multiple external memory devices and protocols for all internal units - CPU, DMA cluster. The memory controller supports up to 64 MBytes of SDRAM (32 MB per region) and up to 16 MByte of Flash.

8.8.1 SDRAM Interface

The SDRAM interface supports x16 and x32 bit modes. The maximum SDRAM capacity is 64 MBytes in 32-bit mode, and 32 MBytes in 16-bit mode.

8.8.2 Flash Interface

The MCS8140 supports an 8-bit parallel Flash interface that can address up to 16 MBytes.

8.9 Cipher Engine (Security Engine)

The Cipher engine accelerates the IPSec protocol by using dedicated hardware blocks. It implements the Encapsulating Security Payload (ESP) and Authentication Header (AH) IPSec protocols. The encryption and authentication algorithms that the MCS8140 uses are DES, 3DES, AES, SHA-1, SHA-256 and MD5. The MCS8140 performs DES, 3DES and AES in both Cipher Block Chaining (CBC) mode and Electronic Code Book (ECB) mode. The AES algorithm can be performed in 128-, 192-, and 256-bit modes.

8.10 Ethernet MAC

The MCS8140 10/100 fast Ethernet controller interface consists of DMA, TLI, MAC, and PHY sub-blocks. The PHY can be directly connected to 1:1 Ethernet transformers.

The DMA automates memory transfers and frees the CPU from this task. The Transaction Layer Interface (TLI) is a 64-bit wide block designed to provide a bridge between the DMA controller and a 10/100 Ethernet MAC. The TLI uses built-in FIFO’s for receive and transmit buffering.

The Ethernet Media Access Controller (MAC) core incorporates the essential protocol requirements for operation of an Ethernet/IEEE 802.3 compliant node and provides an interface between the host sub-

system and the Media Independent Interface (MII). The MAC can operate in 100Mbps/10Mbps modes either in full duplex or half duplex based on the clock provided on the MII interface.

The primary attributes of the MAC block are:

1. Transmit and receive message data encapsulation.
   a. Framing - Frame boundary delimitation, Frame synchronization.
   b. Error detection - physical medium transmission errors.
2. Media access management.
   a. Medium allocation - Collision avoidance, except in full-duplex operation.
   b. Contention resolution - Collision handling, except in full-duplex operation.
3. Flow Control during Full Duplex mode.
   a. Decoding of control frames (PAUSE Command) and disabling the transmitter.
   b. Generation of control Frames.
4. Serial Interface Control.
   a. Support of MII protocol to interface with a MII based PHY.
5. Management Interface support on MII.
   a. Generation of Management frames on the MDC/MDIO pins to communicate to an external PHY.

The MCS8140 implements an address filtering mechanism, controls the packet filter for good/bad frames, a 48-bit MAC address that contains the local station address, a multicast hash table used for filtering multicast frames, etc. The 48-bit MAC address must be loaded into the MAC address buffer during power-up.

The MCS8140 has an integrated physical layer (PHY) connected to the internal MAC. The PHY is designed to connect directly to Ethernet Magnetics to support:

- Reliable data transfers over cable lengths up to 100 meters.
- 1:1 Ethernet transformer.
- Full and half-duplex operation with full-featured auto-negotiation function.
- Media Dependent Interface (MDI) / Media Dependent Interface Crossover (MDIX).
- Built-in loop-back and test modes.

The MCS8140 also has an alternate Ethernet configuration that does not use the internal PHY. In this configuration the MII is available on the external GPIO pins. The GPIO[16:0] pins are dedicated to the MII function and are unavailable for use as general purpose signals in this mode. This configuration is controlled via bootstrap pins at the system level.

Table 2, “Ethernet PHY Alternative Configuration Pins" show the relationship between the GPIO pins and the Ethernet MII when the MCS8140 is configured in the alternate function Ethernet mode.

Table 2. Ethernet PHY Alternative Configuration Pins

Pin Name	Alternate Function	I/O Status in MII Mode
GPIO_0	MII_RX_DATA[0]	I
GPIO_1	MII_RX_DATA[1]	I
GPIO_2	MII_RX_DATA[2]	I
GPIO_3	MII_RX_DATA[3]	I
GPIO_4	MII_TX_CLK	I
GPIO_5	MII_TX_EN	O
GPIO_6	MII_RX_ERR	I
GPIO_7	MII_RX_CLK	I
GPIO_8	MII_RX_VAL	I
GPIO_9	MII_COL	I
GPIO_10	MII_CRS	I
GPIO_11	MII_TX_MDC	O
GPIO_12	MII_MDIO	I/O
GPIO_13	MII_TX_DATA[0]	O
GPIO_14	MII_TX_DATA[1]	O
GPIO_15	MII_TX_DATA[2]	O
GPIO_16	MII_TX_DATA[3]	O

8.11 I²S Audio

The I²S audio interface is a serial link used for transmitting stereo audio between devices in a system. The I²S interface consists of transmitter and receiver cores which operate in Master mode. The I²S bus is multiplexed with the GPIO lines and is enabled using the bootstrap settings.

The I²S controller has 5 pins which are multiplexed with the GPIO lines as follows.

Table 3. I²S Signal Multiplexing on the GPIO Interface

Pin name	Alternate Function	I/O status	Description
GPIO_4	BCLK	O	Bit clock input
GPIO_5	DATAO	O	Data output
GPIO_6	WS	O	Word select (left/right channel)
GPIO_7	DATAI	I	Data input
GPIO_8	I2S_SYS_CLK	O	System clock (256 fs)

8.12 JTAG Interface

The MCS8140 network processor can be controlled during debug through a JTAG interface to the processor. The JTAG interface is multiplexed with selected GPIO pins as shown in the following table. The JTAG interface is enabled on power-up if no other mode is selected.

Table 4. JTAG Signal Multiplexing on the GPIO Interface

Pin name	Alternate Function	I/O status	Description
GPIO_16	TMS	I	Test Mode select
GPIO_17	TCK	I	Test Clock
GPIO_18	TDI	I	Test Data Input
GPIO_19	TDO	O	Test Data Output

8.13 Ethernet List Processing Engine

The List Processing Engine in the MCS8140 helps to implement the ‘interrupt moderation' feature. Interrupt moderation reduces hardware interrupts to the ARM CPU which are generated by the MAC controller in order to request cycles for packet processing.

As traffic rates increase, the system spends more and more time servicing MAC interrupts. The overhead of processing these interrupts begins to degrade overall system performance as the CPU spends

the majority of its time scheduling and executing the interrupt handler.These interrupts must be controlled to achieve optimum throughput. Too few interrupts can lead to latencies and too many can unduly burden the ARM9 processor. By bundling an appropriate number of packets before issuing an interrupt to the ARM, the 'List Processing Engine' in the MAC controller tunes interrupt frequency to match traffic conditions while maintaining packet flow. The List Processing Engine' is enabled by default and can be completely disabled through software, if required. When the List Processing engine is disabled, MCS8140 generates one interrupt for every packet received.

8.14 TCP/IP Offload Engine (TOE)

The MCS8140 has a stateless TOE engine. Amongst other features it has TCP Segmentation offload (TSO) in which TCP layer passes a very large segment through the stack to the TOE hardware, which segments it into a number of packets. This method improves performance by reducing per-packet software overheads within the network stack. The segmentation is performed inside MCS8140 MAC hardware and generates headers for each packet.

Other important offloads handled by the TOE block are TCP, UDP and IP checksum calculation and verification. With the TOE engine programmed, the TCP/IP software stack need not calculate and update checksum fields in the protocol headers.

The TOE block is enabled by default and can be completely disabled through software, if required. When TOE is disabled, the MCS8140 can transmit Ethernet frames without any modifications.

8.15 Memory to Memory DMA Engine

The DMA controller automatically transfers data from the source memory location to the destination without the intervention of CPU.

The DMA controller can be configured for different operations.

8.15.1 DMA Operations

The MCS8140 supports the following DMA operations. Note that for all DMA operations, the source and destination addresses need to be quad-word aligned.

Block Transfer

The block transfer mechanism transfers a block of memory form one location to another location of memory. If block transfer is enabled, the Scatter and Gather DMA transactions must not be enabled.

Block Checksum

This operation can be enabled for checksum on a block of data present in the memory.

IP Checksum

This operation can be enabled for IP checksum on an IP packet present in the memory.

TCP Checksum

This operation can be enabled for TCP checksum on an IP packet present in the memory.

IP and TCP Checksum

This operation can be enabled for TCP and IP checksums on an IP packet present in memory.

Gather DMA

The gather DMA transfer mechanism gathers chunks of data from different locations of memory and writes them into memory as a block of contiguous data.

Scatter DMA

The scatter DMA transfer mechanism scatters a contiguous block of data from memory to different locations in the memory.

8.16 USB 2.0 Host Controller

The USB 2.0 host controller includes one high-speed mode host controller and two USB 1.1 host controllers.The high-speed (USB2.0) host controller implements an EHCI interface. It is used for all high-speed communications to high-speed devices connected to the root ports of the USB 2.0 host controller.

The EHCI specification allows communications to full- and low-speed devices connected to the root ports of the USB 2.0 host controller to be provided by companion USB 1.1 host controllers.

The Companion Host Controller Interface (OHCI) always manages full- and low-speed USB devices connected to the root ports. High-speed (USB2.0) devices are always controlled by the EHCI host controller.

EHCI is the default owner of all the root ports. For example, if the attached device is not a high-speed device, the EHCI driver releases ownership of the port (and thus control of the device) to a companion host controller. For that port, enumeration starts over from the initial attach detect point and the device is enumerated under the OHCI. Otherwise, the EHCI retains ownership of the port and the device completes enumeration under the EHCI.

8.17 OTG Controller

The OTG controller is compliant with USB Specification Rev 2.0 and OTG supplement Rev 1.0a. The host controller supports high (480 Mbps), full (12 Mbps) and low (1.5 Mbps) speed modes of operation. The device controller has two programmable endpoints other than one control and one interrupt IN endpoint.

9. Bootstraps

There are certain attributes of the MCS8140 that must be setup before reset becomes inactive. These configuration settings are controlled via a bootstrap register. The bootstrap register is loaded with values based on the logic levels of the bootstrap pins immediately after reset is inactivated.

Bootstraps control two main aspects of the MCS8140: processor speed and internal or external boot. The ARM926EJ-S core has been designed to operate from 125 MHz to 170 MHz depending on the power/performance requirements of the system. See Table 6, “Processor Speed and Corresponding Bootstrap Settings" for the appropriate settings based on the frequency desired.

The various bootstrap options of the MCS8140 are shown in Table 5.

Table 5. MCS8140 Bootstrap Options

Pin Number	Pin Name	Internal Status	Default Setting for Normal Operation	Description
98	SDRAM_RAS_N	PU	1	Invert bus power enable.
102	SDRAM_WE_N	PU	0	0 - Clock stop disable 1 - Clock stop enable
16	ADC_CS_N_1	PU	0	Invert OVCI.
17	ADC_CS_N_2	PU	0	0 - Disable on-chip ROM 1 - Enable on-chip ROM
46	LED_ACT_N	PD	0	Speed Select. See Table 6, “Processor Speed and Corresponding Bootstrap Settings".
47	LED_SPD_N	PD	0	Speed Select. See Table 6, “Processor Speed and Corresponding Bootstrap Settings".
48	LED_FDX_N	PD	0	Speed Select. See Table 6, “Processor Speed and Corresponding Bootstrap Settings".
52	SP_TX	PU	1	Speed Select. See Table 6, “Processor Speed and Corresponding Bootstrap Settings".
44	USB0_PWR_EN	PU	0	CAS program select.
42	USB1_PWR_EN	PU	1	10 - Ext MII mode 01 - Serial mode 00 – I^2S mode 11 – Normal mode
61	USB2_PWR_EN	PU	1	
126	SDRAM_CS_N_1	PU	1	0 - Enable OTG 1 - Disable OTG

The ARM926EJ-S core has been designed to operate from 125 to 170 MHz depending on the power and performance requirements of the system. See Table 6, “Processor Speed and Corresponding Bootstrap Settings" for the appropriate settings based on the frequency desired.

Table 6. Processor Speed and Corresponding Bootstrap Settings

Processor Clock (MHz)	LED_ACT_N (Pin 46)	LED_SPD_N (Pin 47)	LED_FDX_N (Pin 48)	SP_TX (Pin 52)
125	0	1	0	0
137.5	1	1	0	0
162.5	0	0	0	1
150	1	0	0	1
170	0	0	0	0

The values of these bootstraps are loaded into the bootstrap register and can be used for any user-defined purpose. All bootstraps have default values through internal pull-downs/pull-ups and must be overridden with external pull-ups/pull-downs. In order to override the internal pull-down, an external 10 KΩ resistor is recommended.

10. MCS8140 Boot-Up Sequence and Operation

The internal boot loader is a piece of code that resides in on-chip ROM. This code cannot be modified. The main purpose of the code is to run the necessary initial configuration tasks.

In addition, the boot loader also has a built-in serial EEPROM utility for loading dynamic configuration data from an SPI type serial EEPROM. Usually this data includes factory initialized Ethernet MAC addresses. Any configuration information, up to a maximum of 504 bytes, may be stored in this serial device.

11. Serial EEPROM Layout

On power up, the MCS8140 polls the bootstrap pins, then executes the I-Boot code in order to initialize the system. The internal boot loader is a piece of fixed code that resides in on-chip ROM. This code cannot be modified. The main purpose of the code is to run the necessary initial configuration tasks.

In addition, the boot loader has an in-built serial EEPROM utility for loading dynamic configuration data from SPI type serial EEPROM. Data such as the factory-initialized MAC addresses for Ethernet, and any other configuration information, with a maximum total of 504 bytes, may be stored in the serial EEPROM.

The initial Internal boot code has region 0 and region 7 mapped. It executes this code and depending on the boot strap settings the CPU fetches an instruction either to jump to the Internal Rom code offset of 0x1c000100 address (Region 7 internally), or jump to external Flash. In either cases, after the jump, the boot code initializes the memory controller, disables the internal ROM on region 0 and maps the region 0 to SDRAM's connected. The remaining boot code is then relocated to SDRAM and the CPU fetches an

instruction to jump to the relocated SDRAM address.

Table 7. Tag Structure

Bit	Description
31:28	Command 0 – end of list 1 – write data 2 – jump)
27	0 – memory address, 1 – configuration address
25:24	Data word size: 0 – byte 1 – word 2 – double-word
23:20	Data word count (1 – 16) 0000 = 1 data word ..... 1111 = 16 data words
19:0	Address offset 19:2 for double-word 19:1 for word 19:0 for bytes

Table 8. Serial EEPROM Layout

0:	ID 0	ID 1	ID 2	ID 3	ID4	ID 5	ID 6	ID 7
8:	TAG0				DATA0		TAG1..	
16:	..		DATA1					
24:								
				TAGn				
x*8:	..DATAn							

Table 9. Sample Configuration Structure for Ethernet MAC

Start Address	Size in Bytes	Value	Description
0x8	4	0x1A184004	TAG0 – write conf, 2 double-words, starting at address 84004 (MAC address hi)
0xC	4	0xUUUU1234	Data value for higher order of MAC address (U – undefined)
0x10	4	0x56789ABCD	Data value for lower order of MAC address MAC address will come 12.34.56.78.AB.CD

12. Electrical Specifications

12.1 Absolute Maximum Ratings

Stresses beyond those indicated in Table 10 may cause permanent damage to the MCS8140 device, even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced device life span and reduced reliability.

Table 10. Maximum Ratings

Parameter	Min	Max
Operating Temperature	0	70C
Storage Temperature	-45	125
Core Supply Voltage	1.8V – 5%	1.8V + 5%
I/O Supply Voltage	3.3V-5%	3.3V+5%
Input clamp Current		10mA
Output clamp current		25mA
ESD HBM (MIL-STD 883E Method 3015-7 Class 2)		2000V
ESD MM (JEDEC EIA/JESD22 A115-A)		200V
CDM (JEDEC JESD22 C101-A)		500V

12.2 Recommended Operating Conditions

Table 11. Recommended Operating Conditions

Symbol	Description and Condition	Min	Typ	Max	Unit
VCCK	Digital 1.8 V power supply voltage	1.7	1.8	1.9	V
VCC33AH_USB0, VCC33AH_USB1, VCC33AH_USB2, VCC33AH_USB3.	Digital 3.3 V power supply (USB)	2.97	3.3	3.63	V
VCC18A_PLL1	Analog 1.8 V power supply voltage	1.62	1.8	1.98	V
VCC18A_PLL2	Analog 1.8 V power supply voltage	1.62	1.8	1.98	V
VCCD2_2	Analog 1.8 V power supply voltage	1.62	1.8	1.98	V
VCCA0	Analog 1.8 V power supply voltage	1.62	1.8	1.98	V
VCC3IO	Digital 3.3 V power supply voltage for I/O's	3.14	3.30	3.46	V
VCCA	Analog 3.3 V power supply voltage	2.97	3.3	3.63	V
VCCHSRT	Analog 3.3 V power supply voltage	2.97	3.3	3.63	V
VCC3A3	Analog 3.3 V power supply voltage	2.97	3.3	3.63	V
Ta	Operating temperature	0	25	70	°C
ICC_K	1.8V core current	450	465	550	mA
$I_{I/O}$	3.3V I/O current	45	70	100	mA

13. Mechanical Specifications

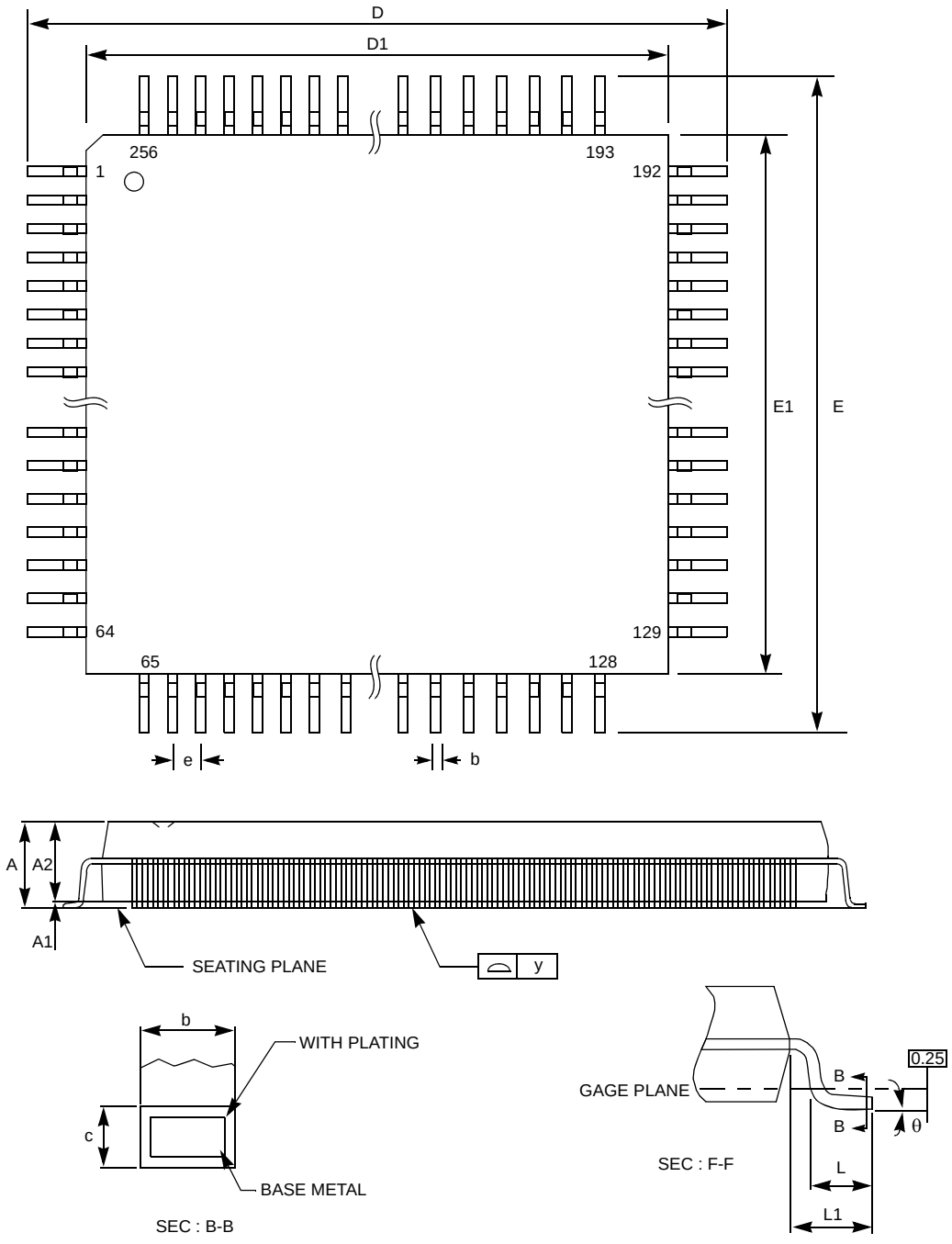

Figure 3. 256-pin QFP Package Drawing

Table 12. 256-pin QFP Package Dimensions

Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	--	4.07
A1	0.25	--	--
A2	3.15	3.23	3.30
b	0.14	0.18	0.23
c	0.13	--	0.23
D	30.35	30.60	30.85
D1	27.90	28.00	28.10
E	30.35	30.60	30.85
E1	27.90	28.00	28.10
e	0.40 BSC		
L	0.50	0.60	0.70
L1	1.30 REF		
y	--	--	0.08
θ	0	3.5	7

14. Revision History

Table 13: Revision History

Version	Description	Author(s)	Date
1.0	First release of MCS8140 Data Sheet	Srikanth & Vamshi Krishna	02/23/2007
1.1	Data Sheet updated as per ASIC bring-up and ASIC Validation findings	Vamshi Krisha, Rohit, Ravinder, GN and Swagath	06/18/07