

# DATA SHEET

## **TDA5051A** Home automation modem

Product specification  
Supersedes data of 1997 Sep 19  
File under Integrated Circuits, IC11

1999 May 31

## Home automation modem

## TDA5051A

## FEATURES

- Full digital carrier generation and shaping
- Modulation/demodulation frequency set by clock adjustment, from microcontroller or on-chip oscillator
- High clock rate of 6-bit A/D (Digital to Analog) converter for rejection of aliasing components
- Fully integrated output power stage with overload protection
- Automatic Gain Control (AGC) at receiver input
- 8-bit A/D (Analog to Analog) converter and narrow digital filtering
- Digital demodulation delivering baseband data
- Easy compliance with EN50065-1 with simple coupling network
- Few external components for low cost applications
- SO16 plastic package.

## APPLICATIONS

- Home appliance control (air conditioning, shutters, lighting, alarms and so on)
- Energy/heating control
- Amplitude Shift Keying (ASK) data transmission using the home power network.

## GENERAL DESCRIPTION

The TDA5051A is a modem IC, specifically dedicated to ASK transmission by means of the home power supply network, at 600 or 1200 baud data rate. It operates from a single 5 V supply.

## QUICK REFERENCE DATA

| SYMBOL        | PARAMETER                                                                                                     | CONDITIONS                                            | MIN.        | TYP.           | MAX.           | UNIT           |
|---------------|---------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|-------------|----------------|----------------|----------------|
| $V_{DD}$      | supply voltage                                                                                                |                                                       | 4.75        | 5.0            | 5.25           | V              |
| $I_{DD(tot)}$ | total supply current<br>reception mode<br>transmission mode ( $\overline{DATA_{IN}} = 0$ )<br>power-down mode | $f_{osc} = 8.48 \text{ MHz}$<br><br>$Z_L = 30 \Omega$ | –<br>–<br>– | 28<br>47<br>19 | 38<br>68<br>25 | mA<br>mA<br>mA |
| $f_{cr}$      | carrier frequency                                                                                             | note 1                                                | 95          | 132.5          | 148.5          | kHz            |
| $f_{osc}$     | oscillator frequency                                                                                          |                                                       | 6.08        | 8.48           | 9.504          | MHz            |
| $V_{o(rms)}$  | output carrier signal on CISPR16 load (RMS value)                                                             |                                                       | 120         | –              | 122            | dB $\mu$ V     |
| $V_{i(rms)}$  | input signal (RMS value)                                                                                      | note 2                                                | 82          | –              | 122            | dB $\mu$ V     |
| THD           | total harmonic distortion on CISPR16 load with coupling network                                               |                                                       | –           | –55            | –              | dB             |
| $Z_L$         | load impedance                                                                                                |                                                       | 1           | 30             | –              | $\Omega$       |
| BR            | baud rate                                                                                                     |                                                       | –           | 600            | 1200           | bits/s         |
| $T_{amb}$     | ambient temperature                                                                                           |                                                       | 0           | –              | 70             | °C             |

## Notes

1. Frequency range corresponding to the EN50065-1 band. However, the modem can operate at any lower oscillator frequency.
2. The minimum value can be improved by using an external amplifier, see application diagrams Figs 22 and 23.

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ORDERING INFORMATION

| TYPE<br>NUMBER | PACKAGE |                                                            |          |
|----------------|---------|------------------------------------------------------------|----------|
|                | NAME    | DESCRIPTION                                                | VERSION  |
| TDA5051AT      | SO16    | plastic small outline package; 16 leads; body width 7.5 mm | SOT162-1 |

BLOCK DIAGRAM

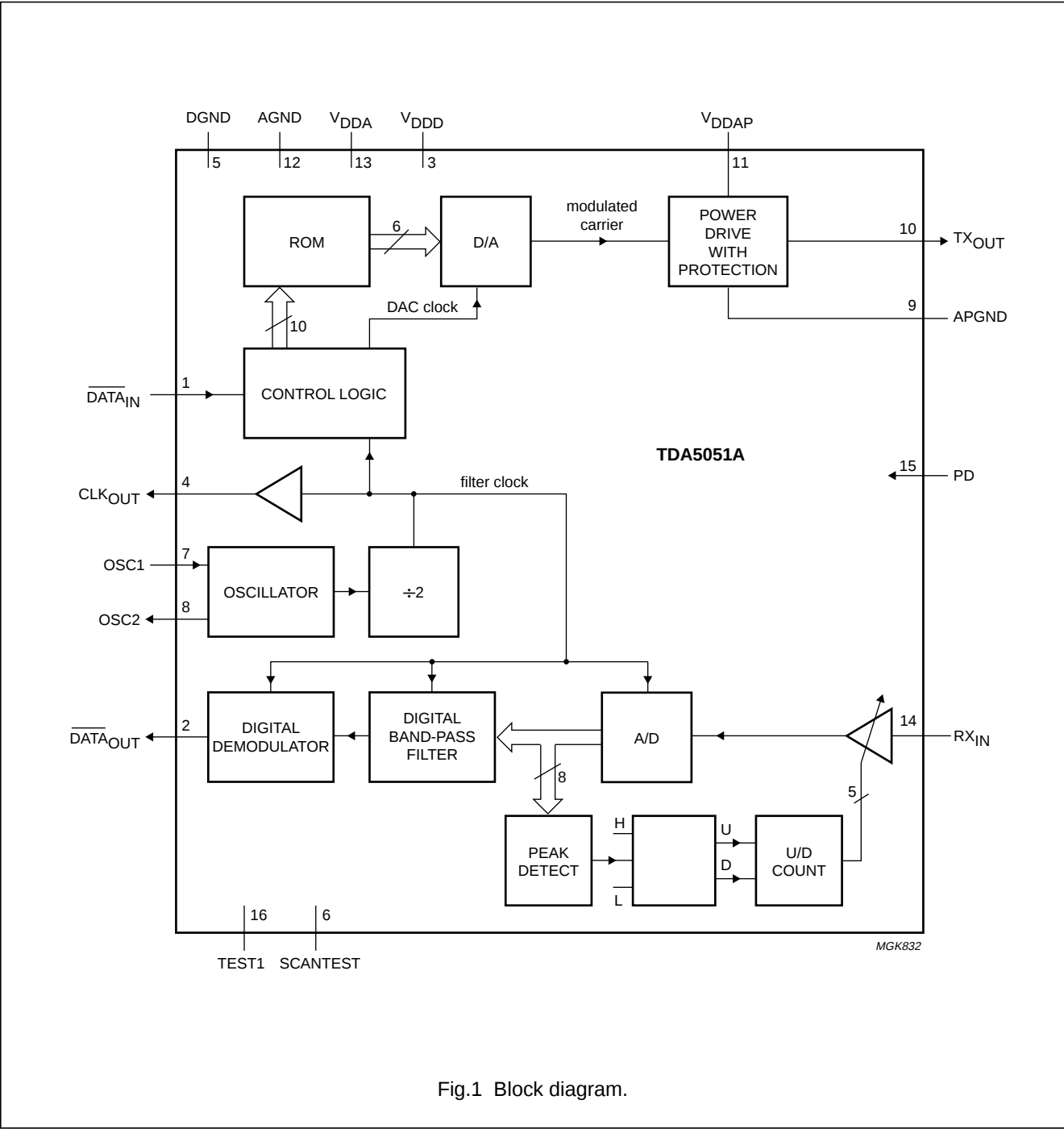


Fig.1 Block diagram.

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## PINNING

| SYMBOL                                | PIN | DESCRIPTION                               |
|---------------------------------------|-----|-------------------------------------------|
| $\overline{\text{DATA}}_{\text{IN}}$  | 1   | digital data input (active LOW)           |
| $\overline{\text{DATA}}_{\text{OUT}}$ | 2   | digital data output (active LOW)          |
| $V_{\text{DDD}}$                      | 3   | digital supply voltage                    |
| $\text{CLK}_{\text{OUT}}$             | 4   | clock output                              |
| DGND                                  | 5   | digital ground                            |
| SCANTEST                              | 6   | test input (LOW in application)           |
| OSC1                                  | 7   | oscillator input                          |
| OSC2                                  | 8   | oscillator output                         |
| APGND                                 | 9   | analog ground for power amplifier         |
| $\text{TX}_{\text{OUT}}$              | 10  | analog signal output                      |
| $V_{\text{DDAP}}$                     | 11  | analog supply voltage for power amplifier |
| AGND                                  | 12  | analog ground                             |
| $V_{\text{DDA}}$                      | 13  | analog supply voltage                     |
| $\text{RX}_{\text{IN}}$               | 14  | analog signal input                       |
| PD                                    | 15  | power-down input (active HIGH)            |
| TEST1                                 | 16  | test input (HIGH in application)          |

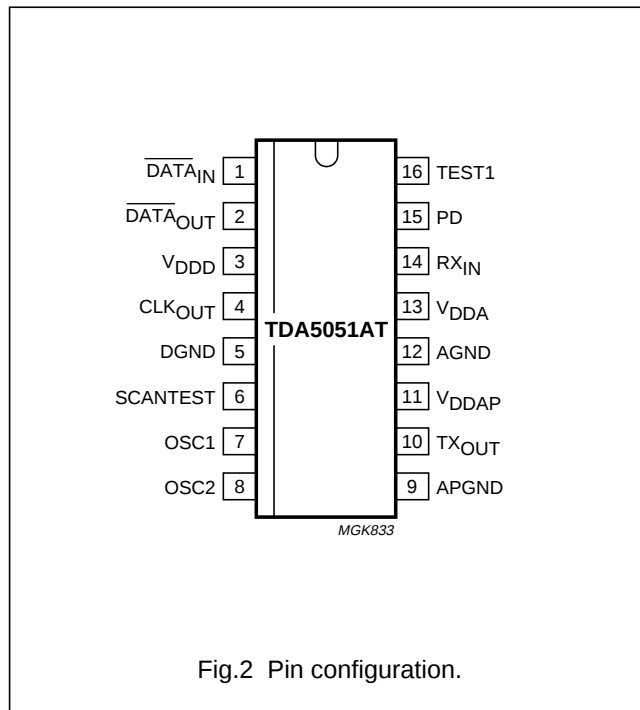


Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

Both transmission and reception stages are controlled either by the master clock of the microcontroller or by the on-chip reference oscillator connected to a crystal. This ensures the accuracy of the transmission carrier and the exact trimming of the digital filter, thus making the performance totally independent of application disturbances such as component spread, temperature, supply drift and so on.

The interface with the power network is made by means of an LC network (see Fig.18). The device includes a power output stage that feeds a 120 dB $\mu$ V (RMS) signal on a typical 30  $\Omega$  load.

To reduce power consumption, the IC is disabled by a power-down input (pin PD): in this mode, the on-chip oscillator remains active and the clock continues to be supplied at pin  $\text{CLK}_{\text{OUT}}$ . For low-power operation in reception mode, this pin can be dynamically controlled by the microcontroller, see Section "Power-down mode".

When the circuit is connected to an external clock generator (see Fig.6), the clock signal must be applied at pin OSC1 (pin 7); OSC2 (pin 8) must be left open-circuit. Fig.7 shows the use of the on-chip clock circuit.

All logic inputs and outputs are compatible with TTL/CMOS levels, providing an easy connection to a standard microcontroller I/O port.

The digital part of the IC is fully scan-testable. Two digital inputs, SCANTEST and TEST1, are used for production test: these pins must be left open-circuit in functional mode (correct levels are internally defined by pull-up or pull-down resistors).

## Transmission mode

To provide strict stability with respect to environmental conditions, the carrier frequency is generated by scanning the ROM memory under the control of the microcontroller clock or the reference frequency provided by the on-chip oscillator. High frequency clocking rejects the aliasing components to such an extent that they are filtered by the coupling LC network and do not cause any significant disturbance. The data modulation is applied through pin  $\overline{\text{DATA}}_{\text{IN}}$  and smoothly applied by specific digital circuits to the carrier (shaping). Harmonic components are limited in this process, thus avoiding unacceptable disturbance of the transmission channel (according to CISPR16 and EN50065-1 recommendations). A -55 dB Total Harmonic Distortion (TDH) is reached when the typical LC coupling network (or an equivalent filter) is used.

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The DAC and the power stage are set in order to provide a maximum signal level of 122 dB $\mu$ V (RMS) at the output.

The output of the power stage (TX<sub>OUT</sub>) must **always** be connected to a decoupling capacitor, because of a DC level of 0.5V<sub>DD</sub> at this pin, which is present even when the device is not transmitting. This pin must also be **protected against overvoltage and negative transient signals**. The DC level of TX<sub>OUT</sub> can be used to bias a unipolar transient suppressor, as shown in the application diagram; see Fig.18.

Direct connection to the mains is done through an LC network for low-cost applications. However, a HF signal transformer could be used when power-line insulation has to be performed.

**CAUTION**

In transmission mode, the receiving part of the circuit is **not disabled** and the detection of the transmitted signal is normally performed. In this mode, the gain chosen before the beginning of the transmission is stored, and the **AGC is internally set to -6 dB** as long as  $\overline{\text{DATA}}_{\text{IN}}$  is LOW. Then, the old gain setting is **automatically restored**.

**Reception mode**

The input signal received by the modem is applied to a wide range input amplifier with AGC (-6 to +30 dB). This is basically for noise performance improvement and signal level adjustment, which ensures a maximum sensitivity of the ADC. An 8-bit conversion is then performed, followed by digital band-pass filtering, to meet the CISPR normalization and to comply with some additional limitations met in current applications.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL           | PARAMETER            | MIN. | MAX. | UNIT |
|------------------|----------------------|------|------|------|
| V <sub>DD</sub>  | supply voltage       | 4.5  | 5.5  | V    |
| f <sub>osc</sub> | oscillator frequency | –    | 12   | MHz  |
| T <sub>stg</sub> | storage temperature  | –50  | +150 | °C   |
| T <sub>amb</sub> | ambient temperature  | –10  | +80  | °C   |
| T <sub>j</sub>   | junction temperature | –    | 125  | °C   |

**HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

After digital demodulation, the baseband data signal is made available after pulse shaping.

The signal pin (RX<sub>IN</sub>) is a high-impedance input which has to be protected and DC decoupled for the same reasons as with pin TX<sub>OUT</sub>. The high sensitivity (82 dB $\mu$ V) of this input requires an efficient 50 Hz rejection filter (realized by the LC coupling network), which also acts as an anti-aliasing filter for the internal digital processing; see Fig.18.

**Data format****TRANSMISSION MODE**

The data input ( $\overline{\text{DATA}}_{\text{IN}}$ ) is active LOW: this means that a burst is generated on the line (pin TX<sub>OUT</sub>) when  $\overline{\text{DATA}}_{\text{IN}}$  pin is LOW.

Pin TX<sub>OUT</sub> is in a high-impedance state as long as the device is not transmitting. Successive logic 1s are treated in a Non-Return-to-Zero (NRZ) mode, see pulse shapes in Figs 8 and 9.

**RECEPTION MODE**

The data output (pin  $\overline{\text{DATA}}_{\text{OUT}}$ ) is active LOW; this means that the data output is LOW when a burst is received. Pin  $\overline{\text{DATA}}_{\text{OUT}}$  remains LOW as long as a burst is received.

**Power-down mode**

Power-down input (pin PD) is active HIGH; this means that the power consumption is minimum when pin PD is HIGH. Now, all functions are disabled, except clock generation.

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**CHARACTERISTICS**

$V_{DD} = V_{DDA} = 5\text{ V} \pm 5\%$ ;  $T_{amb} = 0\text{ to }70\text{ }^{\circ}\text{C}$ ;  $V_{DD}$  connected to  $V_{DDA}$ ; DGND connected to AGND.

| SYMBOL                                                                                                                                                   | PARAMETER                                           | CONDITIONS                                                                                                        | MIN.              | TYP.  | MAX.              | UNIT          |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-------------------|-------|-------------------|---------------|
| <b>Supply</b>                                                                                                                                            |                                                     |                                                                                                                   |                   |       |                   |               |
| $V_{DD}$                                                                                                                                                 | supply voltage                                      |                                                                                                                   | 4.75              | 5     | 5.25              | V             |
| $I_{DD(RX/TX)(tot)}$                                                                                                                                     | total analog + digital supply current               | $V_{DD} = 5\text{ V} \pm 5\%$<br>TX or RX mode                                                                    | –                 | 28    | 38                | mA            |
| $I_{DD(PD)(tot)}$                                                                                                                                        | total analog + digital supply current;              | $V_{DD} = 5\text{ V} \pm 5\%$ ;<br>PD = HIGH<br>Power-down mode                                                   | –                 | 19    | 25                | mA            |
| $I_{DD(PAMP)}$                                                                                                                                           | power amplifier supply current                      | $V_{DD} = 5\text{ V} \pm 5\%$ ;<br>$Z_L = 30\text{ }\Omega$ ;<br>$DATA_{IN} = \text{LOW}$<br>in transmission mode | –                 | 19    | 30                | mA            |
| $I_{DD(PAMP)(max)}$                                                                                                                                      | maximum power amplifier supply current              | $V_{DD} = 5\text{ V} \pm 5\%$ ;<br>$Z_L = 1\text{ }\Omega$ ;<br>$DATA_{IN} = \text{LOW}$<br>in transmission mode  | –                 | 76    | –                 | mA            |
| <b><math>DATA_{IN}</math> and PD inputs: <math>DATA_{OUT}</math> and <math>CLK_{OUT}</math> outputs</b>                                                  |                                                     |                                                                                                                   |                   |       |                   |               |
| $V_{IH}$                                                                                                                                                 | HIGH-level input voltage                            |                                                                                                                   | $0.2V_{DD} + 0.9$ | –     | $V_{DD} + 0.5$    | V             |
| $V_{IL}$                                                                                                                                                 | LOW-level input voltage                             |                                                                                                                   | –0.5              | –     | $0.2V_{DD} - 0.1$ | V             |
| $V_{OH}$                                                                                                                                                 | HIGH-level output voltage                           | $I_{OH} = -1.6\text{ mA}$                                                                                         | 2.4               | –     | –                 | V             |
| $V_{OL}$                                                                                                                                                 | LOW-level output voltage                            | $I_{OL} = 1.6\text{ mA}$                                                                                          | –                 | –     | 0.45              | V             |
| <b>OSC1 input and OSC2 output (OSC2 only used for driving external quartz crystal; must be left open-circuit when using an external clock generator)</b> |                                                     |                                                                                                                   |                   |       |                   |               |
| $V_{IH}$                                                                                                                                                 | HIGH-level input voltage                            |                                                                                                                   | $0.7V_{DD}$       | –     | $V_{DD} + 0.5$    | V             |
| $V_{IL}$                                                                                                                                                 | LOW-level input voltage                             |                                                                                                                   | –0.5              | –     | $0.2V_{DD} - 0.1$ | V             |
| $V_{OH}$                                                                                                                                                 | HIGH-level output voltage                           | $I_{OH} = -1.6\text{ mA}$                                                                                         | 2.4               | –     | –                 | V             |
| $V_{OL}$                                                                                                                                                 | LOW-level output voltage                            | $I_{OL} = 1.6\text{ mA}$                                                                                          | –                 | –     | 0.45              | V             |
| <b>Clock</b>                                                                                                                                             |                                                     |                                                                                                                   |                   |       |                   |               |
| $f_{osc}$                                                                                                                                                | oscillator frequency                                |                                                                                                                   | 6.080             | –     | 9.504             | MHz           |
| $\frac{f_{osc}}{f_{cr}}$                                                                                                                                 | ratio between oscillator and carrier frequency      |                                                                                                                   | –                 | 64    | –                 |               |
| $\frac{f_{osc}}{f_{CLKOUT}}$                                                                                                                             | ratio between oscillator and clock output frequency |                                                                                                                   | –                 | 2     | –                 |               |
| <b>Transmission mode</b>                                                                                                                                 |                                                     |                                                                                                                   |                   |       |                   |               |
| $f_{cr}$                                                                                                                                                 | carrier frequency                                   | $f_{osc} = 8.48\text{ MHz}$                                                                                       | –                 | 132.5 | –                 | kHz           |
| $t_{su}$                                                                                                                                                 | set-up time of the shaped burst                     | $f_{osc} = 8.48\text{ MHz}$ ;<br>see Fig.8                                                                        | –                 | 170   | –                 | $\mu\text{s}$ |
| $t_h$                                                                                                                                                    | hold time of the shaped burst                       | $f_{osc} = 8.48\text{ MHz}$ ;<br>see Fig.8                                                                        | –                 | 170   | –                 | $\mu\text{s}$ |

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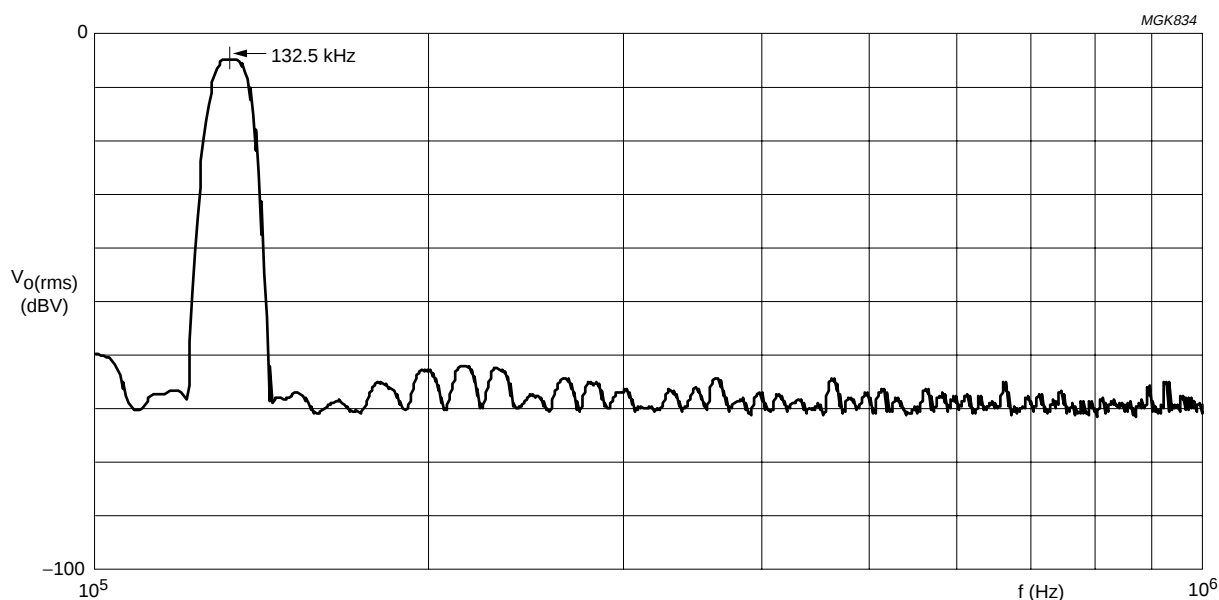
## TDA5051A

| SYMBOL                | PARAMETER                                                                                                             | CONDITIONS                                                                                                                                                          | MIN. | TYP. | MAX. | UNIT                   |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------------------------|
| $t_{W(DI)(min)}$      | minimum pulse width of $DATA_{IN}$ signal                                                                             | $f_{OSC} = 8.48 \text{ MHz}$ ;<br>see Fig.8                                                                                                                         | –    | 190  | –    | $\mu\text{s}$          |
| $V_{O(rms)}$          | output carrier signal<br>(RMS value)                                                                                  | $Z_L = \text{CISPR16}$ ;<br>$DATA_{IN} = \text{LOW}$                                                                                                                | 120  | –    | 122  | $\text{dB}\mu\text{V}$ |
| $I_{O(max)}$          | power amplifier maximum<br>output current (peak value)                                                                | $Z_L = 1 \Omega$ ;<br>$DATA_{IN} = \text{LOW}$                                                                                                                      | –    | 160  | –    | $\text{mA}$            |
| $Z_O$                 | output impedance of the<br>power amplifier                                                                            |                                                                                                                                                                     | –    | 5    | –    | $\Omega$               |
| $V_O$                 | output DC level at<br>pin $TX_{OUT}$                                                                                  |                                                                                                                                                                     | –    | 2.5  | –    | $\text{V}$             |
| THD                   | total harmonic distortion on<br>CISPR16 load with the<br>coupling network<br>(measured on the first ten<br>harmonics) | $V_{O(rms)} = 121 \text{ dB}\mu\text{V}$ on<br>CISPR16 load;<br>$f_{OSC} = 8.48 \text{ MHz}$ ;<br>$DATA_{IN} = \text{LOW}$<br>(no modulation);<br>see Figs 3 and 16 | –    | –55  | –    | $\text{dB}$            |
| $B_{-20\text{dB}}$    | bandwidth of the shaped<br>output signal (at –20 dB)<br>on CISPR16 load with the<br>coupling network                  | $V_{O(rms)} = 121 \text{ dB}\mu\text{V}$ on<br>CISPR16 load;<br>$f_{OSC} = 8.48 \text{ MHz}$ ;<br>$DATA_{IN} = 300 \text{ Hz}$ ;<br>duty factor = 50%;<br>see Fig.4 | –    | 3000 | –    | $\text{Hz}$            |
| <b>Reception mode</b> |                                                                                                                       |                                                                                                                                                                     |      |      |      |                        |
| $V_{i(rms)}$          | analog input signal<br>(RMS value)                                                                                    |                                                                                                                                                                     | 82   | –    | 122  | $\text{dB}\mu\text{V}$ |
| $V_I$                 | DC level at pin $RX_{IN}$                                                                                             |                                                                                                                                                                     | –    | 2.5  | –    | $\text{V}$             |
| $Z_i$                 | $RX_{IN}$ input impedance                                                                                             |                                                                                                                                                                     | –    | 50   | –    | $\text{k}\Omega$       |
| $R_{AGC}$             | AGC range                                                                                                             |                                                                                                                                                                     | –    | 36   | –    | $\text{dB}$            |
| $t_{c(AGC)}$          | AGC time constant                                                                                                     | $f_{OSC} = 8.48 \text{ MHz}$ ;<br>see Fig.5                                                                                                                         | –    | 296  | –    | $\mu\text{s}$          |
| $t_{d(dem)(su)}$      | demodulation delay set-up<br>time                                                                                     | $f_{OSC} = 8.48 \text{ MHz}$ ;<br>see Fig.15                                                                                                                        | –    | 350  | 400  | $\mu\text{s}$          |
| $t_{d(dem)(h)}$       | demodulation delay hold<br>time                                                                                       | $f_{OSC} = 8.48 \text{ MHz}$ ;<br>see Fig.15                                                                                                                        | –    | 420  | 470  | $\mu\text{s}$          |
| $B_{det}$             | detection bandwidth                                                                                                   | $f_{OSC} = 8.48 \text{ MHz}$                                                                                                                                        | –    | 3    | –    | $\text{kHz}$           |
| BER                   | bit error rate                                                                                                        | $f_{OSC} = 8.48 \text{ MHz}$ ;<br>600 baud; S/N = 35 dB;<br>signal 76 $\text{dB}\mu\text{V}$ ;<br>see Fig.17                                                        | –    | 1    | –    | $1 \times 10^{-4}$     |

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| SYMBOL                   | PARAMETER                                                              | CONDITIONS                                                                                                                                               | MIN. | TYP. | MAX. | UNIT          |
|--------------------------|------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| <b>Power-up timing</b>   |                                                                        |                                                                                                                                                          |      |      |      |               |
| $t_{d(pu)(TX)}$          | delay between power-up and $DATA_{IN}$ in transmission mode            | XTAL = 8.48 MHz;<br>C1 = C2 = 27 pF;<br>$R_p = 2.2\text{ M}\Omega$ ; see Fig.10                                                                          | –    | 1    | –    | $\mu\text{s}$ |
| $t_{d(pu)(RX)}$          | delay between power-up and $DATA_{OUT}$ in reception mode              | XTAL = 8.48 MHz;<br>C1 = C2 = 27 pF;<br>$R_p = 2.2\text{ M}\Omega$ ;<br>$f_{RXIN} = 132.5\text{ kHz}$ ;<br>120 dB $\mu\text{V}$ sine wave;<br>see Fig.11 | –    | 1    | –    | $\mu\text{s}$ |
| <b>Power-down timing</b> |                                                                        |                                                                                                                                                          |      |      |      |               |
| $t_{d(pd)(TX)}$          | delay between PD = 0 and $DATA_{IN}$ in transmission mode              | $f_{OSC} = 8.48\text{ MHz}$ ;<br>see Fig.12                                                                                                              | –    | 10   | –    | $\mu\text{s}$ |
| $t_{d(pd)(RX)}$          | delay between PD = 0 and $DATA_{OUT}$ in reception mode                | $f_{OSC} = 8.48\text{ MHz}$ ;<br>$f_{RXIN} = 132.5\text{ kHz}$ ;<br>120 dB $\mu\text{V}$ sine wave;<br>see Fig.13                                        | –    | 500  | –    | $\mu\text{s}$ |
| $t_{active(min)}$        | minimum active time with T = 10 ms power-down period in reception mode | $f_{OSC} = 8.48\text{ MHz}$ ;<br>$f_{RXIN} = 132.5\text{ kHz}$ ;<br>120 dB $\mu\text{V}$ sine wave;<br>see Fig.14                                        | –    | 1    | –    | $\mu\text{s}$ |



Resolution bandwidth = 9 kHz; top: 0 dBV (RMS) = 120 dB $\mu\text{V}$  (RMS); marker at –5 dBV (RMS) = 115 dB $\mu\text{V}$  (RMS); the CISPR16 network provides an attenuation of 6 dB, so the signal amplitude is 121 dB $\mu\text{V}$  (RMS).

Fig.3 Carrier spectrum.

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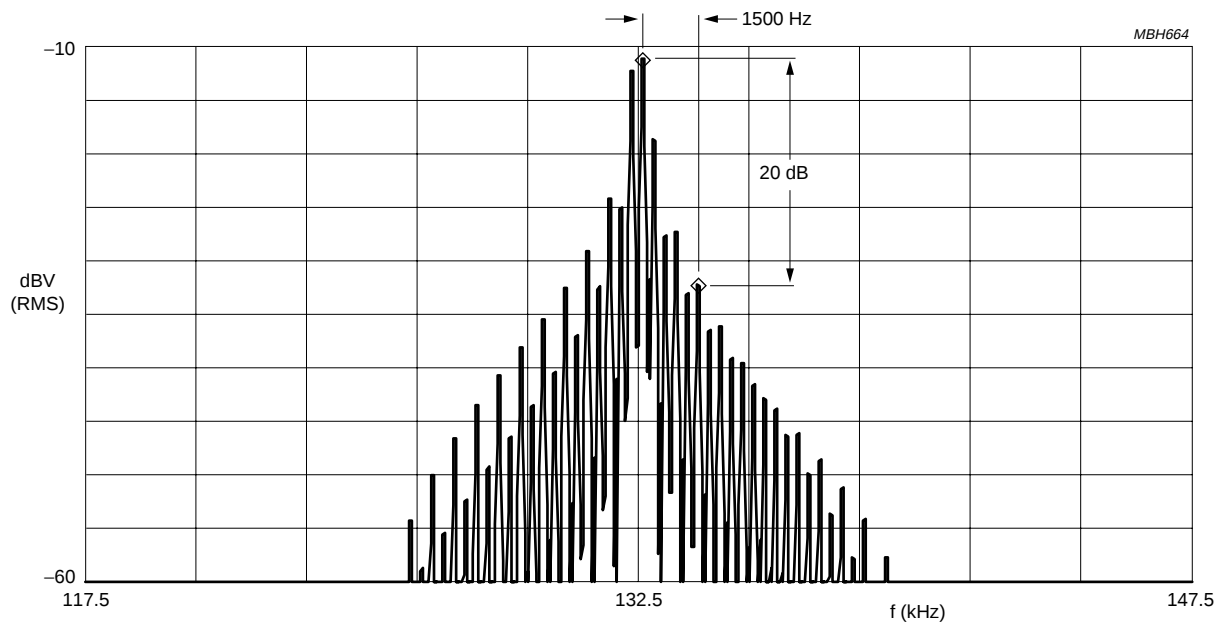
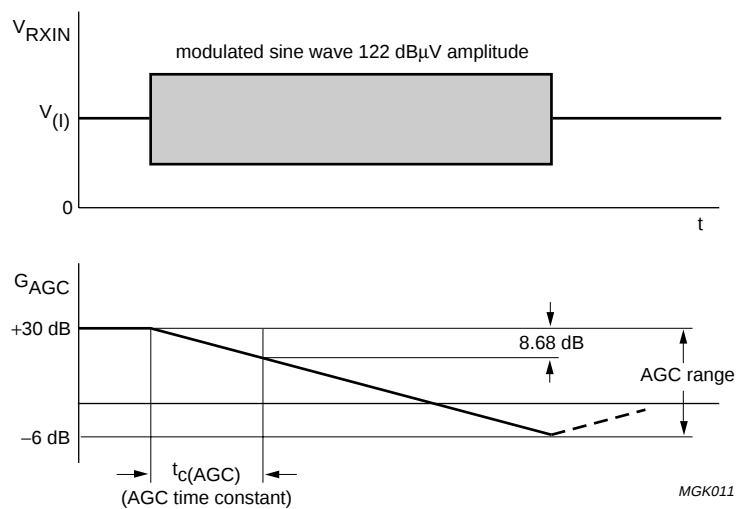


Fig.4 Shaped signal spectrum.

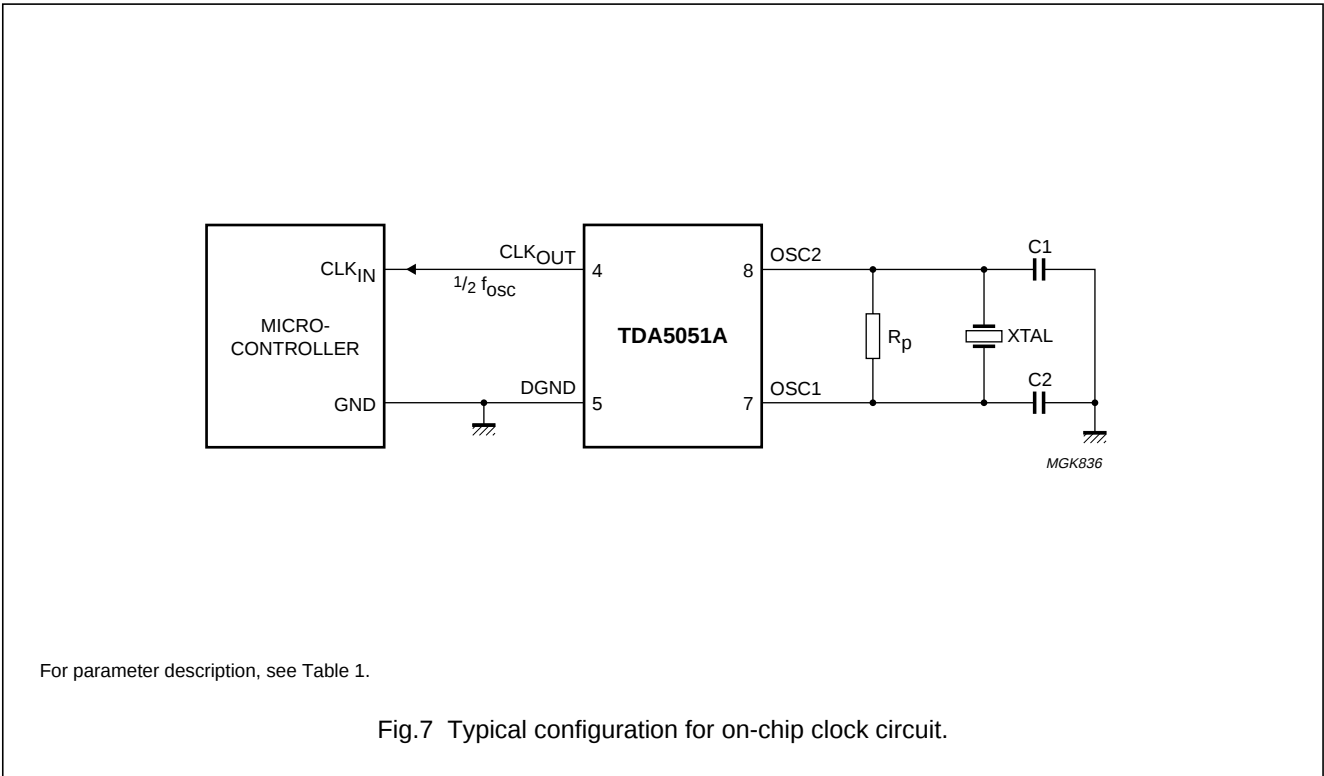
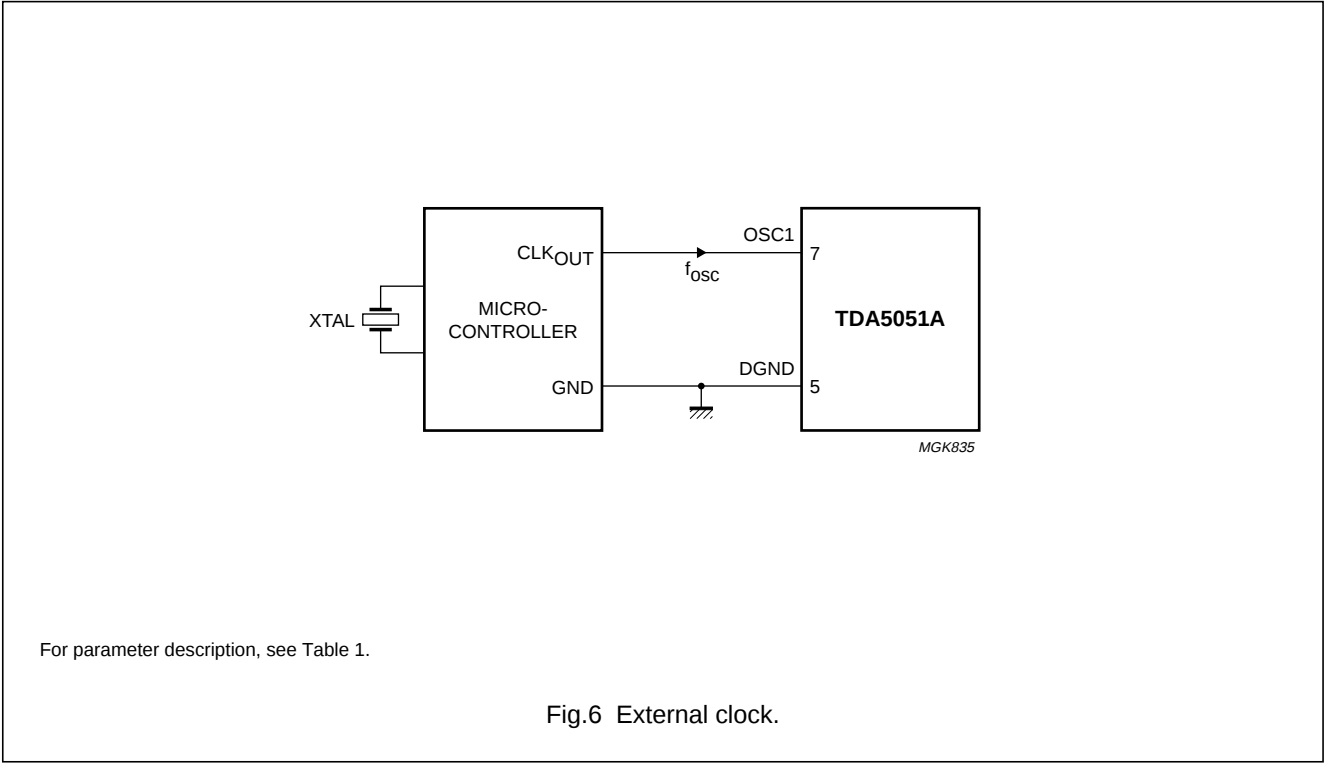


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TIMING

Configuration for clock



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**Table 1** Clock oscillator parameters

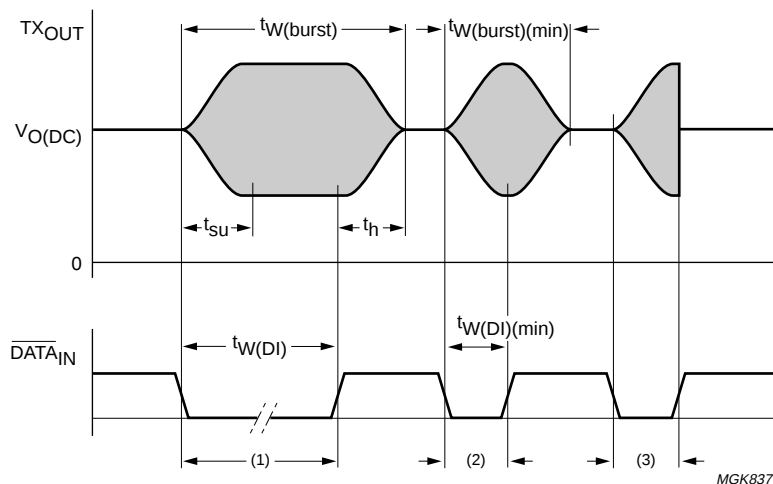
| OSCILLATOR<br>FREQUENCY<br>$f_{osc}$ | CARRIER FREQUENCY<br>$f_{cr}$ | CLOCK OUTPUT<br>FREQUENCY<br>$\frac{1}{2}f_{osc}$ | EXTERNAL COMPONENTS                                                                         |
|--------------------------------------|-------------------------------|---------------------------------------------------|---------------------------------------------------------------------------------------------|
| 6.080 to 9.504 MHz                   | 95 to 148.5 kHz               | 3.040 to 4.752 MHz                                | C1 = C2 = 27 to 47 pF;<br>R <sub>p</sub> = 2.2 to 4.7 MΩ;<br>XTAL = standard quartz crystal |

**Table 2** Calculation of parameters depending on the clock frequency

| SYMBOL              | PARAMETER                                            | CONDITIONS                                                                                                             | UNIT |
|---------------------|------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|------|
| $f_{osc}$           | oscillator frequency                                 | with on-chip oscillator: frequency of the crystal quartz; with external clock: frequency of the signal applied at OSC1 | Hz   |
| $f_{CLKOUT}$        | clock output frequency                               | $\frac{1}{2}f_{osc}$                                                                                                   | Hz   |
| $f_{cr}$            | carrier frequency/digital filter tuning frequency    | $\frac{1}{64}f_{osc}$                                                                                                  | Hz   |
| $t_{su}$            | set-up time of the shaped burst                      | $\frac{23}{f_{cr}}$ or $\frac{1472}{f_{osc}}$                                                                          | s    |
| $t_h$               | hold time of the shaped burst                        | $\frac{23}{f_{cr}}$ or $\frac{1472}{f_{osc}}$                                                                          | s    |
| $t_{W(DI)(min)}$    | minimum pulse width of $\overline{DATA_{IN}}$ signal | $t_{su} + \frac{1}{f_{cr}}$                                                                                            | s    |
| $t_{W(burst)(min)}$ | minimum burst time of $V_{O(DC)}$ signal             | $t_{W(DI)(min)} + t_h$                                                                                                 | s    |
| $t_{c(AGC)}$        | AGC time constant                                    | $\frac{2514}{f_{osc}}$                                                                                                 | s    |
| $t_{su(demod)}$     | demodulation set-up time                             | $\frac{3200}{f_{osc}}$ ( $\approx$ max.)                                                                               | s    |
| $t_{h(demod)}$      | demodulation hold time                               | $\frac{3800}{f_{osc}}$ ( $\approx$ max.)                                                                               | s    |

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- (1)  $t_{W(DI)} > t_{W(DI)(min)}$ .
- (2)  $t_{W(DI)(min)} = t_{su} + \frac{1}{f_{cr}}$
- (3)  $t_{W(DI)(min)} < t_{su}$ ; wrong operation.

Fig.8 Relationship between  $\overline{\text{DATA}}_{\text{IN}}$  and  $\text{TX}_{\text{OUT}}$  (see Table 3).

**Table 3** Relationship between  $\overline{\text{DATA}}_{\text{IN}}$  and  $\text{TX}_{\text{OUT}}$

| PD | $\overline{\text{DATA}}_{\text{IN}}$ | TX <sub>OUT</sub>                      |
|----|--------------------------------------|----------------------------------------|
| 1  | X <sup>(1)</sup>                     | high-impedance                         |
| 0  | 1                                    | high-impedance (after t <sub>h</sub> ) |
| 0  | 0                                    | active with DC offset                  |

### Note

1.  $X = \text{don't care.}$

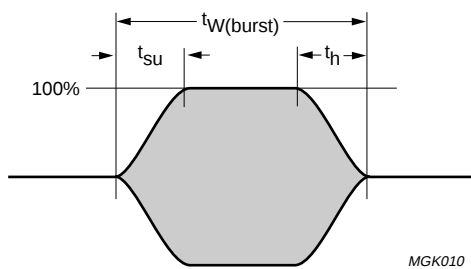
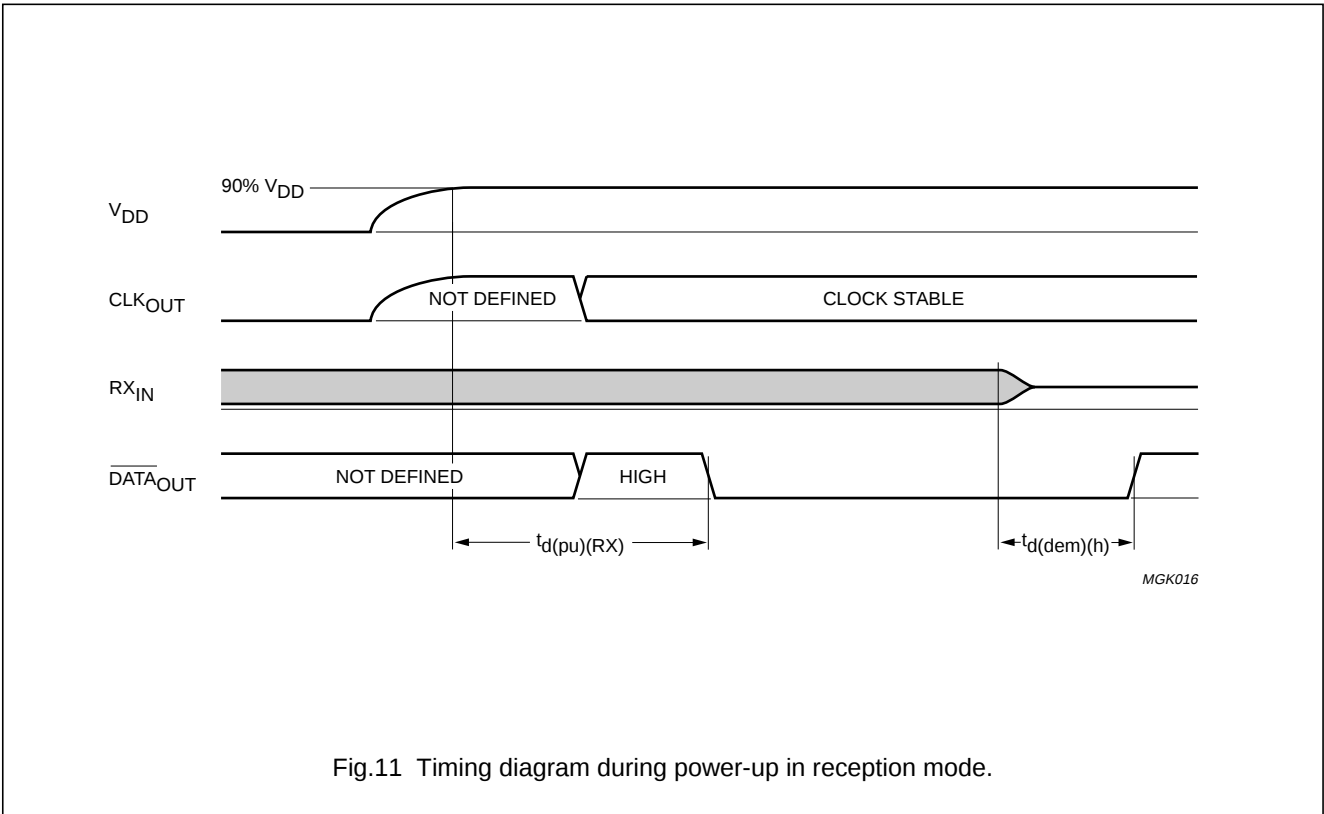
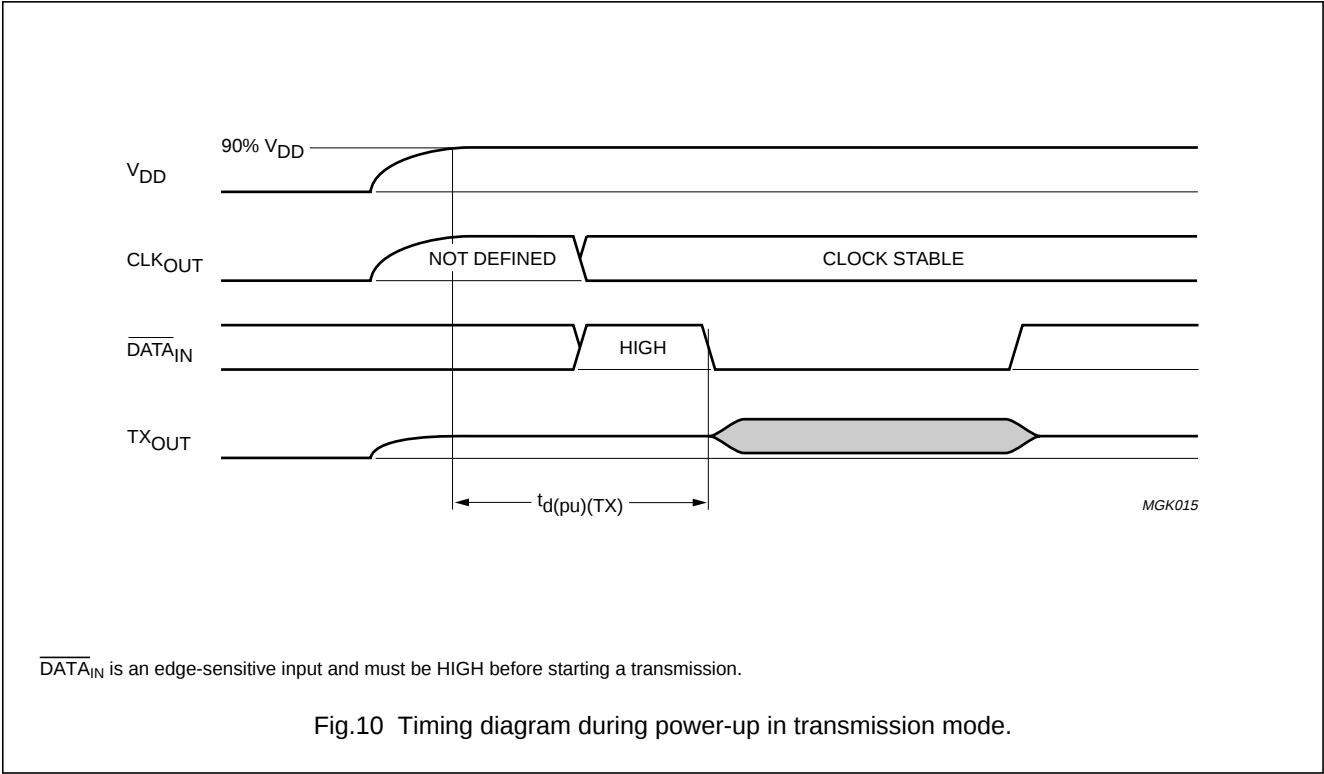


Fig.9 Pulse shape characteristics.

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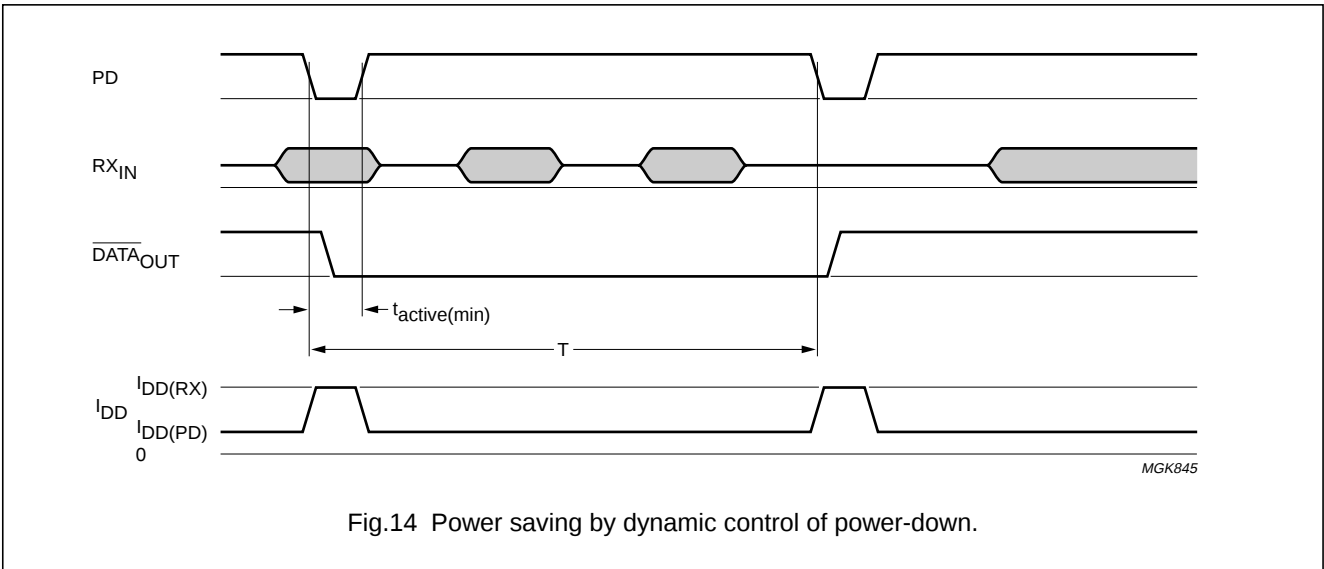
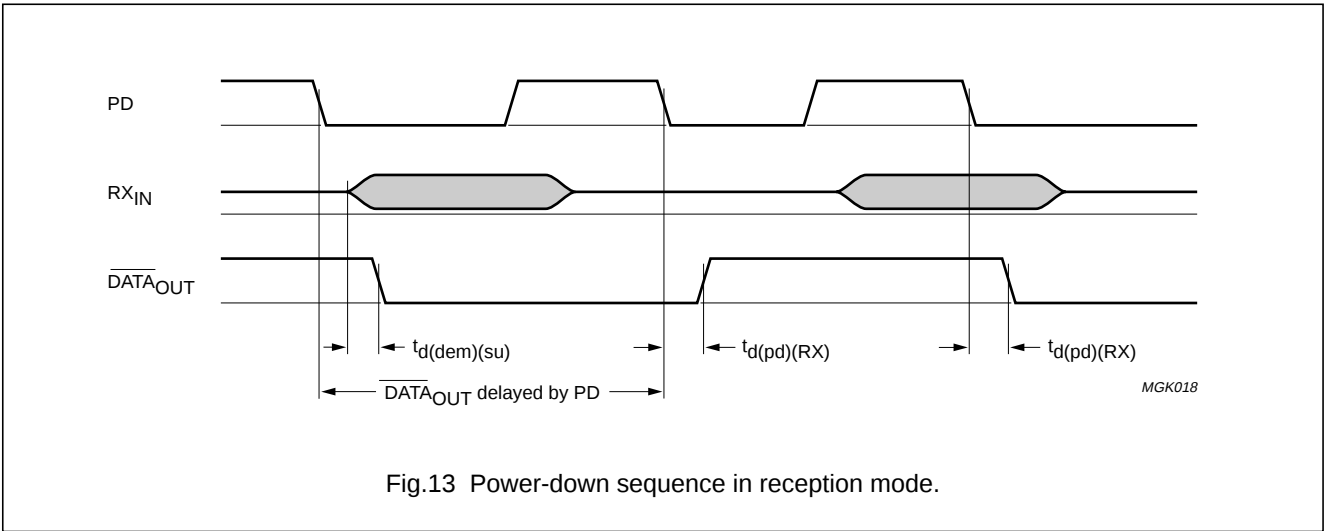
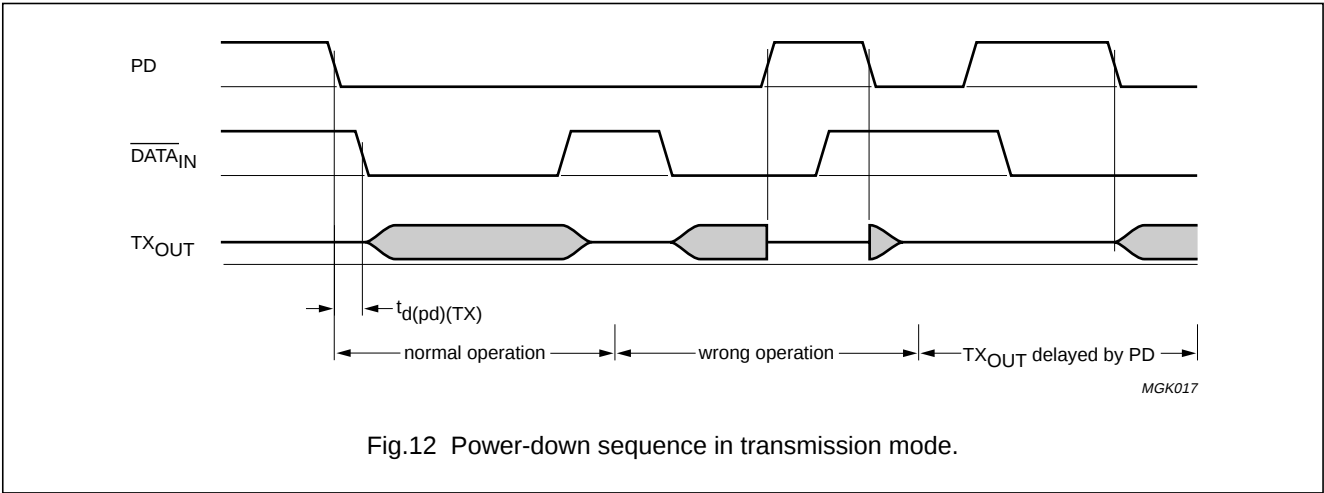
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Timing diagrams



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## TEST INFORMATION

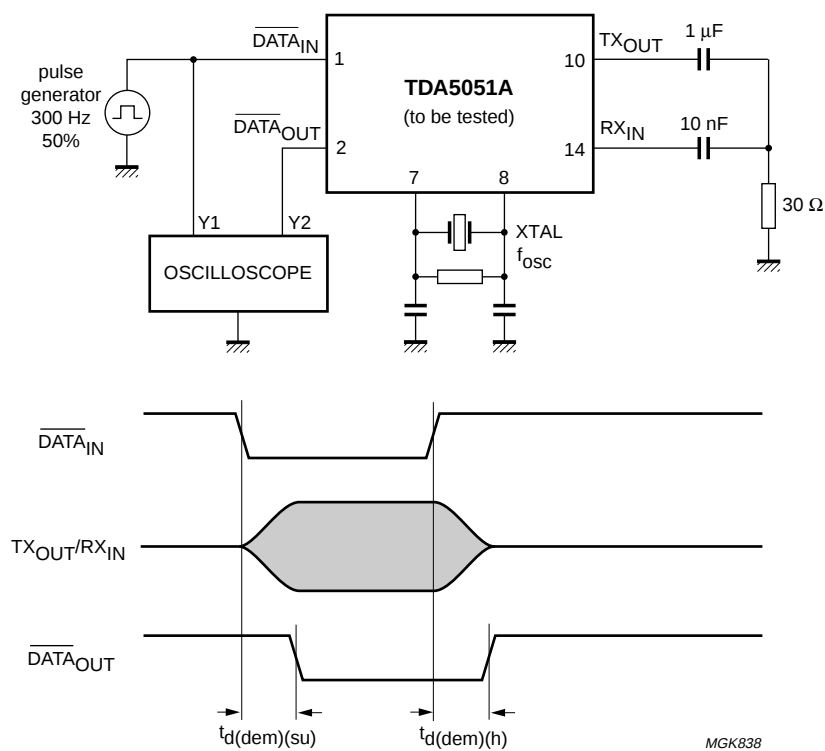
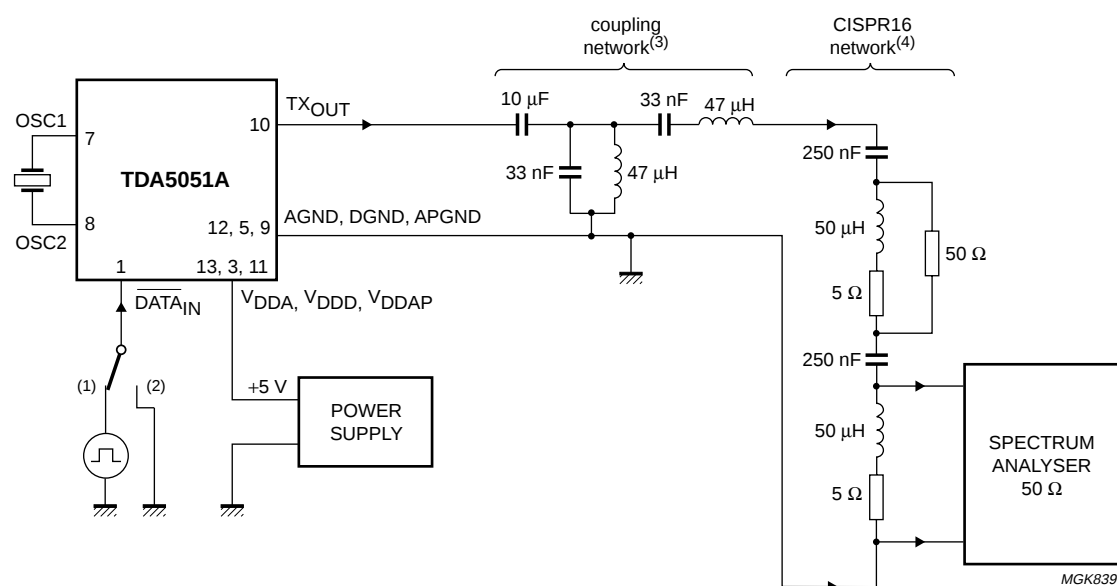


Fig.15 Test set-up for measuring demodulation delay.

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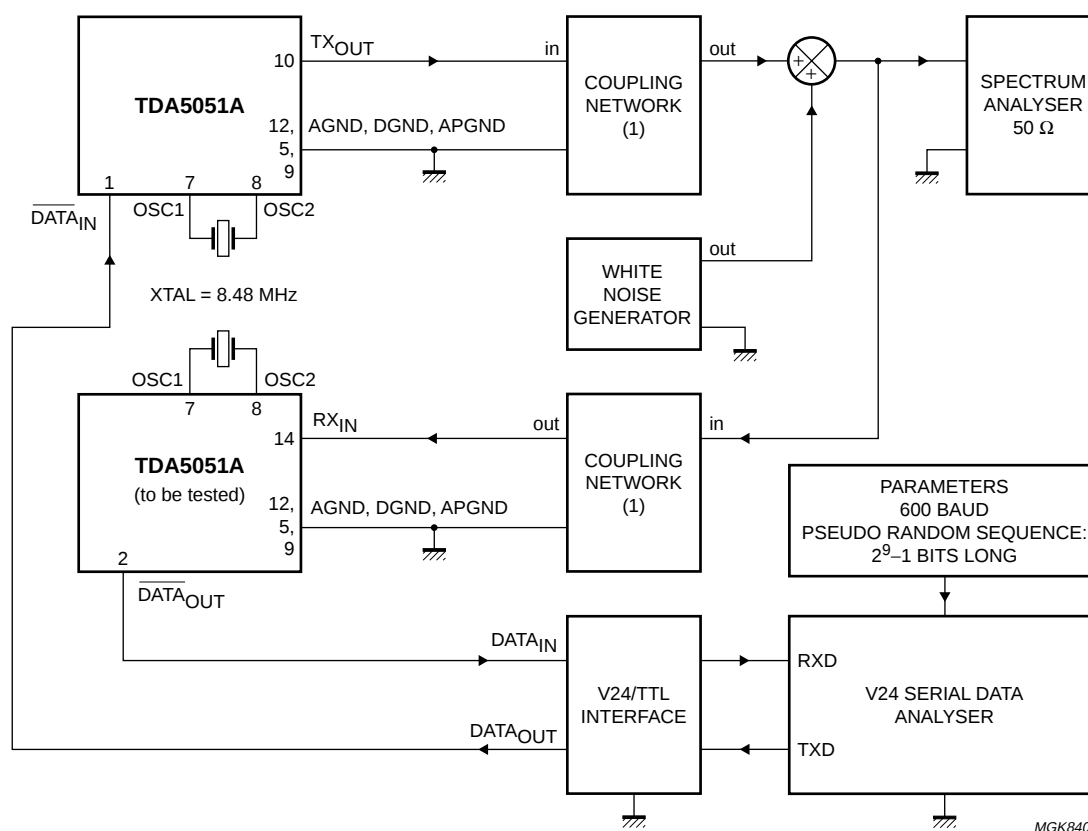


- (1) Square wave TTL signal 300 Hz, duty factor = 50% for measuring signal bandwidth (see spectrum Fig.3).
- (2)  $\overline{\text{DATA}}_{\text{IN}}$  = LOW for measuring total harmonic distortion (see spectrum Fig.3).
- (3) Tuned for  $f_{\text{cr}} = 132.5$  kHz.
- (4) The CISPR16 network provides a -6 dB attenuation.

Fig.16 Test set-up for measuring THD and bandwidth of the TX<sub>OUT</sub> signal.

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(1) See Fig.16.

Fig.17 Test set-up for measuring Bit Error Rate (BER).

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## APPLICATION INFORMATION

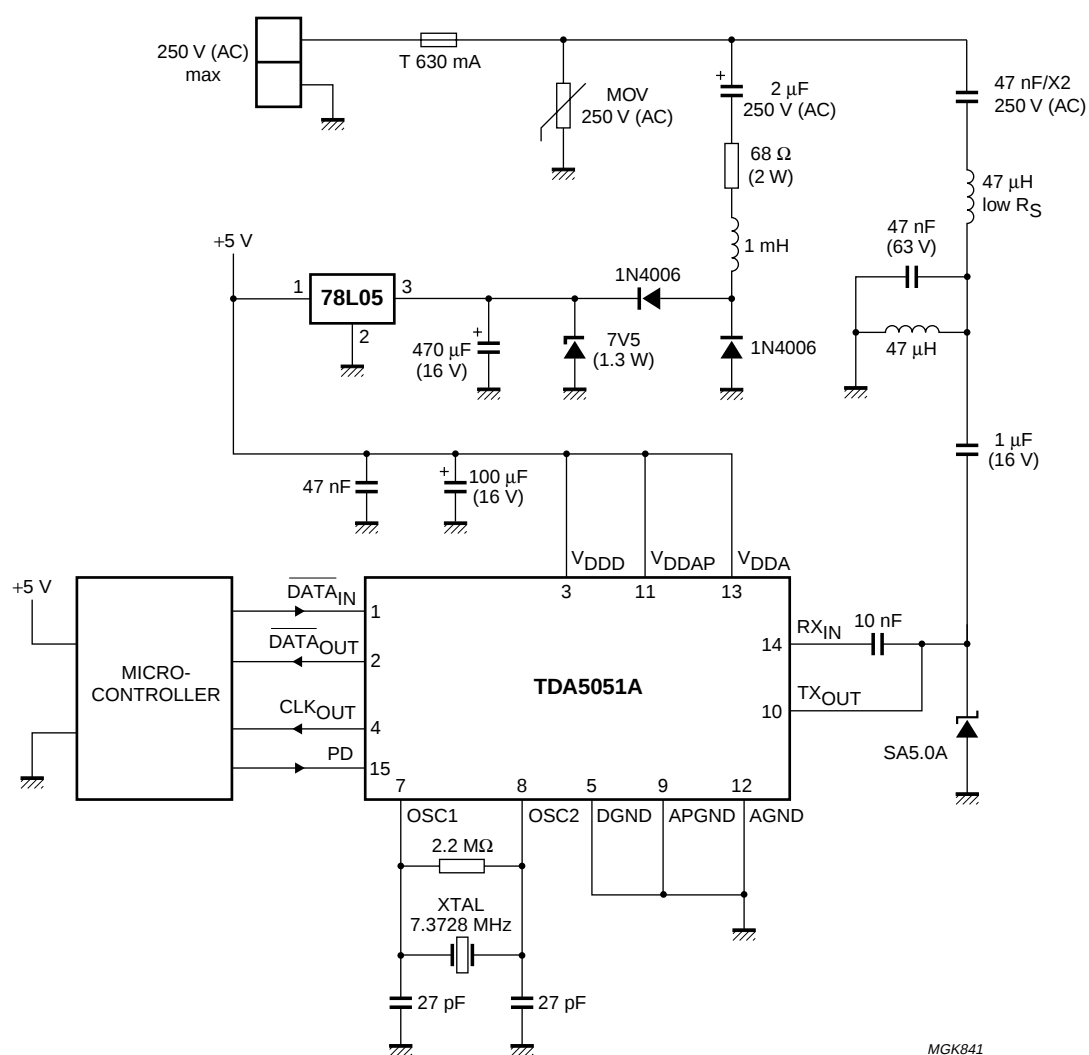
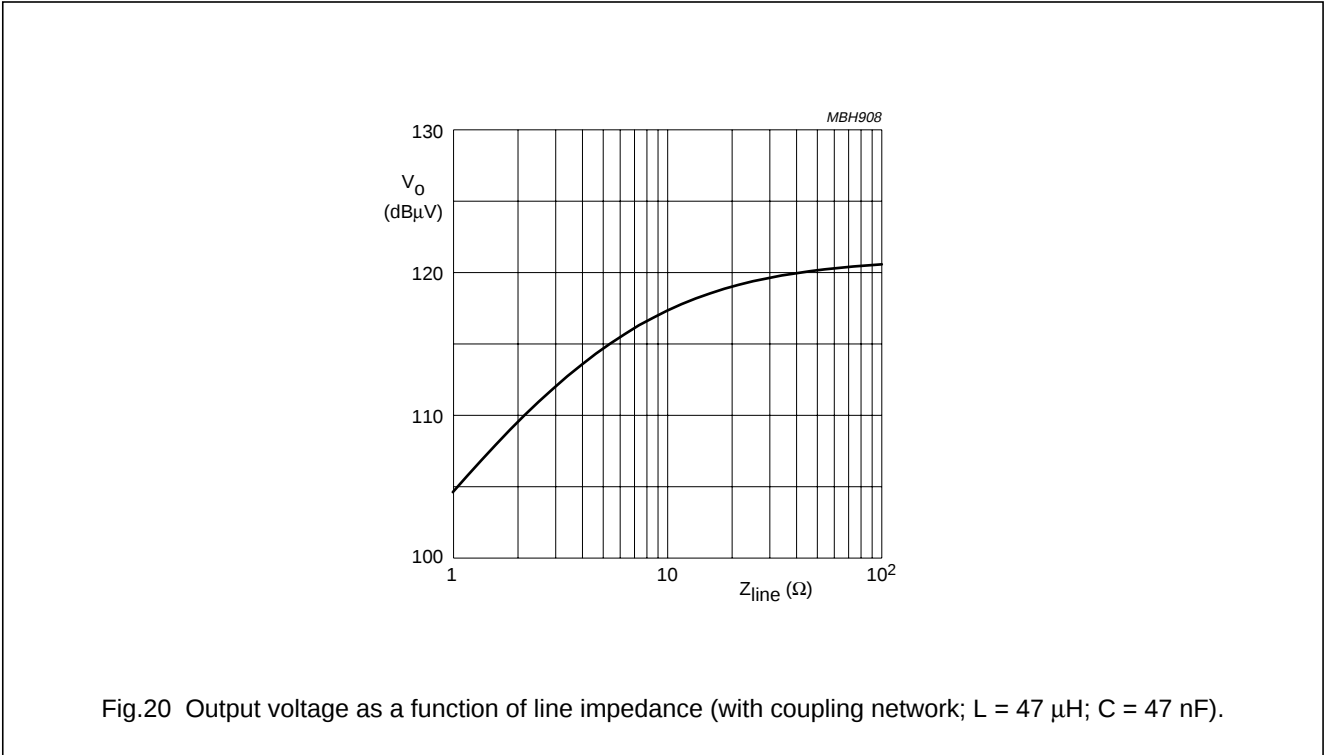
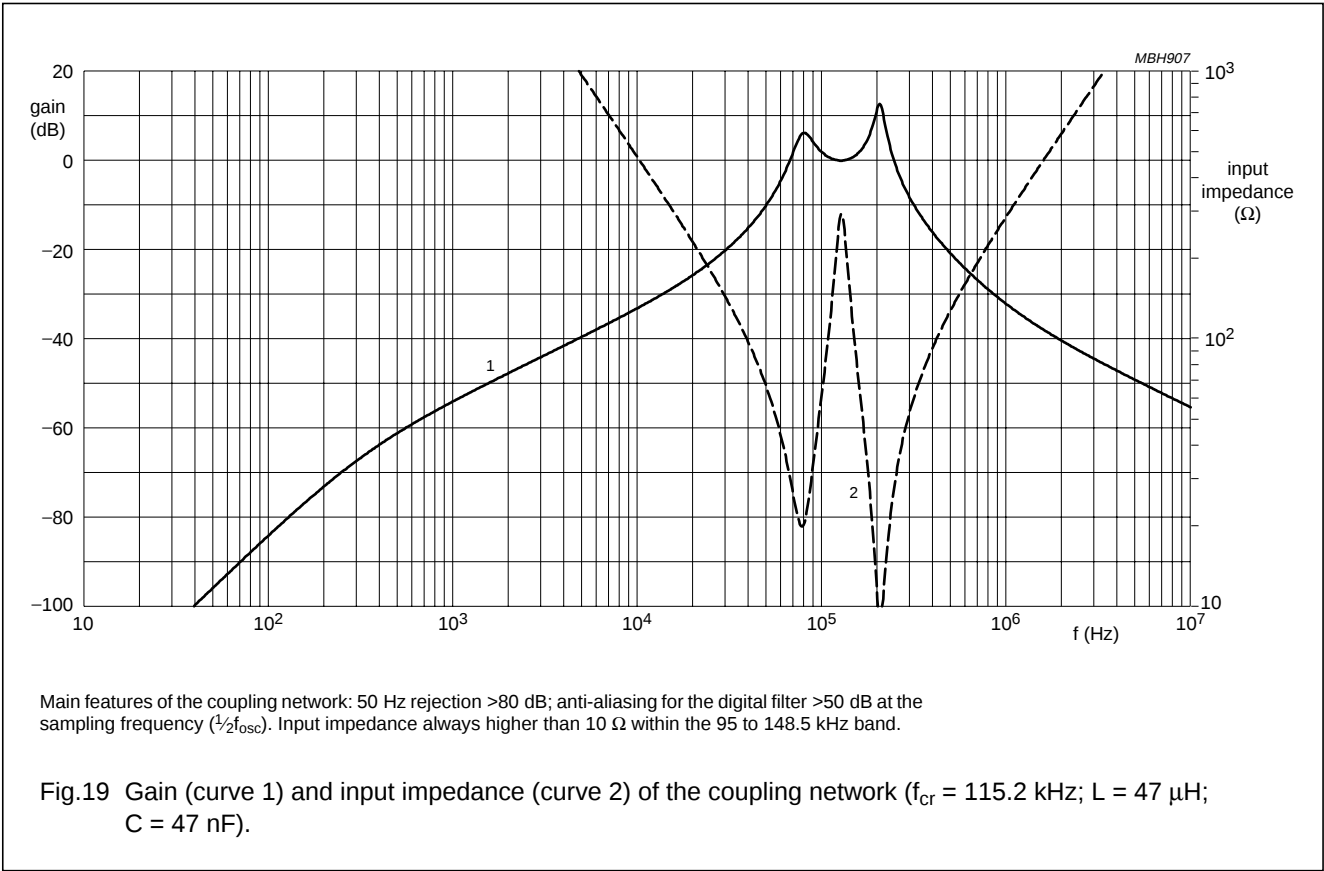

$$f_{cr} = 115.2 \text{ kHz for a XTAL} = 7.3728 \text{ MHz standard crystal.}$$

Fig.18 Application diagram without power line insulation.

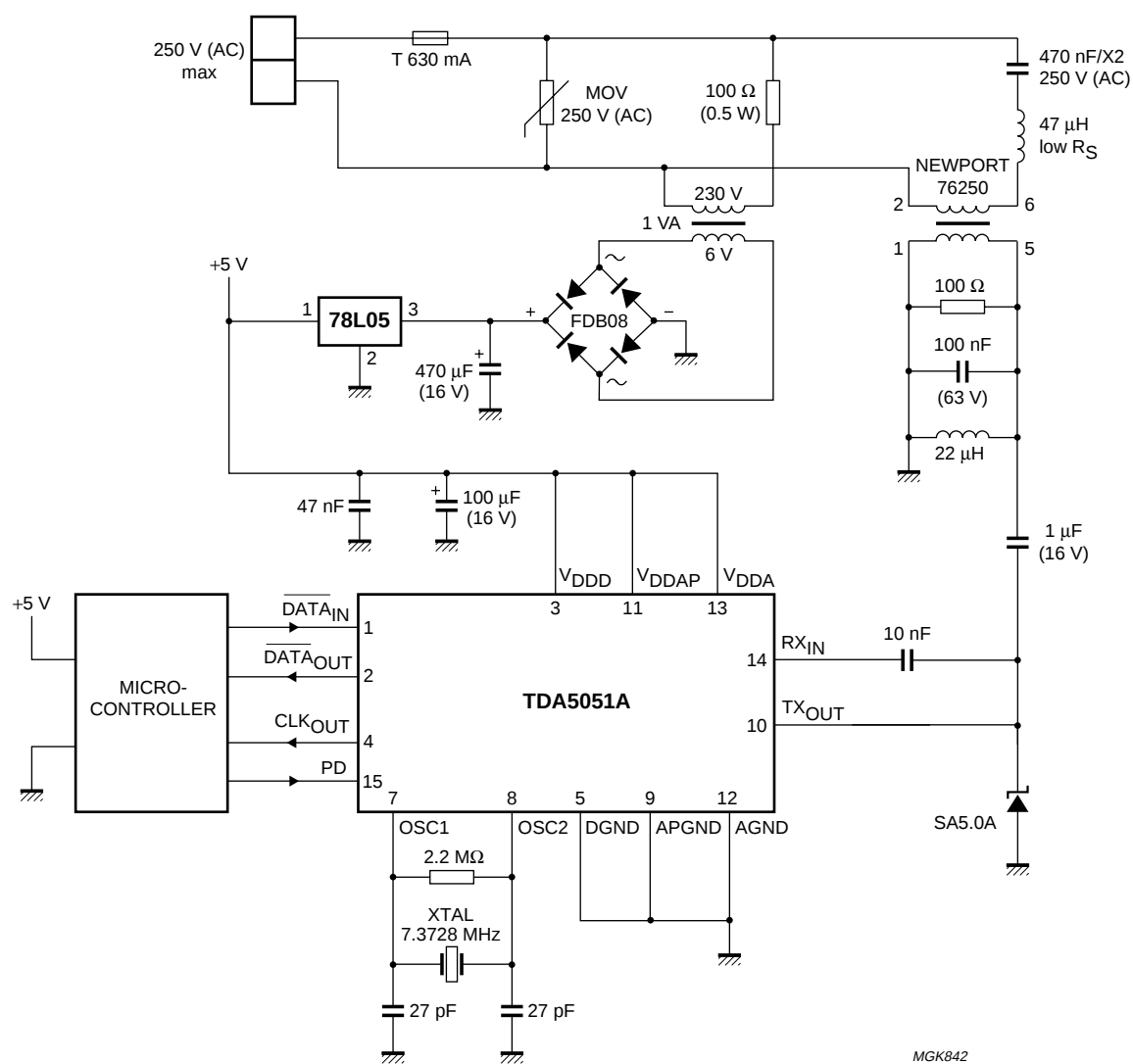
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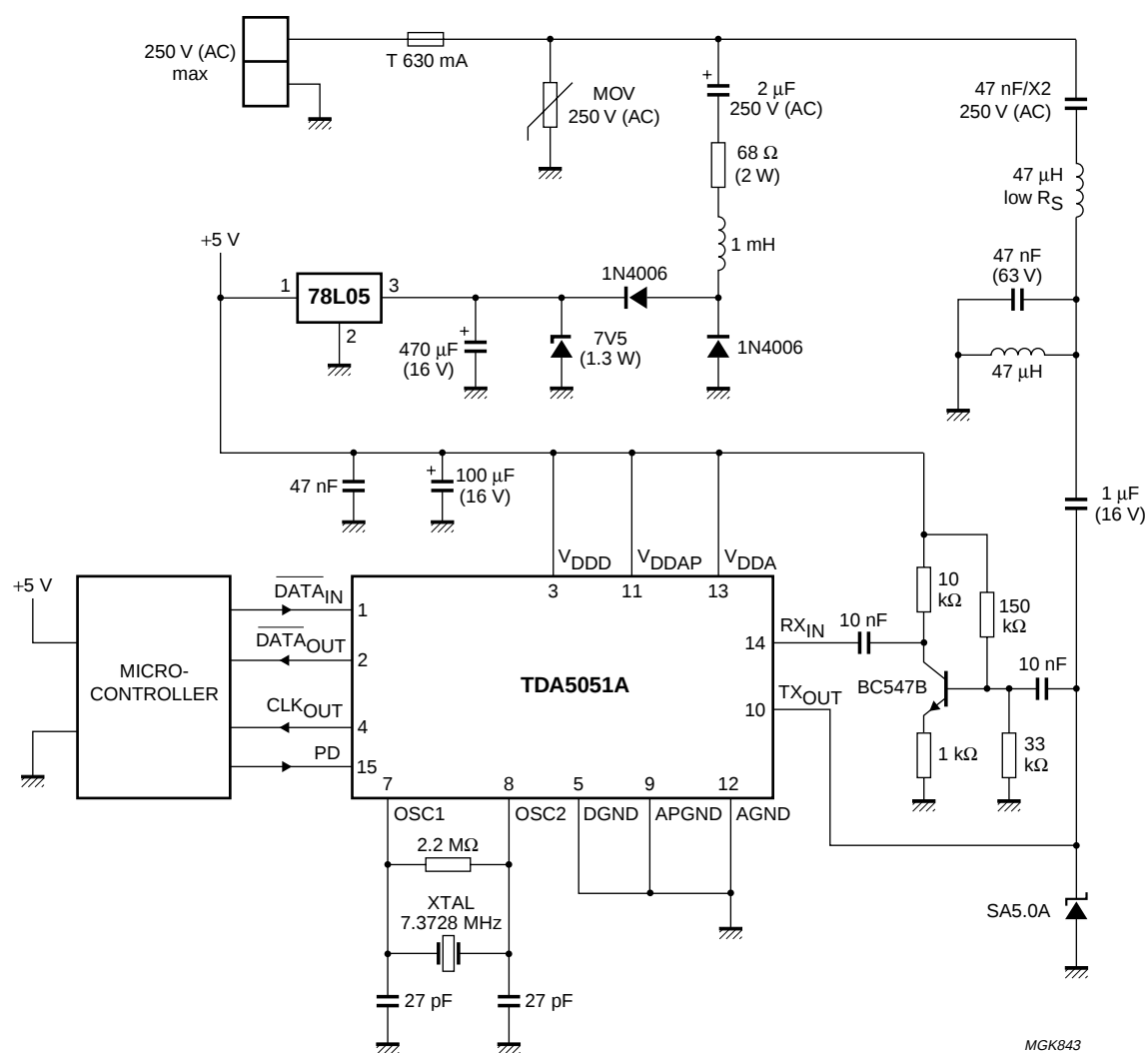


$f_{cr} = 115.2$  kHz for a XTAL = 7.3728 MHz standard crystal.

Fig.21 Application diagram with power line insulation.

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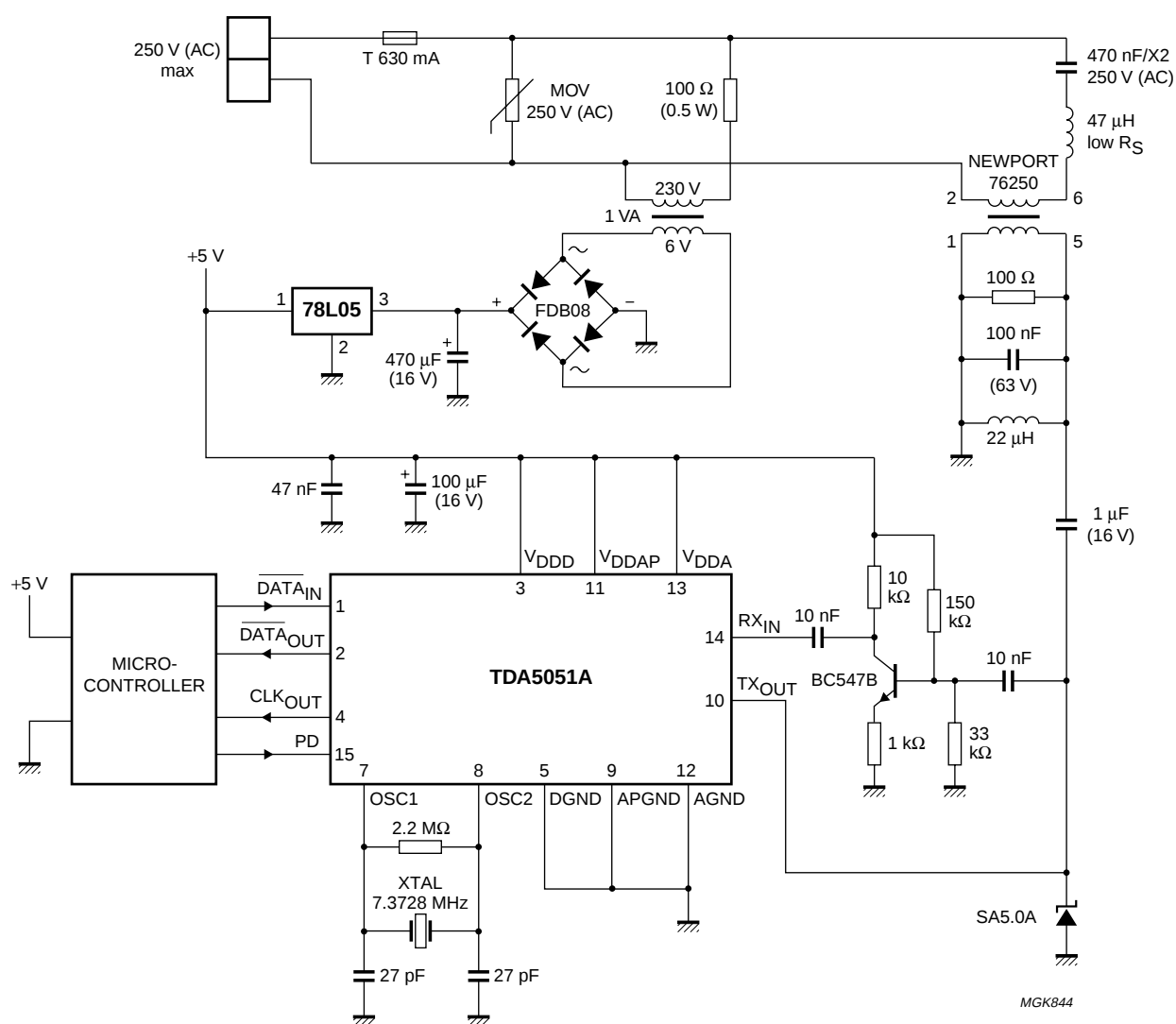


$f_{cr} = 115.2 \text{ kHz}$  for a XTAL = 7.3728 MHz standard crystal.

Fig.22 Application diagram without power line insulation, with improved sensitivity (68 dBµV typ.).

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$f_{cr} = 115.2$  kHz for a XTAL = 7.3728 MHz standard crystal.

Fig.23 Application diagram with power line insulation, with improved sensitivity (68 dB $\mu$ V typ.).

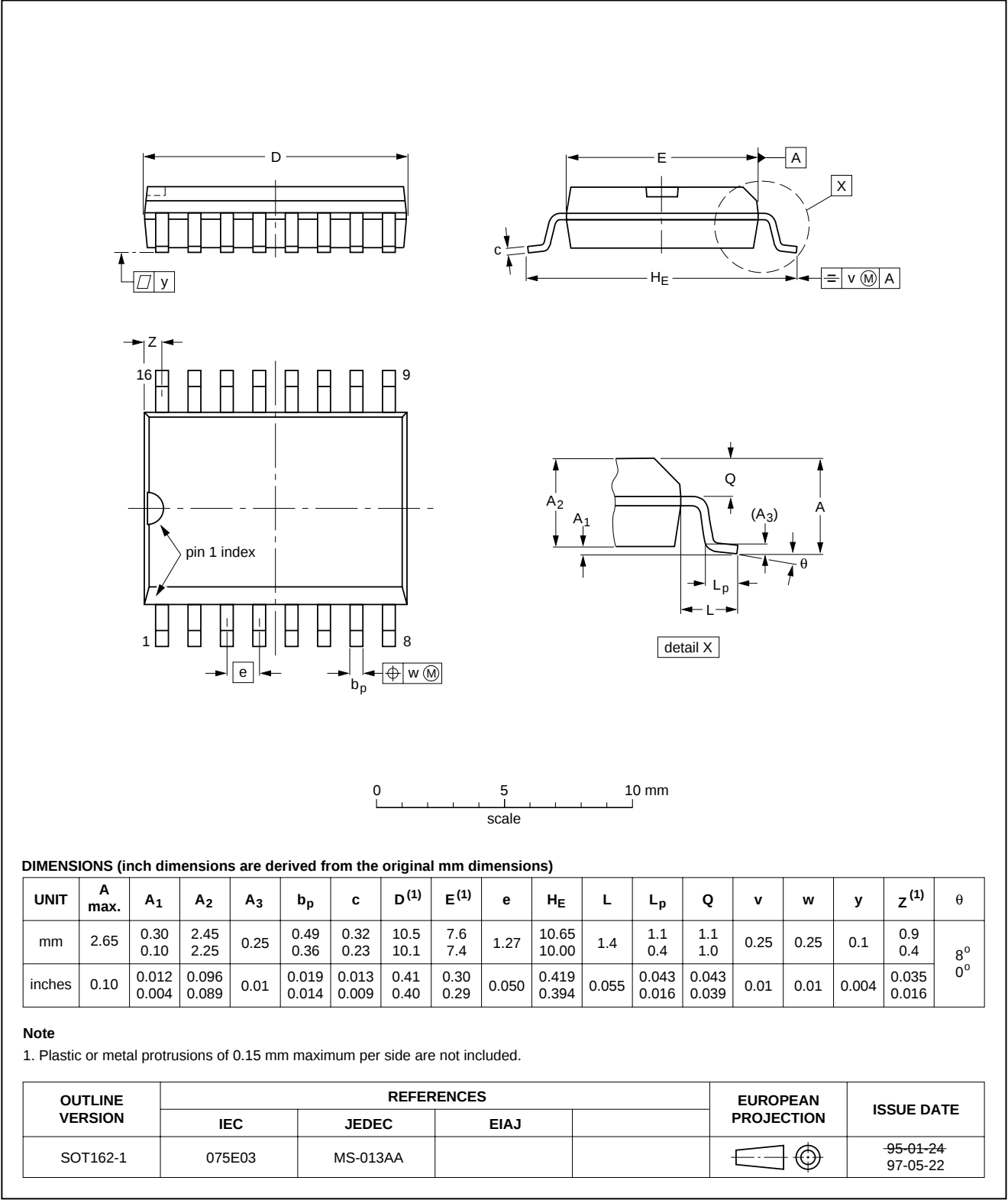
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PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



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**SOLDERING****Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

**Reflow soldering**

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

**Wave soldering**

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**Manual soldering**

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE                         | SOLDERING METHOD                  |                       |
|---------------------------------|-----------------------------------|-----------------------|
|                                 | WAVE                              | REFLOW <sup>(1)</sup> |
| BGA, SQFP                       | not suitable                      | suitable              |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable <sup>(2)</sup>       | suitable              |
| PLCC <sup>(3)</sup> , SO, SOJ   | suitable                          | suitable              |
| LQFP, QFP, TQFP                 | not recommended <sup>(3)(4)</sup> | suitable              |
| SSOP, TSSOP, VSO                | not recommended <sup>(5)</sup>    | suitable              |

## Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “*Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*”.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

| Data sheet status                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                       |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification                                                                                                                                                                                                                                                                                                                                                                                                                                   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification                                                                                                                                                                                                                                                                                                                                                                                                                                 | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification                                                                                                                                                                                                                                                                                                                                                                                                                                     | This data sheet contains final product specifications.                                |
| Limiting values                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                       |
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| Application information                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                                                                       |
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**NOTES**

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