8.7 AC CHARACTERISTICS

8.7.1 Parallel Interface Characteristics (8080-series MPU)

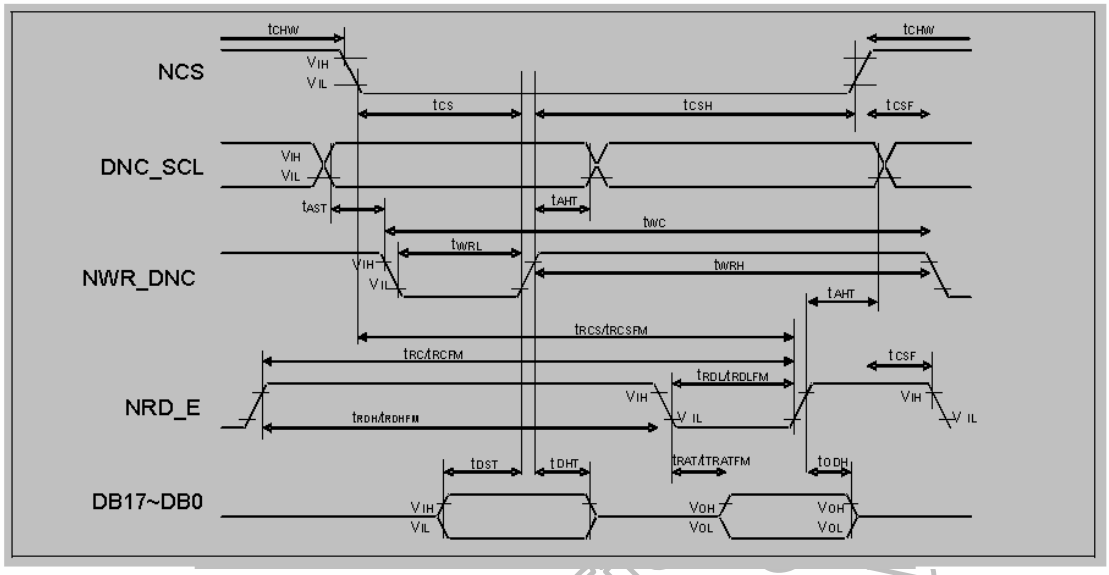
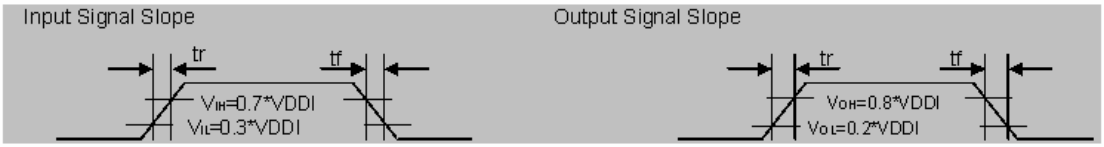


Figure 8. 1 Parallel Interface Characteristics (8080-series MPU)

(VSSA=0V, VCC=1.65V to 2.50V, VCI=2.3V to 2.9V,Ta = -30 to 70° C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
NCS	t_{CHW} t_{CS} t_{RCS} t_{RCSFM} t_{CSF} t_{CSH}	Chip select "H" pulse width Chip select setup time (Write) Chip select setup time (Read ID) Chip select setup time (Read FM) Chip select wait time (Write/Read) Chip select hold time	0 35 45 355 10 10	- - - - - -	ns	-
NWR_RNW	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse "H" duration Control pulse "L" duration	10 35 35	- - -	ns	-
NRD_E (ID)	t_{RC} t_{RDH} t_{RDL}	Read cycle (ID) Control pulse "H" duration (ID) Control pulse "L" duration (ID)	160 90 45	- - -	ns	When read ID data
NRD_E (FM)	t_{RCFM} t_{RDHFM} t_{RDLFM}	Read cycle (FM) Control pulse "H" duration (FM) Control pulse "L" duration (FM)	450 90 355	- - -	ns	When read from frame memory
D15 to D0	t_{DST} t_{DHT} t_{RAT} t_{RATFM} t_{ODH}	Data setup time Data hold time Read access time (ID) Read access time (FM) Output disable time	15 10 - - 20	- - 40 340 80	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals. For output, see Section 7.7.6.1



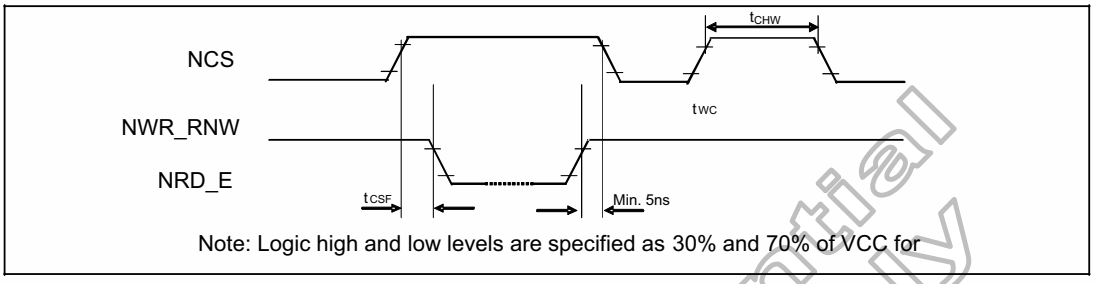


Figure 8. 2 Chip Select Timing

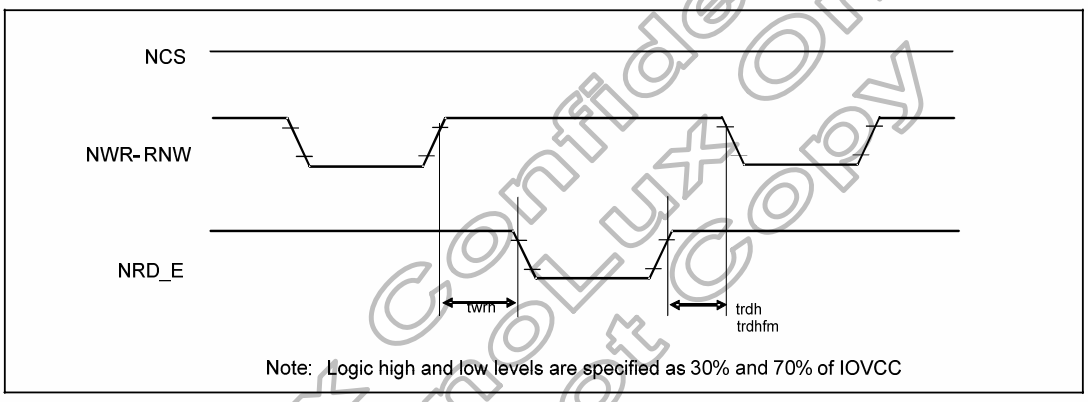


Figure 8. 3 Write to Read and Read to Write Timing